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[1] C. M. Keller, "Diversity-Combining for Frequency-Hop Spread-Spectrum Communications with Partial-Band," UILU-ENG-85-2228, October 1985, University of Illinois at Urbana-Champaign, CSL Technical Report.

This report presents results on the evaluation of several diversity combining techniques that are suggested for frequency-hop (FH) communications with partial-band interference and fading. The analysis covers systems with M-ary orthogonal signaling and noncoherent demodulation. The partial-band interference is modeled as a Gaussian process, although some of the results also apply to general (non-Gaussian) partial-band interference. The performance measures we use to evaluate the diversity combining techniques are the narrowband interference duty factors. We evaluate the exact probability of error for each of the diversity combining techniques studied. The performance of the optimum combining technique for receivers with perfect side information is established. It is shown that for receivers with perfect side information, the system performance does not change significantly with the choice of the diversity-combining technique. However, the same schemes that work well in receivers with perfect side information perform poorly in receivers without side information. The goal of this work is to find and analyze diversity-combining schemes that do not use side information, but that perform nearly as well as the optimum combining technique. Clipped linear combining is proposed as a diversity-combining technique for receivers without side information. The numerical results demonstrate that clipped linear combining can perform nearly as well as the optimum combining technique in terms of both narrowband interference rejection and signal-to-noise ratio requirement. However, knowledge of the signal output voltage is required to set the clipping level. We analyze two alternative diversity-combining techniques that do not have this requirement. These diversity-combining schemes use ratio statistics in a ratio threshold test to determine the quality of each diversity reception. It is shown that the ratio threshold test with diversity combining provides good narrowband interference rejection, but at the expense of an increased signal-to-noise requirement near full-band interference. Although the ratio threshold test with diversity combining does not achieve the optimum performance, it is an effective, as well as practical, scheme for use in FH communication systems with partial-band interference and fading. (109 pp.)

[2] R. G. Ogier, "Flow Optimization in Dynamic and Continuous Networks," UILU-ENG-85-2229, November 1985, University of Illinois at Urbana-Champaign, CSL Technical Report.

The main problem studied in this report is that of computing a minimum-delay time-varying routing assignment in a dynamic network where the node demands and link capacities are deterministic functions of time and where the commodity being routed is represented by continuous variables. A single node is designated to be the destination, and a τ-maximum flow is defined to be a routing assignment which maximizes the amount of commodity reaching the destination before time τ. The key discovery used to solve the problem is that a routing assignment has minimum delay if and only if it is a τ-maximum flow for all τ. When the capacities are constant or piecewise-constant, this discovery and the well-known max-flow min-cut theorem are used to divide the problem into two smaller problems. The result is a polynomial algorithm which finds a minimum-delay routing assignment by solving a series of static maximum-flow problems. In order to apply the above ideas to dynamic networks with continuously varying capacities, a continuous network is defined whose flows and capacities are additive set functions, and a generalization of the max-flow min-cut theorem is proved. An even more general version of this theorem is proved for continuous network models whose capacities are submodular set functions. Various applications are considered, including the finite polymatroid networks of Lawler. (114 pp.)

[3] P. Gee, "Silicon Compilation: A Solution to the Complexity of VLSI Circuit Design," UILU-ENG-85-2230, September 1985, University of Illinois at Urbana-Champaign, CSL Technical Report.

Designing very large-scale integrated circuits requires several months or more and increases the complexity of the design increases. This report proposes to reduce the complexity of the design problem and to reduce the design time by using a high-level language to specify only the behavioral aspects of a circuit. The circuit is then synthesized from this specification. (72 pp.)

[4] D. G. Saab, "Symbolic Switch-Level Logic and Fault Simulation of MOS VLSI Circuits," UILU-ENG-85-2231, September 1985, University of Illinois at Urbana-Champaign, CSL Technical Report.

This paper describes an approach for switch-level logic and fault simulation and symbolic logic expression extraction of MOS circuits. The method is applicable to transistor circuits extracted directly from layout data or specified as input. The method automatically partitions the circuit into subcircuits. Logic expressions are generated which describe the states of the nodes in terms of subcircuit inputs and initial conditions. The expressions provide a functional description of the circuit, and an algebra for evaluating the expressions is derived. The logic evaluation procedure, however, can be applied directly to the switch-level circuit description without the need of generating the expressions first. The method has been implemented in a computer program for logic and fault simulation which uses concurrent simulation techniques. (66 pp.)

[5] R. J. Eickemeyer, "A Parallel Stack Processor to Reduce Procedure-Call Overhead," UILU-ENG-85-2232 (CSG-48), November 1985, University of Illinois at Urbana-Champaign, CSL Technical Report.

A processor organization is presented to reduce the large overhead of procedure calls in high-level languages. In the Parallel Stack Processor (PSP), processor registers are each at the top of a hardware stack of registers. Saving processor registers on a procedure call takes place in one cycle by pushing all registers simultaneously. A detailed performance model, driven by dynamic high-level language statistics, is presented. Results from the model indicate the effect on performance of the parallel stack architecture when compared to a processor without parallel stacks. The processor architecture is specified in the report along with a discussion of implementation details for the VLSI single-chip processor. (84 pp.)

[6] R. Tamassia and I. G. Tollis, "A Provably Good Linear Algorithm for Embedding Graphs in the Rectilinear Grid," UILU-ENG-85-2233 (ACT-64), December 1985, University of Illinois at Urbana-Champaign, CSL Technical Report.

In this report we consider planar embeddings of n-node planar graphs in the rectilinear grid, where vertices are grid points and edges are nonintersection grid paths. We present a new embedding algorithm that runs in linear time. The total number of bends in the embeddings constructed by our algorithm is very small. Furthermore, the embeddings occupy O(n) area, which is the best possible in the worst case. Our results are important in the design of VLSI chips. Other applications can be found in the areas of communication by light or microwave, transportation in space, and aesthetic layout of diagrams. (19 pp.)

[7] W.-T. Cheng, "Testing and Error Detection in Iterative Logic Arrays," UILU-ENG-85-2234 (CSG-44), August 1985, University of Illinois at Urbana-Champaign, CSL Technical Report.

The test methods of general iterative logic arrays (ILAs) composed of combinational cells are considered in the first part of this report. The fault model assumed is that

faults in a cell can change a cell behavior in any arbitrary way, as long as the cell remains a combinational circuit. At the array level, two fault-models are considered: in the single-cell fault model (SCFM) we assume only one cell can be faulty; and in the multiple-cell fault model (MCFM) we assume any number of cells can be faulty. Previous reports have solved the testing problems of C-testable and linear testable unilateral one-dimensional (1-D) ILAs under SCFM. The necessary and sufficient condition of a test set in unilateral 1-D ILAs under MCFM is derived here. With this condition, two procedures that can generate near-minimum test sets for linear testable and C-testable unilateral 1-D ILAs respectively are proposed. Furthermore, the results are extended to generate test sets for bilateral 1-D ILAs, unilateral tree-structured ILAs, and unilateral two-dimensional ILAs under SCFM and MCFM. Finally, improving all the testing methods to cover sequential faults are proposed. In the second part of this report, using the methods of Recomputing with Shifted Operands (RESO) to detect errors in ILAs are discussed. Here, our fault model covers all kinds of faults within a cell, including permanent, nonpermanent, combinational, sequential, static, dynamic and indeterminate-logic faults. Necessary and sufficient conditions on the basic cell flow table are derived to determine if a unilateral 1-D ILA is RESO-detectable. The problems of fault location are also considered. It is shown that an arbitrary cell flow table can be augmented by the addition of some outputs to make it RESO-detectable. The implementation of RESO with rotation instead of shift operation is also considered. The results are extended to bilateral 1-D ILAs and two-dimensional ILAs. (112 pp.)