COORDINATED SCIENCE LABORATORY
TECHNICAL REPORTS

January 1990 through December 1990

Coordinated Science Laboratory
University of Illinois at Urbana-Champaign
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Urbana, Illinois 61801
The relative power of several computational models is considered. These models are the Turing machine and its multidimensional variant, the random access machine (RAM), the tree machine, and the pointer machine. The basic computational properties of the pointer machine are examined in more detail. For example, time and space hierarchy theorems for pointer machines are presented. Every Turing machine of time complexity $t$ and space complexity $s$ can be simulated by a pointer machine of time complexity $O(i)$ using $O(s / \log s)$ nodes. This strengthens a similar result by van Emde Boas (1989). Every alternating pointer machine of time complexity $t$ can be simulated by a deterministic pointer machine using $O(t / \log t)$ nodes. Other results concerning nondeterministic and alternating pointer machines are presented. Every tree machine of time complexity $t$ can be simulated on-line by a log-cost RAM of time complexity $O((t \log t) / \log \log t)$. This simulation is shown to be optimal using the notion of incompressibility from Kolmogorov complexity (Solomonoff, 1964; Kolmogorov, 1965). Every $d$-dimensional Turing machine of time complexity $t$ can be simulated on-line by a log-cost RAM running in time $O(t (\log t)^{1 + O(1/d)} (\log \log t)^{1/d})$. There is a log-cost RAM $R$ running in time $t$ such that every $d$-dimensional Turing machine requires time $\Omega((t (\log t)^{1 + O(1/d)} (\log \log t)^{1/d}))$ to simulate $R$ on-line. Every unit-cost RAM of time complexity $t$ can be simulated on-line by a $d$-dimensional Turing machine in time $O(t (n)^{1/(\log t)} (n))$. (102 pp.)

A new direct adaptive regulation scheme is proposed for nonlinear systems satisfying extended matching conditions. Two sets of additional conditions are given: first, for the regulation to be global, and, second, for asymptotic parameter convergence. It is also shown that the new scheme is robust with respect to unmodeled dynamics. (23 pp.)

The robotics literature of the 1980s contains important advances in our understanding of the dynamics and control of joint flexibility in robotic manipulators. This report contains a survey of the applications of geometric control theory, singular perturbation theory, robots and adaptive control theory to the control of flexible joint robots. (29 pp.)

In many existing model reference adaptive control (MRAC) schemes, the plant order and relative degree are assumed known. Then a full-order control parameterization is specified that allows for an exact transfer function match between the closed-loop plant and a reference model. Often for plants of modest complexity, this leads to a large number of adjustable parameters. Apart from the computational burden, an excessive parameterization imposes, a common assumption used to prove global stability requires the regressor to be Persistently Exciting (PE). This PE requirement has been tied to the spectral content of the system input and is directly proportional to the number of parameters adjusted. Often this imposes unrealistic requirements upon the system
input. This problem is especially pronounced for regulation problems where the reference and system input are zero. In the approach presented in this report, the number of parameters and structure of the controller will not be tied to plant order. Instead, a reduced-order parameterization such as PID or lead-lag will be adapted. For many applications, slow adaptation offers an attractive means of increasing performance while retaining the simplicity of the underlying linear system. (91 pp.)


An empirical analysis of paging, memory allocation, and garbage collection in a Lisp system is presented, based on sampled memory system activity. Workload of varying complexity, consisting of the Boyer benchmark and QPE, a large AI program, is used to derive empirical models for garbage collector performance. The models allow a prediction of garbage collection time for a given amount of scanning and copying work, page faults, and other software overhead. The models account for greater than 90% of the variation in collection time. With some exceptions, the models correctly predicted, within a 95% confidence interval, the mean collection time of a particular run. The models also express the high time cost of a page fault cost; show how much longer copying takes than scanning a word; and show that the cost to scan a word depends on which class of spaces to be scanned it belongs to. In addition, the time-varying characteristics of memory allocation, survival, collector work, and efficiency are presented. Collector efficiency is quantified as words of discovered garbage per unit time (or work) expended by the collector. The variation of collector efficiency over the execution of the measured programs suggests the potential for improved performance by more closely matching garbage collection policy with program characteristics. (48 pp.)


This report describes the results of an extensive measurement-based analysis of real error data collected from a 7-machine DEC Vax Cluster multicomputer system. In addition to evaluating basic system error and failure characteristics, we develop reward models to analyze the impact of failures and errors on the system. The results show that, although 98% of errors in the shared resources recover, they result in 48% of all system failures. The analysis of rewards shows that the expected reward rate for the Vax Cluster decreases to 0.5 in 100 days for a 3-out-of-7 model, which is well over a 100 times that for a 7-out-of-7 model. A comparison of the reward rates for a range of k-out-of-n models indicates that the maximum increase in reward rate (0.25) occurs in going from the 6-out-of-7 model to the 5-out-of-7 model. The analysis also shows that software errors have the lowest reward (0.2 vs. 0.91 for network errors). The large loss in reward rate for software errors is due to the fact that a large proportion (94%) of software errors lead to failure. In comparison, the high reward rate for network errors is due to fast recovery from a majority of these errors (median recovery duration is 0 seconds). (38 pp.)


This report describes the first phase of the development of MEASURE, an integrated data analysis and model identification facility. The facility takes system activity data as input and produces as output representative behavioral models of the system in near real-time. In addition, a wide range of statistical characteristics of the measured system are also available. The usage of the system is illustrated on data collected via
software instrumentation of a network of SUN workstations at the University of Illinois. Initially, statistical clustering is used to identify high-density regions of resource-usage in a given environment. The identified regions form the states for building a state-transition model to evaluate system and program performance in real-time. The model is then solved to obtain useful parameters such as the response-time distribution and the mean waiting time in each state. A graphical interface which displays the identified models and their characteristics (with real-time updates) has also been developed. The results provide an understanding of the resource-usage in the system under various workload conditions. This work is targeted for a testbed of UNIX workstations with the initial phase ported to SUN workstations on the NASA, Ames Research Center Advanced Automation Testbed. (38 pp.)


A new approach for the statistical design and analysis of MOS is introduced. The proposed approach approximates the circuit performances, such as gain and delay, by fitted models. The fitted models are then used as surrogates of the circuit simulator to predict and optimize the parametric yield with computation efficiency and to achieve off-line quality control. The use of statistical design and analysis of experiments for model construction have been investigated theoretically and experimentally, and different methods to assess the adequacy of a fitted performance model have been studied. (112 pp.)


We present modifications of standard sequential decoding algorithms in an attempt to operate at rates greater than \( r_0 \), the computational cut-off rate. We call the new algorithms sequential decoding with reordering (SDR) algorithms. They observe the received message at the channel output and use this information to reorder the digits in the codeword tree. The resulting tree is then searched by a sequential decoder; the goal of reordering is to obtain a tree that is easy to search. However, codeword trees associated with convolutional codes cannot be reordered and still retain their uniform structure and slow growth. For this reason, we use low-density codes, a class of block codes. The SDR algorithms are presented for the binary erasure and binary symmetric channels. Simulation results suggest that at high code rates, the algorithms can be used at rates nearly equal to or greater than \( r_0 \). Because of differences between codeword trees for low-density codes and convolutional codes, we present a new sequential decoding algorithm designed for low-density codes. We also present an SDR algorithm that can be used as a soft decision decoder on channels with side information and channels with real-valued outputs. (137 pp.)


Several methods of scheduling a time-division multiple access, or TDMA, receiver with no feedback capability are evaluated for their throughput performance. Some of the options considered include prior time as opposed to real-time scheduling, optimal as opposed to simple or greedy scheduling, multiple listening capability, and the ability to utilize incremental redundancy techniques. All of these methods are compared by using various values for the rebroadcast redundancy. (52 pp.)

The problem of determining robust, low-order controllers that achieve stability and disturbance attenuation is considered. This is an important problem for the control of very high-order structures where a full order controller is inappropriate. To address this problem, an approach using the Frobenius-Hankel (FH) norm is developed. The FH norm is shown to lead to attractive robustness and performance properties. A parameter optimization method is developed that provides an iterative method for determining the FH optimal parameters of a dynamic system using a gradient approach. Two distinct controller design methods are presented that make use of the FH optimization procedure. The first approach determines a controller that minimizes the FH norm of the closed loop system. While the solution method is iterative, the procedure proves to be straightforward to apply. The second approach uses projective controls as a first step in the design. This allows the designer to take advantage of the attractive features of projective controls. Design parameters in the controllers are then determined by solving the FH optimization problem called the "auxiliary minimization problem." Examples of each approach are given, including a full design problem for the control of a flexible structure using the projective controls approach. The resulting improvement in the disturbance attenuation of the system using only second-order controllers points to the effectiveness of this design procedure. (85 pp.)


Distributed deadlock detection is a difficult problem and several incorrect solutions have appeared in journals. For each invocation on \( |V| \) nodes with \( |E| \) wait-for arcs, the best previous correct algorithms used \( O(|V|^2) \) messages or \( 4|E| \) messages to identify a deadlocked set of processes. This report presents two new distributed algorithms for deadlock detection. One algorithm uses \( 3|E| + |V| \) messages and \( O(|V|) \) time, the other \( 2|E| + 2|V| \) messages and \( O(|E|) \) time. (91 pp.)


A conjecture of Dirac states that every simple graph with \( n \) vertices and \( 3n - 5 \) edges must contain a subdivision of \( K_5 \). We prove that a topologically minimal counterexample is 5-connected and that no minor-minimal counterexample contains \( K_4 - e \). Consequently, we prove Dirac's conjecture for all graphs that can be imbedded in a surface with Euler characteristic at least \(-2\). (25 pp.)


Modern memory systems are composed of levels of cache memories, a virtual memory system, and a backing store. Varying more than a few design parameters and measuring the performance of such systems has traditionally been constrained by the high cost of simulation. Models of cache performance recently introduced reduce the cost simulation but at the expense of accuracy of performance prediction. Stack-based methods predict performance accurately using one pass over the trace for all cache sizes, but these techniques have been limited to fully-associative organizations. This report presents a stack-based method of evaluating the performance of cache memories using a recurrence/conflict model for the miss ratio. Unlike previous work, the performance
of realistic cache designs, such as direct-mapped caches, are predicted by the method. The method also includes a new approach to the problem of the effects of multiprogramming. This new technique separates the characteristics of the individual program from that of the workload. The recurrence/conflict method is shown to be practical, general, and powerful by comparing its performance to that of a popular traditional cache simulator. The authors expect that the availability of such a tool will have a large impact on future architectural studies of memory systems. (22 pp.)


The trend of deep pipelining and multiple instruction issue has made instruction sequencing an extremely critical issue. Traditionally, compiler-assisted instruction sequencing methods have been considered not suitable for deep pipelining and multiple instruction issue. Hardware methods such as Branch Target Buffers have been proposed for deep pipelining and multiple instruction issue. This report defines Inline Target Insertion, a specific compiler and pipeline implementation method for Delayed Branches with Squashing. The method is shown to offer two important features not discovered in previous work. First, branches inserted into branch slots are correctly executed. Therefore, the instruction sequencing efficiency is limited solely by the accuracy of compile-time branch prediction. This feature coupled with highly accurate compile-time branch prediction gives Inline Target Insertion excellent performance characteristics. Second, the execution returns correctly from interrupts or exceptions with only one single program counter. There is no need to reload other sequencing pipeline state information. These two features make Inline Target Insertion a superior alternative (better performance and less software/hardware complexity) to the conventional delayed branching mechanisms. The compiler part of Inline Target Insertion has been shown to be straightforward with an implementation in the IMPACT-I C Compiler. A new code expansion control method has been proposed and included in the implementation. The code expansion and instruction sequencing efficiency are measured for real UNIX and CAD programs. The size of programs, the variety of programs, and the variety of inputs to each program are significantly larger than those used in the previous experiments. The stability of code restructuring based on profile information is proved empirically using a large number of diverse inputs to each benchmark program. The results show that Inline Target Insertion achieves high sequencing efficiency at a small cost of code expansion for deep pipelining and multiple instruction issue. (48 pp.)


This report describes an experimental analysis of the impact of transient faults on a microprocessor-based jet-engine controller used in the Boeing 747 and 757 aircrafts. A hierarchical simulation environment that allows the injection of transients during run-time and the tracing of their impact is described. Verification of the accuracy of this approach is also provided. A determination of the probability that a transient results in latch, pin, or functional errors is made. Given a transient fault, there is approximately an 80% chance that there is no impact on the chip. An empirical model to depict the process of error exploration and degeneration in the target system is derived. The model shows that if no latch errors occur within eight clock cycles, no significant damage is likely to happen. Thus, the overall impact of a transient is well contained. A state transition model is also derived from the measured data to describe the error propagation characteristics within the chip and to quantify the impact of transients on the external environment. The model is used to identify and isolate the critical fault
propagation paths, the module most sensitive to fault propagation, and the module with the highest potential of causing external pin errors. (36 pp.)


Test generation is an important part of a circuit as the test vectors are used during the design, manufacture, system integration, and throughout the life-cycle of the circuit in order to detect the presence of defects. The very large-scale integration (VLSI) test generation problem has been one of the most complex and time-consuming problems. This is a major bottleneck in the design cycle of the circuit. The problem is further complicated by rapid advances in VLSI technology, such as in CMOS, where the traditional stuck-at fault model is inadequate and the increase in gate-to-pin ratio makes it difficult to access and observe the internal signals. In this report, we present two different approaches to attack this problem. The first approach is concerned mainly with the generation of functional-level tests that are used during system debug and integration. A functional diagnostic methodology as well as techniques to diagnose various blocks of a multiprocessor system are presented. The approach has been used successfully to debug and integrate a prototype multiprocessor system. In the second approach, we present a hierarchical and high-level model that uses architectural-level primitives for fault propagation and signal value justification to speed up the automatic test vector generation process. We present methods for fault propagation and value justification through the architectural-level primitives. In order to reduce the number of backtracks, the algorithm employs the strategy of dependency-directed backtracking, which attempts to resolve the conflicts by changing the signal values causing the conflict. Experimental results using this approach for test vector generation are presented. (143 pp.)


In this report we formulate certain specific optimization problems commonly occurring in the physical design process of digital integrated circuits such as the problem of testable nets, exchange, feed-through, and track-reduction. We show that the decision versions of these optimization problems are NP-Complete. The problems considered in this report are often considered as sub-problems within more general problems such as cell-placement and wire-routing and are not given the full attention they deserve. Hence, our major contribution is in identifying these sub-problems as separate problems and showing that they themselves are computationally intractable, thereby justifying the use of heuristics for their solution. (29 pp.)


In this report, the graph bisectioning problem is studied. We begin by presenting a necessary and sufficient condition for optimality of a given bisection. Two other sufficient conditions are then derived. Upper and lower bounds on the cost of an optimal bisection are obtained. A duality between the graph bisectioning problem and a nonlinear programming problem of maximizing a concave function is exhibited. We also show that for dense graphs, a bisection that approximates an optimal one can be easily found. Finally, we exhibit a class of graphs for which the ratio of the upper and lower bounds approaches 1 as the number of vertices in the graph increases. (43 pp.)

An adaptive system controlling weld puddle width is presented. It is based on the method of sensitivity points. The development of the general design is given. Simulated and experimental setup and results are presented. (62 pp.)


Collected here are papers prepared by the students of EE497: High-Speed Computer Communication Networks in the 1990 Spring Semester at the University of Illinois at Urbana-Champaign. Some minor revisions to the papers were made by the students after the end of the semester. The course was a special topics course at the graduate level. The first three papers deal with some aspects of routing in packet-switched networks in which routing decisions are made in a distributed fashion. The next paper considers dynamic routing in a circuit-switched network. The fifth and sixth papers address two different queueing problems that arise in high-speed networks. The final three papers cover optical codes, network resource allocation from the perspective of economic theory, and an existing telecommunication switch. (147 pp.)


Circuit simulation is an indispensable tool in the design and analysis of Very Large Scale Integrated (VLSI) circuits. The most widely used circuit simulators rely on direct methods and offer the most accurate, reliable, and technology-independent means of simulating integrated circuits. The simulation process is inherently very computation intensive and, hence, can require a significant portion of the computational resources available for the development of VLSI circuits. With the use of multiprocessor computers becoming more widespread, there exists an opportunity to speed up the simulation by partitioning the circuit so that the computation may be spread among the processors. To accomplish this, the circuit is partitioned into subcircuits using a node tearing method. If the circuit matrix is ordered subcircuit by subcircuit followed by the tearing nodes, then the matrix takes a bordered-block-diagonal form and the LU-factorization of the diagonal blocks may take place in parallel. This thesis defines the important objectives for this partitioning task and presents two algorithms that may be used to meet the partitioning goals. The first algorithm is an iterative improvement algorithm and the second is a network flow algorithm. Partitioning results and speed-ups are given for a variety of circuits. (100 pp.)


In Very Large Scale Integration (VLSI) chips, metal migration(MM) is an important problem from the reliability standpoint. Furthermore, as the feature size is scaled down, MM becomes an even greater problem because of the higher current densities that would exist in the power and ground busses. Because of the complexity of VLSI power busses, there exists a need for a computer-aided design tool to correctly predict the likely failure site(s). This thesis deals with a primitive splitting algorithm that calculates current density waveforms efficiently. These waveforms are used to find the Median Time to Failure (MTF), a major parameter of concern in predicting MM. This algorithm has been motivated by examining the equipotential plots obtained through
finite-element method analysis of simple regions. It has been successfully implemented and tested, and some examples are described. (61 pp.)


In this report, heuristics that use predicted process resource requirements to make scheduling decisions are proposed. Four heuristics are presented. The first two, MINQ and SMPL, employ centralized scheduling and the remaining two, DMINQ and FDMINQ, use distributed scheduling. These heuristics are first compared against random scheduling and then against two conventional heuristics, CENTEX and DISTED, which schedule processes solely based on system state information. Results based on trace-driven simulations show that the proposed centralized heuristics offer significantly improved mean response times and that they require fewer status update messages. In experiments using the same status update rates, SMPL response times were, on the average, 22% lower than those for CENTEX; and MINQ response times were, on the average, 18% lower. The simulations also showed that MINQ and SMPL can perform as well as, or better than, CENTEX while using up to 70% fewer status update messages. The use of fewer status update messages imposes less overhead on the system. The use of prediction for distributed scheduling produced similar results. When prediction was used to filter small processes and execute them locally, a 50% improvement in response times was obtained. (23 pp.)


This report presents a new method of decentralized linear, time-invariant control system synthesis based on the algebraic Riccati equation (ARE). The basic decentralized design guarantees closed-loop stability and a predetermined level of worst-case disturbance attenuation. Certain modifications of the basic design guarantee the stability and disturbance attenuation to be robust despite plant uncertainty or reliable despite control-component outages. Other modifications guarantee that a subset of the controllers will be open-loop stable. The derived decentralized control law consists of a full-order observer of the plant in each control channel. Each observer includes estimates of the controls generated by the other channels and of plant disturbance inputs, based on its own estimate of the state of the plant. All of the observer gains are computed from the solution of a single Riccati-like algebraic equation, while feedback gains are computed from a state-feedback design ARE. The existence of appropriate solutions to the design equations is sufficient to guarantee the various properties of the closed-loop system. A convexity property of a certain matrix Riccati function allows parameterization of families of control laws with the same desired properties. Each value of the parameter results in controller of the same order as the plant. (86 pp.)


Classical scheduling theory, originating in the 1950s, considers the deterministic problem of scheduling a fixed number of jobs, with known and fixed processing requirements, on a given set of machines so as to minimize a given performance criterion. Performance measures that are most often chosen include (weighted) makespan, tardiness, and lateness. Problems of this type are examples of combinatorial optimization problems. Unfortunately, when the number of jobs and/or machines exceeds single digits, the determination of an optimal solution to the scheduling problem generally becomes computationally infeasible. (54 pp.)

This report describes an efficient approach for solving sparse linear systems using direct method on a shared-memory vector multiprocessor computer. The direct method is divided into three steps: LU factorization, forward substitution and backward substitution. If the size of the linear system is large, LU factorization is a very time-consuming step, so that concurrency and vectorization are exploited to reduce execution time. Parallelism of LU factorization is obtained by partitioning the matrix using multilevel node-tearing techniques. The partitioned matrix is reordered into a NBBD (Nested Bordering-Block Diagonal) form. A nested-block data structure is used to store the sparse matrix, enabling the use of vectorization as well as multiprocessing to achieve high performance. This approach is suitable for many applications that require the repeated direct solution of sparse linear systems with identical matrix structure, such as circuit simulation. The approach has been implemented in a program that runs on an ALLIANT FX/8 vector multiprocessor with shared memory. Speed-ups in execution time compared to conventional serial computation with no vectorization are up to 20 using eight processors. (81 pp.)


This report describes the development of DEPEND, an integrated simulation environment for the design and dependability analysis of fault-tolerant systems. DEPEND models both hardware and software components at a functional level, and allows automatic failure injection to assess system performance and reliability. It relieves the user of the work needed to inject failures, maintain statistics and output reports. The automatic failure injection scheme is geared toward evaluating a system under high stress (workload) conditions. The failures which are injected can affect both hardware and software components. To illustrate the capability of the simulator, a distributed system which employs a prediction-based, dynamic load-balancing heuristic is evaluated. Experiments are conducted to determine the impact of failures on system performance and, to identify the failures to which the system is especially susceptible. (15 pp.)


In this report, the effects of a variety of faults on a neural network is quantified via simulation. The neural network consists of a single-layered clustering network and a three-layered classification network. The percentage of vectors misclassified by the clustering network, the percentage of vectors misclassified by the classification network, the time taken for the network to stabilize, and the output values are all measured. The results show that both transient and permanent faults have a significant impact on the performance of the measured network. The corresponding mistag and misclassification percentages are typically within 5% to 10% of each other. The average mistag percentage and the average misclassification percentage are both about 25%. After relearning, the percentage of misclassifications is reduced to 9%. In addition, transient faults are found to cause the network to be increasingly unstable as the duration of a transient is increased. The impact of link faults is relatively insignificant in comparison with node faults (1% versus 19% misclassified after relearning). There is a linear increase in the mistag and misclassification percentages with decreasing hardware redundancy. In addition, the mistag and misclassification percentages linearly decrease
with increasing network size. (93 pp.)


Simulation has become indispensable in the process of designing, verifying, and testing complex digital systems because it is flexible and cost-effective. As the complexity of the designs grows, the time and memory requirements of simulation increase and simulation can become a bottleneck. At the same time, parallel and distributed processing is becoming available and offers the potential of economical high-performance computing. However, software and applications are lagging behind at this stage. The research reported in this thesis is motivated by both the increased need for simulation and the emergence of general purpose parallel computers. After reviewing previous work in the area of parallel simulation, we relate the issues of portability and scalability to our application and define a high-level process model view for parallel simulation. In the following, we report the results of two application studies. We first address parallel gate-level logic and fault simulation and then investigate parallel switch-level simulation; for both we introduce partitioning and simulation algorithms and present extensive performance evaluations. Directions for future research and an outlook for the future of parallel simulation conclude the thesis. (135 pp.)


An important consideration in the design of high-performance multiprocessor systems is to ensure the correctness of the results computed in the presence of transient and intermittent failures. Concurrent error detection and correction have been applied to such systems in order to achieve reliability. Algorithm Based Fault Tolerance (ABFT) has been suggested as a cost-effective concurrent error detection scheme. The research reported in this report has been motivated by the complexity involved in the analysis and design of ABFT systems. To that end, a matrix-based model has been developed and, based on that, algorithms for both the design and analysis of ABFT systems are formulated. These algorithms are less complex than the existing ones. In order to reduce the complexity further, a hierarchical approach is developed for the analysis of large systems. (135 pp.)


In this report, a new general adaptive algorithm for solving a wide variety of NP-Complete combinatorial problems id developed. The new technique is called Stochastic Evolution (SE). The SE algorithm is applied to Network Bisection, Vertex Cover, Set Partition, Hamilton Circuit, Traveling Salesman, Linear Ordering, Standard Cell Placement, and Multi-way Circuit Partitioning problems. It is empirically shown that SE outperforms the more established general optimization algorithm, namely, Simulated Annealing. (115 pp.)


This report considers the problems arising from VLSI routing design. Algorithms are proposed for solving both global and local routing problems. For routing multiterminal nets in the gate array and sea-of-gates technologies, we present a global router which upper bounds the global density of the routing by 2s, where s is the span of the nets. For standard cell technology, we present a global router which achieves the optimal
horizontal density while upper bounding the vertical density by $2s^*$. The parallel implementations of the proposed global routing algorithms are presented. For the local routing problem, we first investigate the efficiency of the Manhattan routing model. We study in detail how the grid points are used in the Manhattan model and, consequently, establish a general lower bound on the channel width for routing two-terminal nets in a channel. All of the previous known results (lower bounds on the channel width) can be derived from our general lower bound. Furthermore, an asymptotically tight lower bound is obtained. We are also able to establish the lower bounds on the routing area for routings in L-, S-, T- and X-junctions in both the Manhattan and knock-knee models. For routing in an arbitrary rectilinear polygon, which is a generalization of many local routing problems, we present a sublinear time algorithm running in $O(n \log^2 m)$, where $m$ is the number of edges in the boundary of the polygon. The presented algorithm produces the minimal routing area. For routing in the restricted wire-overlap model, we present an optimal algorithm which constructs a routing with minimum channel width. In the routing produced by the algorithm, the length of the wire overlap between any two nets is upper bounded by $O(k)$, where $k$ is the multiplicity of the nets. (135 pp.)


In the past, other researchers have shown that increased use of high-level test knowledge can be used to greatly accelerate the test generation process. The problem was that no techniques were developed to extract this knowledge from a circuit. Typically the only solution was for a circuit designer to manually extract the test knowledge. In cases where designers are using sophisticated high-level synthesis tools (e.g., a silicon compiler), the designer may not be competent to extract this type of knowledge. In this thesis we describe solutions to the problem of automatically extracting this high-level knowledge from the structure of compiled circuit. Two different types of knowledge are addressed. The first type of knowledge is a testability measure. We present solutions to the problem estimating the testability for circuits defined at a functional level. By using an information theoretic testability measure, the concepts of controllability and observability are captured. Instead of requiring exhaustive enumeration of the input space to compute the measure (as has been previously suggested), we present two different methods for efficiently and accurately estimating the measure. In addition, we have presented various applications of this measure, including automatic circuit partitioning and test point insertion. The second type of knowledge is test generation knowledge. We describe techniques to automatically extract high-level test and DFT knowledge from the structure of compiled circuits. These techniques work autonomously and require no user intervention. This system has been implemented in a SUN workstation environment and is known as DELPHI. It operates on a high-level dataflow representation of a compiled circuit and generates the test knowledge in the form of lists of primary input assignments. Achieving both high levels of fault coverage and fast performance, DELPHI can extract test knowledge from both nonsequential and sequential circuits. When test knowledge extraction is unsuccessful, additional DFT knowledge is obtained to efficiently represent design for testability options. In those cases where users are able to provide test knowledge, techniques to verify user provided knowledge are described. (123 pp.)


This report looks at several aspects of solving the Input/Output problem. The increasing processor speeds and the emerging multiprocessor machines have improved the
processing power of a system at a tremendous pace. This has not been followed by corresponding improvements in other parts of the system, mainly the I/O subsystem. This could lead to a huge imbalance in the system and, if not corrected, the gains made in the processing power will be of little use as the problem solving speed will be determined by the slower I/O operations. A number of issues in solving the I/O problem are addressed in this thesis. The effects of I/O on problem solution are studied by tracing a number of applications on a multiprocessor. This study is aimed at gaining an understanding of how I/O accesses can be more efficiently done, how I/O systems need to be organized to effectively address the I/O problem and to explore compiler techniques to reduce the I/O problem. Since the I/O device speeds are not improving dramatically, the I/O power can significantly be improved only through parallel organizations. An extensive evaluation of these parallel organizations is presented. Different parallel I/O (disk) organizations are evaluated in different workloads. A methodology for interfacing I/O processors with a multiprocessor system is presented. This methodology is shown to have a number of advantages over the previous approaches. When data are distributed on multiple disks, fault tolerance becomes a problem. A new technique is presented for achieving fault tolerance in a multiple disk system. A number of compiler techniques are also proposed to reduce the I/O problem by suitable transformation of programs. A number of open problems in this area are highlighted.

(169 pp.)


A methodology for applying optimizing compiler techniques to signature monitoring in order to reduce performance overhead and simplify monitor hardware is introduced. We present models for the monitor architecture and the signature placement. The monitor architecture model is designed to keep both the hardware and integration complexities low. Our signature model is designed to insert reference signatures in order to satisfy a bound on the error detection latency. Justifying signatures are inserted on program arcs using an $O(N^2)$ algorithm which is significantly better than previous exponential node insertion algorithms. We use optimizing compiler techniques to customize the signature placement for various target processors and to minimize the performance overhead due to justifying signatures. Experiments were performed to study the performance and memory overheads of our compiler-assisted arc insertion signature monitoring method for a variety of architectures with different branch handling schemes. Using run-time information for processors with delayed branching or branch target buffers improves the performance overhead by approximately 50%. However, processors that always fetch the instruction following a branch and squash it if the branch is taken (e.g., the MC68000) are able to hide some of the performance overhead and therefore the run-time information only slightly improves the performance overhead. Using the MC68000 as the target processor, the performance and memory overheads for latencies between 10 and 200 instruction cycles, range from 16% to 4% and from 17% to 11%, respectively. After 200 cycles, the overheads remain relatively constant. In general, there is an inverse exponential relationship between the performance and memory overheads and the error detection latency. (41 pp.)


We introduce the new optimization method of Simulated Evolution (SE), which is designed to find near optimal solutions to problems which are hard to solve by standard methods. The new algorithm discussed in detail and a variety of measurements are taken to evaluate its performance under various conditions. In addition, a
theoretical framework is introduced to formally describe the algorithm. A Markov analysis is performed using this mathematical model to analyze convergence properties. The Standard Cell placement problem in the VLSI design area was chosen as a representative problem for applying SE techniques. A new hierarchical placement technique using windowing methods is introduced. A complete placement program has been developed and thoroughly tested on a variety of industrial benchmark circuits. A comparative performance analysis with the most successful Simulated Annealing-based placement program is presented. The SE algorithm has been implemented on several different sequential and parallel computing platforms. An evaluation of the achievable parallelism has been performed in each case. Furthermore, a special purpose coprocessor which speeds up wire length calculations as needed by placement programs has been designed, fabricated and tested. (138 pp.)


Static CMOS circuits can fail in ways that make the traditional stuck-at fault model and test generation techniques inadequate. It will be shown that the layout of these circuits can affect testability and in some cases reduce the number of possible faults in a design. A method is presented to analyze circuits at the symbolic level and to enhance testability using local transformations. A set of standard cells was designed using the layout level techniques. These standard cells are used in the MIS synthesis system allowing the designer to interactively modify designs and perform trade-off analysis in testable design. Examples are run through the system and then fault simulated at the transistor level. It is shown that the modified designs have significantly higher fault coverage than unmodified designs. A synthesis strategy is presented to design easily testable random logic circuits. (52 pp.)


The world is a more competitive place than before, and time is a key component in any winning competitive strategy. This thesis provides methods by which companies can become more efficient time-based competitors in the semiconductor and computer businesses. Methods are presented in two very important areas, design and manufacture. In the design area, the issues of test and design-for-test are examined since they are important and growing parts of the total design cycle. A productivity study is presented and, from the insight gained, models are developed to accurately predict important issues in test and design-for-test. The productivity models are then combined with economic models to achieve a complete life cycle picture of the integrated circuit that not only includes die economics but also time to market effects and quality issues. Examples are presented to demonstrate the use of the models. In the manufacturing end of the semiconductor business, a method is developed that allows just-in-time techniques to be applied to fabrication areas. The technique consists of unraveling the job shop by concentrating on the bottleneck and/or critical workstations and then calculating the number of Kanban cards needed to control inventory and production. An extensive simulation-based evaluation of the method is presented, comparing it to many other techniques for three types of fabrication areas. These are: single bottleneck with no hot-lots, multiple bottlenecks with no hot-lots, and single bottleneck with hot-lots. In all cases the just-in-time method developed performs best overall. (131 pp.)

This report presents the sensitivity point tuning theory and its application for off-line optimization of a controller. A consumable electrode gas metal arc welding process is used to implement the controllers and the tuning procedure. A single-input single-output case is treated, first using a PI controller. The nonlinearity of the system then encourages the realization of a simple nonlinear controller. The tuning procedure is also implemented on a double-input double-output system. The structure of the controller chosen is also a PI with all the crossing terms. Finally the tuned value for this controller is compared to a classical LQ design and the robustness of the method is tested using different operating conditions. (43 pp.)


A versatile, two-dimensional simulator for various types of semiconductor lasers for both steady state and transients has been developed. The simulator is capable of spectral analysis of quantum-well semiconductor lasers, such as gain-spectrum analysis, as well as analysis of the two-dimensional current flow and optical intensity patterns. The simulator is based on the drift-diffusion model with full Fermi-Dirac statistics for the transport equations as well as for the Poisson equation. Simulation of the thermionic emission current is required at the abrupt hetero-interfaces of the quantum well. Energy transfer among the charge carriers, crystal lattice, and optical radiation in an optoelectronic semiconductor device is analyzed in order to obtain details of the internal temperature distribution. Fermi-Dirac statistics and the spatial band-gap variation in a degenerate semiconductor device with nonuniform band structure are included in the analysis. Sources of ill-conditioning in the simulation of thermal flow in semiconductor devices are considered, and a new conditioning scheme which gives a satisfactory convergence for the Newton method is also described. The boundary conditions for the energy flow equation are discussed. For the spectral analysis of quantum-well lasers, we have used the photon rate equation for each Fabry-Perot mode. For the optical intensity pattern, we have solved the two-dimensional Helmholtz eigenvalue equation using the subspace iteration method. The transient simulation is done by the backward-Euler method in conjunction with the full Newton approach for the entire semiconductor equations. To demonstrate the simulator, a model GaAs-AlGaAs graded-index-separate-confinement-heterostructure buried-quantum-well laser is analyzed. (79 pp.)


Circuit extraction is critical in the validation of VLSI circuits since it provides the link between the design and the simulation phases. The use of hierarchical design techniques and hierarchical analysis methods increases design productivity. In this thesis, the development of iCHARM, a hierarchical circuit extractor, is described. The extractor takes its input layout in either the CIF format or the Oct VLSI database format. The extractor produces circuit parasitics including capacitances and resistances. A power bus extraction mode has been developed to calculate power bus currents for reliability estimation. The primary contribution of this work is a method to extract a circuit hierarchically without flattening and with minimal overhead. A full-chip layout was used to test the extractor's functionality and to allow a comparison of the hierarchical and flat extraction modes. (110 pp.)

A workshop was held at The Aerospace Corporation facility in El Segundo, California on May 1 and 2, 1990. The purpose of the workshop was to promote interaction among modelers and experimentalists. Participation was solicited to cover all aspects of experimentation and analysis of computer dependability including but not limited to (1) design of experiments; (2) modeling and analysis; (3) instrumentation and data collection; (4) measurements of reliability and performance; (5) statistical analysis and interpretation; (6) software reliability and fault tolerance; (7) evaluation of experimental systems; and (8) experimental methodology. Participants who made a presentation at this conference submitted a position statement in advance of the workshop. This report contains all the position statements submitted and a summary of key conclusions and recommendations resulting from this workshop. (31 pp.)


This report concerns the problem of timing verification and synthesis of circuits for robust delay fault testability. The timing verification algorithm uses Register Transfer Level (RTL) descriptions to eliminate false paths (nonsensitizeable) due to redundancy, reconvergent fanout, and control signal constraints. The RTL descriptions help to prune the search space because only valid paths are considered. The critical paths obtained from the timing verifier have to be tested for any delay faults. To make the robust delay test generation easier, multilevel combinational logic circuits are synthesized for delay fault testability. Given a multilevel description of a combinational logic circuit, blocked or dependent paths may be present. Blocked or dependent paths due to reconvergent fanout can destroy robustness of tests. A set of path segments called essential paths is checked for blockage or dependency, and a local transformation enhances the delay fault testability of the circuit. It has been shown that a robust delay test can be obtained as a by-product of the logic synthesis procedure. (131 pp.)


With the increase in complexity of digital circuits, it has become extremely important to detect faults to ensure correct operation of a digital circuit. Since test generation and fault simulation for circuits of VLSI complexity can take a prohibitive amount of time, speeding up test generation and fault simulation algorithms by either using better uniprocessor heuristics or by using the tremendous computing power available on multiprocessors thus becomes important. With general purpose multiprocessors becoming more common and affordable, accelerating test generation and fault simulation using parallel processing becomes a very attractive and cost-effective alternative. The design and analysis of parallel algorithms for test generation and fault simulation are the focus of this research. This report is a part of a much larger project called the HIPERCAD project whose objective is to design efficient parallel algorithms for a variety of Computer-Aided Design (CAD) problems. We first categorize various parallel processing techniques available for test generation and fault simulation. We discuss the advantages and disadvantages of each of the proposed techniques. We then propose a parallel search method to overcome the deficiencies of inaccurate search heuristics. It will be shown that this method scales very easily with the number of processors and can be implemented easily on configurations with a large number of processors. We show that this method not only results in faster execution of the test generation
algorithm but also results in a better quality of the solution. We also propose a performance model to evaluate the parallel search technique. We then propose fault partitioning techniques to speed up test generation for faults that are relatively easy to detect. The objective of the fault partitioning techniques is to maximize concurrency without affecting the quality of the overall solution. We propose load balancing techniques that try to minimize the processor idle time with very low communication overhead. We propose a performance model that takes into account the various trade-offs in exploiting parallelism in a test generation/fault simulation environment. Finally, we present a parallel test generation system for sequential circuits. A parallel search technique is used to accelerate test generation for hard-to-detect faults, and a circuit partitioned approach is used to accelerate fault simulation. It is shown that the parallel test generation system is comparable in efficiency as well as performance to most existing test pattern generators. (157 pp.)


This report presents a detailed stability analysis of an adaptive composite control strategy for flexible joint robot manipulators. Our so-called slow/fast control strategy, consisting of a slow adaptive controller designed for a rigid robot together with a fast control to damp the elastic oscillations of the joints, was first derived in previous work of the authors and its performance was detailed by both simulations and experimental results. We now present the mathematical details and rigorous stability proofs of our algorithm Using the composite Lyapunov theory for singularly perturbed systems we present sufficient conditions for adaptive trajectory tracking. For point-to-point motion we show that there is always a range of joint stiffness for which convergence is achieved and we quantify the region of convergence. For tracking of (smooth and bounded) reference trajectories we give sufficient conditions for closed loop stability and uniform boundedness of the tracking error. A residual set to which the tracking error converges is quantified. We also show that for special classes of trajectories, which include step responses generated from reference models and certain joint interpolated trajectories we can achieve asymptotic tracking. We argue that these results are the best that one can expect without additional compensation of the slow subsystem such as with integral manifold based corrective control. (70 pp.)


Processors with private caches have usually been assumed in the study of multiprocessor systems, particularly when the number of processors is large. A private cache organization allows a processor to access only its own cache and some mechanism is required to maintain data coherence between all the caches. A number of solutions for the coherence problem have been proposed but all impose some degree of performance penalty on the system. For a medium-size multi-processor, e.g., where the number of processors is less than or equal to 16, an alternative scheme is to share a single cache among all the processors. A shared cache organization does not generally require a coherence mechanism and potentially offers better performance for accessing shared data. However, when multiple processors attempt to access the cache within the same cache cycle, conflicts occur such that one or more processors must wait for cache service. Furthermore, due to multiple reference streams, how a shared cache handles cache misses can have an important effect on system performance. This report discusses the organization of a shared cache system and looks at the effect on its performance when the number of cache banks is increased and when buffer queues are added. In particular, by evaluating shared cache access conflicts and cache miss
effects, we look at how these changes affect multi-processor performance. To evaluate the effectiveness of increasing the number of cache banks and buffer queues on the performance of the shared cache system, we simulate with a multi-processor model based on the Alliant FX/8. The model is driven by a set of address traces generated by a detailed simulation of an Alliant FX/8. (104 pp.)


An important problem facing numerous research projects on parallelizing compilers for distributed memory machines is that of automatically determining a suitable data partitioning scheme for a program. Most of the current projects leave this tedious problem almost entirely to the user. In this report, we present a novel approach to the problem of automatic data partitioning. We introduce the notion of constraints on data distribution and show how a parallelizing compiler can infer those constraints by looking at the data reference patterns in the source code of the program. We show how these constraints may be combined by the compiler to obtain a complete and consistent picture of the data distribution scheme, one that offers good performance in terms of the overall execution time. We illustrate our approach on an example routine, TRED2, from the EISPACK library, to demonstrate its applicability to real programs. Finally, we discuss briefly some other approaches that have recently been proposed for this problem and argue why ours seems to be more general and powerful. (40 pp.)


A systematic procedure is developed for the design of adaptive regulation schemes for a class of feedback linearizable nonlinear systems. The coordinate-free geometric conditions, which characterize this class of system, neither restrict the location of the unknown parameters nor constrain in any way the growth of the nonlinearities. Instead, they require that the nonlinear system be transformable into the so-called pure-feedback form. This becomes now the broadest class of nonlinear systems for which an adaptive regulation scheme can be systematically designed. We also show that, under additional conditions, global stability properties can be established. (40 pp.)


We present an algorithm for finding the minimum spanning tree of a graph with $n$ vertices and $m$ edges on a Common CRCW PRAM using $m+n^{1+\epsilon}$ processors and $O(m+n^{1+\epsilon})$ space in $O(\log n)$ time, where $\epsilon$ is a constant such that $0 < \epsilon \leq 1/2$. (10 pp.)


In this report we establish a correct "local" criterion for computing the convex hull of the union ("merging") of two disjoint convex polyhedra. This criterion is amenable to parallel implementation and leads to a provably correct algorithm that computes the convex hull of any point set in three-dimensional space in $O(\log^2 n)$ time using $O(n)$ CREW PRAM processors. (10 pp.)

The finite element method (FEM) is very appealing for solving open region digital circuit and scattering problems due to its simplicity in modeling complex-shaped structures and inhomogeneous dielectric scatterers. However, it must deal with the practical problems of mesh truncation and the introduction of an artificial outer boundary in order to limit the number of node points to a manageable size. Therefore, the major difficulty encountered when using FEM is how to find a boundary condition operator which when applied to the artificial outer boundary mimics the asymptotic behavior of the field at infinity and yields reasonably accurate results in the interior region without the need of an exorbitantly large number of mesh points. This report is an effort to provide some techniques to deal with the FEM mesh truncation, in an efficient manner, through the introduction of three new boundary condition concepts, viz., the boundary conditions for arbitrary outer boundaries, the asymptotic boundary condition for digital circuit applications, and the higher-order asymptotic and absorbing boundary conditions. The use of generalized boundary conditions or the boundary conditions for arbitrary outer boundaries enables one to reduce the number of node points significantly and to solve larger sized problems than had been possible in the past. The asymptotic boundary condition for digital circuit applications does not suffer from the complications associated with the infinite elements and yet enables one to bring the outer boundary much closer to the structure than would be possible with a p.e.c. artificial outer boundary. The higher-order asymptotic and absorbing boundary conditions, unlike the available ABCs, e.g., the Bayliss, Gunzburger, and Turkel (BGT), which assume that in the far region the solution can adequately be represented by the first few terms of the series, require that the asymptotic representation be a combination of the lower- and higher-order terms. The higher-order boundary conditions help reduce the error in the finite element solution caused by the neglecting of the higher-order terms in other available ABC assumptions. Various investigations of scattering as well as two- and three-dimensional digital circuit problems are presented. Numerical examples are shown for a variety of scatterers and transmission line configurations. Results show that the boundary condition concepts introduced in this work yield good agreement with work published elsewhere and significant improvements in computation time and storage compared to other available methods. (123 pp.)


As the sizes of VLSI circuits increases in the future, the computational requirements for performing various computer-aided design (CAD) tasks will increase tremendously. In this thesis, we look at the application of parallel processing to computer aided design problems, with special emphasis to the problem of VLSI circuit extraction. We first describe parallel algorithms for VLSI circuit extraction on hypercube and shared memory multiprocessors. We give the performance results of the algorithms on an Intel iPSC2 hypercube and an Encore Multimax shared memory multiprocessor, for different partitioning strategies. There were two sub problems in the above research that are of general importance. The first problem is called the geometric connected component labeling problem, that arises in the combining phase of parallel extraction. We describe some practical algorithms for this problem. The second problem involves maintaining recursively partitioned data structures of points on distributed memory multiprocessors, under the operations of addition and deletion of points. This problem arises when partitioning strategies are considered, that divide a circuit so that the resulting sub regions have approximately the same number of rectangles. We describe
two algorithms for this general problem, and analyze their complexity. The next step is to take a general look at the use of hierarchical methods in computer-aided design. We describe how the benefits of hierarchical analysis and parallelism can be combined. Towards this goal, we formulate the parallelizable dependent task scheduling (PDTTS) problem, which is NP-hard. We describe a heuristic for the problem, and analyze its performance with respect to the optimal. We also consider a special case of the PDTTS problem, wherein the tasks are independent. We present an algorithm for this problem and analyze its performance to get a better bound with respect to the optimal, as compared to the general case of the problem. This theory is then applied for a case study in parallel hierarchical circuit extraction. We present some implementation results on an Encore Multimax multiprocessor. (148 pp.)


The current trend in microwave and millimeter-wave integrated circuits (MICs) is toward higher operating frequencies, high packing densities, and more stringent performance requirements. As a result, earlier models based on approximate analysis techniques are becoming insufficiently accurate for use in computer-aided design (CAD) packages. In particular, simplifying assumptions, such as the quasi-static approximation and the magnetic wall approximation, are becoming inappropriate in the analysis of microstrip discontinuities such as bends, steps, and stubs. Instead, a rigorous full-wave analysis is needed to obtain a more accurate characterization of these passive circuits. Such an analysis captures the increasingly significant effects of coupling, dispersion, and radiation. The objective of this study is to develop an asymptotic acceleration technique for the efficient evaluation of the integrals involved in the full-wave spectral domain method for analyzing microstrip discontinuity problems. (66 pp.)


Reconfiguration of memory arrays with spare rows and columns has been shown to be an NP-complete problem. Numerous heuristics for repairing memories have been recently proposed; however, no average-case analysis has been published. This paper presents the first fundamental analysis of average-case time complexities of several existing heuristics. We also present the first provably average-case polynomial time algorithm for reconfiguration of memories with spare rows and columns. The implemented algorithm runs significantly faster than existing heuristics for most cases examined. (22 pp.)


In this report, a 2-D adaptive structure based on the 1-D joint process estimator, which consists of an adaptive lattice prediction error filter followed by a set of adaptive tap-weights, is developed. The 2-D JPE is made up of a 2-D lattice structure followed by a generalized arrangement of lower tap-weights that allow the 2-D JPE to match any arbitrary unknown response. The new 2-D adaptive filter is shown to offer convergence rate improvement over the direct form 2-D adaptive filter. A drawback of the fully adaptive 2-D JPE is that it exhibits a rather high convergence floor. An analysis of this effect, which provides an overall upper bound for the floor, is presented and it is applicable to both the 1-D and 2-D JPE structures. Computational considerations involved in implementing the new 2-D JPE are also addressed. (74 pp.)

Modeling uncertainty has long been a central issue in control system design. A controller that meets the desired specifications even in the presence of appreciable modeling uncertainty is said to be robust. Parametric modeling uncertainty incorporates error as a result of inaccurately identified parameters, such as coefficients in a mathematical model that are difficult to measure or change with time. Dynamic modeling uncertainty allows for error in the plant’s dynamical order such as the effects of undermodeling. Traction control has recently experienced growing popularity in the automotive field. This report shows that control of the highly nonlinear traction control system is critically linked to knowledge of the tire/surface characteristic. (57 pp.)


For a class of single-input single-output nonlinear systems with unknown constant parameters, we present a direct model-reference adaptive control scheme that requires only output rather than full-state measurement. The nonlinearities are not required to satisfy any growth conditions. The assumptions on the linear part of the nonlinear system are the same as in the standard adaptive control problem for linear systems, which now appears as a special case of the nonlinear problem solved in this report. (39 pp.)


Various schemes for routing in high speed networks with few buffers are investigated. Deflection routing is an adaptive strategy for datagram routing which tries to diffuse congestion wherever it arises in the network. Deflection routing on a shuffle-exchange network under uniform traffic is analyzed by using approximate state equations to predict the distribution of packet states. Whenever two packets simultaneously attempt to traverse a link, a conflict resolution rule is invoked to determine which packet is deflected. It is shown that giving priority to packets closest to their destinations is the optimal conflict resolution rule, in a certain sense. The state equations, for two different priority rules, are also used to derive bounds on the probable amount of time needed for the network to empty and to explore the relationship between delay and throughput in steady state. It is demonstrated that the choice of priority rule greatly influences the performance of the network. Deflection routing is also studied on some other networks based on shuffle interconnections. The second topic is concerned with circuit-switched communication networks in which each route is two links long, and each link can carry one call at a time. No symmetry assumption is made. Simple bounds, depending on the maximum call arrival rate and the maximum sum of rates at a link, are given on the blocking probabilities. An implication is that if the maximum per-route arrival rate converges to zero with a fixed bound on the sum of rates at links, then the well-known reduced-load blocking approximation is asymptotically exact, uniformly over all network topologies. The third and final topic studied is packet routing on bounded degree networks, where the size of the buffers at each node is constrained to be small. An algorithm is presented which does packet routing on an $N$-node butterfly in time $O(\log N)$ with small constants. The algorithm is based on Ranade’s probabilistic PRAM emulation. Bounds on performance of the algorithm are proven for permutation routing and partially balanced traffic. The network is divided into $2^n$ disjoint sets of $n$ nodes, $N = n 2^n$, and $k$-partially balanced traffic is such that no given set of nodes has to send or receive more than $kn$ packets. The main results are upper
bounds on the probability that the routing time exceeds $t$ for a fixed queue size. It is shown that if $t = \Omega(\log N)$, then the probability is less than $c \alpha^t$, where $c, \alpha < 1$. Bounds on the routing time for uniform, random traffic follow as a special case of partially balanced traffic. (114 pp.)