ANALYSIS OF BOOST CONVERTER IN CONTINUOUS CONDUCTION MODE AND DISCONTINUOUS CONDUCTION MODE

BY

HYUN JAE KO

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2018

Urbana, Illinois

Adviser:

Associate Professor Pavan K. Hanumolu

Abstract

This thesis discusses a boost converter using continuous conduction mode and discontinuous conduction mode. The first part of the thesis analyzes a boost converter using continuous conduction mode with voltage mode control. A switch network which eases the analysis of the boost converter is modeled. Important transfer functions are analyzed in detail to figure out the trade-off between input variables and specifications of the boost converter. Several types of compensators are discussed to build a stable system when feedback is included. The second part of the thesis addresses a boost converter using discontinuous conduction mode. The advantages, such as fast tracking and high gain bandwidth, of using discontinuous conduction mode over continuous conduction mode are discussed.

Acknowledgments

I would like to thank my advisor, Prof. Pavan K. Hanumolu, for guiding and supporting my research through my master's degree study. Without his advice, I would not be here. Also, I would like to thank my research group members who helped me answering and discussing questions, especially Ahmed Elmallah, Nilanjan Pal, Da Wei, and Yi Zhu. Finally, I would like to thank my family for the support.

Contents

1. Introduction

Power management integrated circuits (PMICs) have become more and more important as the requirement of power efficiency in power electronics becomes higher, especially in the automotive industry. An essential PMIC component, the boost converter is a DC-DC power converter that boosts the output voltage higher than the input voltage. One of the applications of using a boost converter is to supply voltage from the battery to each individual component in the circuit such as the processor, RF circuit, audio amplifier and so on. To achieve high efficiency and robustness, using appropriate circuit topology is the key in a boost converter design.

Chapter 2 of this thesis describes the analysis and design procedure of a boost converter in continuous control mode (CCM) using voltage mode control (VMC). The chapter analyzes how to model the switching network and basic boost converter without feedback. Transfer functions are derived that will be needed to design a boost converter. The use of feedback is introduced to stabilize the whole system. Several compensators are analyzed along with their advantages. Finally, one of the compensators is used to show how to choose poles and zeros for the design.

Chapter 3 discusses a boost converter in discontinuous control mode (DCM). The chapter compares switching network models for CCM and DCM. Transfer functions of a boost converter in DCM are derived. Lastly, a boost converter in DCM using current mode control (CMC) is illustrated.

2. Boost Converter in CCM Using VMC

A boost converter in continuous control mode (CCM) using voltage mode control(VMC) is one of the most fundamental and basic boost converter designs. In this chapter, analysis and design of a boost converter using VCM are described. In Section 2.1, the basic boost converter transfer function, which will be used for any type of control mode, is explained. A switch network of a boost converter circuit is modeled so that the analysis of the circuit transfer function can be done easily and equivalently. The derivation of important transfer functions is illustrated. In Section 2.2, controller design is introduced so that the boost converter can tolerate disturbances due to input line voltage and load current. The boost converter with voltage mode control has a negative feedback to change the duty cycle itself as needed. Several compensators are introduced to design a negative feedback control. In Section 2.3, an implementation of one of the compensators is introduced.

2.1 Analysis of Boost Converter Transfer Function in CCM

Before going into details of the small-signal equivalent circuit model of the boost converter, the model of the switch network is illustrated so that the analysis of the small-signal model of the boost converter will be much easier.

In Figure 2.1, a basic boost converter with signal waveforms is shown. $V_1(t)$ and $i_2(t)$ are modeled because changing $V_1(t)$ will affect current $i_2(t)$. On the other hand, $V_2(t)$ and $i_1(t)$ are the same as capacitor voltage and inductor current, respectively. Thus, these two signals can be modeled as independent inputs to the switch network.

Figure 2.2 is the step by step derivation of modelling the switch network to an averaged switch model. The first step of modelling is to replace the transistor switch and diode with dependent voltage and current sources, respectively. $V_1(t)$ is the input signal which controls the transistor switch to be on or off. By inspection, $V_1(t)$ is zero when the transistor switch is on, and it is $V_2(t)$ when the diode is on:

$$V_1(t) = \begin{cases} 0 & 0 < t < dT_s \\ V_2(t) & dT_s < t < T_s \end{cases} \tag{2.1}$$

Current $i_2(t)$ is modeled as a voltage dependent current source. For $i_2(t)$, it is zero when the transistor switch is on, and it is $i_1(t)$ when the diode is on:

$$i_2(t) = \begin{cases} 0 & 0 < t < dT_s \\ i_1(t) & dT_s < t < T_s \end{cases} \tag{2.2}$$

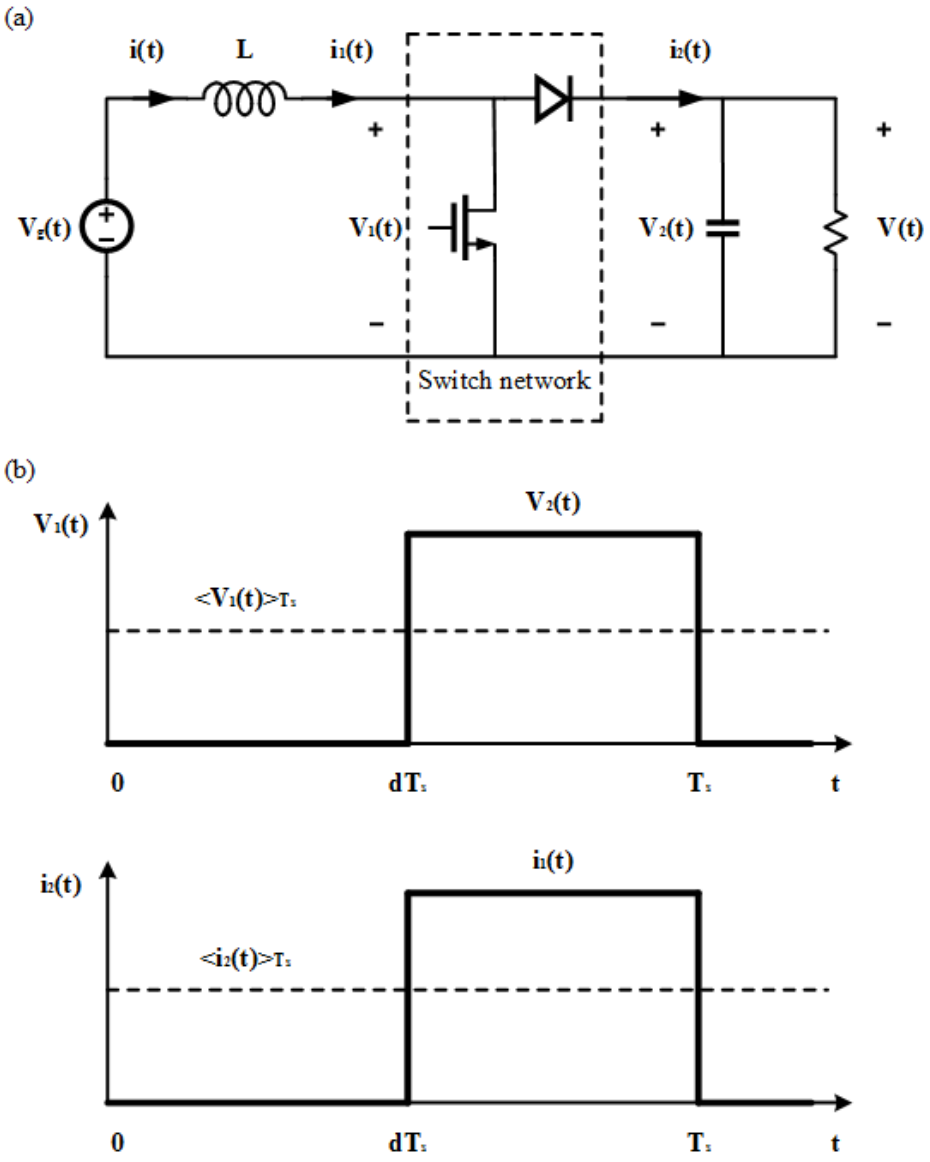


Figure 2.1 A Basic Boost Converter with Signal Waveforms

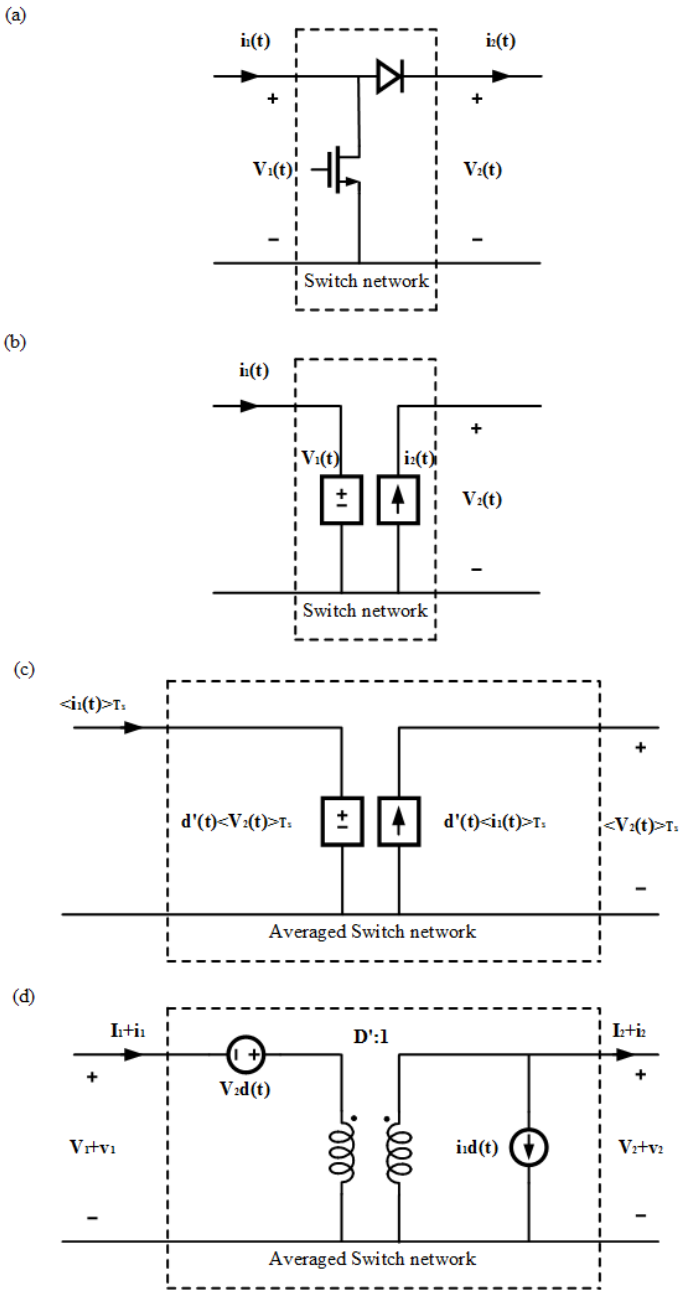


Figure 2.2 Averaged Switch Model for Boost Converter

The voltage and current source will not affect the behavior or waveforms of the circuit, so it is reasonable to modify the switch network using a voltage and a current source. Also, from Figure 2.1, average $V_1(t)$, $< V_1(t) >_{T_s}$, and average $i_2(t)$, $< i_2(t) >_{T_s}$, are

$$< V_1(t) >_{T_s} = d'(t) < V_2(t) >_{T_s} \qquad (2.3)$$
$$< i_2(t) >_{T_s} = d'(t) < i_1(t) >_{T_s}$$

where $d'(t)$ is duty cycle of boost converter. This assumption is valid when the ripples of inductor current and capacitor voltage are small during switching. The signals above are large-signal waveforms. All high-frequency ac components are removed because of the averaging effect. To be more precise on signal waveforms, the following equations have dc and low-frequency ac components:

$$\begin{gathered} < V_g(t) >_{T_s} = V_g + v_g(t) \\ d'(t) = D' - d(t) \\ < i(t) >_{T_s} = < i_1(t) >_{T_s} = I + i(t) \\ < V(t) >_{T_s} = < V_2(t) >_{T_s} = V + v(t) \\ < V_1(t) >_{T_s} = V_1 + v_1(t) \\ < i_2(t) >_{T_s} = I_2 + i_2(t) \end{gathered} \tag{2.4}$$

The voltage source has a nonlinear part and it is equal to

$$\big(D' - d(t)\big)\big(V + v(t)\big) = D'\big(V + v(t)\big) - Vd(t) - v(t)d(t) \tag{2.5}$$

In Equation (2.5), $v(t)d(t)$ is nonlinear and negligible because its variation is smaller than DC value, V. The term $Vd(t)$ is controlled by control input, which is the same as the duty cycle, and can be modeled as an independent voltage source. The term $D'\big(V + v(t)\big)$ is equal to $\big(V + v(t)\big)$ multiplied by D', which can be modeled as primary winding of an ideal transformer.

The current source, like the voltage source, is equal to

$$\big(D' - d(t)\big)\big(I + i(t)\big) = D'\big(I + i(t)\big) - Id(t) - i(t)d(t) \tag{2.6}$$

As in Equation (2.5), in Equation (2.6), $i(t)d(t)$ is nonlinear and negligible under large-signal assumption. Again, the term $Id(t)$ is controlled by control input $d(t)$ and can be modeled as an independent current source. The term $D'\big(I + i(t)\big)$ is equal to $\big(I + i(t)\big)$ multiplied by D', which can be modeled as a secondary winding of an ideal transformer.

Figure 2.3 is the DC and small-signal AC averaged model of the basic boost converter. Instead of transistor switch and diode, the switch network consists of a voltage source, current source and an ideal D': 1 transformer.

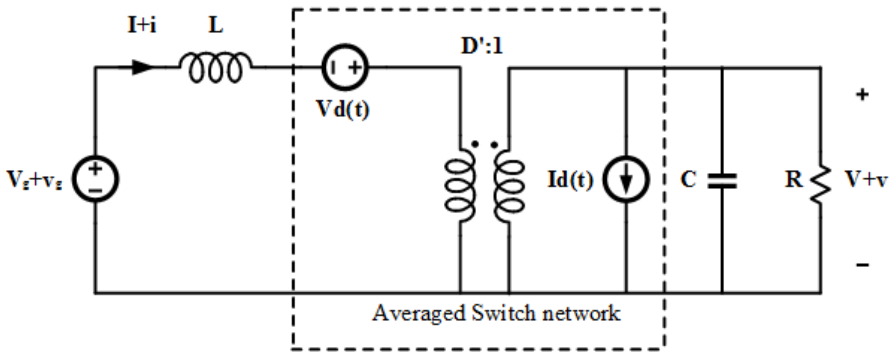


Figure 2.3 DC and Small-signal AC Averaged Model of Boost Converter

There are two input signals affecting ac output response: control input $d(s)$ and line input $V_g(s)$. Control input $d(s)$ is the feedback signal which controls the switch of boost converter to be on or off. Control input $d(s)$ is also known as the duty cycle of the power switch in a DC-DC converter. Line input $V_g(s)$ is the power input of the boost converter, which is same as V_{in}. The output $V(s)$ is controlled by these two signals as follows:

$$V(s) = G_{vd}(s)d(s) + G_{vg}(s)V_g(s) \tag{2.7}$$

where $G_{vd}(s)$ and $G_{vg}(s)$ are defined as:

$$G_{vd}(s) = \left.\frac{V(s)}{d(s)}\right|_{V_g(s)=0} \qquad G_{vg}(s) = \left.\frac{V(s)}{V_g(s)}\right|_{d(s)=0} \tag{2.8}$$

$G_{vd}(s)$ is called the control-to-output transfer function while $G_{vg}(s)$ is called the line-to-output transfer function. As Equation (2.7) suggested, control-to-output transfer function, $G_{vd}(s)$, is output voltage $V(s)$ over control input $d(s)$ when we set line input $V_g(s)$ to zero. Likewise, line-to-output transfer function, $G_{vg}(s)$, is output voltage $V(s)$ over line input $V_g(s)$ when we set control input $d(s)$ to zero.

Figures 2.4 and 2.5 are the derivation of a line-to-output transfer function, $G_{vg}(s)$, and control-to-output transfer function, $G_{vd}(s)$.

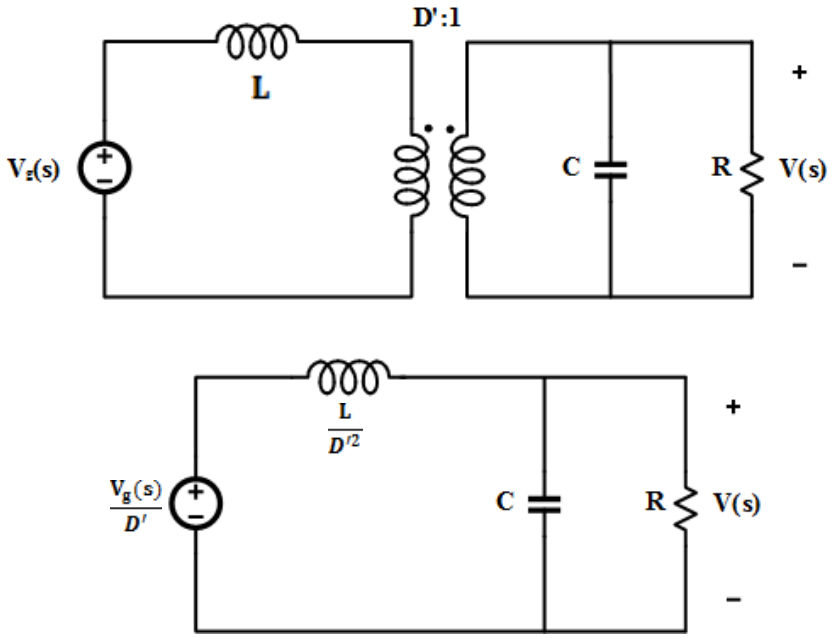


Figure 2.4 Derivation of Line-to-output Transfer Function, $G_{vg}(s)$

Figure 2.4 derives the equation for the line-to-output transfer function. Since the voltage and current sources depend on control input, $d(s)$, and the definition of line-to-output transfer function is to set control input to zero, there is no dependent source in the simplified circuit. To analyze the circuit, only converting an ideal transformer to scaled voltage independent source and inductor is needed. The equation of the bottom of Figure 2.4 is

$$G_{vg}(s) = \frac{V(s)}{V_g(s)}\bigg|_{d(s)=0} = \frac{1}{D'}\frac{R//\frac{1}{sC}}{\frac{sL}{D'^2} + (R//\frac{1}{sC})} = \frac{1}{D'}\frac{1}{1 + +s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}} = G_{g0}\frac{1}{1 + \frac{s}{Q\omega_0} + (\frac{s}{\omega_0})^2} \tag{2.9}$$

where G_{g0} is the DC gain, ω_0 is pole, and Q is the damping factor of the line-to-output transfer function.

As the definition of control-to-output transfer function, the circuit schematic will be like Figure 2.5 (a) when $V_g(s)$ is set to zero. Furthermore, the circuit schematic can be simplified by using

simplification of an ideal transformation. The voltage source will be multiplied by a factor of $\frac{1}{D'}$, while the inductor will be multiplied by a factor of $\frac{1}{D'^2}$, as shown in Figure 2.5 (b). However, analyzing the circuit in Figure 2.5 (b) is difficult. So, the circuit in Figure 2.5 (b) is the superposition of circuits in Figure 2.5 (c) and Figure 2.5 (d). Figure 2.5 (c) gives:

$$G_{vd}(s) = \frac{V(s)}{d(s)}\Big|_{V_g(s)=0} = \frac{V}{D'}\frac{R//\frac{1}{sC}}{\frac{sL}{D'^2} + (R//\frac{1}{sC})} \tag{2.10}$$

Figure 2.5 (d) gives:

$$G_{vd}(s) = \frac{V(s)}{d(s)}\Big|_{V_g(s)=0} = -I(\frac{sL}{D'^2} \;//\; \frac{1}{sC} \;//\; R) \tag{2.11}$$

The summation of Equations (2.10) and (2.11) gives the entire control-to-output transfer function:

$$\begin{aligned} G_{vd}(s) = \frac{V(s)}{d(s)}\Big|_{V_g(s)=0} &= \frac{V}{D'}\frac{R//\frac{1}{sC}}{\frac{sL}{D'^2} + (R//\frac{1}{sC})} - I(\frac{sL}{D'^2} \;//\; \frac{1}{sC} \;//\; R) \\ &= \frac{V}{D'}\frac{1 - \frac{IL}{VD'}s}{1 + s\frac{L}{D'^2R} + s^2\frac{LC}{D'^2}} \end{aligned} \tag{2.12}$$

The above equation is of the form:

$$G_{vd}(s) = G_{d0}\frac{1 - \frac{s}{\omega_z}}{1 + \frac{s}{Q\omega_0} + (\frac{s}{\omega_0})^2} \tag{2.13}$$

where G_{d0} is the DC gain, ω_z is zero, ω_0 is pole, and Q is the damping factor of the control-to-output transfer function. From Equation (2.12), the control-to-output transfer function of the boost converter has one zero lying in the right half-plane, which affects step response such that when the duty cycle increases, the diode current and the output voltage will first decrease, then increase as expected. Because of the delay, the circuit is hard to stabilize in a wide-bandwidth feedback loop. The existence of the right half-plane zero is from the inductor and its position in the circuit.

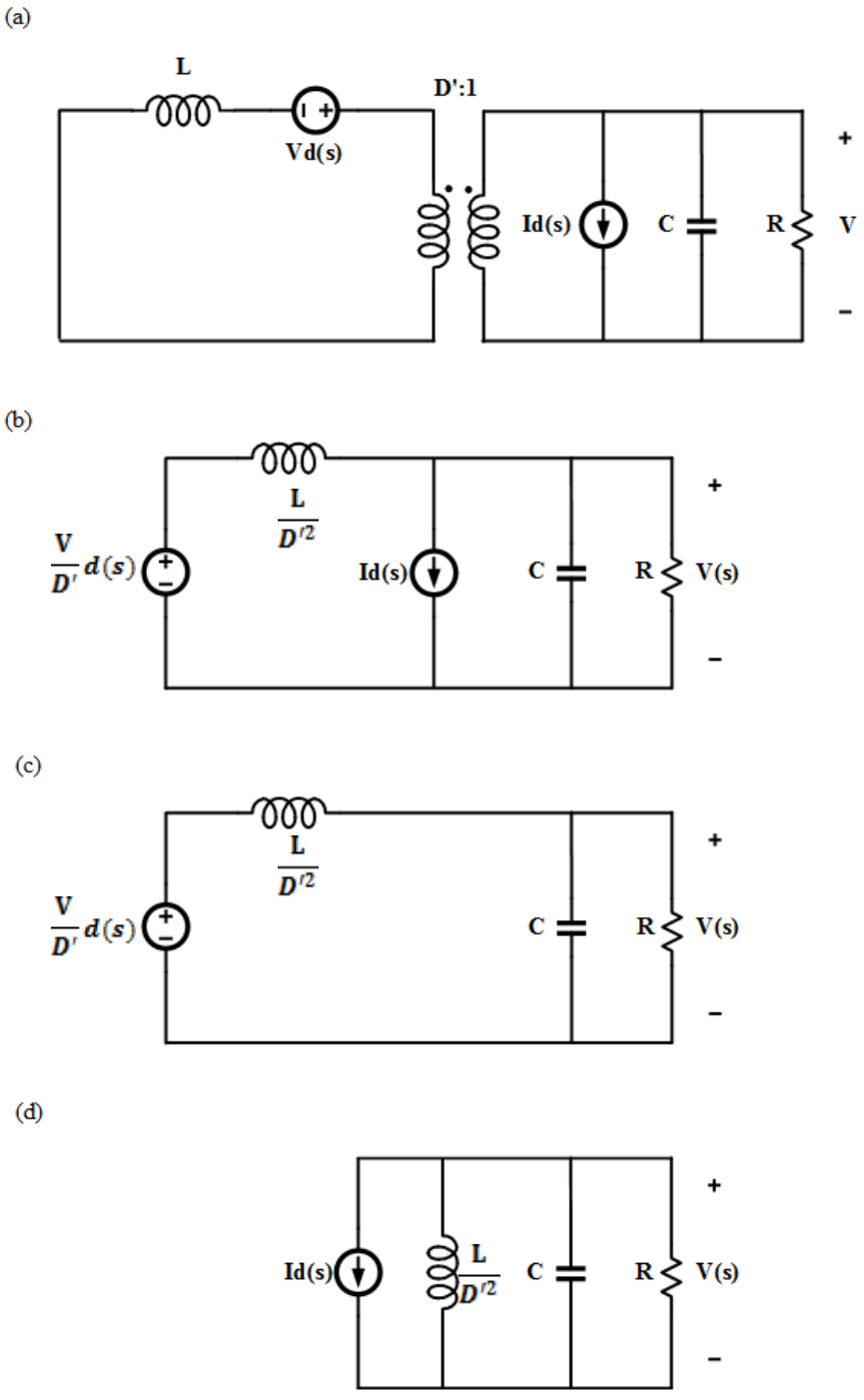


Figure 2.5 Derivation of Control-to-output Transfer Function, $G_{vd}(s)$

The converter's output impedance should be considered for output voltage because the load current variation will cause the output voltage to change [1]. Equation (2.7) is updated to

$$V(s) = G_{vd}(s)d(s) + G_{vg}(s)V_g(s) - Z_{out}(s)i_{load}(s) \tag{2.14}$$

The small-signal model for the boost converter is also updated as Figure 2.6.

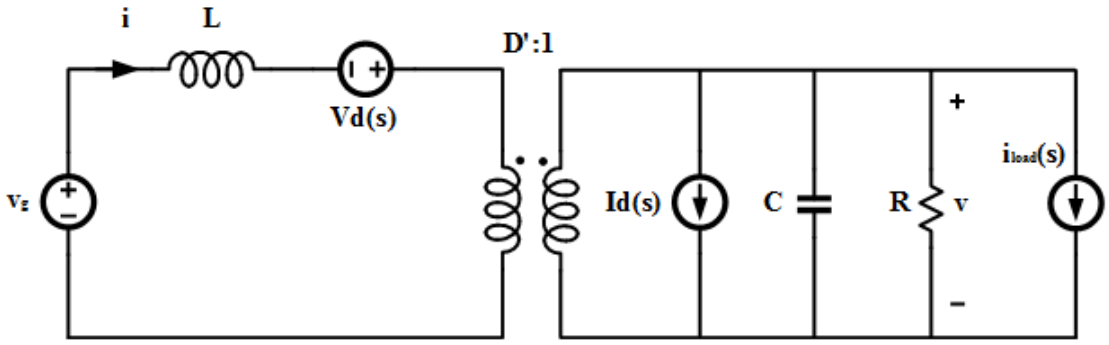


Figure 2.6 Updated Small-signal AC Averaged Model of Boost Converter

2.2 Feedback Using PID Control

In Section 2.1, a boost converter without feedback control was analyzed. In this section, feedback using PID control will be discussed.

2.2.1 Loop Gain

From Equation (2.14), input voltage V_g and load current i_{load} cause a disturbance to the output voltage V. If worst-case variations of input voltage V_g and load current i_{load} are known, the corresponding worst-case open-loop variation of output voltage V can be found. Figure 2.7 is the overall small-signal model for the boost converter with feedback.

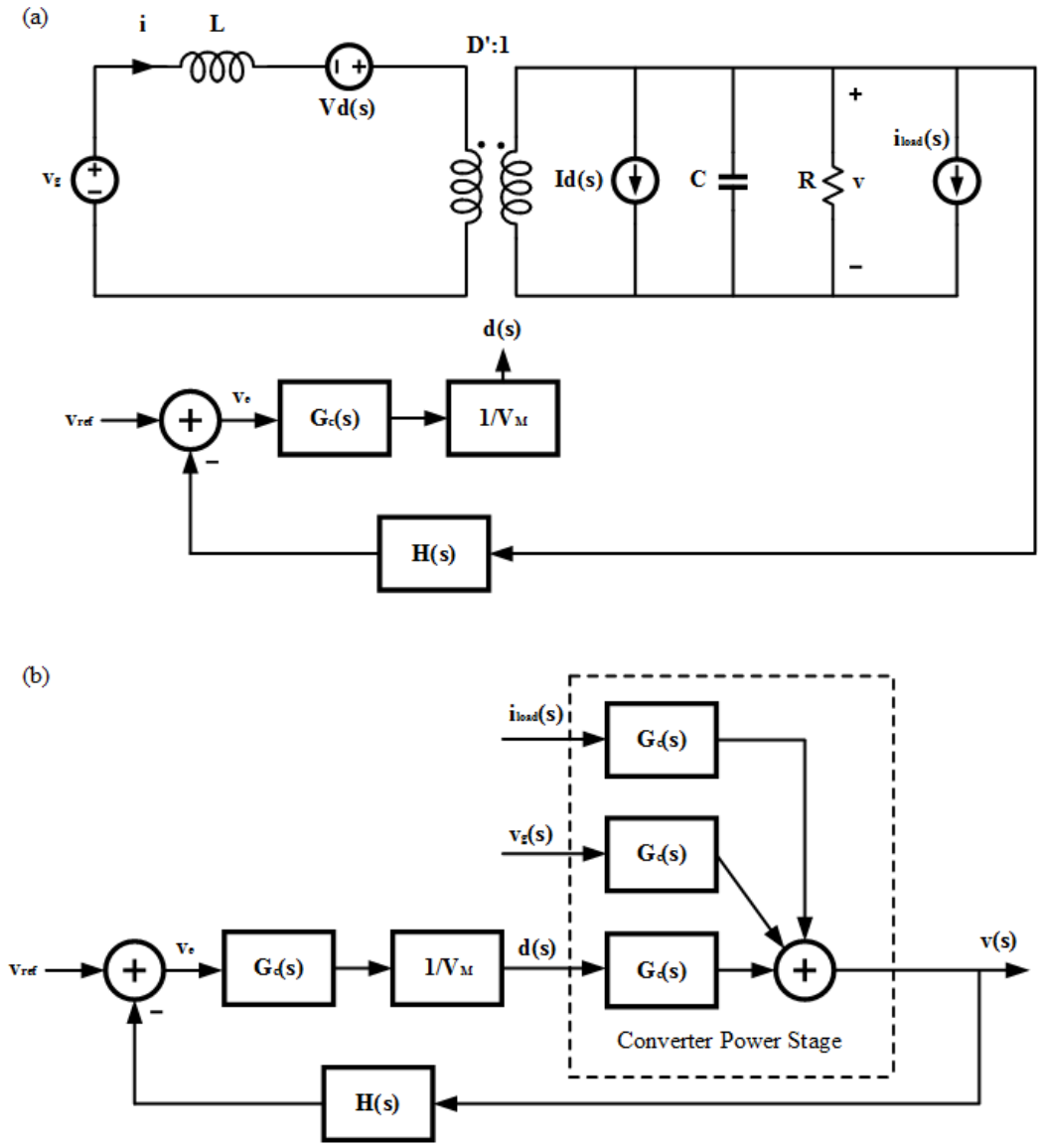


Figure 2.7 Overall Small-signal Model for Boost Converter with Feedback: (a) Equivalent Circuit, (b) Block Diagram

From Figure 2.7 (b), the output voltage variation is

$$v = v_{ref}\frac{\frac{G_c G_{vd}}{V_M}}{1+\frac{HG_c G_{vd}}{V_M}} + v_g\frac{G_{vg}}{1+\frac{HG_c G_{vd}}{V_M}} - i_{load}\frac{Z_{out}}{1+\frac{HG_c G_{vd}}{V_M}} \tag{2.15}$$

Loop gain $T(s)$ is

$$T(s) = \frac{H(s)G_c(s)G_{vd}(s)}{V_M} \tag{2.16}$$

Simplifying Equation (2.15) by plugging in Equation (2.16), the output voltage is

$$v = \frac{v_{ref}}{H}\frac{T}{1+T} + v_g\frac{G_{vg}}{1+T} - i_{load}\frac{Z_{out}}{1+T} \tag{2.17}$$

From Equation (2.17), when v_{ref} and i_{load} are set to zero, the transfer function is reduced to

$$\left.\frac{v(s)}{v_g(s)}\right|_{v_{ref}=0, i_{load}=0} = \frac{G_{vg}(s)}{1+T(s)} \tag{2.18}$$

Compared to Equation (2.9), the transfer function is reduced by a factor of $\frac{1}{1+T(s)}$ because of the feedback. For large loop gain $T(s)$, the variation in input voltage will not affect the output voltage.

Again, from Equation (2.17), when v_{ref} and v_g are set to zero, transfer function is reduced to

$$\left.\frac{v(s)}{-i_{load}(s)}\right|_{v_{ref}=0, v_g=0} = \frac{Z_{out}(s)}{1+T(s)} \tag{2.19}$$

The output impedance is also reduced by a factor of $\frac{1}{1+T(s)}$ because of the feedback. Therefore, large loop gain $T(s)$ is required to reduce the disturbance from input voltage variation v_g and output load current variation i_{load}.

For the transfer function from the reference input v_{ref} to output v, the equation is

$$\left.\frac{v(s)}{v_{ref}(s)}\right|_{v_g=0, i_{load}=0} = \frac{1}{H(s)}\frac{T(s)}{1+T(s)} \tag{2.20}$$

When loop gain $T(s)$ is much greater than 1, Equation (2.20) becomes

$$\left.\frac{v(s)}{v_{ref}(s)}\right|_{v_g=0, i_{load}=0} \approx \frac{1}{H(s)} \tag{2.21}$$

The equation above suggests that compensator gain $G_c(s)$, pulse-width modulator gain V_M and line-to-output transfer function $G_{vd}(s)$ are independent of reference input to output gain when loop gain $T(s)$ is large enough.

The loop gain will not always be large. As the frequency increases, the loop gain amplitude decreases. In many boost converter applications, the crossover frequency for the boost converter is below 100 kHz. The loop gain could be designed so that under crossover frequency the loop gain is compatibly larger than 1. For line-to-output transfer function and output impedance, when the operating frequency is below crossover frequency, the denominator of transfer functions, $1+T(s)$, is equivalent to the loop gain $T(s)$. The disturbance transfer function for line-to-output and that for output impedance are decreased by a factor of $\frac{1}{T(s)}$.

The conclusion of the analysis above is that large loop gain T(s) is beneficial in the way that the large loop gain not only reduces the disturbance from input voltage variation and output load current variation to output voltage, but also makes the circuit insensitive to forward path gain, which makes the design easier.

2.2.2 Stability

Adding a feedback loop to a circuit causes the new system to be unstable. From the analysis of the boost converter transfer function above, the open loop transfer function of the boost converter contains a right half-plane zero, which will appear in the closed loop transfer function. Although the open loop boost converter transfer function has no right half-plane pole, a right half-plane pole might appear in the closed loop system. These undesired right half-plane poles and zeros make the feedback loop unable to regulate stably, and cause the system to oscillate. Even if the poles and zeros are placed in the region so that the feedback system is stable, it is still possible for the feedback system to experience ringing at the output and overshoot for transient response.

There are mainly two methods to test stability: Nyquist test and phase margin test. Nyquist test is simple compared to phase margin test, but phase margin test is much more accurate. The computation of phase margin is the phase of the loop gain at crossover frequency plus 180°. However, if there is a right half-plane pole, the phase margin test cannot verify the stability of the system. For a boost converter, there is no right half-plane pole, so the phase margin test can be used instead of Nyquist test.

Normally, phase margin is set to more than 45° to have resonant poles with high damping factor Q near crossover frequency and to ensure the system is stable. As the phase margin decreases,

damping factor Q increases, causing ringing longer. When phase margin is below zero, the whole system is unstable.

2.2.3 Compensator Design

To design a boost converter, there are five most important specifications that should be considered: line regulation, load regulation, transient response, overshoot and ringing. Line regulation is the ability of the power converter to maintain the voltage at a desired value when the input voltage is swept. Equation (2.18), the same as the line-to-output transfer function, is the corresponding equation for line regulation. From Equation (2.18), increasing the magnitude of the loop gain reduces the output voltage ripple caused by variation in input voltage. Load regulation is the ability of the power converter to maintain the voltage at a desired value when the output load current is swept. Equation (2.19), the same as the output impedance transfer function, is the corresponding equation for load regulation. Equation (2.19) also suggests that increasing the magnitude of the loop gain reduces the output voltage ripple caused by variation in output load current. Transient response time is the time required for the feedback loop of the power converter to regulate the output voltage back in a certain range when there is a large step in input voltage or output current. The crossover frequency of the closed loop system determines the transient response time, and the higher the crossover frequency, the faster the transient response time. Overshoot and ringing can be reduced by giving sufficient phase margin, as mentioned in Section 2.2.2.

Three types of compensator are discussed below to better meet specifications. These three compensators are lead PD compensator, lag PI compensator and PID compensator.

The advantage of a lead PD compensator is to increase the phase margin. A lead PD compensator consists of two paths: proportional and derivative. The proportional path has constant gain to output while the derivative path differentiates the error signal between reference and feedback signals. A lead PD compensator introduces a zero placed below the crossover frequency such that the overall phase margin is increased. Not only the phase margin but also the gain increases when a zero is introduced to the system. The loop gain at crossover frequency should remain the same. In practice, the gain of a real amplifier drops as frequency increases, which means the compensator transfer function $G_c(s)$ has high-frequency poles. These high-frequency poles attenuate the high-frequency noise. The lead PD compensator transfer function has a low-

frequency zero and high-frequency poles. Equation (2.22) is the lead PD compensator transfer function with single pole.

$$G_c(s) = G_{c0}\frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}} \tag{2.22}$$

From the equation, the maximum phase is at the frequency of the geometrical mean of pole and zero, and is equal to

$$f_{max} = \sqrt{f_z f_p} \tag{2.23}$$

The compensator should be designed such that maximum frequency equals the desired loop gain crossover frequency.

$$\theta = \angle f_{G_c,max} = \tan^{-1}\left(\frac{\sqrt{\frac{f_p}{f_z}} - \sqrt{\frac{f_z}{f_p}}}{2}\right) \tag{2.24}$$

Rearranging Equation (2.24) leads to:

$$\frac{f_p}{f_z} = \frac{1+\sin(\theta)}{1-\sin(\theta)} \tag{2.25}$$

The loop gain crossover frequency f_c can be related to f_z and f_p by Equations (2.25) and (2.26).

$$f_p = f_c\sqrt{\frac{1+\sin(\theta)}{1-\sin(\theta)}} \tag{2.26}$$

$$f_z = f_c\sqrt{\frac{1+\sin(\theta)}{1-\sin(\theta)}} \tag{2.27}$$

In this way, the crossover frequency does not change even though pole and zero frequencies change.

The second type of compensator, lag PI compensator, increases low-frequency loop gain. This enables better regulation of the output at a frequency below the crossover frequency. A lag PI

compensator consists of two paths: proportional and integral. The inverted zero integrates the error signal at low frequencies. The equation for the lag PI compensator is as follows:

$$G_c(s) = G_{c\infty}(1 + \frac{\omega_L}{s}) \tag{2.28}$$

Because of the inverted zero, the Bode plot of the transfer function has a slope of -20 dB/dec at low frequency. When zero frequency f_L is set to be much smaller than crossover frequency, the phase margin will not be affected. Then the DC gain of the transfer function can be large, which is good for reducing the effect of disturbance on output. The loop gain without compensation is

$$T_u(s) = \frac{T_{u0}}{(1 + \frac{s}{\omega_0})} \tag{2.29}$$

With the compensation transfer function of Equation (2.29), the overall compensated loop gain is $T(s) = T_u(s)G_c(s)$. At high frequencies, the compensated loop gain can be approximately equal to

$$T(s) \approx \frac{T_{u0}G_{c\infty}}{\frac{f}{f_0}} \tag{2.30}$$

At crossover frequency, the loop gain should be designed to be unity. This gives the following relationship between crossover frequency and other parameters:

$$f_c \approx T_{u0}G_{c\infty}f_0 \tag{2.31}$$

Thus, the compensator gain is

$$G_{c\infty} = \frac{f_c}{T_{u0}f_0} \tag{2.32}$$

The last type of compensator is a PID compensator, which is the combination of lead PD compensator and lag PI compensator. Because of the combination, the PID compensator has advantages over other compensators: wide bandwidth and zero steady-state error. At low frequency, the lag PI compensator dominates and integrates the error signal. This results in large loop gain and accurate regulation at low frequency. At high frequency, the lead PD compensator improves phase margin and stabilizes the whole system. The transfer function of the PID compensator is

$$G_c(s) = G_c \frac{\left(1+\frac{s}{\omega_z}\right)(1+\frac{\omega_L}{s})}{(1+\frac{s}{\omega_{p1}})(1+\frac{s}{\omega_{p2}})} \tag{2.33}$$

In Section 2.3, an implementation of a PID compensator will be shown with the proper way to choose poles and zeros.

2.3 Type-III Voltage Mode Compensator

To implement a PID compensator, a type-III voltage mode compensator is most widely used. Figure 2.8 is the conventional type-III voltage mode compensator with gain curve [2].

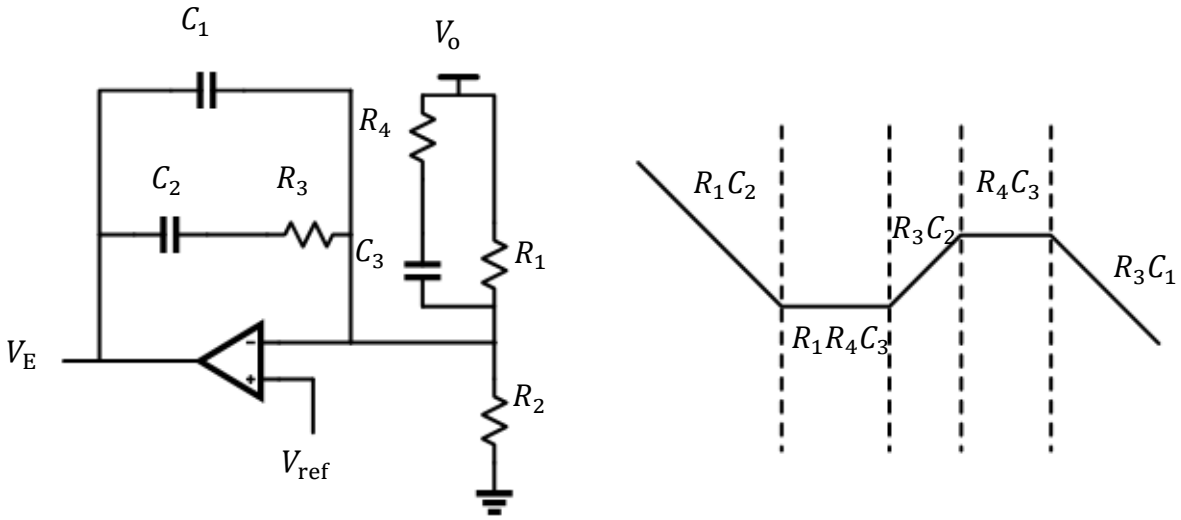


Figure 2.8 Type-III Voltage Mode Compensator with Gain Curve

The transfer function for the voltage mode type-III compensator is

$$\frac{V_E}{V_o} = -\frac{1}{sR_1(C_1+C_2)} \frac{1+sR_3C_2}{1+sR_3\frac{C_1C_2}{C_1+C_2}} \frac{1+s(R_1+R_4)C_3}{1+sR_4C_3} \tag{2.34}$$

Assuming $C_2 \gg C_1$, $R_1 \gg R_4$, Equation (2.34) can be simplified as:

$$\frac{V_E}{V_o} = -\frac{1}{sR_1C_1} \frac{1+sR_3C_2}{1+sR_3C_1} \frac{1+sR_1C_3}{1+sR_4C_3} \tag{2.35}$$

$$= -\frac{\frac{R_3}{R_1}+\frac{1}{sR_3C_2}}{1+sR_3C_1} \frac{1+sR_1C_3}{1+sR_4C_3}$$

$$\approx G_c \frac{1+sR_1C_3}{1+sR_4C_3} \frac{1+\frac{1}{sR_3C_2}}{1+sR_3C_1}$$

$$= G_c \frac{\left(1 + \frac{s}{\omega_z}\right)(1 + \frac{\omega_L}{s})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})}$$

where $\omega_z = \frac{1}{R_1 C_3}$, $\omega_L = \frac{1}{R_3 C_2}$, $\omega_{p1} = \frac{1}{R_4 C_3}$, $\omega_{p2} = \frac{1}{R_3 C_1}$.

3. Boost Converter in DCM

Several power converter designs in continuous control mode (CCM) are difficult because of the trade-off between the power efficiency and the size of the chip components [3], [4], [5]. Generally, a smaller inductor results in a converter operating at up to thousands of MHz. High operating frequency causes switching loss and lowers the efficiency when the load resistance is small. A boost converter in DCM has higher loop bandwidth than one in CCM. Also, the boost converter in DCM is smaller because it has smaller inductor. On the other hand, the boost converter in DCM has lower efficiency and a larger ripple current at output load.

In Section 3.1, analysis of the conversion ratio of a boost converter is discussed to verify the boundary of CCM and DCM. In Section 3.2, discontinuous control mode and its small signal model are explained. A switch network of the boost converter is modeled first. In Section 3.3, a boost converter in DCM using current mode control is illustrated.

3.1 Analysis of Conversion Ratio of Boost Converter

In Chapter 2, the circuit analysis was in continuous conduction mode. In this section, the boundary of CCM and DCM is derived to summarize the conversion ratio of a boost converter. Figure 3.1 is a simple boost converter.

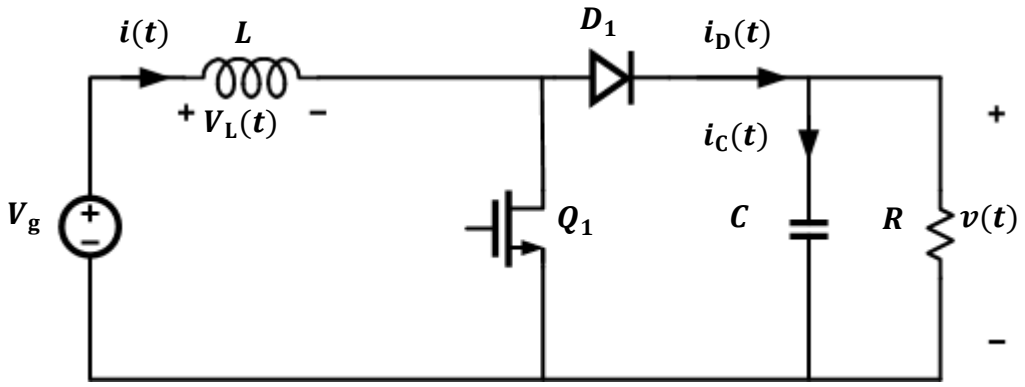


Figure 3.1 Simple Boost Converter

In CCM, the boost converter has two phases, as shown in Figure 3.2. When the power switch is Q_1 on, the diode D_1 is off, which is Figure 3.2 (a). Figure 3.2 (b) is the phase when the power switch Q_1 is off and the diode D_1 is on.

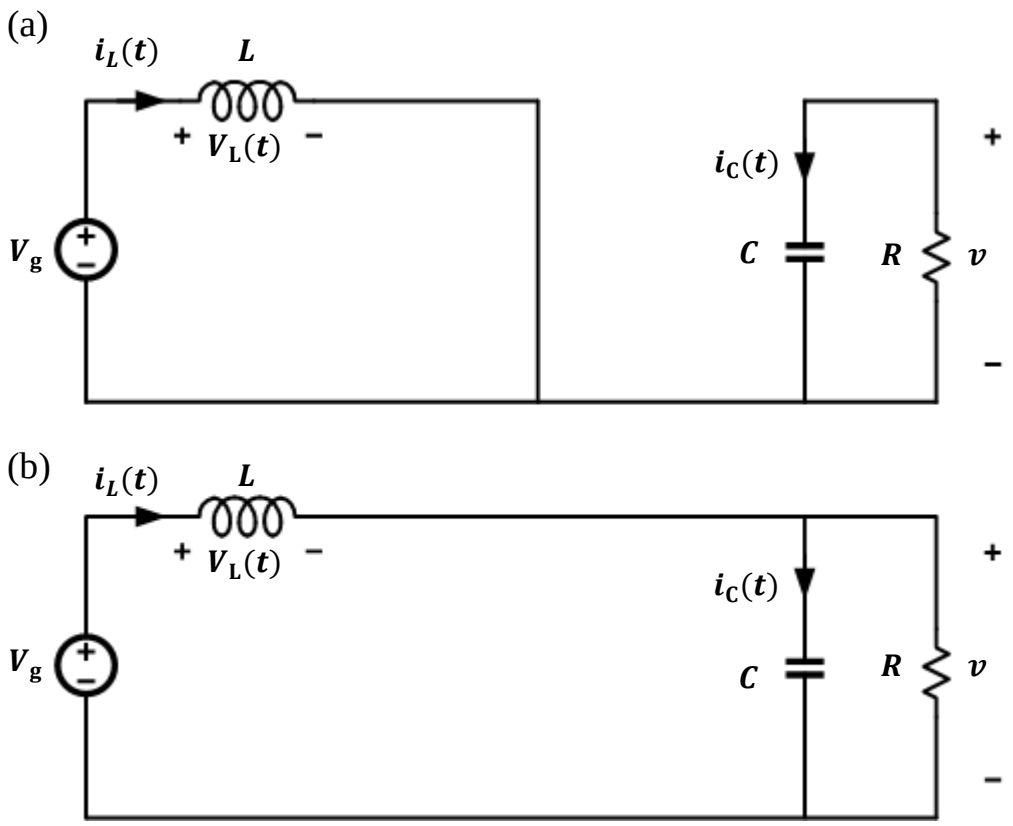


Figure 3.2 Boost Converter in CCM in (a) Phase 1, (b) Phase 2

From Phase 1, the voltage across the inductor v_L and the current through the capacitor i_c can be written as

$$v_L = V_g \tag{3.1}$$
$$i_c = -\frac{V}{R}$$

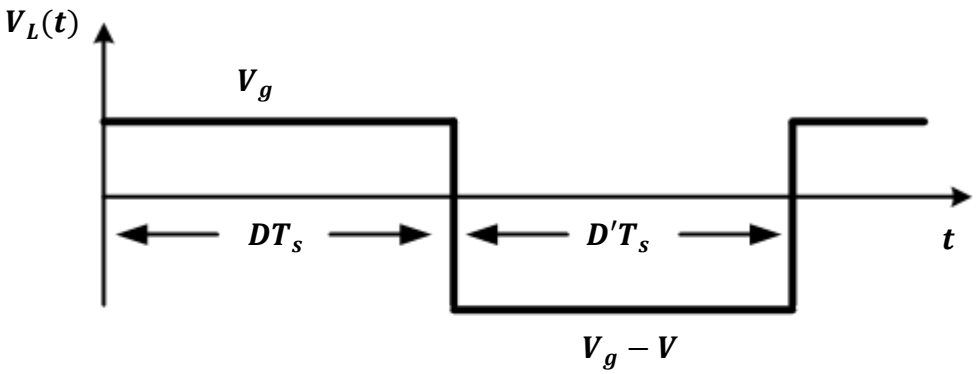
By using KVL and KCL at Phase 2, the inductor voltage and capacitor current are

$$v_L = V_g - V \tag{3.2}$$
$$i_c = I - \frac{V}{R}$$

where voltage $V \approx v$ and $I \approx i_L$ using the small ripple approximation.

From Equations (3.1) and (3.2), the inductor voltage and capacitor current waveforms are shown in Figure 3.3.

(a)



(b)

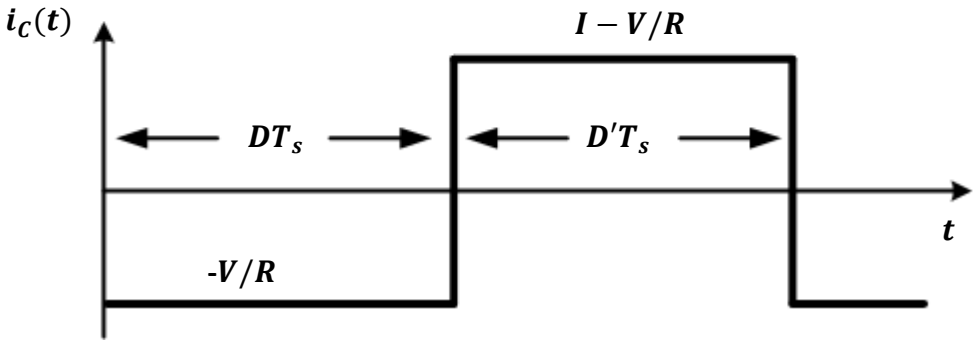


Figure 3.3 Inductor Voltage and Capacitor Current Waveforms of Boost Converter in CCM

By applying volt-second balance to the inductor over one switching period, the relationship between V and V_g is

$$\int_0^{T_s} v_L(t)dt = V_g DT_s + (V_g - V)D'T_s \tag{3.3}$$

Equation (3.3) equals to zero because the average voltage of the inductor is zero. This leads to

$$V_g(D + D') - VD' = 0 \tag{3.4}$$

By plugging in $D + D' = 1$, the equation is simplified as

$$V = \frac{V_g}{D'} = \frac{V_g}{1 - D} \tag{3.5}$$

The conversion ratio $M(D)$ is the ratio of the output voltage V to the input voltage V_g and is equal to

$$M(D) = \frac{1}{1-D} \tag{3.6}$$

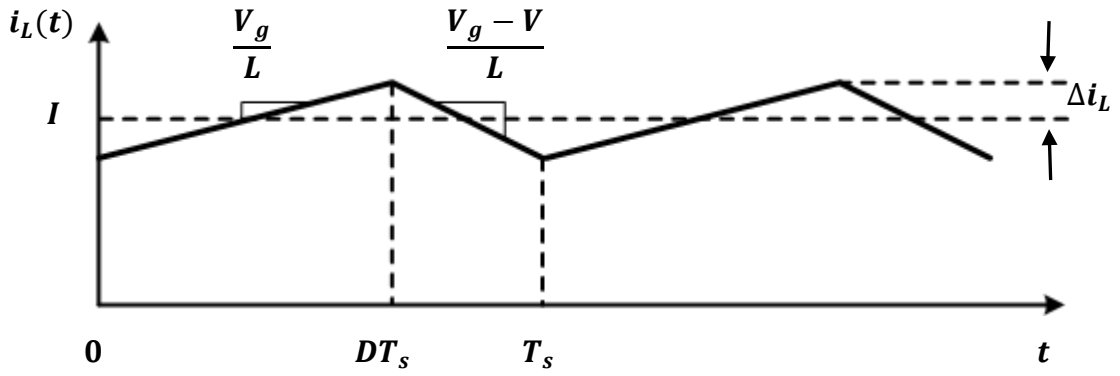


Figure 3.4 Inductor Current Waveforms of Boost Converter in CCM

Figure 3.4 is the inductor current waveform of a boost converter. The inductor current ripple at Phase 1 is related to the voltage across the inductor v_L and inductance L:

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g}{L} \tag{3.7}$$

The inductor current ripple at Phase 2 is

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} = \frac{V_g - V}{L} \tag{3.8}$$

From Figure 3.4, the current ripple can be written as

$$\Delta i_L = \frac{V_g}{2L} DT_s \tag{3.9}$$

When the average current through the inductor is greater than the current ripple, the circuit is in CCM. However, when the average current is smaller than the current ripple, the circuit is in DCM and a new phase is introduced. Once the current through the inductor goes to zero, the current will stay constant at zero until a new period starts. The revised phases and inductor and diode current waveforms of a boost converter in DCM are shown in Figures 3.5 and 3.6.

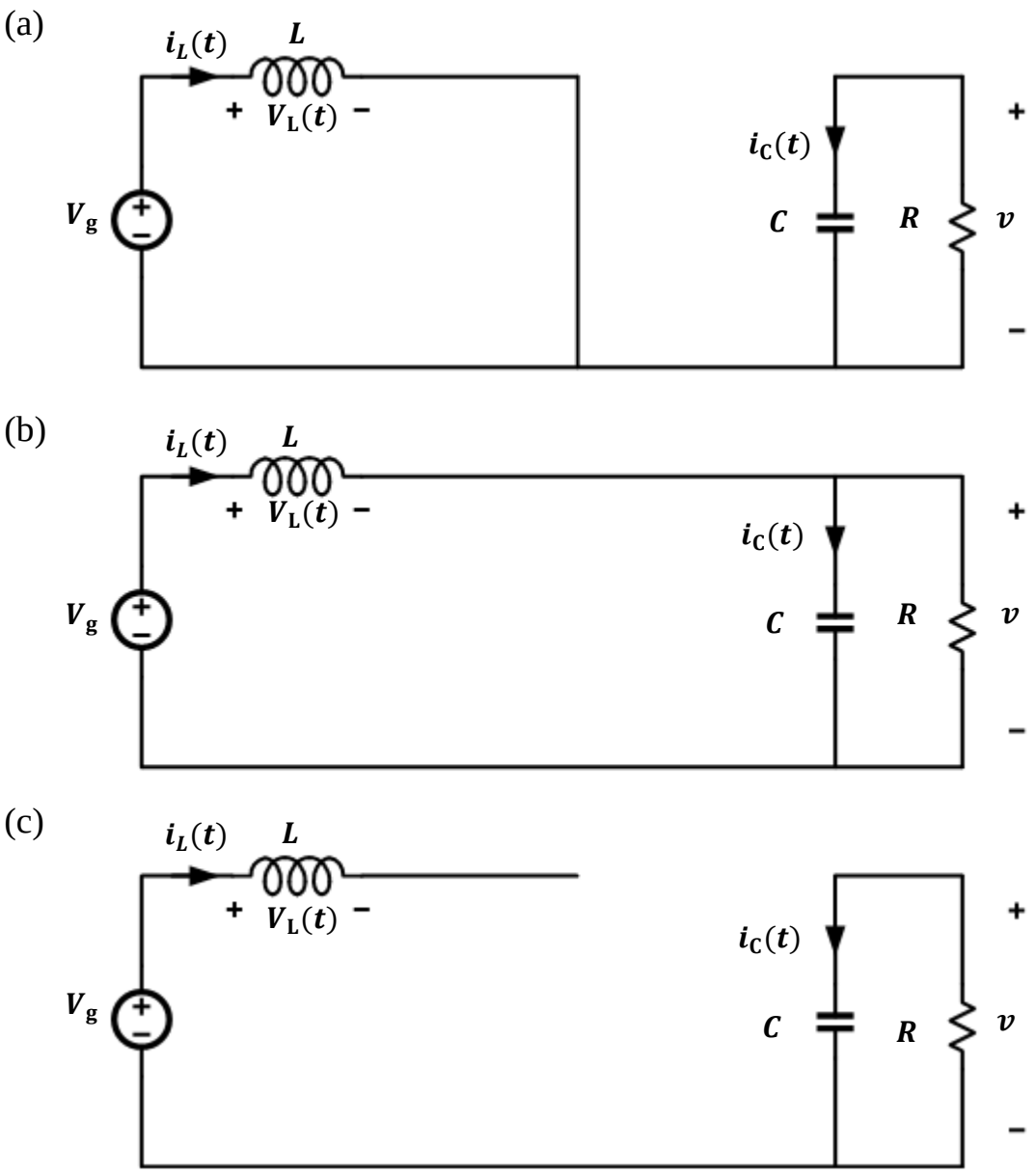


Figure 3.5 Boost Converter in DCM in (a) Phase 1, (b) Phase 2, (c) Phase 3

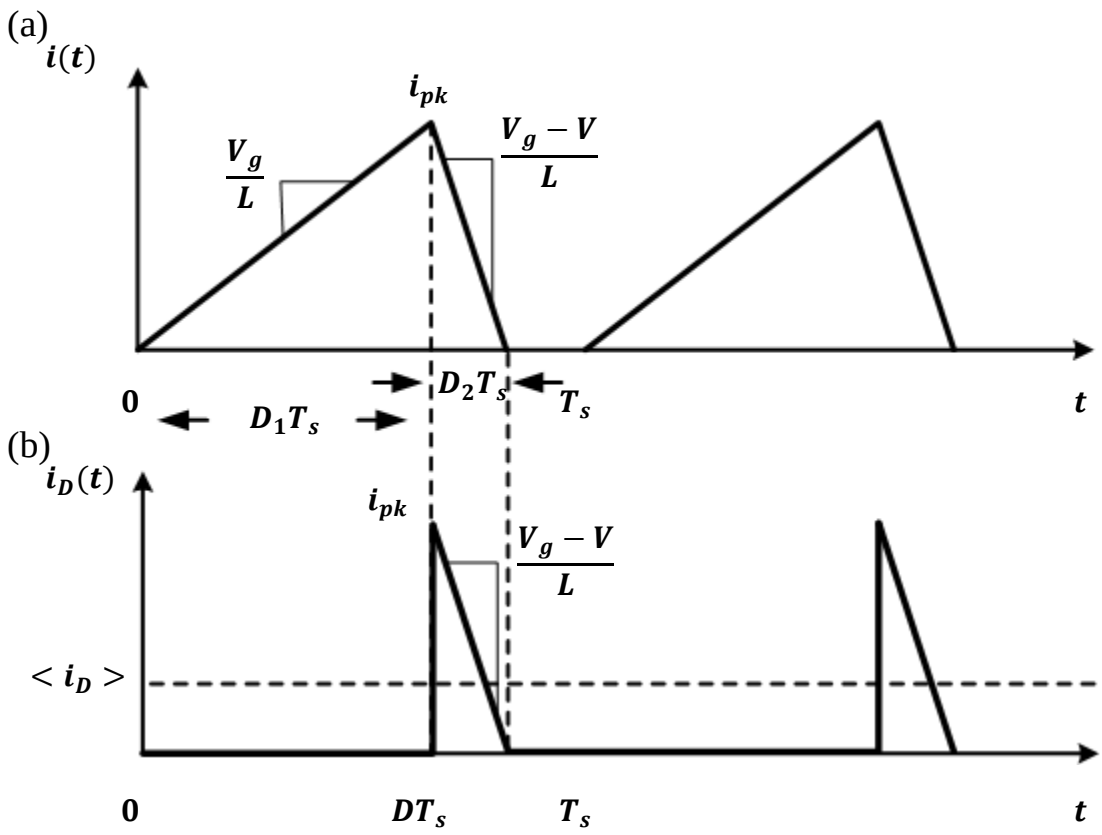


Figure 3.6 Inductor and Diode Current Waveforms of Boost Converter in DCM

From Figure 3.6, the maximum current is

$$i_{pk} = \frac{V_g}{L} D_1 T_s \tag{3.10}$$

The average diode current $< i_D >$ is

$$< i_D >= \frac{1}{T} \int_0^{T_s} i_D(t) dt = \frac{1}{2} i_{pk} D_2 T_s \tag{3.11}$$

Combining Equations (3.10) and (3.11) gives

$$< i_D >= \frac{V_g D_1 D_2 T_s}{2L} = \frac{V}{R} \tag{3.12}$$

With volt-second balance, the duty cycle of Phase 2 can be written as

$$D_2 = \frac{V_g}{V - V_g} D_1 \tag{3.13}$$

By inserting Equation (3.13) into Equation (3.12), a quadratic equation comes out

$$V^2 - VV_g - \frac{{V_g}^2 {D_1}^2}{K} = 0 \tag{3.14}$$

where $K = \frac{2L}{RT_s}$. The solution of this quadratic equation is

$$\frac{V}{V_g} = \frac{1 \pm \sqrt{1 + \frac{4{D_1}^2}{K}}}{2} \tag{3.15}$$

The overall conversion ratio of a boost converter M is

$$M = \frac{1 \pm \sqrt{1 + \frac{4{D_1}^2}{K}}}{2} \tag{3.16}$$

3.2 Analysis of Boost Converter Transfer Function in DCM

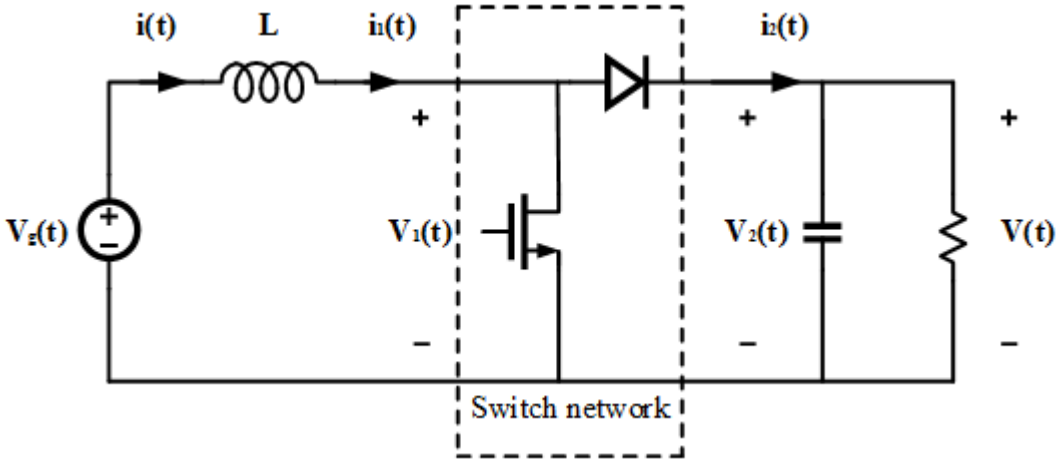


Figure 3.7 Boost Converter Circuit Schematic

Consider the basic boost converter circuit schematic in Figure 3.7. The average switch network input voltage $< v_1(t) >_{T_s}$ is the same as the average voltage across the transistor, and is equal to

$$< v_1(t) >_{T_s} = d_1(t) \cdot 0 + d_2(t) < v(t) >_{T_s} + d_3(t) < v_g(t) >_{T_s} \tag{3.17}$$

where $d_1(t)$ is the duty cycle of Phase 1, $d_2(t)$ is the duty cycle of Phase 2 and $d_3(t)$ is the duty cycle of Phase 3. The property of these duty cycles, $d_3(t) = 1 - d_1(t) - d_2(t)$, simplifies Equation (3.17) to

$$< v_1(t) >_{T_s} = d_2(t) < v(t) >_{T_s} + (1 - d_1(t) - d_2(t)) < v_g(t) >_{T_s} \tag{3.18}$$

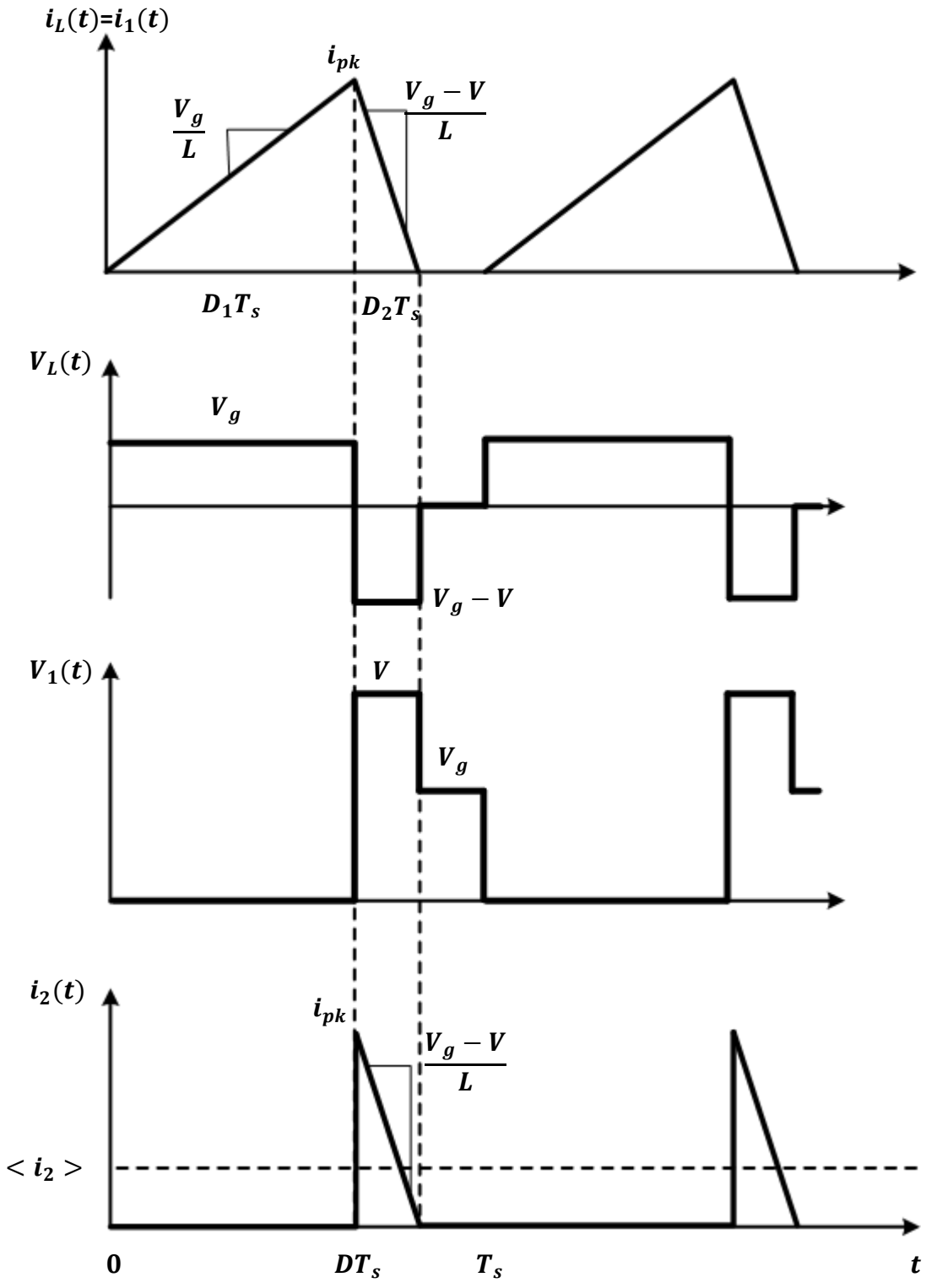


Figure 3.8 Switch Network Voltage and Current Waveforms

The average voltage of the output port of the switch network $< v_2(t) >_{T_s}$ is same as the average output of the boost converter circuit $< v(t) >_{T_s}$.

$$< v_2(t) >_{T_s} = < v(t) >_{T_s} \tag{3.19}$$

By integrating the current waveform $i_1(t)$ in Figure 3.8, the average switch network input current $< i_1(t) >_{T_s}$ is equal to

$$< i_1(t) >_{T_s} = \frac{1}{T_s}\int_0^{T_s} i_1(t)dt = \frac{1}{2} i_{pk}(d_1(t) + d_2(t)) \tag{3.20}$$

Combining Equations (3.10) and (3.20) gives

$$< i_1(t) >_{T_s} = \frac{(d_1(t)^2 + d_1(t)d_2(t))T_s}{2L} < v_g(t) >_{T_s} \tag{3.21}$$

The current $< i_2(t) >_{T_s}$ can be found using the similar analysis of the current $< i_1(t) >_{T_s}$:

$$< i_2(t) >_{T_s} = \frac{d_1(t)d_2(t)T_s}{2L} < v_g(t) >_{T_s} \tag{3.22}$$

Equations (3.18), (3.19), (3.21) and (3.22) are the average voltage and current equations for the switch network in a DCM boost converter. To find the relationship among those voltage and current signals, one of the duty cycles should be substituted. Since there is no net charge on the inductor over a switching period, the average inductor voltage should be zero:

$$< v_L(t) >_{T_s} = d_1(t) < v_g(t) >_{T_s} + d_2(t)\big(< v_g(t) >_{T_s} - < v(t) >_{T_s}\big) = 0 \tag{3.23}$$

From Equation (3.23), duty cycle $d_2(t)$ can be written as

$$d_2(t) = \frac{d_1(t) < v_g(t) >_{T_s}}{< v(t) >_{T_s} - < v_g(t) >_{T_s}} \tag{3.24}$$

Plugging in Equation (3.24) into Equations (3.18) gives

$$< v_1(t) >_{T_s} = \frac{< v(t) >_{T_s} < v_g(t) >_{T_s}}{< v(t) >_{T_s} - < v_g(t) >_{T_s}} \tag{3.25}$$

Using Equations (3.21) and (3.25), the relation between the current $< i_1(t) >_{T_s}$ and the voltage $< v_1(t) >_{T_s}$ can be found

$$< i_1(t) >_{T_s} = \frac{d_1(t)^2 T_s}{2L} < v_1(t) >_{T_s} \tag{3.26}$$

Equation (3.26) is in the form of Ohm's law. Thus, when it is in the low-frequency range, the switch network can be modeled as a resistive component and has effective resistance R_e

$$R_e(d_1) = \frac{2L}{{d_1}^2 T_s} \tag{3.27}$$

The equivalent circuit of the modeled switch network is shown in Figure 3.9

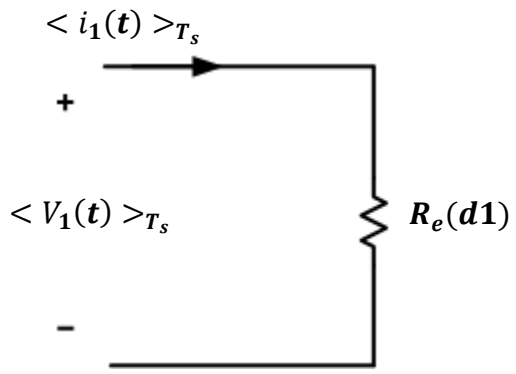


Figure 3.9 Equivalent Circuit of Switch Network of the Input Port

$$< v_2(t) >_{T_s} < i_2(t) >_{T_s} = \frac{< v_1(t) >_{T_s}^{\,2}}{R_e(d_1)} = < p(t) >_{T_s} \tag{3.28}$$

Equation (3.28) suggests that the power consumed by the effective resistor is equal to the power of the output port of the switch network model. Using the relationship shown in Equation (3.28), the switch network model is revised as shown in Figure 3.10, and Figure 3.11 shows the small-signal model for boost converter in DCM.

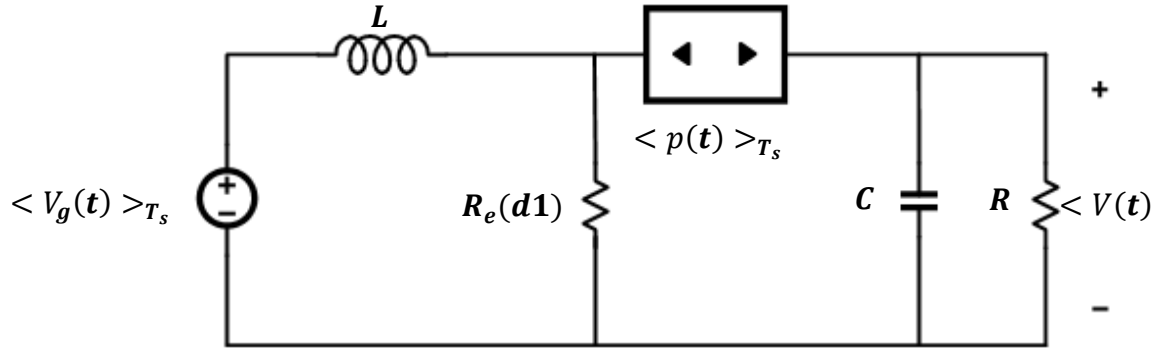


Figure 3.10 Equivalent Circuit of Switch Network of the Input Port

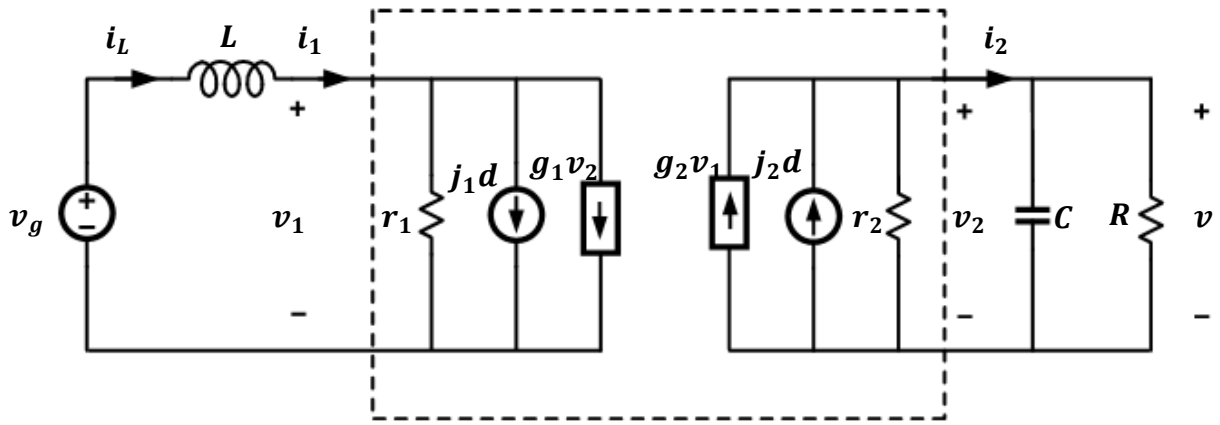


Figure 3.11 Small-signal Model for Boost Converter in DCM

The control-to-output transfer function and the line-to-output transfer function of Figure 3.11 are

$$G_{vd}(s) = \frac{v(s)}{d(s)}\Big|_{v_g=0} = \frac{G_{d0}}{1+\frac{s}{\omega_p}} \tag{3.29}$$

$$G_{vg}(s) = \frac{v(s)}{v_g(s)}\Big|_{d=0} = \frac{G_{g0}}{1+\frac{s}{\omega_p}} \tag{3.30}$$

where $G_{d0} = j_2(R//r_2) = \frac{2V}{D}\frac{M-1}{2M-1}$, $\omega_p = \frac{1}{(R//r_2)C} = \frac{2M-1}{(M-1)RC}$, $G_{g0} = g_2(R//r_2) = M$, and M is the conversion ratio of the boost converter [6], [7].

3.3 Boost Converter in DCM Using CMC

The advantages of VMC are good noise margin and cross-regulation for multiple output supplies. On the other hand, one disadvantage of VMC is that the output needs to sense the change in load or line and use the feedback loop to correct the change, which responds slowly. Another disadvantage is that VMC introduces two poles, one of which is a dominant low frequency pole, and a zero to compensate. Current mode control (CMC) solves the drawbacks of VMC. Because one of the properties of the inductor is that the inductor current is determined by the input and the output voltage, CMC immediately responds to the change in the line input voltage or the load current. Also, the error amplifier senses a current output rather than the voltage. This allows the filter to only have a single pole, which makes compensation easier and enables gain bandwidth than the voltage-mode control.

There are mainly two kinds of CMC: peak current mode control (PCMC) and valley current mode control (VCMC). In [8], analysis and simulation results show that both PCMC and VCMC provide active damping, which effectively removes the RHP poles. VCMC has an advantage over PCMC for operating at low duty cycle. PCMC is difficult to operate at low duty cycle because of the switching noise.

4. Conclusion

This thesis discusses different boost converter design topologies and analyzes the stability using small signal analysis. A designer needs to choose one of the topologies according to which specification is most important in the desired application. A boost converter in CCM is generally used to achieve higher efficiency while a boost converter in DCM is used to achieve smaller dimension of the circuit. For a boost converter in DCM, current mode control solves the drawbacks of voltage mode controls.

References

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, Springer, New York, NY, 2001.

[2] *Demystifying Type II and Type III Compensator Using Op-Amp and OTA for DC/DC Converters*, Texas Instruments, Inc., 2014. Available at: http://www.ti.com/lit/an/slva662/slva662.pdf

[3] T. Y. Man, "A 0.9-V input discontinuous-conduction-mode boost converter with CMOS-control rectifier," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 9, September 2008.

[4] C. Y. Leung, P. K. T. Mok, and K. N. Leung, "A 1-V integrated current mode boost converter in standard 3.3/5-V CMOS technologies," *IEEE Journal of Solid-state Circuits*, vol. 40, no. 11, November 2005.

[5] S. K. Reynolds, "A DC-DC converter for short-channel CMOS technologies," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 1, January 1997.

[6] S. Cuk and R. D. Middlebrook, "A general unified approach to modeling switching dc-to-dc converters in discontinuous conduction mode," *IEEE Power Electronics Specialists Conference*, 1977.

[7] S. Cuk, "Modeling, analysis, and design of switching converters," Ph.D. dissertation, California Institute of Technology, November 1976.

[8] Y. Li, "Current mode control for boost converters with constant power loads," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, January 2012.