DESIGNING LOW-POWER COMMUNICATION SYSTEMS VIA NOISE-TOLERANCE

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The rapid growth in demand for high-performance computing and communication systems is driving the need for minimizing power dissipation, integrating higher functionality, increasing throughput, extending operational life, and improving reliability. The ability to scale feature sizes in semiconductor technology enables tremendous advances in building computationally complex VLSI systems at an affordable cost. However, with semiconductor technology being scaled into the deep submicron (DSM) regime, DSM noise consisting of ground bounce, crosstalk, leakage, process variations, etc., has become the primary cause of a reliability problem that challenges the very foundation of the cost and performance benefits of very large scale integration.

In this dissertation, we demonstrate that the energy-efficiencies of present-day integrated circuits are at least an order of magnitude away from the lower bounds, and that noise-tolerance is a practical method of approaching these bounds. We propose design techniques based on noise-tolerance where reliability and energy-efficiency are addressed in a cohesive manner to push the limits of energy reduction. In particular, we develop energy-efficient, noise-tolerant circuit techniques to ensure reliable operation of DSP and communication systems in the presence of DSM noise. We also propose energy-optimum algorithmic noise-tolerant (ANT) techniques to combat DSM noise-like errors induced by aggressive low-power design practices. ANT techniques allow us to achieve substantial energy savings beyond that achievable in conventional design without incurring loss in algorithmic performance.

We develop the soft-decision channel (SDC) model for deriving the lower bounds on energy dissipation of noisy digital systems. We compare the energy-efficiency bounds for dominant and noise-tolerant dynamic circuits, and demonstrate that noise-tolerant techniques improve the energy-efficiency when operating at the lower bound. Furthermore, we show that the gap between the lower bounds and the actual energy dissipation is reduced significantly via noise-tolerance. We propose an average noise threshold energy (ANTE) to quantify the noise-immunity and propose an energy-efficient, noise-tolerant dynamic circuit technique referred to as the motar technique. Simulation results in a 0.35-um CMOS technology are provided in comparison to static and domino circuits. A MAC ASIC design is presented along with the measured results. We investigate the reliability degradation due to leakage in two 0.1-um CMOS technologies. Two performance metrics, unity noise gain (UNG) and four-stage delay, are proposed to quantify the noise-immunity and speed, respectively. We also propose an energy-efficient, noise-tolerant circuit technique, the boosted-source (BS) technique, for wide fan-in OR gates. We propose the adaptive error-cancellation (AEC) as a practical ANT technique suitable for low-power broadband signal processing. An energy-optimum ABC design strategy is proposed and extended to the design of multi-input, multi-output (MIMO) communication systems.
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DESIGNING LOW-POWER COMMUNICATION SYSTEMS
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In this dissertation, we demonstrate that the energy-efficiencies of present-day integrated circuits are at least an order of magnitude away from the lower bounds, and that noise-tolerance is a practical method of approaching these bounds. We propose design techniques based on noise-tolerance where reliability and energy-efficiency are addressed in a cohesive manner to push the limits of energy reduction. In particular, we develop energy-efficient, noise-tolerant circuit techniques to ensure reliable operation of DSP and communication systems in the presence of DSM noise. We also propose energy-optimum algorithmic noise-tolerant (ANT) techniques to combat DSM noise-like errors induced by aggressive low-power design practices. ANT techniques allow us to achieve substantial energy savings beyond that achievable in conventional design without incurring loss in algorithmic performance.
We develop the soft-decision channel (SDC) model for deriving the lower bounds on energy dissipation of noisy digital systems. We compare the energy-efficiency bounds for domino and noise-tolerant dynamic circuits, and demonstrate that noise-tolerant techniques improve the energy-efficiency when operating at the lower bound. Furthermore, we show that the gap between the lower bounds and the actual energy dissipation is reduced significantly via noise-tolerance. We propose the metric of average noise threshold energy (ANTE) to quantify the noise-immunity and propose an energy-efficient, noise-tolerant dynamic circuit technique referred to as the mirror technique. Simulation results in a 0.35-\(\mu\)m CMOS technology are provided in comparison to static and domino circuits. A MAC ASIC design is presented along with the measured results. We investigate the reliability degradation due to leakage in two \(\sim 0.1-\mu\)m CMOS technologies. Two performance metrics, unity noise gain (UNG) and four-stage delay, are proposed to quantify the noise-immunity and speed, respectively. We also propose an energy-efficient, noise-tolerant circuit technique, the boosted-source (BS) technique, for wide fan-in OR gates. We propose the adaptive error-cancellation (AEC) as a practical ANT technique suitable for low-power broadband signal processing. An energy-optimum AEC design strategy is proposed and extended to the design of multi-input, multi-output (MIMO) communication systems. Simulation results of a Gigabit Ethernet 1000Base-T transceiver are evaluated.
Dedicated to My Family.
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CHAPTER 1

INTRODUCTION

The rapid growth in demand for high-performance computing and communication systems is driving the need for minimizing power dissipation, integrating higher functionality, increasing throughput, extending operational life, and improving reliability [1], [2]. The ability to scale feature sizes in semiconductor technology enables tremendous advances in building computationally complex VLSI systems at an affordable cost. This combined with other features of semiconductor technology such as low cost and high integration capability has led to the proliferation of energy-efficient implementations of computing and communication systems. However, with semiconductor technology being scaled into the deep submicron (DSM) regime, many physical properties approach their fundamental limits and do not scale in proportion to the feature size. This not only makes affordable scaling difficult to achieve but also introduces new design challenges in the DSM era.

At present, integrated circuits are deemed as an inherently reliable medium. However, with feature sizes being reduced from the current 0.18 $\mu$m – 0.13 $\mu$m to future 0.1 $\mu$m – 0.05 $\mu$m generations, noise [3], [4] has emerged as a critical factor that may ultimately determine the performance achievable in future VLSI systems. The 1999 International Technology Roadmap for Semiconductors [5] indicates that integrated circuits and systems in the year 2008 will need to be designed with high-leakage transistors, large $V_t$ variations, low supply voltages, and for operation at high clock-frequencies and in the presence of ground bounce, $IR$ drops, crosstalk, and clock jitter. DSM noise (due to physical phenomena such as ground bounce [6],
[7], crosstalk [8], [9], leakage [10], process variations [11], etc.) has become the primary cause of a reliability problem that challenges the very foundation of the cost and performance benefits of very large scale integration.

1.1 Motivation

Power reduction is essential for high-performance computing and communication systems such as Gigabit Ethernet [12], [13], next generation digital subscriber loop (DSL) [14], [15], and future 3G wireless [16], [17]. The emergence of DSM noise due to technology scaling raises questions about our ability to design reliable and energy-efficient (hence affordable) systems and hence the ability to extend Moore’s law [18] well into the deep submicron regime. This demands a new design paradigm where reliability and energy-efficiency are addressed in a cohesive manner.

Conventional DSP and communication design addresses algorithm specifications and implementation parameters in separate phases. A significant amount of effort is directed towards developing appropriate algorithms and transformations to meet algorithmic performance specifications (e.g., signal-to-noise ratio (SNR) and bit-error rate (BER)) subject to given channel models, interference environments, and signal statistics. The algorithm designers assume the availability of an error-free hardware platform and hence ignore the possible system degradation that may arise due to unreliable hardware. In the hardware design phase, IC designers need to make choices regarding hardware platforms (programmable DSP, field programmable gate array (FPGA), application specific integrated circuit (ASIC)), arithmetic architectures (adders, multipliers, finite precisions), and circuit styles (static logic, dynamic logic, transmission gates) suitable for the implementation of the given algorithm while satisfying stringent algorithmic specifications and power budgets. Power reduction cannot go beyond a minimum necessary
for ensuring reliable hardware operation. Thus, conventional DSP and communication design approaches ignore the possibility of joint optimization of reliability and energy-efficiency.

In this dissertation, we seek to break this barrier by proposing design techniques based on noise-tolerance where reliability and energy-efficiency are addressed together at various levels of the design hierarchy. In particular, we develop energy-efficient, noise-tolerant circuit techniques to ensure reliable operation of DSP and communication systems in the presence of DSM noise. We also propose energy-optimum algorithmic noise-tolerant (ANT) techniques to combat DSM noise-like errors induced by aggressive low-power design practices. ANT techniques allow us to achieve substantial energy savings beyond that achievable in conventional design without incurring loss in algorithmic performance.

The fundamental principle for the work presented in this dissertation comes from our research on determining the lower bounds on energy-efficiency of digital integrated systems in the presence of DSM noise using the information-theoretic framework [19]–[21]. It was clearly demonstrated that the energy-efficiencies of present-day integrated circuits are at least an order of magnitude away from the lower bounds, and that noise-tolerance is a practical method of approaching these bounds. Thus, our vision for reliable VLSI system design in future technologies is to employ noise-tolerance at various levels of the design hierarchy, in particular at the circuit and algorithmic levels, whereby the energy-efficiency and reliability issues are addressed jointly to push the limits of energy-efficiency.

In the next two sections, we provide an overview of DSM noise phenomena and discuss the existing techniques for the design of low-power, reliable VLSI systems.
1.2 Impact of DSM Noise

Noise in integrated circuits is defined as any disturbance that drives node voltages away from a nominal value. The deviated voltage value may cause logic failure and increase delay. Noise sources that have a substantial impact on digital systems include [3], [4]:

- **Supply bounce**, due to the RLC response to current switch on power and ground wires.
- **IR drop**, due to parasitic resistance on interconnection wires.
- **Crosstalk**, due to coupling capacitance between adjacent signal wires.
- **Charge sharing**, occurring mainly in dynamic circuits between dynamic and internal nodes.
- **Charge leakage**, due to subthreshold conduction.
- **Process variations**, due to manufacturing induced parameter mismatches, usually manifesting themselves as delay skews.

Consider the circuit in Fig. 1.1(a). A noise-injection circuit (NIC-GB) injects ground bounce noise into the power supply \( V_{dd} \) and ground \( V_{ss} \) of an inverting dynamic D-latch. The circuit is designed in a 0.35-\( \mu \)m CMOS technology and simulated via HSPICE at 5-ns clock period with load capacitance of 20 fF. The input and output waveforms are shown in Fig. 1.1(b). As indicated, one logic error occurs during the simulation, where the polarities of \( D \) and \( \overline{Q} \) are seen to be identical. This is because ground bounce noise on \( V_{dd} \) turns on the transistor M1, which should otherwise be off when \( D = 1 \) and \( CLK = 0 \). Although the above experiment demonstrates the impact of ground bounce noise only, more comprehensive experiments have shown the composite influences of several noise sources, including the impact of noise on delay [3].

Traditionally, digital circuits are deemed as an error-free medium due to their regenerative transfer characteristics being able to overcome physical disturbances described above. However,
Figure 1.1 Noise impact on a dynamic D-latch: (a) circuit schematic and (b) input and output waveforms.

The rationale for this viewpoint becomes weaker as noise problems worsen with technology scaling. This is because shrinking the minimum feature size and reducing the supply voltage result in reduced node capacitances to store information-bearing charges, while high-speed and low-power design techniques make these nodes more vulnerable to noise. Using the noise models given in [22, 23], one can show that peak noise due to ground bounce and crosstalk increases by 70% and 30%, respectively, from 0.35-μm to 0.13-μm CMOS. DSM noise significantly affects the performance of integrated circuits and makes the design of reliable and energy-efficient DSP and communication systems a challenging problem.

Many techniques [24]–[27] have been proposed to improve the noise-immunity of integrated circuits. However, these techniques do not explicitly consider energy-efficiency as a design metric of interest and thus are not energy-efficient in general. It is of interest to develop energy
and throughput-efficient, noise-tolerant circuit techniques such as the mirror technique [28], [29] and the boosted-source (BS) technique [30] presented in Chapters 2 and 3, respectively.

1.3 Design for Energy-Efficiency

In digital CMOS circuits, the total power dissipation consists of three major sources: dynamic (capacitive), static, and short-circuit power dissipations [31]. A substantial amount of research in low-power design has been conducted at various levels of VLSI design abstraction ranging from technology to algorithm and system levels. Most of this work focuses on developing power reduction techniques at various design levels [32]–[37], estimating power dissipation for a given architecture [38]–[41], and investigating the lower bounds on power dissipation [42]–[46].

Given the advent of DSM noise, it has become important to determine the limits to which energy-efficiency can be improved without sacrificing reliability. In particular, the energy-efficiency bounds need to be a function of DSM noise and the complexity of the algorithm being implemented. In the past, we have proposed an information-theoretic framework [19] that enables us to determine these bounds in a rigorous manner. The central thesis of this framework is to establish an energy-related correspondence between an algorithm and its architectural implementation. Specifically, we view a complex VLSI system implemented in a noisy medium as a network of communication channels. The algorithm being implemented has a computational complexity that is described by the information transfer rate $R$. An implementation of the system is viewed as a noisy communication channel that has an information transfer capacity $C$. The value of $C$ is determined by the architecture, circuit style, technology, and noise parameters. Information theory [47] indicates that it is possible to achieve an information transfer rate $R$ with arbitrarily low probability of error (by properly coding the input) as long as $C > R$. Employing this fundamental reliability constraint, a common basis for various power
reduction techniques such as pipelining, parallel processing, adiabatic logic, etc., was presented in [19]. The same constraint was utilized in [46] to obtain the fundamental limit on signal energy transfer during a binary switching transition, which was found to be \((\ln 2)kT\), where \(k\) is the Boltzmann’s constant and \(T\) is the absolute temperature. In [20], a binary symmetric channel (BSC) model was employed to determine the lower bounds on energy dissipation for single-output static gates under reliable operation. We will extend this framework in Chapter 4 by proposing a general soft-decision channel (SDC) model [48] for noisy digital systems and employing noise-tolerance to reduce the gap between the bounds on energy-efficiency and the actual energy dissipation.

While low-power design is still an active area of research, very little work has been done in developing power reduction techniques in the presence of noise. In other words, reliability and energy-efficiency issues have not been addressed together. Fault-tolerant computing [49]–[53] improves reliability via introducing substantial hardware redundancy or employing sophisticated (and usually energy-consuming) error-control schemes at the algorithm and system levels. In general, these techniques do not exploit domain-specific information for energy savings that is typically available in the design of DSP and communication systems.

Our research in algorithmic noise-tolerance (ANT) enables joint optimization of energy-efficiency and reliable operation. ANT is developed for combating DSM noise-like behavior induced by aggressive low-power design techniques at the algorithmic level. One such example is voltage overscaling (VOS) [54] for dedicated DSP implementations. Supply voltage scaling [32] is an effective and commonly employed low-power technique which enables a linear reduction in static power dissipation and a quadratic reduction in dynamic power dissipation. However, scaling the supply voltage increases the propagation delay and reduces the throughput. Therefore, the achievable energy reduction of a conventional DSP system is limited by the minimum voltage (referred to as \(V_{dd-crit}\)) necessary for correct operation. Supply voltage over-
scaling (VOS) takes voltage scaling one step further to the point where voltage is scaled below $V_{dd-crit}$. The resulting input-dependent soft errors due to delay violation are then corrected by low-complexity error-control techniques referred to as algorithmic noise-tolerance (ANT). This overall approach (see Fig. 1.2) of employing VOS in combination with ANT for low-power is referred to as soft DSP. Soft DSP works best in the context of DSP and communication systems, where the system performance metric is measured in terms of SNR and BER.

Past work [74] has reported a prediction-based error-control (PEC) scheme (see Fig. 1.3) for narrowband filters which achieves substantial energy savings over present-day optimally voltage-scaled systems (defined as systems operating at $V_{dd-crit}$). Many modern-day DSP and communications employ broadband signal processing. Thus, ANT techniques suitable for broadband signal processing are required. In Chapter 5, we present the adaptive error-
cancellation (AEC) [55]−[59] that is suitable for broadband systems and employ it in the design of a low-power Gigabit Ethernet receiver.

1.4 Organization

The remainder of this dissertation is organized as follows. In Chapter 2, we propose the metric of average noise threshold energy (ANTE) to quantify the noise-immunity and propose an energy-efficient, noise-tolerant dynamic circuit technique referred to as the mirror technique [28], [29]. Simulation results in a 0.35-μm CMOS technology are provided in comparison to static and domino circuits. A MAC ASIC design is presented along with the measured results. In Chapter 3, we investigate the reliability degradation due to leakage in two ~ 0.1-μm CMOS technologies. Two performance metrics, unity noise gain (UNG) and four-stage delay, are proposed to quantify the noise-immunity and speed, respectively. We also propose an energy-efficient, noise-tolerant circuit technique, the boosted-source (BS) technique [30], for wide fan-in OR gates. In Chapter 4, we develop the soft-decision channel (SDC) model [48] for deriving the lower bounds on energy dissipation of noisy digital systems. We compare the energy-efficiency bounds for domino and noise-tolerant dynamic circuits, and demonstrate that noise-tolerant techniques improve the energy-efficiency when operating at the lower bound [21]. Furthermore, we show that the gap between the lower bounds and the actual energy dissipation is reduced significantly via noise-tolerance. In Chapter 5, we propose the adaptive error-cancellation (AEC) [55] as a practical ANT technique suitable for low-power broadband signal processing. An energy-optimum AEC design strategy [56]−[59] is proposed and extended to the design of multi-input, multi-output (MIMO) communication systems. Simulation results of a Gigabit Ethernet 1000Base-T system are evaluated. Finally, in Chapter 6, we conclude this dissertation and discuss future work.
CHAPTER 2

NOISE-TOLERANCE VIA THE MIRROR TECHNIQUE

The need for high-speed and low-power operations [60]–[63] has forced IC designers to consider dynamic circuit techniques [64]–[67] in the next generation of VLSI systems. Dynamic circuits are faster but are sensitive to noise and thus require noise-tolerant techniques to enhance their noise-immunity. The existing noise-tolerant techniques [24]–[27] do not explicitly consider energy-efficiency as a design metric and thus are not energy-efficient in general. In this chapter, we present a new noise-tolerant technique, referred to as the mirror technique [28], [29], that has better noise-immunity, energy-efficiency, speed, and area, as compared to the existing techniques [25], [26]. Also presented in this chapter is the design of a multiply-accumulate (MAC) ASIC in a 0.35-μm CMOS process. Experimental results demonstrate the advantages of the proposed mirror technique over conventional circuits.

In Section 2.1, we discuss the existing noise-tolerant circuit techniques. In Section 2.2, we present the mirror technique and propose the metric of average noise threshold energy (ANTE) to quantify the noise-immunity. Simulation results in a 0.35-μm CMOS are presented in Section 2.3 in comparison to static and domino circuits. In Section 2.4, we describe the design of the MAC ASIC, along with the measured results.

2.1 Existing Noise-Tolerant Techniques

Dynamic circuits are inherently susceptible to noise [4] due to their low switching threshold voltage $V_{th}$, defined as the input voltage at which the output changes state. For the domino
NAND gate shown in Fig. 2.1(a), \( V_{th} = V_{in} \), where \( V_{in} \) is the threshold voltage of an NMOS transistor. Thus, one method to improve noise-immunity is to increase the switching threshold voltage \( V_{th} \) of the gate. Doing this inevitably sacrifices performance metrics such as speed and power dissipation, which are features that make dynamic circuits attractive in the first place. Thus, any noise-tolerant technique should provide substantial improvement in noise-immunity with minimal speed and power penalty.

Several techniques have been developed so far to improve the noise-immunity of dynamic circuits. The first technique, referred to as the CMOS inverter technique [25] (see Fig. 2.1(b)), modifies the NMOS evaluation net by utilizing PMOS transistors for noisy inputs. Obviously, the switching threshold voltage \( V_{th} \) of the gate will be equal to that of the static inverter, which can be adjusted by tuning the transistor width-to-length ratio. Thus, noise-immunity is enhanced if \( V_{th} \) is increased above \( V_{in} \). The CMOS inverter technique can be applied in the design of noise-tolerant CMOS receivers, dynamic AND/NAND gates, multiplexing circuits, and differential input circuits. However, it cannot be used for dynamic OR/NOR gates because certain input combinations will short power supply \( V_{dd} \) to ground.

The second technique, referred to as the PMOS pull-up technique [26] (see Fig. 2.1(c)), is intended to reduce leakage noise. This technique employs a pull-up device, either a voltage source or a PMOS transistor, to increase the source potential of the NMOS network. Due to the body-effect, this increases the transistor threshold voltage \( V_{in} \) and, in turn, \( V_{th} \) during the evaluate phase. Although this technique is easy to implement, it suffers from a large static power dissipation due to the direct path from the pull-up PMOS transistor to the foot-switch NMOS transistor. Thus, it is not suitable in low-power applications.

Note that keeper transistors (which are employed mainly to combat charge sharing noise [31]) cannot effectively protect dynamic circuits from input noise such as ground bounce, crosstalk, etc.. This is because the keepers are usually designed in such a way that the dynamic node
Figure 2.1 Dynamic NAND gates: (a) domino, (b) CMOS inverter technique, and (c) PMOS pull-up technique.

switches as soon as the inputs switch. An input noise pulse with sufficient amplitude and duration can easily turn off the keeper transistor and discharge the protected dynamic node. Thus, the existing noise-tolerant techniques present certain drawbacks and are not energy-efficient in general.

2.2 Mirror Technique for Noise-Tolerance

We now present an energy-efficient, noise-tolerant dynamic circuit technique referred to as the mirror technique [28], [29]. In order to quantify the noise-immunity and the energy penalty incurred in improving noise-immunity, we propose the metrics of average noise threshold energy (ANTE) and energy normalized ANTE (NANTE).

2.2.1 The mirror technique

As shown in Fig. 2.2, the proposed mirror technique (based on the Schmitt trigger [31], [68]) requires two identical NMOS evaluation nets. One additional NMOS transistor M1, whose gate voltage is controlled by the dynamic node voltage, provides a conduction path between the
Figure 2.2 The proposed mirror technique: (a) general schematic and (b) NAND gate.

common node of the two evaluation nets and \( V_{dd} \). During the precharge phase, transistor M1 is turned on and the common node voltage is charged up to the value of \((V_{dd} - V_{in})\). Due to body-effect, the switching threshold voltage of the upper NMOS net is increased, thereby improving the noise-immunity.

Note that the serial arrangement of two NMOS evaluation nets in the mirror technique guarantees zero static power dissipation. However, there can be a speed penalty if the transistors are not resized. On the other hand, resizing transistors for speed costs more area. Nevertheless, the area penalty of the mirror technique has been found to be less than or close to that of the existing noise-tolerant techniques and static circuits. This will be shown in Section 2.3.

2.2.2 Average noise threshold energy (ANTE)

We know that noise pulses must have sufficiently high amplitude and long duration to cause unrecoverable logic errors in dynamic circuits. This fact is embodied in the noise-immunity curves (denoted by \( C_{nic} \)) [69]. Figure 2.3 depicts two typical noise-immunity curves, where all the points on and above the curves represent the noise pulses that will cause logic errors. A
Figure 2.3 Noise-immunity curves.

gate with noise-immunity curve given by $C_{nic1}$ is more robust to noise than the one with $C_{nic2}$ as its noise-immunity curve. This is because $C_{nic1}$ lies above $C_{nic2}$.

Note that the vertical asymptote of $C_{nic}$ reflects the best-case circuit speed. This is because the noise-immunity curve, say for a NOR gate, is measured when all the pull-down NMOS transistors are subject to the input noise, whereas the delay of the gate is measured with only one pull-down NMOS transistor being on.

For comparison of different noise-tolerant techniques, we propose the metric of average noise threshold energy (ANTE), which is defined as the average input noise energy that a logic gate can tolerate. Note that each point on the noise-immunity curve $C_{nic}$ represents the amplitude $V_n$ and duration $T_n$ of an input noise pulse that generates a logic error. Defining the pulse energy as being equal to the energy dissipated in a 1-$\Omega$ resistor subject to a voltage drop equal to the pulse amplitude $V_n$, the ANTE measure is defined as

$$ANTE = E \left( V_n^2 T_n \right),$$  \hspace{1cm} (2.1)
where $E(\cdot)$ denotes the expectation operator.

Obviously, an input noise pulse with amplitude $V_n \geq V_{th}$ will turn on pull-down NMOS transistors and discharge a dynamic node. On the other hand, if $V_n < V_{th}$, subthreshold leakage current will become dominant. The dynamic node can still be discharged erroneously provided that the duration $T_n$ of the noise pulse is sufficiently long.

In order to motivate the ANTE metric further, we consider a generic dynamic node shown in Fig. 2.4, where the input noise pulse $V_n$ discharges the dynamic node $x$ that has a voltage $V_x$. The differential equation describing this event is

$$C_x \frac{dV_x}{dt} = -i_x.$$  \hspace{1cm} (2.2)

We consider $V_n \geq V_{th}$ for the sake of simplicity. Assuming the transistor to be in saturation region, the discharging current $i_x$ can be expressed as

$$i_x = \frac{k_m}{2} (V_n - V_{tn})^2 - i_{\text{pull-up}},$$ \hspace{1cm} (2.3)

where $k_m$ is the NMOS transconductance and $i_{\text{pull-up}}$ accounts for the counteracting current if present (such as the current from a keeper). Substituting for $i_x$ from (2.3) into (2.2) and
integrating, we obtain

$$\frac{2C_x}{k_m} \Delta V - V_{th}^2 T_n + 2V_{in} \int_{T_n} V_n \, dt + \frac{2}{k_m} \int_{T_n} i_{\text{pull-up}} \, dt = \int_{T_n} V_n^2 \, dt,$$

(2.4)

where $\Delta V$ is the voltage drop at the dynamic node $x$ that causes a logic error and $T_n$ is the corresponding duration of the input noise pulse $V_n$. Note that $\Delta V$ is a constant depending only upon the circuit to which the node $x$ is connected as input. For example, $\Delta V = V_{th}$ for domino circuits, where $V_{th}$ is the switching threshold voltage of the inverter. Considering $V_n$ and $T_n$ as random variables, we take the expectation of (2.4) to obtain

$$\frac{2C_x}{k_m} \Delta V - V_{in}^2 E(T_n) + 2V_{in} E \left( \int_{T_n} V_n \, dt \right) + \frac{2}{k_m} E \left( \int_{T_n} i_{\text{pull-up}} \, dt \right) = \text{ANTE}.$$

(2.5)

Note that the first two terms on the left side of (2.5) are constants for different circuit techniques. In most cases, $i_{\text{pull-up}}$ will be small compared to the current generated by the noise $V_n$. Thus, a larger ANTE measure in (2.5) implies that a higher noise amplitude $V_n$, or equivalently a larger noise energy, is needed to discharge the dynamic node $x$ and cause a logic error.

Noise-tolerant techniques provide improvement in noise-immunity at the expense of area, speed, and power. While noise-immunity curves, such as those in Fig. 2.3, and the ANTE measure (2.1) allow comparisons of noise-immunity, they do not indicate the energy being involved. Therefore, we propose the energy normalized ANTE (NANTE) as a measure of the energy penalty incurred in improving noise-immunity, which is defined as

$$\text{NANTE} = \frac{\text{ANTE}}{\mathcal{E}},$$

(2.6)
where $E$ represents the energy dissipation which includes all the energy components, such as those from the increased fan-in (input) capacitance, static power dissipation, etc.

2.3 Simulation Results and Comparisons

In this section, we employ the mirror technique in the design of a NAND gate and a full adder. Simulation results are presented in comparison with static circuits, conventional domino circuits, as well as the existing noise-tolerant techniques [25], [26].

2.3.1 Simulation results for NAND gates

Figure 2.2(b) shows the NAND gate implemented by the proposed mirror technique, while those using the CMOS inverter technique [25] and PMOS pull-up technique [26] are shown in Figs. 2.1(b) and 2.1(c), respectively. We choose NAND gates for comparison because the CMOS inverter technique cannot be employed for NOR gates. To account for the fan-in (input) capacitance of different techniques, we simulate three serially connected identical NAND gates and measure the delay of the first two gates. Power dissipation is obtained by averaging over the three gates.

The noise-tolerant circuits in Figs. 2.1(b), 2.1(c), and 2.2(b) are designed to meet the following specifications: (1) power supply $V_{dd} = 3.3$ V, (2) load capacitance $C_L = 20 \mu F$, (3) two-stage delay $\tau = 500$ ps, (4) clock frequency $f_c = 1$ GHz, and (5) switching threshold voltage $V_{th} \approx 1.8$ V. The domino gate in Fig. 2.1(a) is designed to meet the specifications (1) to (4).

Figure 2.5 shows the noise-immunity curves obtained via simulation for different NAND gates. Table 2.1 indicates that noise-tolerant techniques improve noise-immunity at the expense of higher power dissipation and larger layout area. The proposed mirror technique improves the ANTE and energy normalized ANTE by $1.84X$ and $1.42X$ over conventional domino circuits. The improvement in the energy normalized ANTE is 11% higher than the existing noise-tolerant
techniques. In addition, the mirror technique has a smaller area overhead (41%) as compared to the PMOS pull-up technique whose area overhead is 49%. Note that the mirror technique and the CMOS inverter technique have similar performance in terms of area, power, ANTE, and NANTE. However, the CMOS inverter technique cannot be used for dynamic OR/NOR logic. Another observation is that the PMOS pull-up technique degrades the NANTE by 36%. This is to be expected because it consumes large static power dissipation.

### 2.3.2 Simulation results for full adders

We now present the noise-tolerant full adder design employing the mirror technique. Performance comparisons of the domino full adder (see Fig. 2.6(a)), static CMOS full adder [68],
Figure 2.6 Full adder schematics: (a) conventional dynamic technique and (b) the proposed mirror technique.

and the mirror full adder (see Fig. 2.6(b)) are provided. Note that the SUM output of the full adder cannot be implemented by conventional dynamic logic and thus is not protected by the mirror technique, but the CARRY output is. Even so, the mirror technique still improves the noise-immunity of a MAC by 27%, as will be shown in Section 2.4.

All the full adder designs satisfy the following specifications: (1) power supply $V_{dd} = 3.3$ V, (2) load capacitance $C_L = 20 \text{fF}$, and (3) clock frequency $f_c = 1$ GHz. The switching threshold
Figure 2.7  Noise-immunity curves of full adders.

Table 2.2  Performance of full adders.

<table>
<thead>
<tr>
<th></th>
<th>Area ($\mu m^2$)</th>
<th>Energy (pJ)</th>
<th>ANTE (nJ)</th>
<th>ANANTE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mirror Tech.</td>
<td>487.2</td>
<td>1.693</td>
<td>5.203</td>
<td>3073</td>
</tr>
<tr>
<td>Static</td>
<td>574.3</td>
<td>2.202</td>
<td>3.115</td>
<td>1414</td>
</tr>
<tr>
<td>Conventional Dynamic</td>
<td>358.9</td>
<td>1.251</td>
<td>2.599</td>
<td>2078</td>
</tr>
</tbody>
</table>

voltage $V_h$ for the CARRY output equals 0.6 V, 1.65 V, and 1.8 V for the domino full adder, static full adder, and noise-tolerant full adder, respectively.

Noise-immunity curves in Fig. 2.7 demonstrate that the proposed mirror technique has better noise-immunity than conventional domino and static circuits. Table 2.2 indicates that the mirror technique improves the ANTE and energy normalized ANTE by 2X and 1.48X over the domino full adder. In comparison, the static full adder improves the ANTE by 1.2X but degrades the energy normalized ANTE by 32%. The proposed mirror technique also has a smaller area overhead (36%) as compared to the static full adder whose area overhead is 60%.
2.4 MAC ASIC Design

In this section, we present the design of a MAC ASIC in 0.35-μm CMOS that employs the conventional domino and the proposed mirror technique. Measured results are presented to demonstrate the improvement in noise-immunity via the mirror technique.

2.4.1 Chip architecture

As shown in Fig. 2.8, the MAC ASIC consists of five functional blocks: the input block, noise-injection circuits (NICs), dynamic multiplier-accumulator (dynamic MAC), noise-tolerant (mirror) multiplier-accumulator (mirror NT MAC), and the output block.

Note that ground bounce noise has been identified as a major noise source in high-performance VLSI systems [70], [71]. For this reason, we primarily consider the ground bounce noise generated by the NICs and its impact on the operation of the two MACs. To operate each MAC against the ground bounce noise generated by its own NIC only, we provide the two MACs with independent power supply, shared by its NIC. We also provide separate power supply for the input and output blocks in order to protect them from the ground bounce noise.
2.4.1.1 MAC architecture

The dynamic MAC and mirror NT MAC are implemented by the domino and the proposed mirror technique, respectively. We choose the multiply-accumulate function for performance comparison because it is commonly employed in DSP and communication systems.

Both MACs are bit-level pipelined array structure. Pipelining at full adder level facilitates the detection of logic errors because the output D-latch can easily capture an erroneous output. Pipelined architectures also lead to high-speed, thereby stressing the noise-immunity of the underlying circuits.

As illustrated in Fig. 2.9, the two MACs have 8-bit inputs and 22-bit outputs, indicating that a 64-tap FIR filter can be programmed. In addition, the inputs of two MACs are identical so that any discrepancy between the two outputs will be due to the logic errors in the MACs. Figure 2.6 shows the circuit schematics of the domino full adder and noise-tolerant full adder employed in the corresponding MACs.

2.4.1.2 Noise-injection circuit (NIC)

Figure 2.10 depicts the block diagram of a noise-injection circuit (NIC) for generating ground bounce noise. Each NIC contains eight 4-stage super buffers [31] with a scale factor $\beta = 3$. The number of the external load capacitors connected to each NIC can be adjusted to control the magnitude of the ground bounce noise being injected. A 26-tap linear feedback shift register
(LFSR) [72] provides eight pseudo-random sequences as the inputs of the super buffers. The control signal ENABLE activates the NIC when it is logic high.

2.4.1.3 Input and output blocks

As shown in Fig. 2.11, the input block provides data and coefficients to the two MACs. Both the data and the coefficients are in bit-serial format to reduce the pin count. Thus, two serial-to-parallel converters are needed to transform the data into an appropriate format within the chip. A global clock signal CLOCK/8 is obtained by dividing an external clock signal CLOCK by 8 and employed to synchronize the two MACs. Figure 2.11 also indicates that the input data can be read from an external data source or generated internally by an on-chip LFSR. The on-chip LFSR employs four primitive polynomials with the orders of 20, 21, 22, and 23 to generate pseudo-random sequences [72]. Control signal POLY-SET determines which primitive polynomial is selected. Pseudo-random sequences minimize the data-dependent logic errors during the testing.
Figure 2.11 Input block diagram.

Figure 2.12 Output block diagram.

Figure 2.12 illustrates the output block. Control signals S0 and S1 determine which output is selected. Once again, for the purpose of reducing pin count, the 22-bit output data are converted to three bit-serial outputs. The ASIC is designed and fabricated in a 0.35-μm CMOS process through MOSIS. Table 2.3 summarizes the main features of the ASIC. The chip final layout is shown in Fig. 2.13.

2.4.2 Experimental results

We now compare the noise-immunity of the mirror NT MAC and dynamic MAC. A general expression for ground bounce noise is given by [31]

$$L \left[ \frac{di}{dt} \right]_{max} \approx L \left[ \frac{4C_L V_{dd}}{t_s^2} \right],$$  \hspace{1cm} (2.7)
Table 2.3 Features of the MAC ASIC.

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>HP GMOS10QA 0.35 ( \mu )m CMOS</td>
</tr>
<tr>
<td>MOSFET Threshold</td>
<td>PMOS: -0.61 V, NMOS: 0.62 V</td>
</tr>
<tr>
<td>Transistor Count</td>
<td>21,642 (including pads)</td>
</tr>
<tr>
<td>Chip Size</td>
<td>2.94 ( \times ) 1.61 mm(^2)</td>
</tr>
<tr>
<td>Pin Count</td>
<td>48</td>
</tr>
<tr>
<td>Package</td>
<td>LCC52</td>
</tr>
<tr>
<td>Estimated Power</td>
<td>2 mW ((V_{dd} = 2.0\text{ V}, f_c = 10\text{ MHz}))</td>
</tr>
</tbody>
</table>

Figure 2.13 Chip final layout.

where \( L \) is the inductance of the bonding wire, \( C_L \) is the load capacitance, and \( t_s \) is the gate switching time, which we assume to be twice the gate delay. In the case of NMOS and PMOS transistors being balanced, \( t_s \) is approximated by [73], [74]

\[
t_s = \frac{2C_L V_{dd}}{k_m (V_{dd} - V_{tn})^\alpha},
\]

where \( k_m \) is the transconductance of the balanced NMOS and PMOS transistors, \( V_{tn} \) is the threshold voltage for an NMOS transistor, and \( \alpha \) is the velocity saturation index that ranges
Figure 2.14 Measured maximum error-free power supply versus clock period.

From 1 (velocity saturated) to 2 (without velocity saturation). Substituting for \( t_s \) from (2.8) into (2.7), we obtain

\[
L \left[ \frac{di}{dt} \right]_{\text{max}} \propto \frac{(V_{dd} - V_{in})^{2\alpha}}{V_{dd}}. \tag{2.9}
\]

From (2.9), ground bounce noise increases with the supply voltage \( V_{dd} \). Hence, we tested the two MACs under different speeds and measured the maximum supply voltage at which errors start appearing at the outputs. A higher error-free supply voltage implies better noise-immunity. Figure 2.14 shows the experimental results, where we find that the maximum error-free supply voltage increases with the speed. This is because the available discharging time reduces at a faster speed and thus only those noise pulses with large amplitude can cause logic errors. Figure 2.15 shows two ground bounce noise waveforms measured on the power supply when the control signal ENABLE becomes logic high. We have observed that the outputs of the two MACs become correct when the control signal ENABLE is logic low. This verifies that the output errors are indeed caused by the injected ground bounce noise.

As it is hard to measure the noise-immunity directly, we compute the relative noise-immunity improvement from (2.9) normalized by the corresponding error-free supply voltages. Assuming
Figure 2.15 Measured ground bounce noise: (a) at 50-ns clock period and (b) at 1-μs clock period.

that the load capacitance and bonding wire inductance are the same for the two MACs, the relative noise-immunity improvement (RNI) is obtained as

\[ RNI = \left( \frac{V_{\text{max}}^{\text{dd,NT}} - V_{\text{tn}}}{V_{\text{max}}^{\text{dd,D}} - V_{\text{tn}}} \right)^{2a} \left( \frac{V_{\text{max}}^{\text{dd,D}}}{V_{\text{max}}^{\text{dd,NT}}} \right)^2 - 1, \]  

(2.10)

where \( V_{\text{max}}^{\text{dd,NT}} \) and \( V_{\text{max}}^{\text{dd,D}} \) are the maximum error-free supply voltages for the Mirror NT MAC and Dynamic MAC, respectively.

Figure 2.16 illustrates the RNI estimated at different speeds. As indicated, the proposed mirror technique improves the noise-immunity over conventional dynamic circuits by approximately 27% on average.
2.5 Summary

In this chapter, we present a new noise-tolerant dynamic circuit technique referred to as the mirror technique. In addition, the average noise threshold energy (ANTE) and energy normalized ANTE (NANTE) metrics are proposed to quantify the noise-immunity and energy-efficiency, respectively. Simulation results of NAND gates in 0.35-μm CMOS demonstrate that the proposed mirror technique improves the ANTE and energy normalized ANTE by 1.84X and 1.42X over conventional domino circuits. The improvement in the energy normalized ANTE is 11% higher than the existing noise-tolerant techniques. A full adder design using the mirror technique improves the ANTE and energy normalized ANTE by 2X and 1.48X over conventional domino circuits. In comparison, static circuits improve the ANTE by 1.2X but degrade the energy normalized ANTE by 32%. Furthermore, the proposed mirror technique has a smaller area overhead (36%) as compared to static circuits whose area overhead is 60%. Also presented in this chapter is a MAC ASIC designed in 0.35-μm CMOS to evaluate the performance of the proposed mirror technique. Experimental results demonstrate a 27% improvement in noise-immunity over conventional domino circuits.
CHAPTER 3

NOISE-TOLERANCE VIA THE BOOSTED-SOURCE TECHNIQUE

With the scaling of supply voltage, transistor threshold voltage $V_t$ needs to be scaled properly to offset the undesired loss in speed [32]. Unfortunately, such design practice not only exponentially increases leakage power but also deteriorates noise-immunity. Furthermore, given the trend that leakage power increases by a factor of $3X - 7X$ with each technology generation and will become a significant portion of the total power in future ICs [33], active leakage-control becomes critical to high-performance VLSI systems. Many techniques [75]–[77] have been developed so far to reduce leakage power; however, not much work has been done in addressing the leakage reduction in the presence of DSM noise. In this chapter, we investigate the leakage-induced reliability degradation in deep submicron CMOS technologies. We also present an energy-efficient, noise-tolerant dynamic circuit technique [30] for wide fan-in gates.

In Section 3.1, we analyze the reliability degradation due to leakage in two ~ 0.1-$\mu$m CMOS technologies. Two performance metrics, unity noise gain (UNG) and four-stage delay, are proposed to quantify the noise-immunity and speed, respectively. In Section 3.2, we present a new energy-efficient, noise-tolerant dynamic circuit technique referred to as the boosted-source (BS) technique. Simulation results demonstrating the performance of wide fan-in OR gates are presented and evaluated in Section 3.3.
Figure 3.1 Wide fan-in domino gates: (a) $d1$ domino and (b) $d2$ domino.

3.1 Characterization of Leakage-Induced Reliability

Degradation

In this section, we investigate the reliability degradation due to high leakage for digital circuits designed in two ~ 0.1-μm CMOS technologies provided by Intel Corporation.

3.1.1 Noise characterization

We are primarily concerned with wide fan-in domino gates, which are prone to leakage-induced noise. Figure 3.1 depicts two domino topologies of wide fan-in OR gates, where $d1$ domino denotes the conventional domino gate with a foot-switch NMOS transistor and $d2$ domino denotes that without the foot-switch NMOS transistor [33]. We need to point out that a $d2$ domino gate is faster than a $d1$ domino gate of the same design; however, the input signals of a $d2$ domino gate need to remain at "0" during the precharge phase to prevent DC conduction between the power supply and ground.

We inject identical noise pulses into all the gate inputs $V_{in1} - V_{inN}$ during the evaluate phase and measure the resulting voltage waveforms at dynamic node $V_D$ and output $V_{out}$. The input noise pulse (see Fig. 3.2(a)) consists of a DC offset $V_{DC}$ (to account for the possible IR drops)
Figure 3.2 Noise characterization: (a) input noise waveforms, (b) dynamic node waveforms, and (c) output waveforms.

and a scalable pulse $V_{\text{pulse}}$, i.e.,

$$V_{\text{noise}} = V_{\text{DC}} + V_{\text{pulse}},$$  \hspace{1cm} (3.1)

where the shape of $V_{\text{pulse}}$ is chosen to mimic real noise pulses due to glitches, crosstalk, and ground bounce, etc. Figures 3.2(b)-(c) illustrate typical waveforms of $V_D$ and $V_{out}$ with the input noise present. To quantify the noise-immunity, we propose the metric of unity noise gain (UNG), which is defined as the amplitude of input noise $V_{\text{noise}}$ that causes an equal-amplitude noise pulse at $V_{out}$, i.e.,

$$UNG = \{ V_{\text{noise}} : V_{\text{noise}} = V_{out} \}.$$  \hspace{1cm} (3.2)

UNG captures the critical input noise amplitude because any noise pulse higher than UNG will be amplified due to the nonlinear transfer function of MOS transistors. While the UNG measure is easy to obtain, for some cases where the duration of DSM noise needs to be accounted for, a more comprehensive noise-immunity metric such as the ANTE [28], [29] proposed in Chapter 2 can be adopted. In what follows, we primarily consider noise amplitude for the sake of simplicity.

In addition to noise-immunity, we are also interested in the speed improvement achievable in DSM technologies. For this purpose, we simulate five serially-connected identical OR gates and
measure the worst-case delay of the first four gates, termed as four-stage delay (see Fig. 3.3). This accounts for the fan-in (input) capacitance associated with the circuit style being employed.

3.1.2 Performance comparison and problem statement

We have designed 4-wide, 8-wide, and 16-wide OR gates in two $\sim 0.1\mu m$ CMOS technologies, termed as $T$-1 and $T$-2, where $T$-1 is a single-threshold technology and $T$-2 is a scaled dual-threshold technology with smaller threshold voltages denoted as high-$V_t$ and low-$V_t$. Due to this, $T$-2 technology induces higher leakage. For example, the leakage currents (measured at room temperature) in low-$V_t$ and high-$V_t$ transistors are 25X and 6X larger than that of the transistors in $T$-1 technology of the same design. To investigate the degradation in noise-immunity, two design schemes have been applied to the gates in $T$-2 technology: (1) single-$V_t$ implementation, where all the transistors are low-$V_t$, and (2) dual-$V_t$ implementation, where the pull-down NMOS transistors are replaced by high-$V_t$ transistors for the purpose of reducing leakage current. The size of pull-down NMOS transistors in these OR gates is determined by the specifications on speed and fan-in (input) capacitance.
Figure 3.4 Noise-immunity versus speed for two ~ 0.1-μm technologies.

Figure 3.4 shows the results of UNG versus four-stage delay, both normalized by the corresponding values in T-1 technology. As indicated, single-\( V_t \) \( d2 \) domino gates in T-2 technology achieve about 2X delay reduction over those in T-1 technology. However, the leakage problem worsens because the scaled \( V_t \) makes transistors more susceptible to DSM noise, thus resulting in 60% – 70% degradation in UNG. Dual-\( V_t \) \( d2 \) domino gates mitigate the UNG degradation by 30% – 40% as compared with the T-1 technology; however, they lead to a 20% speed loss over single-\( V_t \) \( d2 \) domino gates. Within the same technology, 16-wide gates are found to be slower and less robust than 4-wide gates due to their larger parasitic capacitance and stronger leakage paths. In particular, the 16-wide \( d1 \) domino and \( d2 \) domino gates in T-2 technology with single-\( V_t \) are nonfunctional, which implies that a small DC offset \( V_{DC} \) (around 100 mV) at the inputs is sufficient to switch the output erroneously.

A possible means to improve noise-immunity is to use \( d1 \) domino instead of \( d2 \) domino, as the stacked foot-switch NMOS transistor can reduce leakage current. This approach, however, incurs a speed penalty due to the reduced pull-down strength. For example, dual-\( V_t \) \( d1 \) domino gates lead to a 10% UNG improvement but introduce a 30% speed loss as compared with
Figure 3.5 The proposed boosted-source (BS) technique (output inverters are not shown). dual-$V_t$ $d2$ domino gates. Therefore, design techniques that have a better trade-off between noise-immunity and speed are needed.

3.2 The Boosted-Source Technique

Noise-immunity degradation due to high leakage makes robust performance difficult for low-power digital circuits, especially for wide fan-in domino gates. In this section, we will present a new noise-tolerant dynamic circuit technique, the boosted-source (BS) technique [30], which achieves significant improvement in noise-immunity without incurring large design overheads.

Figure 3.5 shows the circuit schematic of a $d1$-compatible wide fan-in OR gate employing the proposed BS technique. A sense amplifier (SA) is utilized to generate two full-swing, dual rail outputs. The gate works as follows. During the precharge phase when $CLK = 0$, dynamic node A, outputs $\overline{V_{out}}$ and $V_{out}$ are charged up to $V_{dd}$, whereas node C is discharged. The voltage level of node B depends upon the inputs. In case 1 (see Fig. 3.6(a)), some of the inputs $A_1 - A_n$ are low. Thus, node B is also charged up to $V_{dd}$. During the evaluate phase when $CLK = 1$, nodes A and B will be pulled down due to charge redistribution with the dummy capacitor at node C. Meanwhile, both $V_{out}$ and $\overline{V_{out}}$ will be momentarily discharged. However, by properly
Figure 3.6 Voltage waveforms of a BS gate when the inputs are \((a)\) not all high and \((b)\) all high.

skewing the pull-down strength of \(Path1\) and \(Path2\), \(V_{out}\) will be fully discharged while \(\overline{V_{out}}\) returns back to \(V_{dd}\). Nodes \(A\), \(B\), and \(C\) will converge to an intermediate voltage level due to charge-sharing. Note that this is the highest voltage level that node \(B\) can achieve at the end of each evaluate phase. In case 2 (see Fig. 3.6(b)), all the inputs \(A_1 - A_n\) are high. Thus, nodes \(A\) and \(B\) will be at \(V_{dd}\) and an intermediate voltage level, respectively. This voltage difference makes \(Path1\) slower than \(Path2\). After \(CLK\) turns to high, \(\overline{V_{out}}\) will be discharged while \(V_{out}\) stays at \(V_{dd}\). Node \(B\) will converge to a lower voltage level due to charge-sharing with node \(C\). Note that in both cases the small glitch at the nonswitching output can be reduced by the output inverter.

In comparison with the existing circuit techniques [28], [29], [64], the proposed BS technique has the following advantages:

1.) The BS technique significantly improves the noise-immunity. While noise pulses may affect the outputs of a BS gate when all the inputs are high during the precharge phase and at the beginning of evaluate phase when the SA starts latching, the impact of noise is greatly reduced due to the body-effect and low mobility of PMOS transistors. In addition, during most of the evaluate phase, noise will only cause charge-sharing between nodes \(A\), \(B\), and \(C\), but
will not affect the outputs due to the latching nature of the SA. Note that conventional domino gates are not noise-tolerant even if they are followed by a latch. This is because the latch will capture a wrong logic value at the end of evaluate phase if an error occurs.

2.) The delay of a BS gate is determined by the speed of SA. This implies a speed benefit for wide fan-in gates due to the relief of discharging large drain capacitance and parasitic capacitance at dynamic nodes. Moreover, the BS technique does not increase the fan-in (input) capacitance and thus allows an easy interface to other circuits.

3.) Due to partial voltage swing at nodes A, B, and C, dynamic power dissipation is reduced and the extra power dissipation due to the SA can be offset. As the number of fan-ins increases, drain capacitance and parasitic capacitance at dynamic nodes become larger, and the power reduction due to partial voltage swing will be significant.

Several design issues regarding the BS technique need to be addressed. First, it is necessary to determine the value of the capacitance at node C. A small capacitance reduces the voltage drop at node B and therefore may not be able to skew the pull-down speed when all the inputs are high. On the other hand, a large capacitance wastes power. From the simulations we found that such capacitance should be around 30% – 50% of the total capacitance at nodes A and B. Thus, a dummy capacitor might be needed.

Note that the BS gate shown in Fig. 3.5 is $d1$-compatible, which is desired for many applications such as wide fan-in address decoders in memory design. It is possible to modify the circuit configuration in Fig. 3.5 for $d2$-compatible. In such case the foot-switch NMOS transistor N1 and the dummy capacitor at node C are no longer needed. This leads to additional energy savings. Also, the clock signal of the SA must be delayed properly with respect to $CLK$ to wait for stable inputs. This delayed clock signal can be generated locally, but it may increase the gate delay.
Finally, we need to point out that the BS technique increases the clock load and thus an up-sized local clock driver is needed. While this leads to extra power dissipation, the simulation results in the next section demonstrate that the power reduction due to partial voltage swing dominates for wide fan-in gates.

Note that although here we are primarily concerned with wide fan-in gates, the proposed BS technique is equally applicable to narrow fan-in gates and other logic gates which will become leakage-prone in future CMOS technologies.

3.3 Implementation and Results

Simulation results of 8-wide, 16-wide, and 32-wide OR gates designed in the Predictive Berkeley BSIM3v3 0.13-µm CMOS technology [78] are presented in this section. Performance in terms of delay, power dissipation, and noise-immunity is compared with the conventional domino gates shown in Fig. 3.1(a). All the gates are designed with the same speed specification at a given output load.

Figure 3.7(a) shows the energy dissipation of 8-wide, 16-wide, and 32-wide BS gates, normalized by the corresponding measures of domino gates. We find that the energy dissipation of the 32-wide BS gate is comparable to that of the 32-wide domino gate. This is because the power reduction due to partial voltage swing in BS gates becomes dominant as the fan-in number increases. Therefore, the BS technique is a better choice for wide fan-in gates, which according to Fig. 3.4 are very prone to leakage-induced noise.

As mentioned before, noise pulses may affect the outputs of a BS gate when all the inputs are high during the precharge phase and at the beginning of evaluate phase when the SA starts latching. As the UNG metric defined in (3.2) cannot be applied directly to BS gates, we compare the noise-immunity in terms of the amplitude of noise pulses that will make output
Figure 3.7 Performance of wide fan-in BS gates: (a) energy dissipation and (b) noise-immunity.

in error. Figure 3.7(b) shows the noise-immunity of 8-wide, 16-wide, and 32-wide BS gates, normalized by the corresponding measures of domino gates. The BS technique achieves $1.6X - 3X$ improvement in noise-immunity, and the improvement is significant for wide fan-in gates. Also shown in Fig. 3.7(b) is that the noise-immunity of conventional domino gates degrades at a faster rate with increase in fan-in number as compared with that of the BS gates.

3.4 Summary

In this chapter, we have shown that deep submicron CMOS technologies lead to 60% - 70% degradation in noise-immunity due to high-leakage. Dual-$V_t$ domino designs mitigate the noise-immunity degradation by 30% - 40% but inevitably result in a loss of 20% - 30% in circuit speed. To achieve a better noise-immunity versus performance (in terms of power and speed) trade-off, a new dynamic circuit technique referred to as the boosted-source (BS) technique is proposed. Simulation results of wide fan-in OR gates designed in the Predictive Berkeley BSIM3v3 0.13-$\mu$m technology demonstrate $1.6X - 3X$ improvement in noise-immunity over the existing circuit techniques at the expense of minor energy overhead but no loss in delay.
CHAPTER 4

ENERGY-EFFICIENCY BOUNDS FOR DEEP SUBMICRON VLSI SYSTEMS

In this chapter, we extend the information-theoretic framework [19]–[21] by proposing a general soft-decision channel (SDC) model [48] for the lower bounds on energy dissipation of complex digital systems. Considering the fact that all logic signals and noise are inherently analog, we choose to model them according to their analog behaviors in a VLSI implementation. Specifically, we characterize ideal (noiseless) logic signals as binary signals switching between 0 V and $V_{dd}$ with an average transition probability $t$, whereas the noise is assumed to be a continuous random signal with a certain statistical distribution. We then derive the corresponding expressions for information-theoretic measures such as channel capacity, and compute the lower bounds on energy dissipation analytically by solving an energy optimization problem subject to the reliability constraint $C > R$. It is shown that the SDC model provides accurate lower bounds. The minimum energy dissipation is found to be 37.5% lower than that obtained via the previously proposed binary symmetric channel (BSC) model [20]. Furthermore, the lower bounds are easy to compute making the proposed model applicable to complex digital systems.

We determine the lower bounds on energy for various digital systems including single-output static gates, multimodule systems, dynamic circuits such as domino [79] and noise-tolerant mirror technique [28], [29]. In particular, we compare the energy-efficiency bounds for conventional domino and noise-tolerant circuits. Noise-tolerant circuit techniques [24]–[26], [28], [29], [80] improve noise-immunity by employing additional elements to prevent logic errors from occurring in the presence of noise. Hence, questions arise such as whether these techniques are energy-
efficient and to what extent noise-immunity needs to be enhanced before the energy overhead starts to dominate. In this chapter, we show that noise-tolerance improves the energy-efficiency when operating at the lower bound. Furthermore, we demonstrate that the gap between the lower bounds and the actual energy dissipation is reduced significantly via noise-tolerance. Past work [20] has reported a scheme employing error-control codes to approach the lower bounds for chip I/O signaling. In this chapter, we consider general Boolean logic and employ high-speed arithmetic circuits as a demonstration vehicle. A wide adder in the context of a code-division multiple access (CDMA) communication system [81] demonstrates 31.2% – 51.4% energy reduction over conventional implementations and 1.9X reduction in the gap between the bounds on energy-efficiency and the actual energy dissipation at the same algorithmic performance.

In Section 4.1, we review our past work on the information-theoretic framework. In Section 4.2, we propose the SDC model for noisy VLSI systems and develop the associated information-theoretic measures. In Section 4.3, we determine the lower bounds on energy dissipation by solving an energy optimization problem. In Section 4.4, we employ noise-tolerance to approach the lower bounds for high-speed arithmetic circuits.

4.1 Information-Theoretic Framework

In this section, we review our past work on the information-theoretic framework for deriving the lower bounds on energy dissipation of noisy logic gates.

4.1.1 Information-theoretic preliminaries

From Shannon's joint source-channel coding theory [47], the information content of a discrete data source $\mathcal{X}$ generating random symbols $X$ is measured in terms of its entropy $H(X)$, defined
as

\[ H(X) = - \sum_{X \in \mathcal{X}} P(X) \log_2 P(X), \]  

(4.1)

where \( P(X) \) is the probability mass function of \( X \) and \( H(X) \) is expressed in binary bits. This definition of the measure of information implies that the greater the uncertainty in the source output, the higher is its information content. The corresponding expression for the entropy of a continuous source is given by

\[ H(X) = - \int_{\mathcal{X}} f_X(x) \log_2 f_X(x) dx, \]  

(4.2)

where \( f_X(x) \) is the probability density function (PDF) of the continuous-valued output \( X \).

Assume that the output of the source \( \mathcal{X} \) is passed through a noisy transformation \( \mathcal{F} : \mathcal{X} \to \mathcal{Y} \), i.e.,

\[ Y = \mathcal{F}(X) + N, \]  

(4.3)

where \( \mathcal{F} \) is a deterministic mapping function from \( X \in \mathcal{X} \) to \( Y \in \mathcal{Y} \), and \( N \) denotes the noise, which is typically assumed to be a white Gaussian distribution but could also have an arbitrary distribution. Note that in a communication system, \( \mathcal{F} \) represents the channel response and \( N \) is the channel noise. In a similar fashion, for a digital gate \( \mathcal{F} \) represents the Boolean function that the gate implements and \( N \) is the DSM noise from the underlying circuits. The maximum information content that the noisy transformation \( \mathcal{F} \) can transfer per use with arbitrarily low probability of error is given by its capacity as

\[ C_u = \max_{\forall P(X)} I(X; Y), \]  

(4.4)
where $I(X; Y)$ is the mutual information, which is defined as

$$I(X; Y) = H(X) - H(X|Y) = H(Y) - H(Y|X), \quad (4.5)$$

and $H(X|Y)$ is the conditional entropy of $X$ conditioned on $Y$. The conditional entropy $H(X|Y)$ is given by

$$H(X|Y) = -\sum_{X \in \mathcal{X}} \sum_{Y \in \mathcal{Y}} P(X, Y) \log_2 P(X|Y). \quad (4.6)$$

Intuitively, the conditional entropy $H(X|Y)$ can be viewed as the residual uncertainty in $X$ given the knowledge of $Y$. Hence, the mutual information $I(X; Y)$ can be interpreted as the reduction in uncertainty in $X$ due to the knowledge of $Y$. This reduction in uncertainty is due to the information transferred per use from the input of the transformation to its output. Note that the conditional entropy $H(Y|X)$ in (4.5) is related directly to the channel noise $N$.

### 4.1.2 The BSC model

The lower bounds on energy dissipation for single-output static gates have been studied previously [20] by modeling noisy gates as a binary symmetric channel (BSC) and employing information-theoretic concepts. Consider a two-input OR gate as shown in Fig. 4.1(a), where the input $X$ is generated from $\mathcal{X} = \{00, 01, 10, 11\}$. Due to noise, the output of the gate will deviate from its nominal values. Assume that the output is passed through a hard-decision device such as a latch. The latched output, denoted by $Y$, can be regarded as a binary signal that contains errors with a probability $\epsilon$. This can be represented by the BSC model as shown in Fig. 4.1(b).

Employing the BSC model, the lower bounds on energy dissipation of single-output static gates can be determined under the information-theoretic constraint $C > R$ [20]. Note that the
average power dissipation $P_{\text{tot}}$ of these gates is given by

$$P_{\text{tot}} = P_{\text{dyn}} + P_{\text{sc}} + P_{\text{stat}}, \quad (4.7)$$

where $P_{\text{dyn}}$, $P_{\text{sc}}$, and $P_{\text{stat}}$ are the dynamic (capacitive), short-circuit, and static power dissipations, respectively. The dynamic power dissipation $P_{\text{dyn}}$ is given by

$$P_{\text{dyn}} = tC_LV_{dd}^2f_c, \quad (4.8)$$

where $t$ is the transition probability, $C_L$ is the load capacitance, $V_{dd}$ is the supply voltage, and $f_c$ is the signaling rate.

The average short-circuit power dissipation $P_{\text{sc}}$ can be described as

$$P_{\text{sc}} = tI_{sc}V_{dd}, \quad (4.9)$$

where $I_{sc}$ denotes the average short-circuit current evaluated over each signaling period. We include the transition probability $t$ in (4.9) because the short-circuit current $I_{sc}$ is present only when the gate switches.
The static power dissipation has two components

$$P_{stat} = P_{sub} + P_{DC},$$

(4.10)

where $P_{sub}$ is due to the subthreshold leakage current and $P_{DC}$ is due to the DC current. The subthreshold leakage power dissipation $P_{sub}$ can be approximated by [82]

$$P_{sub} = I_{sub}e^{-V_{fn}/V_T}V_{dd},$$

(4.11)

where $I_{sub}$ is a technology and device size dependent constant, $V_{fn}$ is the NMOS threshold voltage, and $V_T$ is the thermal voltage, which is equal to 26 mV at room temperature.

4.2 The Soft-Decision Channel Model

In this section, we extend the information-theoretic framework by modeling noisy VLSI systems as a soft-decision information transfer channel. We first provide a physical basis for the proposed model and then develop the channel capacity formula to compute the energy bounds.

4.2.1 Soft-decision channel (SDC) model

The proposed soft-decision channel (SDC) model [48] for a single-output noisy gate is illustrated in Fig. 4.2(a). In the presence of noise, the voltage waveform at the output $Y_N$ is composed of an ideal output voltage $Y$ and additive noise voltage $N$ that is assumed to be independent of the input and output $Y$, i.e.,

$$Y_N = Y + N.$$  

(4.12)
Figure 4.2 The proposed soft-decision channel (SDC) model for noisy gates: (a) voltage waveforms and (b) distribution of a noisy output.

The ideal output $Y$ is a binary signal with a statistical distribution given by $P(Y = V_{dd}) = p_y$ and $P(Y = 0) = 1 - p_y$, where $p_y$ is determined by the input statistics and the logic function of the gate. The noise voltage $N$ represents a composite effect due to thermal noise and other DSM phenomena such as ground bounce, crosstalk, charge-sharing, leakage, and process variations. We assume that the noise voltage $N$ has a probability density function (PDF) denoted by $f_N(v)$. From (4.12), this results in a statistical distribution $f_{Y_N}(v)$ for the noisy output $Y_N$, as expressed by

$$f_{Y_N}(v) = \begin{cases} 
  f_N(v - V_{dd}), & \text{if } Y = V_{dd}, \\
  f_N(v), & \text{if } Y = 0.
\end{cases} \quad (4.13)$$

Note that $Y_N$ can be considered as a bimodal continuous random signal whose value is either $V_{dd} + N$ or $N$. A typical distribution of $Y_N$ is depicted in Fig. 4.2(b), from which we can rewrite $f_{Y_N}(v)$ as

$$f_{Y_N}(v) = p_y f_N(v - V_{dd}) + (1 - p_y) f_N(v). \quad (4.14)$$

It can be shown that the previously proposed BSC model [20] is a special case of the proposed SDC model when the input and output of a noisy gate are latched synchronously. Assume that the latch being employed has a logic threshold denoted by $V_{th}$. Thus, noise voltage $N$ can
introduce logic errors at the output of the latch with a probability $\epsilon$ given by

$$\epsilon = (1 - p_y) \int_{V_{th}}^{\infty} f_N(v) dv + p_y \int_{-\infty}^{V_{th}} f_N(v - V_{dd}) dv. \quad (4.15)$$

The fundamental difference between the BSC model and the proposed SDC model comes from two aspects. First, the BSC model quantizes noise contributions by employing error probability $\epsilon$ in the computation of lower bounds. This requires noiseless hard-decision devices (e.g., latches) employed at the inputs and outputs of noisy gates. The proposed SDC model relaxes this constraint by modeling desired (noiseless) logic signals and DSM noise as binary (with a voltage level $V_{dd}$ and signaling probability $p_y$) and continuous (with a certain statistical distribution) random signals, respectively. Thus, all the signals and noise are captured in such a way that reflects their inherent analog nature. This is akin to a generic soft-decision communication system [83], where the information from both the ideal signals and channel noise are retained for signal recovery. Hence, the proposed SDC model is a generalized approach suitable for various digital systems. Furthermore, it will be shown later that the bounds on energy dissipation derived via the SDC model are much lower than those of the BSC model.

Second, the proposed SDC model leads to an efficient algorithm to compute the lower bounds on energy dissipation. The computational complexity of the algorithm increases linearly with system complexity, making the proposed SDC model applicable to complex digital systems. We will discuss this point in detail in Section 4.3.

4.2.2 Information transfer capacity

We now derive the information transfer capacity for noisy digital systems using the proposed SDC model. We start with a simple $n$-input, single-output logic gate and then extend the framework to complex systems. Lemma 1 presented below provides the formula of mutual
information for noisy gates. It is then employed in deriving the information transfer capacity in Theorem 1.

**Lemma 1:** Consider a noisy digital gate with \( n \) binary inputs \( X_0, X_1, \cdots, X_{n-1} \) and single output \( Y_N = Y + N \), where \( Y \) is the noiseless output with \( P(Y = V_{dd}) = p_y \) and all the noise sources contribute a noise voltage \( N \) with a distribution denoted by \( f_N(v) \). The mutual information \( I(Y_N; X_0, X_1, \cdots, X_{n-1}) \) for this gate is given by

\[
I(Y_N; X_0, X_1, \cdots, X_{n-1}) = -\int_{-\infty}^{\infty} \left[ f_{Y_N}(v) \log_2 f_{Y_N}(v) - f_N(v) \log_2 f_N(v) \right] dv, \tag{4.16}
\]

where \( f_{Y_N}(v) \) is the PDF of \( Y_N \), given by

\[
f_{Y_N}(v) = p_y f_N(v - V_{dd}) + (1 - p_y) f_N(v). \tag{4.17}
\]

The proof of Lemma 1 is straightforward. From the definition of mutual information (4.5), we have

\[
I(Y_N; X_0, X_1, \cdots, X_{n-1}) = H(Y_N) - H(Y_N | X_0, X_1, \cdots, X_{n-1})
\]

\[
= H(Y_N) - H(N), \tag{4.18}
\]

where both \( Y_N \) and \( N \) are continuous-valued signals. Substituting \( f_{Y_N}(v) \) and \( f_N(v) \) into (4.18) and using (4.2), we get (4.16).

Note that \( I(Y_N; X_0, X_1, \cdots, X_{n-1}) \) given by (4.16) is a function of supply voltage \( V_{dd} \), noise distribution \( f_N(v) \), and output probability \( p_y \). The value of \( p_y \) is determined by the input
statistics and the logic function of the gate. From Lemma 1, we obtain the information transfer capacity per use as summarized below.

**Theorem 1:** The information transfer capacity per use $C_u$ of an $n$-input, single-output noisy gate is given by

$$C_u = \max_{\mathcal{P}_x} I(Y_N; X_0, X_1, \cdots, X_{n-1})$$

$$= I(Y_N; X_0, X_1, \cdots, X_{n-1}) |_{p_y=0.5}. \quad (4.19)$$

The proof of Theorem 1 is provided in Appendix A. Theorem 1 indicates that the capacity per use $C_u$ is achieved when the ideal output $Y$ has a uniform distribution (i.e., $P(Y = V_{dd}) = P(Y = 0) = 0.5$). This is consistent with the observation that $p_y = 0.5$ implies the maximum uncertainty in $Y$ and hence the largest information content being transferred.

Figure 4.3(a) plots the mutual information $I(Y_N; X)$ from Lemma 1 for a two-input OR gate in a 0.25-μm CMOS process. The noise voltage $N$ is assumed to be a zero-mean Gaussian distribution with a variance $\sigma_N = 0.4$ V. As indicated, for every supply voltage $V_{dd}$, $I(Y_N; X)$ reaches the maximum when $p_y = 0.5$. In addition, $I(Y_N; X)$ is symmetric around $p_y = 0.5$. This is consistent with the BSC model. The capacity per use $C_u$ approaches 1 bit/use as $V_{dd}$ increases. This can be interpreted as the ability of the two-input OR gate to transfer 1 bit of information for every use provided the supply voltage $V_{dd}$ is sufficiently high with respect to noise. This is to be expected given the fact that at a high $V_{dd}$, noise becomes negligible and the gate can be approximated as being noiseless. On the other hand, $C_u$ decreases towards zero with the reduction in $V_{dd}$. This reflects the practical scenario where the gate fails to function when being powered off.
Figure 4.3 Mutual information with respect to $V_{dd}$ and $p_y$: (a) with $\sigma_N = 0.4$ V and (b) the increase for $\sigma_N = 0.3$ V.

The impact of noise on $C_u$ is illustrated in Fig. 4.3(b), where we observe an increase in $I(Y_N; X)$ (and hence $C_u$) as noise variance $\sigma_N$ being reduced from 0.4 V to 0.3 V. Obviously, a gate operating in a less noisy medium is more robust and hence can transfer more information.

We now compute the information transfer capacity. Assume that the NMOS and PMOS transistors being used are balanced, implying identical low-to-high and high-to-low delays. The maximum signaling rate $f_c$ at a supply voltage $V_{dd}$ can be approximated by [73]

$$f_c = \frac{k_m(V_{dd} - V_t)^{\alpha}}{C_L V_{dd}},$$

(4.20)

where $k_m$ is the transconductance of the balanced NMOS and PMOS transistors, $C_L$ is the load capacitance, $V_t$ is the transistor threshold voltage, and $\alpha$ is the velocity saturation index ranging from 1 (velocity saturated) to 2 (without velocity saturation). The information transfer capacity can be obtained as $C = C_u f_c$, where $C_u$ and $f_c$ are given by (4.19) and (4.20), respectively.

As an example, we consider the two-input OR gate in a 0.25-$\mu$m CMOS process with the following parameters: (1) $k_m = 80 \mu A/V^2$, (2) $V_m = |V_{tp}| = 0.4$ V, (3) $C_L = 30 fF$, (4) $\alpha = 1.2$, and (5) information transfer rate $R = 800$ Mbit/s. The noise voltage $N$ is assumed to be
a zero-mean Gaussian distribution with a variance $\sigma_N = 0.4$ V. At $V_{dd} = 2.5$ V, we obtain $C = 1$ bit/use and $f_c = 2.598$ GHz. Therefore, the information transfer capacity of the gate is given by $C = C_u f_c = 2.598$ Gbit/s. Similarly, at $V_{dd} = 1.0$ V, we obtain $C_u \approx 0.6$ bit/use and $f_c = 1.445$ GHz. This gives $C = 867$ Mbit/s, which is still larger than the information transfer requirement $R$, implying that the gate is possible to achieve reliable operation even at a supply voltage as low as 1.0 V. Present-day digital circuits operate at sufficiently high voltages so that $C_u = 1$ bit/use and hence $R$ can be as high as $f_c$.

It is worth mentioning that (4.19) and (4.20) provide a direct correspondence between the information transfer capacity $C$ and implementation details such as supply voltage, load capacitance, circuit style, CMOS process, and noise parameters. While in this chapter we employ rather general models for speed and noise, any specific assumptions or changes can be easily incorporated into the framework. One such example is the computation of bounds on energy dissipation for noise-tolerant circuit techniques (see Section 4.3.5), where noise contributions are modeled as an input noise voltage rather than at the output as in the SDC model. Assuming the gate with a voltage transfer characteristic (VTC) function $T$ [31], the equivalent output noise voltage can be expressed as

$$N_{out} = T(N_{in}), \quad (4.21)$$

and has a distribution given by [84]

$$f_{N_{out}}(v) = \sum_{i=1}^{p} \frac{f_{N_{in}}(v_i)}{|T'(v_i)|}, \quad (4.22)$$

where $f_{N_{in}}(v)$ and $f_{N_{out}}(v)$ are the PDFs for the input noise voltage $N_{in}$ and the equivalent output noise voltage $N_{out}$, respectively, and $v_i = v_i(v)$ is the root of (4.21). By substituting $f_{N_{out}}(v)$ as $f_N(v)$ into (4.16), (4.17), and (4.19), we can compute the information transfer capacity.
4.3 Lower Bounds on Energy Dissipation

In this section, we determine the lower bounds on energy dissipation using the proposed SDC model. These bounds are obtained by solving an energy optimization problem while being subject to the information-theoretic constraint $C > R$. In Section 4.3.1, we formulate the constrained optimization problem and develop an analytical solution by employing the Lagrange multiplier method [85]. In Section 4.3.2, we present an algorithm for computing the lower bounds and then apply it to static gates, multimodule systems, dynamic circuits, and noise-tolerant dynamic circuits in Section 4.3.3 to Section 4.3.5, respectively.

4.3.1 Problem formulation and solution

Consider a generic digital system as depicted in Fig. 4.4. We assume without loss of generality that the system consists of $m$ noisy modules, each generating an ideal (noiseless) output denoted by $Y_i$ for $i = 0, 1, \cdots, m-1$. The input of the system is given by $X = \{X_0, X_1, \cdots, X_{n-1}\}$, where $X_i$ is a binary signal. From the SDC model, the total noise contribution can be represented by $m$ output noise voltages $N_0, N_1, \cdots, N_{m-1}$. In addition, we assume these noise voltages are independent of each other. Thus, the outputs of the system can be expressed as

$$Y_{N_i} = Y_i + N_i, \quad i = 0, 1, \cdots, m - 1,$$

(4.23)
where $Y_{N_i}$ denotes the actual voltage waveform at the $i^{th}$ output and $N_i$ is the corresponding noise voltage with a distribution given by $f_{N_i}(v)$.

We consider a silicon implementation where all the NMOS and PMOS transistors share a common power supply and ground. In addition, the NMOS and PMOS transistors are properly sized so that the modules can be operated at the same maximum speed given by (4.20). For the sake of simplicity, we assume that all the capacitances including the parasitic capacitance, interconnect capacitance, and input capacitance from the following stage are lumped into the load capacitance at the output of the system. The total power dissipation $P_{tot}$ of the system is given by (4.7), where $P_{dyn}$, $P_{sc}$, and $P_{stat}$ are composed of power components from the $m$ different modules. In particular, the dynamic power dissipation $P_{dyn}$ is given by

$$P_{dyn} = \sum_{i=0}^{m-1} t_i C_{L_i} V_{dd}^2 f_c,$$  \hspace{1cm} (4.24)

where $t_i$ and $C_{L_i}$ are the average transition probability and the equivalent load capacitance, respectively, for the $i^{th}$ output, and $f_c$ is given by (4.20).

We note that for dynamic circuits such as conventional domino, $t_i$ will be equal to the probability of output $Y_i$ being $V_{dd}$ (or a logic "1"). i.e., $t_i = p_y$. This is valid for static circuits as well provided transition signaling [20] (i.e., a logic "1" is represented with a transition and a logic "0" is represented with no transition) is employed at the output. Therefore, in the rest of this chapter we will replace $p_y$ in the information capacity expressions (4.16)–(4.19) with the transition probability $t$ as these two measures are equivalent.

Past work [20] studied the lower bounds on energy dissipation using the BSC model for the special case of single-output static gates (i.e., $m = 1$). It was shown that the lower bounds are achieved when $I(Y_N; X)f_c = [h(t) - h(e)]f_c = R$, where $h(x) = -x\log_2(x) - (1-x)\log_2(1-x)$ is the entropy function for binary signals, $R$ is the information transfer rate, and $e$ is the probability
of output being in error which can be obtained from (4.15). In this chapter, we determine the lower bounds for noisy systems as shown in Fig. 4.4 using the SDC model. As discussed in Section 4.2, the mutual information \( I(Y_{N_0}, \cdots, Y_{N_{m-1}}; X_0, \cdots, X_{n-1}) \) for such systems is determined by the supply voltage \( V_{dd} \), output transition probabilities \( t_0, t_1, \cdots, t_{m-1} \), and noise parameters. Thus, we rewrite \( I(Y_{N_0}, \cdots, Y_{N_{m-1}}; X_0, \cdots, X_{n-1}) \) as an explicit function of these parameters as

\[
I(Y_{N_0}, \cdots, Y_{N_{m-1}}; X_0, \cdots, X_{n-1}) = I_{Y;X}(V_{dd}, t_0, \cdots, t_{m-1}, \sigma_{N_0}^2, \cdots, \sigma_{N_{m-1}}^2),
\]

where \( \sigma_{N_i}^2 \) is the variance (energy) of noise voltage \( N_i \), which is determined by the distribution function. Employing similar arguments as in [20], the lower bounds on energy dissipation can be obtained by solving the following optimization problem:

\[
\begin{align*}
\text{minimize: } & E_b = \frac{P_{tot}}{R} \\
\text{subject to: } & I_{Y;X}(V_{dd}, t_0, \cdots, t_{m-1}, \sigma_{N_0}^2, \cdots, \sigma_{N_{m-1}}^2) f_c = R,
\end{align*}
\]

where \( E_b \) is the energy per information bit.

Note that for any given supply voltage \( V_{dd} \) and noise parameters, the power dissipation \( P_{tot} \) and information-theoretic constraint (4.27) are functions of output transition probabilities \( t_0, t_1, \cdots, t_{m-1} \). Hence, the optimum solution to (4.26)–(4.27) results in a combination of \( t_i \)'s that minimizes the power dissipation of the system while satisfying the information-theoretic constraint. In what follows, we will consider \( P_{tot} \) as primarily consisting of dynamic power dissipation for the purpose of illustration. Extending \( P_{tot} \) to include other power components (e.g., short-circuit and static power) is straightforward and the corresponding lower bounds are
determined for domino and noise-tolerant circuits in Section 4.3.5. Employing the Lagrange multiplier method [85], we obtain the optimum solution to (4.26)-(4.27) as summarized in Theorem 2.

**Theorem 2:** The lower bound on energy dissipation for a digital system consisting of \( m \) noisy modules is achieved at the transition probabilities \( t_0^{\text{opt}}, t_1^{\text{opt}}, \ldots, t_{m-1}^{\text{opt}} \) satisfying

\[
\frac{\partial I_{Y_N;X}(V_{dd}, t_i, \sigma_{N_i}^2)}{\partial t_i} \bigg|_{(t_i = t_i^{\text{opt}})} = \beta_{\text{max}} C_{L_i} V_{dd}^2,
\]

\[i = 0, 1, \ldots, m-1,
\]

(4.28)

where \( C_{L_i} \), \( t_i \), and \( \sigma_{N_i}^2 \) are the load capacitance, transition probability, and noise variance, respectively, at the \( i \)th output, \( \beta_{\text{max}} \) is a constant determined via the information-theoretic constraint (4.27), and \( I_{Y_N;X}(V_{dd}, t_i, \sigma_{N_i}^2) \) is the mutual information for the \( i \)th output, which is given by

\[
I_{Y_N;X}(V_{dd}, t_i, \sigma_{N_i}^2)
= - \int_{-\infty}^{\infty} \left( t_i f_{N_i}(v - V_{dd}) + (1 - t_i) f_{N_i}(v) \right) \log_2 \left( t_i f_{N_i}(v - V_{dd}) + (1 - t_i) f_{N_i}(v) \right)
- f_{N_i}(v) \log_2 f_{N_i}(v) \, dv,
\]

(4.29)

where \( f_{N_i}(v) \) is the distribution function for the output noise \( N_i \).

The proof of Theorem 2 is provided in Appendix B. In the following sections, we will demonstrate the use of Theorem 2 to compute the lower bounds on energy dissipation for various digital VLSI systems.
Figure 4.5 The algorithm to compute the lower bounds on energy dissipation.

4.3.2 Computation of lower bounds

We assume that the NMOS and PMOS transistors being used are properly sized to meet speed requirements. Thus, the parameters $k_m$ and $C_{L,t}$'s are fixed making the lower bounds a function of the supply voltage $V_{dd}$ and transition probabilities $t_i$'s. From Theorem 2, the objective is to find an optimum combination $(t_0^{opt}, t_1^{opt}, \ldots, t_{m-1}^{opt})$ at each $V_{dd}$ such that the power dissipation is minimized subject to the information-theoretic requirement $R$. Figure 4.5 shows the algorithm for computing the lower bounds. For each $V_{dd}$ we start with a sufficiently small $\beta$ and compute the values of $t_i$'s using (4.28)–(4.29). These $t_i$'s are then employed to compute the information transfer metric $I_{Y_{N:1}}(V_{dd}; t_0, \ldots, t_{m-1}, \sigma_{N_0}^2, \ldots, \sigma_{N_{m-1}}^2)f_c$ and the result is compared to the information transfer rate $R$. If $I_{Y_{N:1}}(V_{dd}; t_0, \ldots, t_{m-1}, \sigma_{N_0}^2, \ldots, \sigma_{N_{m-1}}^2)f_c > R$, the value of $\beta$ will be increased in small steps till (4.27) is just satisfied. The correspond-
ing transition probabilities $t_i$'s are then employed with $V_{dd}$ to obtain the bounds on power dissipation.

Note that in contrast to the BSC model [20] for single-output gates, the proposed algorithm determines the lower bounds analytically by joint optimization of power components from all the modules in the system. The associated computational complexity increases linearly with system complexity, making the proposed algorithm suitable for determining the energy-efficiency bounds of complex digital systems.

We now determine the lower bounds on energy dissipation for single-output static gates, multimodule systems, dynamic circuits, and noise-tolerant techniques. We first consider a two-input OR gate which is a special case of Theorem 2 where the system is simply a single-output noisy gate.

### 4.3.3 Lower bounds for a two-input OR gate

We make the following assumptions in deriving the lower bounds on energy dissipation for the two-input OR gate:

1.) The gate is implemented in a 0.25-μm CMOS process in static CMOS logic style with dual NMOS and PMOS networks.

2.) The NMOS and PMOS transistors are balanced with the same propagation delay. The speed of the gate is given by (4.20), where $C_L = 30\text{fF}$, $k_m = 80\ \mu A/V^2$, $V_n = |V_{tp}| = 0.4\ \text{V}$, and $\alpha = 1.2$.

3.) The noise voltage $N$ has a zero-mean Gaussian distribution with $\sigma_N = 0.4\ \text{V}$. The noise is uncorrelated to the desired input and output signals.

4.) The gate has an information transfer rate requirement $R = 800\ \text{Mbit/s}$.

Using the algorithm in Fig. 4.5, we obtain the lower bound on energy per information bit $E_b$ with respect to the supply voltage $V_{dd}$ as shown in Fig. 4.6. For the purpose of comparison,
we also plot the bound estimated via the BSC model [20]. As indicated, with the increase in $V_{dd}$ we first observe a net reduction on energy dissipation. This is because that increasing $V_{dd}$ leads to a faster speed (higher $f_c$) enabling us to reduce the transition probability $t$ while still satisfying the information transfer requirement. The decrease in $t$ offsets the increase in $V_{dd}$ initially. Further increasing $V_{dd}$ does not result in sufficient reduction in $t$ and hence we see an increase in the energy bound. Thus, the minimum supply voltage for reliable operation is smaller than the voltage for the minimum energy. This is consistent with our past work [20].

An important result from Fig. 4.6 is that the bound derived via the SDC model is lower than that of the BSC model. The minimum energy dissipation is found around 15 fJ/bit at $V_{dd} = 1.18$ V, which is 37.5% below that of the BSC model (24 fJ/bit at $V_{dd} = 1.21$ V). This is to be expected because the SDC model retains signal and noise characteristics without incurring any information loss.

In addition to the lower bound on energy dissipation, we can also derive the bounds on other design parameters such as transition probability $t$, supply voltage $V_{dd}$, signaling rate $f_c$, and noise variance (energy) $\sigma_N^2$. The lower bound on $t$ is obtained at $I(V_{dd}, t, \sigma_N^2)f_c = R$ because
$I(V_{dd}, t, \sigma_N^2)$ is an increasing function with respect to $t$ for $0 \leq t \leq 0.5$. In fact, this bound is equal to the optimum solution $t^{opt}$ in (4.28) for single-output gates. This indicates that for reliable operation, an information-bearing output signal needs to have a transition probability in the range of $t^{opt} \leq t \leq t_{max} = 0.5$. Note that from the information-theoretic viewpoint, increasing $t$ beyond 0.5 will reduce the information content of a signal (see Fig. 4.3(a)).

The minimum value of supply voltage $V_{dd}$ is obtained at $I(V_{dd}, t, \sigma_N^2)f_c = R$ when $t = t_{max}$. This is because both $I(V_{dd}, t, \sigma_N^2)$ and $f_c$ are increasing functions with respect to $V_{dd}$. In addition, the same value of $I(V_{dd}, t, \sigma_N^2)f_c$ can be obtained by decreasing $V_{dd}$ while increasing $t$ till $t = t_{max}$. The minimum value of signaling rate $f_c$ can be determined correspondingly from (4.20).

From Fig. 4.6, $V_{dd,min} = 0.95$ V for the two-input OR gate using the SDC model. Also, $V_{dd,min}$ is smaller than the voltage for the minimum energy, which is 1.18 V from our simulation. Note that $t = t_{max}$ when $f_c = f_{c,min}$. From Theorem 1, the gate is operating at its capacity.

The upper bound on noise energy $\sigma_N^2$ that a gate can tolerate for reliable operation is also obtained at $I(V_{dd}, t, \sigma_N^2)f_c = R$ when $t = t_{max}$. This is because $I(V_{dd}, t, \sigma_N^2)$ is a decreasing function with respect to $\sigma_N^2$ and the same value of $I(V_{dd}, t, \sigma_N^2)f_c$ can be obtained by increasing $t$ if $\sigma_N^2$ becomes larger.

Figure 4.7 shows the upper bound on $\sigma_N$ for the two-input OR gate. The gate can achieve reliable operation at a signal-to-noise ratio (SNR) as low as 5 dB. This is consistent with conventional understanding that digital circuits are relatively robust to noise. However, with feature sizes being reduced towards future DSM generations, noise is emerging as a critical factor that may ultimately determine the performance achievable in complex digital systems. This necessitates effective noise-tolerant techniques as will be discussed later.
Figure 4.7 Upper bound on $\sigma_N$ for reliable operation.

4.3.4 Lower bounds for multimodule systems

We now determine the lower bounds on energy dissipation for digital systems consisting of multiple logic modules, each of which generates a noisy output while consuming a certain amount of power. In contrast to the bounds of single-output gates, the power dissipation is minimized by jointly optimizing the power components of different modules under the information-theoretic constraint. For the purpose of demonstration, we will consider a full adder which has a SUM module and a CARRY module. The lower bounds for more complex digital systems can be determined in a similar manner.

We assume the same design parameters for the full adder as those for the two-input OR gate. Note that in practice the CARRY and SUM modules are possibly subject to noise with different amplitudes or drive different load capacitances. This results in different energy bounds and hence we will evaluate them separately.

We first consider the case where the two modules are subject to different noise amplitudes but with the same load capacitance of 30 fF. We assume that the noise voltages $N_{\text{sum}}$ and $N_{\text{carry}}$ are zero-mean Gaussian distributions with $\sigma_{N_{\text{sum}}} = 0.4 \text{ V}$ and $\sigma_{N_{\text{carry}}} = 0.3 \text{ V}$, respectively.
Figure 4.8 Lower bounds on energy dissipation for multmodule systems subject to (a) different noise and (b) different load capacitances.

This implies a more reliable CARRY module. Figure 4.8(a) illustrates the lower bounds for the SUM module, CARRY module, and the full adder. We observe that these bounds have a similar trend as those of single-output gates. The minimum values of energy per information bit $E_b$ for the SUM module, CARRY module, and full adder equal 5.1 fJ/bit, 6.7 fJ/bit, and 12 fJ/bit at $V_{dd} = 1.1 \text{ V}$, 1.0 V, and 1.08 V, respectively. Also shown in Fig. 4.8(a) is that the lower bound for the full adder is achieved when the CARRY module consumes more energy than the SUM module does. This is the same as saying that to achieve an information transfer requirement with minimum energy; we need to allocate more energy to the more reliable modules. This observation is similar to the water-filling argument [86] in the spectral domain.

Figure 4.8(b) illustrates the lower bounds on energy dissipation when the SUM and CARRY modules drive different load capacitances of 20 fF and 30 fF, respectively, but subject to the same noise amplitude ($\sigma_N = 0.4 \text{ V}$). It indicates that the lower bound for the full adder is achieved when the output driving a larger capacitance consumes less energy. This is to be expected because such output will have a smaller transition probability (see (4.28)) which offsets the energy overhead due to a large capacitance.
Figure 4.9 Dynamic style three-input OR gates: (a) conventional domino and (b) the mirror technique.

4.3.5 Energy-efficiency bounds for noise-tolerant circuits

Noise-tolerant circuit techniques [24]–[26], [28], [29], [80] improve noise-immunity by employing additional elements to prevent logic errors from occurring in the presence of noise. Thus, one would expect noise-tolerant circuits to be less energy-efficient than conventional circuits. In this section, we determine the lower bounds on total power dissipation including dynamic, short-circuit, and static power components for noise-tolerant circuit techniques such as the mirror technique [28], [29]. It will be shown that noise-tolerance improves the energy-efficiency when operating at the lower bound.

Figure 4.9 depicts two three-input OR gates implemented by the conventional domino (with a keeper) and the mirror technique in a 0.25-μm CMOS technology. It is known that domino circuits are inherently susceptible to noise [4] due to their low switching threshold voltage $V_{th}$, defined as the input voltage at which the output changes state. For the domino OR gate shown in Fig. 4.9(a), $V_{th} = V_{in}$, where $V_{in}$ is the threshold voltage of an NMOS transistor. The previously proposed mirror technique [28], [29] improves noise-immunity via employing two identical NMOS evaluation nets. One additional NMOS transistor M1, whose gate voltage is controlled by the dynamic node voltage, provides a conduction path between the common node

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$x$ of the two evaluation nets and $V_{dd-nt}$. During the precharge phase, transistor M1 is turned on and the common node voltage $V_x$ is charged up to $(V_{dd-nt} - V_{tn})$. Due to the body-effect, the switching threshold voltage of the upper NMOS net is increased, thereby improving the noise-immunity. Note that the noise-immunity of the gate can be tuned by either changing the voltage $V_{dd-nt}$ or resizing the transistor M1.

The total power dissipation of digital gates consists of dynamic power $P_{dyn}$, short-circuit power $P_{sc}$, and static power $P_{stat}$, where $P_{stat}$ has two components $P_{sub}$ (due to subthreshold leakage) and $P_{DC}$ (due to DC power dissipation). Considering the fact that the two gates in Fig. 4.9 consume no $P_{DC}$ and $P_{sub}$ is relatively small for this technology ($V_{tn} = 0.4$ V), we express the total power dissipation as

$$P_{tot} = tC_L V_{dd}^2 f_c + tI_{sc} V_{dd}, \quad (4.30)$$

where $I_{sc}$ is the average short-circuit current evaluated over each signaling period. Note that the two gates consume nontrivial short-circuit power as indicated in Fig. 4.9.

From (4.30), the problem of deriving the energy-efficiency bounds for domino and mirror circuits is stated as

$$\begin{align*}
\text{minimize:} & \quad E_b = \frac{tC_L V_{dd}^2 f_c + tI_{sc} V_{dd}}{R}, \\
\text{subject to:} & \quad I_{YN,X}(V_{dd}, t, \sigma_N^2) f_c = R. \quad (4.31) \quad (4.32)
\end{align*}$$

From Theorem 2, the solution to (4.31)–(4.32) can be obtained as

$$\frac{\partial I_{YN,X}(V_{dd}, t, \sigma_N^2)}{\partial t}(t = t^{opt}) = \beta_{max} \left( C_L V_{dd}^2 + I_{sc} V_{dd} T_c \right), \quad (4.33)$$

where $T_c = 1/f_c$ is the signaling period.
Figure 4.10 Lower bounds on energy dissipation via the BSC model for (a) different $V_{dd-nt}$ and (b) different M1.

Figure 4.10 compares the lower bounds on energy dissipation for the domino and mirror three-input OR gates using the BSC model. As shown, the lower bound on energy dissipation of the mirror gate lies below that of the conventional domino gate at an optimum design point of $V_{dd-nt} = V_{dd}$ and transistor M1 being 8X the minimum size. This implies that noise-tolerant circuits are more energy-efficient than conventional domino when operating at the lower bound. If $V_{dd-nt} = 1.5V_{dd}$ then $P_{sc}$ starts to dominate, and if $V_{dd-nt} = 0.75V_{dd}$ then error probability $e$ starts to increase and so does $t$. Also, increasing the width of M1 beyond the optimum point leads to larger parasitic capacitances and higher short-circuit currents. These result in an energy overhead that offsets the noise-immunity improvement, thereby leading to a higher energy-efficiency bound.

Figure 4.11 illustrates the lower bounds derived from the proposed SDC model, where the mirror three-input OR gate has $V_{dd-nt} = V_{dd}$ and M1 being 8X the minimum size. As we designed the two gates with the same speed, the pull-down NMOS transistors in Fig. 4.9(b) are sized up resulting in larger parasitic capacitances. We account for this design overhead by extracting the capacitances from the layout and adding them to a 30-fF load capacitance. Note
that the mirror technique was developed primarily to protect digital gates from input noise. Thus, we assume both gates with an input noise voltage $N_{in}$ which is zero-mean Gaussian with $\sigma_{N_{in}} = 0.4\, V$. The equivalent output noise voltages are obtained from (4.21)–(4.22) and employed in (4.33) in deriving the lower bounds. As shown, the minimum $E_b$ of the conventional domino gate is found to be $20\, fJ$/bit, whereas that of the mirror gate is $13\, fJ$/bit, which is 35% lower. This again proves that noise-tolerant circuits improve energy-efficiency when operating at the lower bound. Noise-tolerant circuits are robust to noise and this property can be utilized to reduce the transition probability $t$ and supply voltage $V_{dd}$ while still satisfying the information-theoretic constraint. A net reduction in total power dissipation can be obtained if the reduction in $t$ and $V_{dd}$ offsets the design overhead.

As seen in Fig. 4.11, the minimum supply voltage for reliable operation of noise-tolerant circuits is lower than that of the conventional domino. This is because a smaller equivalent output noise due to improvement in noise-immunity leads to a smaller signaling rate $f_c$ when the transition probability $t$ achieves its maximum value.
4.4 Application to High-Speed, Low-Power Arithmetic Circuits

In this section, we propose to employ noise-tolerance in high-speed arithmetic circuits to reduce power dissipation subject to a specified level of algorithmic performance, thereby reducing the gap between the bounds on energy-efficiency and the actual energy dissipation of practical systems. In particular, we consider adders with large word sizes which are a key datapath element in the design of high-performance microprocessors and digital signal processing systems. The problem of improving reliability while maintaining energy-efficiency is of great importance given the design challenge of achieving high data rate in noisy media. This requires joint optimization of noise-immunity, energy dissipation, and speed, as well as other design parameters.

Wide adders are typically constructed by combining identical addition modules from a smaller size. One commonly used module is the Manchester domino adder [31] which employs the concept of carry lookahead for speed improvement. In Section 4.4.1, we propose a noise-tolerant scheme based on the mirror technique to improve the noise-immunity of conventional Manchester adders. In Section 4.4.2, we quantify the performance of the proposed noise-tolerant scheme. In Section 4.4.3, we insert this noise-tolerant module into a 16-bit adder for a digital signal processing system and demonstrate 31.2% - 51.4% energy reduction and 1.9X gap reduction at the same algorithmic performance.

4.4.1 Noise-tolerant, high-speed adder design

The speed of wide adders is limited by the speed of carry signals propagating through the carry chain. Carry lookahead technique [31] computes carry signals to each stage in parallel, thereby improving the speed. For the $i^{th}$ stage, the carry signal $C_i$ and sum signal $S_i$ are
obtained as

\[ C_i = G_i + P_i C_{i-1}, \]  \hspace{1cm} (4.34)

\[ S_i = P_i \oplus C_{i-1}, \]  \hspace{1cm} (4.35)

where "\( \oplus \)" denotes the XOR operation, \( G_i \) and \( P_i \) are the generate and propagate signals, respectively, which are given by

\[ G_i = A_i B_i, \]  \hspace{1cm} (4.36)

\[ P_i = A_i + B_i, \]  \hspace{1cm} (4.37)

where \( A_i \) and \( B_i \) are the \( i \)th bit of two input operands \( A \) and \( B \), respectively. Expanding (4.34), we get

\[ C_i = G_i + P_i G_{i-1} + P_i P_{i-1} G_{i-2} + \cdots + P_i \cdots P_1 C_0. \]  \hspace{1cm} (4.38)

From (4.38), the complexity of computing \( C_i \) becomes large very quickly as the bit-width increases. Hence, carry lookahead addition typically spans no more than four stages.

Manchester adders employ a domino style of carry lookahead addition for high-speed and low-complexity. Figure 4.12(a) illustrates the circuit schematic of a conventional Manchester adder, where the carry signals \( \overline{C_0} - \overline{C_4} \) are generated in parallel from internal nodes. A carry-bypass scheme is employed to reduce the worst-case delay when all \( P_i = 1 \).

While Manchester adders are faster, the inherent domino style is susceptible to noise, thereby putting a tight requirement on supply voltage for reliable operation. This combined with high data rates results in high power dissipation of these systems. In Section 4.3.5, we have shown that noise-tolerance is an effective way to improve the lower bound on energy-efficiency. In this section, we apply the mirror technique to the design of a noise-tolerant Manchester adder. As
shown in Fig. 4.12(b), the proposed scheme protects the error-prone dynamic nodes $\overline{C_0} - \overline{C_4}$ by employing mirror transistors for short pull-down paths (which are the paths consisting of NMOS transistors with $G_1$ and CLK as their inputs). Note that this approach is effective because a longer pull-down path with more stacked NMOS transistors is more robust to noise. In addition, short pull-down paths are not on the critical delay paths and hence do not affect the overall speed.

4.4.2 Performance measures

We assume that the magnitude and duration of intermittent noise pulses are sufficient to cause logic errors. The error probability $\epsilon$ for dynamic gates can be obtained from the noise-immunity curves (denoted by $C_{nic}$) [69]. As shown in Fig. 4.13, a point on the $C_{nic}$ indicates the duration $T_n$ and amplitude $V_n$ of an input noise pulse that will erroneously discharge dynamic nodes and cause an output error. Thus, noise pulses corresponding to the points that lie above
the $C_{nic}$ will cause output errors. Obviously, the more noise-immune a circuit technique is, the higher its $C_{nic}$ will be.

Assume that the evaluation time equals $T_e/2 = 1/(2f_c)$ and that the corresponding point on the $C_{nic}$ is denoted by $V_N$. Given a noise model that consists of a distribution $f_{V_n,T_n}(v,t)$ on the amplitude and duration as shown in Fig. 4.13, the error probability $\epsilon$ can be obtained as

$$\epsilon = \int_{V_N}^{\infty} \int_{t_v}^{T_e/2} f_{V_n,T_n}(v,t)dt dv,$$

(4.39)

where the second integral starts from $t_v$ (determined by the variable $v$ of the first integral and the given $C_{nic}$) and ends at $T_e/2$. From (4.39), $\epsilon$ is a function of supply voltage $V_{dd}$ because both $T_e$ and $V_N$ are functions of $V_{dd}$. Note that noise-tolerant circuits have a smaller probability of error $\epsilon$ as compared to conventional domino. Also, a higher $V_{dd}$ reduces $\epsilon$.

It is more convenient to use the measure of mean-squared error (MSE) for arithmetic circuits because errors at different output bits have different weights (e.g., an error occurring at the $i^{th}$ bit has a value of $\pm 2^i$). The MSE, denoted by $\sigma_{\epsilon}^2$, for an $n$-bit adder is defined as

$$\sigma_{\epsilon}^2 = \sum_{i=0}^{n-1} \epsilon_i (2^i)^2,$$

(4.40)

where $\epsilon_i$ is the error probability at the $i^{th}$ output bit and can be computed via (4.39).
4.4.3 Performance comparison

We now present the results of algorithmic performance and energy dissipation for the proposed noise-tolerant adder scheme in the context of a CDMA wireless communication system [81]. The basic principle of CDMA is to spread the spectrum of a narrowband message signal by multiplying it with a wideband binary pseudo-noise (PN) sequence whose rate is $N_c$ times that of the original signal, where $N_c$ is the length of the PN sequence. It can be shown that this type of modulation has the advantage of suppressing jamming, interference from other users, and self-interference due to multipath propagation. Due to this, CDMA techniques have been widely employed in multiuser wireless communications.

At the receive end, the incoming signal needs to be despread by the same PN sequence to recover the transmitted symbols. This can be achieved by a correlation operation as illustrated in Fig. 4.14, where the multiplication simply obtains the absolute value of the received signal. We assume that the received signal $r[n]$ has 8-bit precision and the length of the binary PN sequence $p[n]$ is $N_c = 256$. The accumulation is conducted in 16-bit precision, requiring four 4-bit Manchester adders (see Fig. 4.12) for high-speed addition. The noise from the underlying circuits is assumed to have an amplitude $V_n$ which is zero-mean Gaussian with $\sigma_n = 0.4 \, \text{V}$, and a duration $T_n$ which is uniformly distributed between 0 and $T_c/2$. The magnitude and duration of intermittent noise pulses are sufficient to cause logic errors during accumulation. The error probability is computed from (4.39) and then employed to flip the adder outputs in order to
Figure 4.15  Performance of the proposed noise-tolerant scheme: (a) energy dissipation versus algorithmic performance and (b) in comparison with the lower bounds.

emulate a noisy hardware. The final output has a SNR requirement of 20 dB as recommended in [87], which is expressed as

$$SNR = 10 \log_{10} \left( \frac{\sigma_s^2}{\sigma_n^2 + \sigma_e^2} \right) \geq 20dB,$$  \hspace{1cm} (4.41)

where $\sigma_s^2$ and $\sigma_n^2$ are the variances of the desired signal and signal noise, respectively, and $\sigma_e^2$ is given by (4.40).

Figure 4.15(a) shows the plot of energy dissipation versus SNR for different designs. The curve denoted by "NT(i)" refers to the 16-bit adder where the top $i$ MSBs are implemented via the mirror technique (see Fig. 4.12(b)). To achieve the specified SNR, the domino Manchester adder consumes the maximum energy due to its low noise-immunity requiring a high $V_{dd}$ for reliable operation. For the proposed noise-tolerant scheme, NT(8) consumes the minimum amount of energy, indicating that it the optimum in terms of energy-efficiency. Figure 4.15(b) plots the energy per information bit $E_b$ at the specified SNR of 20 dB for different implementations along with the lower bounds. We observe that noise-tolerant designs reduce energy dissipa-
tion by 31.2% – 51.4% over conventional implementations. Furthermore, the lower bounds and the actual energy dissipation are closer by a factor of 1.9X from conventional domino (5.3X above the bound) to NT(8) (2.3X above the bound). This is primarily due to the improvement in noise-immunity making reliable operation easy to achieve at low supply voltages. Using noise-tolerance for more MSBs (e.g., NT(12) and NT(16)) makes design overhead offset the noise-immunity improvement, thereby increasing the energy dissipation. On the other hand, NT(4) is shown to be insufficient in noise-immunity and thereby incurring a large energy as well.

4.5 Summary

A general algorithm has been presented in this chapter for deriving the lower bounds on energy dissipation of noisy digital systems. These bounds are obtained by modeling digital systems as a soft-decision communication network and employing information-theoretic considerations. We determine the lower bounds analytically for various digital systems including static gates, multmodule systems, dynamic circuits, and noise-tolerant techniques. It is shown that the energy bounds are lower than those obtained in our previous work due to the more accurate and comprehensive model being used. We also compare the energy-efficiency bounds for conventional domino and noise-tolerant circuits, and determine to what extent noise-immunity needs to be enhanced before the energy overhead starts to dominate. Furthermore, we employ the concept of noise-tolerance to approach the lower bounds on energy dissipation for high-speed arithmetic circuits. A 16-bit carry lookahead adder in the context of a CDMA communication system demonstrates 31.2% – 51.4% energy reduction over conventional implementations and a factor of 1.9X reduction in the gap between the information-theoretic bounds and the actual energy dissipation without algorithmic performance loss.
CHAPTER 5

ADAPTIVE ERROR-CANCELLATION FOR LOW-POWER SIGNAL PROCESSING

In this chapter, we present an algorithmic noise-tolerance (ANT) technique referred to as the adaptive error-cancellation (AEC) [55] for combating transient (soft) errors that can arise in integrated circuit implementations of signal processing and communication systems in current and future semiconductor technologies. These errors arise in high-performance systems due to a combination of inherent process nonidealities and aggressive low-power design styles. An example of the latter is voltage scaling in general, and voltage overscaling (VOS) [54], in particular. VOS reduces the voltage beyond the minimum (referred to as $V_{dd-crit}$) necessary for correct operation. This results in soft output errors if critical paths and other longer paths are excited. The proposed AEC technique is derived from the observation that these soft errors exhibit a complicated dependence on the input signal and the underlying datapath architecture. Hence, by modeling the soft errors as a stochastic signal and exploiting its correlation with the input signal, one can devise a low-complexity error-cancellation scheme that is akin to echo cancellation employed in voiceband modems.

In order to optimize energy-efficiency, we develop an energy-optimum AEC [56], [57] to mitigate the degradation in algorithmic performance while consuming minimal energy. It is shown that the energy-optimum AEC is well-suited for broadband signal processing. We extend the proposed AEC to adaptive multi-input, multi-output (MIMO) signal processing, which is commonly employed in many modern-day communication systems such as crosstalk suppression in Gigabit Ethernet 1000Base-T transceivers, multiuser detection and multiantenna systems in
wireless applications. Power dissipation is a critical concern for these systems. The proposed MIMO-AEC [58], [59] exploits the inherent correlations in MIMO systems via MIMO decorrelating (MIMO-DECOR) to improve the energy-efficiency of AEC. Simulation results in the design of a low-power Gigabit Ethernet 1000Base-T device demonstrate 25.2% - 44.3% overhead reduction due to MIMO-DECOR and 64.2% - 69.1% energy savings over conventional implementations at the same algorithmic performance.

In Section 5.1, we study the performance degradation due to VOS for commonly employed DSP architectures. In Section 5.2, we propose the AEC as a new ANT technique suitable for the design of low-power broadband DSP and communication systems. An energy-optimum AEC is derived in Section 5.3 and extended to adaptive signal processing and MIMO signal processing in Sections 5.4 and 5.5, respectively. Simulation results for a Gigabit Ethernet 1000Base-T device are provided in Section 5.6.

5.1 Algorithmic Noise-Tolerance (ANT)

In this section, we present VOS and ANT and describe their use in the design of low-power signal processing systems.

5.1.1 Voltage overscaling (VOS)

Dedicated DSP implementations are designed subject to an application-specific throughput requirement. Specifically, for correct operation, the critical path delay $T_{cp}$ of the DSP architecture should be less than or equal to the sample period $T_s$ of the application, i.e.,

$$T_{cp} \leq T_s.$$  \hspace{1cm} (5.1)
Figure 5.1 Delay of datapath architectures: (a) general architecture and (b) a simple example of a four-tap filter.

The critical path delay $T_{cp}$ is a function of supply voltage. As voltage is scaled down, power dissipation reduces quadratically (assuming that dynamic power is the dominant source) while the delay (including the critical path delay $T_{cp}$) increases. At a certain point, Equation (5.1) is violated and soft errors start to appear at the output. The supply voltage at which $T_{cp} = T_d$ is referred to as the critical supply voltage and is denoted as $V_{dd-crit}$. Present-day voltage scaling stops at the point where $V_{dd} = V_{dd-crit}$. Overscaling supply voltage beyond $V_{dd-crit}$ results in output errors if critical paths and other longer paths are excited by certain input patterns, i.e., soft errors occur. This induces algorithmic performance degradation such as a loss in the output SNR.

For the purpose of illustration, consider a commonly employed FIR filter architecture as shown in Fig. 5.1(a), where we employ an adder tree (see Fig. 5.1(b)) to improve the throughput. Adder trees also help in reducing unnecessary power dissipation due to spurious transitions (glitches) because of their delay-balanced structure. The critical path delay $T_{cp,V_{dd}}$ of an $N$-tap filter at a supply voltage $V_{dd}$ can be expressed as

$$T_{cp,V_{dd}} = T_{m,V_{dd}} + (2\log_2 N)T_{a,V_{dd}}, \quad (5.2)$$

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where $T_{m,V_{dd}}$ and $T_{a,V_{dd}}$ are the propagation delays at $V_{dd}$ for a two-operand multiplier and a one-bit full adder, respectively. Note that in (5.2) the term $2\log_2 N$ (instead of $\log_2 N$) is due to sign extension which requires one more full-adder delay $T_{a,V_{dd}}$ to compute. Assuming a carry-save array multiplier architecture, we obtain the propagation delay $T_{m,V_{dd}}$ as

$$T_{m,V_{dd}} = (B_x + B_c)T_{a,V_{dd}}, \quad (5.3)$$

where $B_x$ and $B_c$ are the precisions of the filter input and coefficients, respectively. Substituting for $T_{m,V_{dd}}$ from (5.3) into (5.2), we obtain

$$T_{cp,V_{dd}} = (B_x + B_c + 2\log_2 N)T_{a,V_{dd}}. \quad (5.4)$$

We note that $T_{cp,V_{dd}}$ is a function of algorithmic ($B_x, B_c, N$), architectural (array multipliers, tree adders), as well as the underlying circuit ($V_{dd}, T_{a,V_{dd}}$) parameters. Figure 5.1(b) depicts the worst-case delay (in terms of the number of $T_{a,V_{dd}}$'s) of a four-tap filter with $B_x = 8$ bits and $B_c = 10$ bits. From (5.4), the throughput of this filter under conventional voltage scaling is given by

$$T_s = T_{cp,V_{dd-crit}} = 22T_{a,V_{dd-crit}}. \quad (5.5)$$

Now, assume that the supply voltage is overscaled to a value $V_{dd-sub} < V_{dd-crit}$ such that $T_{a,V_{dd-sub}} = 1.3T_{a,V_{dd-crit}}$, i.e., VOS is applied. With the same data rate (throughput), we see that

$$T_s = 22T_{a,V_{dd-crit}} = 16T_{a,V_{dd-sub}}, \quad (5.6)$$

but

$$T_{cp,V_{dd-sub}} = 22T_{a,V_{dd-sub}}. \quad (5.7)$$
This indicates that, while the filter still functions correctly at the lower LSBs, the top six MSBs of the output will be in error provided input patterns exciting the critical paths and other longer paths are applied. Hence, the filter output under VOS can be written as

\[ y_{\text{vos}}[n] = y[n] + e_s[n] = s[n] + \eta[n] + e_s[n], \]  
(5.8)

where \( y[n] \) is the error-free output composed of a desired signal \( s[n] \) and signal noise \( \eta[n] \), and \( e_s[n] \) denotes the soft error due to VOS. Note that \( e_s[n] \) can be viewed as hardware noise. While the relationship between \( e_s[n] \) and the input is deterministic, it is extremely complex for any reasonable-sized filters. Hence, we choose to model this relationship in a statistical manner by quantifying the degradation in the output SNR as

\[ \text{SNR} = 10 \log_{10} \left( \frac{\sigma_s^2}{\sigma_n^2 + \sigma_{es}^2} \right) < 10 \log_{10} \left( \frac{\sigma_s^2}{\sigma_n^2} \right), \]  
(5.9)

where \( \sigma_s^2, \sigma_n^2, \) and \( \sigma_{es}^2 \) are the variances of the desired signal \( s[n] \), signal noise \( \eta[n] \), and soft error \( e_s[n] \), respectively.

Note that most arithmetic modules employed in practice use LSB-first computation. This makes soft errors appear at the MSBs first, thereby creating errors of large magnitude. Hence, error detection is easy but error correction is difficult to achieve. This opens up a unique opportunity for ANT as described in this chapter.

From (5.8), the error-free output \( y[n] \) of an \( N \)-tap filter \( H(z) \) is given by

\[ y[n] = \sum_{j=0}^{N-1} h_j x[n - j], \]  
(5.10)
where $h_j$ is the $j^{th}$-tap coefficient and $x[n]$ is the input. If soft-error components due to different filter taps are statistically independent (which would be the case if the input is an uncorrelated signal), then we can express the soft-error energy $\sigma_{es}^2$ in (5.9) as

$$\sigma_{es}^2 = \sum_{j=0}^{N-1} \sigma_{h_j}^2,$$

where $\sigma_{h_j}^2$ is the variance of the input-dependent soft-error component from the $j^{th}$ tap with coefficient $h_j$.

Employing a logic-level simulation (see Section 5.6 for details of simulation setup) for the architecture in Fig. 5.1(b), we show in Fig. 5.2 a plot of $\sigma_{h_j}^2$ with respect to $h_j$ for the VOS scheme given by (5.6), where the input $x[n]$ is uniformly distributed in the range of $[-128, 127]$. The upper bound in Fig. 5.2 is given by

$$\sigma_{h_j}^2 = \begin{cases} 
49.49 \left( \frac{|h_j|}{h_{j,\text{max}}} \right)^5 - 155.04 \left( \frac{h_j}{h_{j,\text{max}}} \right)^4 \\
+ 186.69 \left( \frac{|h_j|}{h_{j,\text{max}}} \right)^3 - 105.03 \left( \frac{h_j}{h_{j,\text{max}}} \right)^2 \\
+ 27.57 \left( \frac{|h_j|}{h_{j,\text{max}}} \right)^2 - 2.69 |\sigma_{h_j,\text{max}}|^2 & \text{if } h_{\text{ef,max}} < |h_j| \leq h_{j,\text{max}}, \\
0 & \text{else},
\end{cases}$$

where $h_{j,\text{max}}$ and $h_{\text{ef,max}}$ denote the maximum coefficient and maximum error-free coefficient, respectively. For this example, $h_{j,\text{max}} = 511$ and $h_{\text{ef,max}} = 127$.

Figure 5.2 indicates that filter taps having coefficients with large magnitude can easily excite the critical paths and other longer paths, thereby contributing more to the performance degradation. This implies that as the filter bandwidth increases, the predominant contribution to the soft-error energy at the output will be from fewer taps due to the narrower impulse
Figure 5.2 Distribution of the soft-error energy with respect to the coefficient for a tap designed with an array multiplier and a ripple-carry adder.

response. Hence, we can simplify (5.11) as

$$\sigma_{es}^2 \approx \sum_{i=0}^{N_c-1} \sigma_{h_{k_i}}^2,$$

(5.13)

where $\sigma_{h_{k_i}}^2$ is the soft-error energy from the $k_i^{th}$ tap with coefficient $h_{k_i}$, and $N_c \leq N$. In Section 5.3, we will develop a low-complexity error-cancellation technique by determining the energy-optimum values of $k_i$'s and $N_c$.

5.1.2 Energy-efficiency via ANT

The key idea of ANT is to employ a low-complexity error-control block that detects and corrects errors that may arise in a comparatively large VOS block (see Fig. 1.2, page 8). An effective ANT technique is one that is low-complexity (compared to the VOS block) and is able to mitigate the performance degradation due to soft errors. These techniques may observe the input, output, and certain intermediate signals of the VOS block to generate an output $\hat{y}_o[n] \approx y[n]$, where $y[n]$ is the error-free output of the VOS block.
It is easy to derive the condition under which soft DSP leads to energy savings over conventional voltage-scaled systems. The dynamic energy dissipation per clock cycle $\mathcal{E}_{\text{orig}}$ of such a system is given by

$$\mathcal{E}_{\text{orig}} = C_{\text{orig}} V_{\text{dd-crit}}^2,$$

(5.14)

where $C_{\text{orig}}$ is the average switching capacitance that accounts for signal transition activities, voltage swing ranges, load and parasitic capacitances at all of the circuit nodes. It can be regarded as a measure of the hardware complexity of the underlying architecture. Note that $\mathcal{E}_{\text{orig}}$ is the minimum energy dissipation that conventional voltage scaling schemes can achieve.

In comparison, the dynamic energy dissipation per clock cycle $\mathcal{E}_{\text{soft}}$ of the corresponding soft DSP system is given by

$$\mathcal{E}_{\text{soft}} = C_{\text{orig}} (k_{\text{vos}} V_{\text{dd-crit}})^2 + C_{\text{ANT}} V_{\text{dd-ant}}^2,$$

(5.15)

where $C_{\text{ANT}}$ represents the overhead complexity due to ANT, $V_{\text{dd-ant}}$ is the critical supply voltage for the ANT-based error-control block, and $k_{\text{vos}} < 1$ is the VOS factor (VOSF). From (5.14)–(5.15), it can be shown that $\mathcal{E}_{\text{soft}} < \mathcal{E}_{\text{orig}}$ provided

$$C_{\text{ANT}} V_{\text{dd-ant}}^2 < C_{\text{orig}} V_{\text{dd-crit}}^2 (1 - k_{\text{vos}}^2).$$

(5.16)

In practice, the condition in (5.16) can be satisfied by making $C_{\text{ANT}}$ and $k_{\text{vos}}$ as small as possible. There is indeed an interesting direct relationship between $k_{\text{vos}}$ and $C_{\text{ANT}}$. When $k_{\text{vos}}$ is reduced, the performance degradation becomes larger as more critical paths and other longer paths start to fail. This requires increasingly complex ANT techniques which may increase $C_{\text{ANT}}$. 

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5.2 Adaptive Error-Cancellation (AEC)

In this section, we will develop an ANT technique referred to as adaptive error-cancellation (AEC) that exploits the cross-correlation between the input signal and the soft-error signal for error-control. As soft errors are input-dependent, they can be regarded as an echo of the input signal and hence echo cancellation algorithms used in communication systems can be employed to effectively restore the system performance. The proposed AEC technique belongs to this broad category.

5.2.1 The AEC algorithm

Figure 5.3 illustrates the proposed AEC technique. In the presence of soft errors due to VOS, the output $y_{voc}[n]$ of an $N$-tap VOS filter $H(z)$ can be expressed as

$$y_{voc}[n] = \sum_{j=0}^{N-1} h_j x[n - j] + e_s[n]$$

$$= y[n] + e_s[n], \quad (5.17)$$
where \( y[n] \) is the error-free output, \( e_s[n] \) is the soft output error, \( h_j \) is the \( j^{th} \)-tap coefficient, and \( x[n - j] \) is the \( j^{th} \) delayed input sample.

For a given implementation of \( H(z) \), the soft error \( e_s[n] \) depends upon the input samples \( x[n], x[n-1], \ldots, x[n-N+1] \). Thus, an error canceler \( H_c(z) \) can be employed to generate a statistical replica of the soft errors from these input samples and then subtract it from the output. The resulting estimate of \( e_s[n] \), denoted by \( \widehat{e}_s[n] \), is given by

\[
\widehat{e}_s[n] = \sum_{j=0}^{N-1} w_j x[n-j],
\]

(5.18)

where \( w = \{w_0, w_1, \ldots, w_{N-1}\} \) is the coefficient vector of the error canceler \( H_c(z) \). It can be chosen to minimize the estimation error \( e[n] \), defined as

\[
e[n] = e_s[n] - \widehat{e}_s[n].
\]

(5.19)

Here we use the commonly employed minimum mean-squared error (MMSE) criterion that minimizes

\[
\sigma_e^2 = E(e[n]^2).
\]

(5.20)

While the value of \( w \) that minimizes (5.20) can be obtained as a solution of the Weiner-Hopf equation \cite{88}, in practice the cross-correlation between the input signal and the soft-error signal can vary due to process and temperature variations. In addition, the input signal may itself be nonstationary, thereby necessitating the use of an adaptive algorithm such as the least mean

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square (LMS) algorithm given by [88]

\[
\hat{e}_s[n] = \sum_{j=0}^{N-1} h_{c,j}[n-1]x[n-j],
\]

\[e[n] = e_s[n] - \hat{e}_s[n],\]  \hspace{1cm} (5.22)

\[h_{c,j}[n] = h_{c,j}[n-1] + \mu e[n]^*x[n-j],\]  \hspace{1cm} (5.23)

where \(h_c = \{h_{c,0}[n], h_{c,1}[n], \cdots, h_{c,N-1}[n]\}\) is an estimate of the optimum tap-weight vector of \(H_c(z)\), \(e[n]^*\) is the complex conjugate of \(e[n]\), and \(\mu\) is the step size. The computations in (5.21) are done in the filter (F) block of the AEC and those in (5.23) are executed in the weight-update (WUD) block.

A practical approach to implement the AEC algorithm described above is to have an auto-calibration phase during power-up. During this phase, a predefined input signal is passed through the VOS filter \(H(z)\) and a precomputed error-free output \(y[n]\) is used as the desired signal (see the multiplexer in Fig. 5.3). After the tap-weight vector \(h_c\) has converged, the WUD-block can be powered-down and the multiplexer control signal can be flipped so that \(\hat{e}_s[n]\) gets subtracted directly from the output \(y_{vos}[n]\) thereby canceling out the soft errors.

### 5.2.2 Algorithmic performance measures

We now define the algorithmic performance measures needed for characterizing the effectiveness of the proposed AEC technique.

Definition 1: The output SNR of a conventional filter under VOS is defined as \(SNR_{VOS}\), which is given by

\[
SNR_{VOS} = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_n^2 + \sigma_{es}^2}\right),
\]

\[(5.24)\]
where $\sigma_s^2$, $\sigma_n^2$, and $\sigma_{es}^2$ are the variances of the desired signal $s[n]$, signal noise $\eta[n]$, and soft error $e_s[n]$, respectively.

*Definition 2:* The output SNR of a soft filter employing the AEC for ANT is defined as $SNR_{ANT}$, which is given by

$$SNR_{ANT} = 10 \log_{10} \left( \frac{\sigma_s^2}{\sigma_n^2 + \sigma_{es}^2} \right),$$

(5.25)

where $\sigma_{es}^2$ is the variance of the residual soft error $e[n]$ (or estimation error, see (5.22)) after the AEC.

In practice, AEC-based soft filters are designed for an application-specific performance requirement $SNR_{design}$, such that

$$SNR_{ANT} \geq SNR_{design} = 10 \log_{10} \left( \frac{\sigma_s^2}{\sigma_{n,design}^2} \right),$$

(5.26)

where $\sigma_{n,design}^2$ denotes the variance of the worst-case signal noise $\eta[n]$ at the filter output.

The error canceler $H_c(z)$ in Fig. 5.3 is an adaptive filter that takes the soft error $e_s[n]$ as the desired signal and generates the estimated signal $\hat{e}_s[n]$ as its output. Thus, the estimation error $e[n]$ between $e_s[n]$ and $\hat{e}_s[n]$ is seen as the output noise. This leads to the following definition of SNR for the error canceler $H_c(z)$.

*Definition 3:* The output SNR of the error canceler $H_c(z)$ is given by

$$SNR_{AEC} = 10 \log_{10} \left( \frac{\sigma_{es}^2}{\sigma_{e}^2} \right).$$

(5.27)

The AEC algorithm given in (5.21)–(5.23) must achieve the algorithmic performance as specified in (5.26) for a given $SNR_{design}$. Parameters that determine the $SNR_{ANT}$ include the frequency response of $H(z)$, VOSF, length $N_c$ of the error canceler $H_c(z)$, precision $B_F$ of
the F-block, and precision $B_{WUD}$ of the WUD-block. The energy-optimum choices of these
parameters will be discussed in Section 5.3.

5.2.3 Energy-savings measures

The average energy savings $\varepsilon_{sav}$ achieved by an AEC-based soft DSP system is defined as

$$\varepsilon_{sav} = \left(1 - \frac{\varepsilon_{soft}}{\varepsilon_{conv}}\right) \times 100\%,$$

(5.28)

where $\varepsilon_{conv}$ is the energy dissipation of the conventional filter at the optimally scaled voltage of
$V_{dd-crit}$ and $\varepsilon_{soft}$ is the energy dissipation of the soft filter at the overscaled voltage of $V_{dd-sub}$.

It can be seen from Fig. 5.3 that $\varepsilon_{soft}$ is given by

$$\varepsilon_{soft} = \varepsilon_H + \varepsilon_{AEC},$$

(5.29)

where $\varepsilon_H$ and $\varepsilon_{AEC}$ are the energy dissipations of the primary filter $H(z)$ and the error canceler
$H_c(z)$, respectively. Note that $\varepsilon_H$ and $\varepsilon_{AEC}$ are not independent of each other because $\varepsilon_H$ can
be reduced by decreasing VOSF. Doing so will induce a larger performance degradation which
would necessitate a more complex AEC and hence a higher $\varepsilon_{AEC}$. Thus, there is a need for
developing a systematic design method that minimizes the energy dissipation $\varepsilon_{soft}$. This can
be formulated as an energy optimization problem subject to a performance constraint, which is

**minimize:** $\varepsilon_{soft},$

**subject to:** $SNR_{ANT} \geq SNR_{design}.$

(5.30)

In the next section, we will derive the energy-optimum AEC based on the solution of (5.30).
5.3 Energy-Optimum Error-Cancellation Algorithm

One can decompose the problem in (5.30) into three interdependent subproblems: Determine (1) the optimum choice for the primary filter $H(z)$, (2) the optimum value of VOSF, and (3) the parameters of the optimum AEC for a given $H(z)$ and VOSF. In this section, we show that while it is difficult to obtain a closed-form solution to the first two subproblems, one can employ numerical methods as described in Section 5.3.1. The third subproblem is tractable and an analytical solution is presented in Section 5.3.2. In Section 5.3.3, we propose a reduced-order LMS algorithm for the energy-optimum AEC, along with its finite precision requirements.

5.3.1 Energy-optimum solutions for $H(z)$ and VOSF

The answer to the first subproblem determines an optimum ratio of $\sigma_n^2$ and $\sigma_e^2$ (see (5.25)), as a larger $\sigma_n^2$ relaxes the design of $H(z)$ (smaller $\mathcal{E}_H$) but requires a more complex AEC (larger $\mathcal{E}_{AEC}$). Similarly, for the second subproblem, a smaller VOSF leads to more energy savings in $H(z)$ (smaller $\mathcal{E}_H$) but also induces a larger performance degradation (larger $\sigma_{es}^2$) and thus requires a more complex AEC (larger $\mathcal{E}_{AEC}$). In general, these two subproblems involve a set of nonlinear equations describing the relationship between the algorithmic performance and the corresponding energy dissipation. For example, most filter design techniques use iterative algorithms to compute the coefficients $h_j$'s of $H(z)$ (which determine the $\mathcal{E}_H$) for a given set of frequency domain specifications (bandwidth, transition band, etc., which determine the $\sigma_n^2$).

Also, soft-error energy $\sigma_{es}^2$ as a function of VOSF can be expressed numerically via a logic-level simulation. In addition, these nonlinear equations also depend on the datapath architectures being employed. Therefore, numerical methods are practical for the first two subproblems.

However, it can be shown that the optimum solution to (5.30) is obtained at the point where (i) $H(z)$ has the minimal complexity (corresponding to the smallest $\mathcal{E}_H$ and in general the largest
possible \( \sigma_n^2 \) and (ii) VOSF achieves the smallest value that makes \( \text{SNR}_{\text{ANT}} = \text{SNR}_{\text{design}} \). To show (i), we note that for a given filter bandwidth (which is determined by the signal bandwidth), a reduction in transition band (and hence a "tighter" \( H(z) \)) results in a linear increase in the filter length \( N \) and hence in the energy dissipation \( \mathcal{E}_H \) but a sublinear reduction in \( \sigma_n^2 \) (as \( \sigma_n^2 \) is largely due to the in-band noise). This leads to a small reduction in \( \mathcal{E}_{\text{AEC}} \). As will be shown in Section 5.3.3, \( \mathcal{E}_H \) is normally larger than the energy-optimum \( \mathcal{E}_{\text{AEC}} \). Therefore, the increased energy in \( \mathcal{E}_H \) can easily override the energy reduction in \( \mathcal{E}_{\text{AEC}} \). As a result, \( \mathcal{E}_H \) needs to be minimized to achieve the overall energy optimization.

To show (ii), we note that a smaller VOSF leads to a quadratic reduction in \( \mathcal{E}_H \) but a linear increase in \( \mathcal{E}_{\text{AEC}} \) (due to the increased \( \sigma_{\text{err}}^2 \) requiring a more complex AEC). As mentioned above, \( \mathcal{E}_H \) is larger than the energy-optimum \( \mathcal{E}_{\text{AEC}} \), thus a smaller VOSF enables a net reduction in the overall energy.

In summary, \( \mathcal{E}_{\text{soft}} \) is minimized when \( \mathcal{E}_H \) and VOSF are minimized. In the next section, we will derive an energy-optimum AEC for any given \( H(z) \) and VOSF, i.e., the solution of the third subproblem.

### 5.3.2 Energy-optimum AEC

The reason for the existence of energy-optimum AEC is that performance degradation due to VOS is dominated by soft errors from a few of the taps of \( H(z) \) having large coefficient magnitude. Thus, a reduced-order AEC exists that can restore the algorithmic performance.

We define a vector \( \mathbf{b} = \{b_0, b_1, \ldots, b_{N-1}\} \in \mathcal{B}^N \), where \( N \) is the order of a given filter \( H(z) \) and \( \mathcal{B}^N \) is an \( N \)-dimension vector space with binary elements \( b_j \)'s \( \in \{0, 1\} \). We denote \( b_j = 1 \) if the \( j^{th} \) tap of the error canceler \( H_c(z) \) is powered up and \( b_j = 0 \) otherwise. The length \( N_c \) of \( H_c(z) \) can be written as

\[
N_c = \sum_{j=0}^{N-1} b_j.
\]  

(5.31)
Assume that the input signal \( x[n] \) is a zero-mean and uncorrelated random signal. The variance of residual soft error \( e[n] \) after cancellation by the AEC can be expressed as [88]

\[
\sigma_e^2 = \sigma_{es}^2 - \sum_{j=0}^{N-1} b_jw_j^2 \sigma_x^2,
\]

where \( \sigma_x^2 \) and \( \sigma_{es}^2 \) are the variances of the input signal \( x[n] \) and soft output error \( e_s[n] \), respectively, for the given \( H(z) \) and VOSF, and \( w_j \)'s are the optimum coefficients of \( H_c(z) \), given by [88]

\[
w_j = \frac{E(x[n-j]e_s[n])}{\sigma_x^2}.
\]

Note that from (5.25)–(5.26), \( \sigma_e^2 \) in (5.32) due to the \( N_c \)-tap \( H_c(z) \) needs to satisfy the following constraint

\[
\sigma_e^2 \leq \sigma_{n,design}^2 - \sigma_n^2,
\]

where \( \sigma_n^2 \) is determined by the given \( H(z) \).

To quantify the energy overhead \( E_{AEC} \), we assume that the WUD-block is switched off after \( H_c(z) \) has converged. This implies

\[
E_{AEC}(b) = \sum_{j=0}^{N-1} b_j E_{Fj},
\]

where \( E_{Fj} \) is the energy dissipation due to the \( j^{th} \) tap of \( H_c(z) \). Given the coefficient \( w_j \), the value of \( E_{Fj} \) can be estimated via the weighted multiplier energy model [89].
Using the above notations, the energy optimization problem (5.30) for AEC can be expressed as an explicit function of the vector \( \mathbf{b} \), as follows:

\[
\begin{align*}
\text{minimize:} & \quad \mathcal{E}_{\text{AEC}}(\mathbf{b}), \\
\text{subject to:} & \quad \sigma_{\epsilon}^2 \leq \sigma_{n,\text{design}}^2 - \sigma_n^2, \tag{5.36}
\end{align*}
\]

where \( \mathcal{E}_{\text{AEC}}(\mathbf{b}), \sigma_{\epsilon}^2, \sigma_n^2, \) and \( \sigma_{n,\text{design}}^2 \) are given by (5.35), (5.32), (5.25), and (5.26), respectively.

The optimization problem (5.36) can be solved via the Lagrange multiplier method [85]. We define the Lagrangian function \( L(\mathbf{b}, \lambda) \) as

\[
L(\mathbf{b}, \lambda) = \mathcal{E}_{\text{AEC}}(\mathbf{b}) + \lambda(\sigma_{\epsilon}^2 + \sigma_n^2 - \sigma_{n,\text{design}}^2) = \sum_{j=0}^{N-1} b_j(\mathcal{E}_{F,j} - \lambda w_j^2 \sigma_{\epsilon}^2) + \lambda(\sigma_{\epsilon}^2 + \sigma_n^2 - \sigma_{n,\text{design}}^2), \tag{5.37}
\]

where \( \lambda \) is the sensitivity vector of the Lagrange multiplier. The solution to (5.36) is obtained at the point \((\mathbf{b}^*, \lambda^*)\) satisfying

\[
L(\mathbf{b}^*, \lambda) \leq L(\mathbf{b}^*, \lambda^*) \leq L(\mathbf{b}, \lambda^*), \tag{5.38}
\]

for any \( \mathbf{b} \in B^N \) and \( \lambda \geq 0 \). It can be shown [89] that \( \mathbf{b}^* = \{b_0^*, b_1^*, \ldots, b_{N-1}^*\} \in B^N \) is given by

\[
b_j^* = \begin{cases} 
1 & \text{if } \frac{\mathcal{E}_{F,j}}{w_j^2 \sigma_{\epsilon}^2} < \lambda^*, \\
0 & \text{if } \frac{\mathcal{E}_{F,j}}{w_j^2 \sigma_{\epsilon}^2} \geq \lambda^*,
\end{cases} \tag{5.39}
\]
where \( \lambda^* \) is the optimum value of \( \lambda \). The energy-optimum length \( N_c^{\text{opt}} \) of the error canceler \( H_c(z) \) is obtained as

\[
N_c^{\text{opt}} = \sum_{j=0}^{N-1} b_j^*.
\]  
(5.40)

From (5.39), if the \( j^{\text{th}} \) tap of \( H_c(z) \) has a large coefficient \( w_j \) while consuming a relatively small energy \( \mathcal{E}_{F,j} \), then \( b_j^* = 1 \). In other words, the input \( x[n - j] \) has to be utilized to cancel the soft output errors. On the other hand, we can switch off the \( j^{\text{th}} \) tap of \( H_c(z) \) if this tap consumes large energy \( \mathcal{E}_{F,j} \) but has a minor contribution in terms of error cancellation (small \( w_j \)). In practice, we can avoid the computation of \( \lambda^* \) by powering down those taps in \( H_c(z) \) starting with the tap with the largest value of \( \frac{\mathcal{E}_{F,j}}{w_j + \sigma^2} \) and continuing until the performance constraint in (5.36) is violated.

We now describe the relationship between the performance degradation due to VOS and the configuration of energy-optimum AEC. Denote \( e_{s,j}[n] \) as the soft-error component from the \( j^{\text{th}} \) tap of \( H(z) \). As \( e_{s,j}[n] \) is excited by the input \( x[n - j] \), it is reasonable to assume that \( e_{s,j}[n] \) is statistically independent of \( e_{s,i}[n] \) and \( x[n - i] \) for \( i \neq j \). Thus, we can rewrite (5.33) as

\[
w_j = \frac{E \left( x[n - j] \left( \sum_{i=0}^{N-1} e_{s,i}[n] \right) \right)}{\sigma_x^2} = \frac{E (x[n - j] e_{s,j}[n])}{\sigma_x^2}.
\]  
(5.41)

In general, if the \( j^{\text{th}} \) tap of \( H(z) \) has a large coefficient \( h_j \), then the critical paths and other longer paths get excited easily, thereby resulting in a larger value for \( e_{s,j}[n] \) and for \( E (x[n - j] e_{s,j}[n]) \). From (5.41), this implies that \( w_j \) is large, which in turn implies (from (5.39)) \( b_j^* = 1 \). This is to be expected as \( e_{s,j}[n] \) is induced by \( x[n - j] \) and thus can only be canceled by the \( j^{\text{th}} \) tap of \( H_c(z) \). As the filter bandwidth increases, the predominant contribution to the soft-error energy at the output will be from fewer taps of \( H(z) \). This is because wideband
filters have a narrow impulse response. Thus, more \( b_j^* \)'s will be zero resulting in a smaller \( N_c^{\text{opt}} \). This indicates that the proposed AEC technique is best suited for wideband signal processing.

### 5.3.3 Reduced-order AEC algorithm

Employing the energy-optimum AEC derived above, we propose a reduced-order LMS algorithm to compute the AEC coefficients, as shown below:

\[
\hat{e}_s[n] = \sum_{i=0}^{N_c^{\text{opt}}-1} h_{c,k_i}[n-1]x[n-k_i],
\]

\[
e[n] = y_{\text{cas}}[n] - y[n] - \hat{e}_s[n],
\]

\[
h_{c,k_i}[n] = h_{c,k_i}[n-1] + \mu e[n]^*x[n-k_i],
\]

where \( N_c^{\text{opt}} \) is given by (5.40) and \( k_i = j \) if \( b_j^* = 1 \) in (5.39).

The precisions of F-block and WUD-block in the energy-optimum AEC can be determined as follows. Assuming a uniform stochastic model for the quantization errors in the coefficients \( h_{c,k_i} \)'s, the mean-squared quantization noise \( J_Q \) at the output of \( H_c(z) \) is given by [90]

\[
J_Q = \frac{N_c^{\text{opt}} \sigma_x^2 A^2 q_{2-2(B_F-1)}}{12},
\]

where \( \sigma_x^2 \) is the variance of the input signal \( x[n] \), \( A \) is the maximum magnitude of \( h_{c,k_i} \)'s, and \( B_F \) denotes the precision of \( h_{c,k_i} \)'s in the F-block.

To make quantization errors arbitrarily small, we define a factor \( \alpha < 1 \) such that \( J_Q \leq \alpha \sigma_x^2 \), where \( \sigma_x^2 \) is given by (5.32). The precision \( B_F \) is then obtained as [91]

\[
B_F \geq \frac{1}{2} \log_2 \left( \frac{N_c^{\text{opt}} A^2 \sigma_x^2}{3 \alpha \sigma_x^2} \right).
\]
From (5.46), a smaller $N_e^{opt}$ also reduces the precision of F-block, thereby favoring energy reduction.

We employ the stopping criterion [92] to determine the precision of WUD-block. The stopping criterion asserts that the WUD-block will stop adapting if the correction term $(\mu e[n]x[n-k])$ in (5.44) becomes smaller than half of the least significant bit of $h_{c,k_i}$'s. This can be expressed as

$$\mu^2 \sigma_e^2 \sigma_x^2 \geq A^2 2^{-2B_{WUD}}, \tag{5.47}$$

where $B_{WUD}$ is the precision of $h_{c,k_i}$'s in the WUD-block. From (5.47), the lower bound on $B_{WUD}$ is given by

$$B_{WUD} \geq \frac{1}{2} \log_2 \left( \frac{A^2}{\mu^2 \sigma_e^2 \sigma_x^2} \right). \tag{5.48}$$

Figure 5.4 shows the architecture of the proposed reduced-order AEC. Simulation results in Section 5.6 demonstrate significant reduction in hardware complexity as compared with the conventional LMS algorithm. Thus, we are able to satisfy the constraint (5.16) easily.
Furthermore, even if the supply voltage of the reduced-order AEC is made identical to that of
the VOS $H(z)$ for simplicity of implementation, the reduced-order AEC is error-free because
its critical path is much shorter than that of the filter $H(z)$.

5.4 AEC-Based Adaptive Signal Processing

In this section, we propose to apply the energy-optimum AEC in the design of low-power
adaptive filters. We first develop an AEC-based adaptive filtering scheme in Section 5.4.1
and then present the performance analysis in Section 5.4.2. The proposed AEC-based adaptive
filtering scheme will be employed with MIMO-AEC for the design of low-power Gigabit Ethernet
systems in Section 5.6.

5.4.1 AEC-based adaptive filter

Figure 5.5 shows the proposed AEC-based adaptive filtering scheme. Here both the primary
adaptive filter, denoted by $H_a(z)$, and the error canceler $H_c(z)$ need to compute their coefficients
adaptively. We assume that (1) the primary adaptive filter $H_a(z)$ and the error canceler $H_c(z)$
are calibrated separately and (2) the WUD-block is powered-down during the steady-state
filtering operation. Hence, a common weight-update (CWUD) block can be shared by both
filters in order to reduce the hardware overhead of AEC. Note that the two-phase calibration of
$H_a(z)$ and $H_c(z)$ is necessary because otherwise the estimation errors due to $H_a(z)$ and $H_c(z)$
become indistinguishable, thereby preventing the convergence of the two filters. In addition,
for a given input signal, soft errors are dependent upon the coefficients of $H_a(z)$. Updating
the coefficients of $H_a(z)$ changes the underlying soft-error model at every update cycle, thereby
making it impossible for $H_c(z)$ to track. For these reasons, the calibration of $H_c(z)$ needs to be
done after $H_a(z)$ has converged.
The operation of AEC-based adaptive filters consists of three phases, as described below with reference to Fig. 5.5:

1.) Filter Calibration Phase: During this phase, the supply voltage is set to $V_{dd-crit}$, control signals WUD.A and DS.IN are ON, WUD.C and SE.IN are OFF, and a predefined training sequence is fed into $H_a(z)$. Note that during this phase soft error $e_s[n]$ is always zero. Hence, the coefficients $h_{a,j}$'s of $H_a(z)$ get updated by the error signal $e_a[n]$ between the filter output $y_a[n]$ and a precomputed desired signal $y_d[n]$, as given below:

$$y_a[n] = \sum_{j=0}^{N-1} h_{a,j}[n-1]x[n-j],$$  

(5.49)

$$e_a[n] = y_d[n] - y_a[n],$$  

(5.50)

$$h_{a,j}[n] = h_{a,j}[n-1] + \mu_a e_a[n]^* x[n-j].$$  

(5.51)

2.) AEC Calibration Phase: During this phase, the supply voltage is overscaled to $V_{dd-sub}$, control signals WUD.C, SE.IN, and DS.IN are ON, while WUD.A is OFF. Due to VOS,
soft errors start to appear at the output of $H_a(x)$. The coefficients $h_{c,k_i}$s of the energy-optimum error canceler $H_c(x)$ are computed according to

$$
\bar{e}_s[n] = \sum_{i=0}^{N_{e_{opt}}-1} h_{c,k_i}[n-1]x[n-k_i],
$$

(5.52)

$$
e_c[n] = (e_s[n] + e_a[n]) - \bar{e}_s[n],
$$

(5.53)

$$
h_{c,k_i}[n] = h_{c,k_i}[n-1] + \mu_c e_c[n]^* x[n-k_i],
$$

(5.54)

where $N_{e_{opt}}$ is given by (5.40) and $k_i = j$ if $b_j^g = 1$ in (5.39). Note that the error signal in (5.53) contains residual error $e_a[n]$ from the first phase (see (5.50)). However, it will be shown later that $e_a[n]$ has a minor effect on the optimum configuration of $H_c(x)$ as described in (5.39)–(5.40).

3.) Soft Filtering Phase: After $H_c(x)$ has converged, the supply voltage is kept at $V_{dd-sub}$, control signal SE_IN is ON, while the others are OFF. The filter output $y_o[n]$ is computed as

$$
y_o[n] = y_a[n] + e_s[n] - \bar{e}_s[n],
$$

(5.55)

where $y_o[n]$ and $\bar{e}_s[n]$ are given by (5.49) and (5.52), respectively, and $e_s[n]$ is the soft error due to VOS. This starts the steady-state filtering operation where significant energy reduction is achieved via VOS while the required algorithmic performance is guaranteed by AEC.

5.4.2 Performance analysis

We now study the error-control performance of the proposed AEC-based adaptive filtering scheme. From (5.53), the error signal seen by $H_c(x)$ in the AEC calibration phase is composed of soft error $e_s[n]$ and the residual estimation error $e_a[n]$ from $H_a(x)$. However, it can be proved that the optimum Weiner-Hopf solutions for $H_c(x)$ and $H_a(x)$ are independent of each other.
To show this, we assume that the input $x[n]$ is a zero-mean and uncorrelated random signal. In the filter calibration phase, we obtain the optimum coefficients $h_{a,j}^{\text{opt}}$'s of $H_a(z)$ as [88]

$$h_{a,j}^{\text{opt}} = \frac{E(x[n-j]y_d[n])}{\sigma_x^2}, \quad (5.56)$$

where $\sigma_x^2$ is the variance of the input signal $x[n]$ and $y_d[n]$ is the desired signal for the adaptive filter $H_a(z)$. Substituting for $h_{a,j}^{\text{opt}}$ from (5.56) into (5.49) and (5.50), we obtain the residual estimation error $e_a^{\text{opt}}[n]$ as

$$e_a^{\text{opt}}[n] = y_d[n] - \sum_{j=0}^{N-1} h_{a,j}^{\text{opt}} x[n-j]. \quad (5.57)$$

In the AEC calibration phase, due to the presence of nonzero $e_a^{\text{opt}}[n]$, the optimum coefficients $h_{c,j}^{\text{opt}}$'s of the error canceler $H_c(z)$ can be expressed as

$$h_{c,j}^{\text{opt}} = \frac{E((e_s[n] + e_a^{\text{opt}}[n])x[n-j])}{\sigma_x^2} = \frac{E(e_s[n]x[n-j])}{\sigma_x^2} + \frac{E(e_a^{\text{opt}}[n]x[n-j])}{\sigma_x^2}, \quad (5.58)$$

where $e_s[n]$ denotes the soft output error from the converged VOS filter $H_a(z)$. Note that the residual estimation error $e_a^{\text{opt}}[n]$ in the Weiner-Hopf solution is statistically orthogonal to the input signal $x[n]$, i.e.,

$$E(e_a^{\text{opt}}[n]x[n-j]) = 0. \quad (5.59)$$

Hence, $h_{c,j}^{\text{opt}}$'s in (5.58) are an unbiased optimum solution even if a nonzero $e_a^{\text{opt}}[n]$ is present.

The LMS calibrations given by (5.49)–(5.51) and (5.52)–(5.54) result in filter coefficients that approach their Weiner-Hopf solutions. It can be shown that after $H_a(z)$ has converged,
the residual estimation error $e_a[n]$ can be expressed as

$$e_a[n] = e_a^{opt}[n] + \bar{e}_a[n],$$  
(5.60)

where $e_a^{opt}[n]$ is given by (5.57) and $\bar{e}_a[n]$ denotes the input-dependent excess error which is statistically small.

From (5.53) and (5.60), the error canceler $H_e(z)$ is in fact canceling $e_a[n] + \bar{e}_a[n]$, as $e_a^{opt}[n]$ is orthogonal to the input signal $z[n]$ and therefore cannot be canceled by $H_e(z)$. However, $\bar{e}_a[n]$ has a minor effect on the configuration of $H_e(z)$ because it is much smaller than $e_a[n]$.

Note that during the soft filtering phase, it is usually needed to monitor the time-varying input statistics and update $H_a(z)$ and $H_e(z)$ accordingly. In practical systems, this can be achieved by monitoring the output SNR or including a training sequence into actual data samples and updating the filters periodically. In either case, the AEC-based adaptive filter can be recalibrated according to the procedure given in Section 5.4.1.

Figure 5.6 shows the architecture of an AEC-based adaptive filter. Simulation results in Section 5.6 demonstrate that the tap-length $N_e^{opt}$ of the energy-optimum AEC is around $N/4$. Thus, the energy overhead incurred in AEC can be compensated for easily by the energy savings obtained from VOS. Also, the AEC block has a shorter critical path, thus being error-free during VOS.

### 5.5 MIMO-AEC for Low-Power MIMO Signal Processing

In this section, we extend the energy-optimum AEC to multi-input, multi-output (MIMO) signal processing. In particular, we develop an MIMO-AEC technique that exploits the inherent correlations in MIMO systems via MIMO decorrelating (MIMO-DECOR) transform to improve the energy-efficiency of AEC. As will be shown in Section 5.6, the proposed MIMO-
Figure 5.6 VLSI architecture of the energy-optimum AEC-based adaptive filter.

AEC technique achieves substantial energy savings in practical MIMO systems such as Gigabit Ethernet 1000Base-T transceivers. A matrix representation of MIMO systems is given in Section 5.5.1 and the MIMO-AEC is proposed in Section 5.5.2. In Section 5.5.3, we derive the MIMO-DECOR transform for practical MIMO systems.
5.5.1 MIMO model

Consider a generic $p$-input, $q$-output MIMO system composed of $p \times q$ adaptive or fixed-coefficient filters and expressed in matrix form as

\[
\begin{bmatrix}
  y_1[n] \\
  y_2[n] \\
  \vdots \\
  y_q[n]
\end{bmatrix} =
\begin{bmatrix}
  h_{11} & h_{12} & \cdots & h_{1p} \\
  h_{21} & h_{22} & \cdots & h_{2p} \\
  \vdots & \vdots & \ddots & \vdots \\
  h_{q1} & h_{q2} & \cdots & h_{qp}
\end{bmatrix} \otimes
\begin{bmatrix}
  x_1[n] \\
  x_2[n] \\
  \vdots \\
  x_p[n]
\end{bmatrix},
\]

where $x_j[n] = [x_j[n], x_j[n-1], \cdots, x_j[n-N+1]]^T$ is the $j^{th}$ input sequence; $h_{ij} = [h_{ij}[0], h_{ij}[1], \cdots, h_{ij}[N-1]]$ is the coefficient vector of the filter taking the $j^{th}$ input and generating the $i^{th}$ output; $y_i[n] = \sum_{j=1}^{p} h_{ij} \otimes x_j[n]$ is the $i^{th}$ output; and "\otimes" denotes the element-by-element convolution operation, i.e., $h_{ij} \otimes x_j[n] = \sum_{k=0}^{N-1} h_{ij}[k]x_j[n-k]$.

A special case of (5.61) is a system with a diagonal transfer matrix (i.e., $h_{ij} = 0$ for $i \neq j$) representing independent single-input, single-output (SISO) filtering operations, such as the channel equalizers in Gigabit Ethernet 1000Base-T transceivers (see Section 5.6).

Henceforth, we refer to the filter with coefficient vector $h_{ij}$ as filter $h_{ij}$. Note that in practical MIMO systems the filters in (5.61) usually exhibit certain correlations in frequency or time domain. For example, the interference suppression scheme in a 1000Base-T device (see Section 5.6) contains twelve NEXT cancelers, among which every three NEXT cancelers share the same input. These three NEXT cancelers have similar impulse responses, as they are designed to cancel three similar NEXT interferences which are induced by the same input signal on three spatially correlated crosstalk paths. Exploiting these inherent correlations allows us to develop effective energy reduction techniques as discussed below.
5.5.2 MIMO-AEC

We now present the MIMO-AEC technique for low-power MIMO signal processing. Assume that all the filters $h_{ij}$'s in (5.61) operate in parallel. Energy reduction via VOS induces soft errors at all the filter outputs $y_i[n]$'s. This necessitates a bank of error cancelers, for which the Weiner-Hopf solution [88] is given by

\[
\begin{bmatrix}
h_{c,11} & h_{c,12} & \cdots & h_{c,1p} \\
h_{c,21} & h_{c,22} & \cdots & h_{c,2p} \\
\vdots & \vdots & \ddots & \vdots \\
h_{c,q1} & h_{c,q2} & \cdots & h_{c,qp}
\end{bmatrix}
= E \left( \begin{bmatrix}
e_{s1[n]} \\
e_{s2[n]} \\
\vdots \\
e_{sq[n]}
\end{bmatrix}
\begin{bmatrix}
x_1[n] \\
x_2[n] \\
\vdots \\
x_p[n]
\end{bmatrix}^T \right)^{-1}
E \left( \begin{bmatrix}
x_1[n] \\
x_2[n] \\
\vdots \\
x_p[n]
\end{bmatrix}
\begin{bmatrix}
x_1[n] \\
x_2[n] \\
\vdots \\
x_p[n]
\end{bmatrix}^T \right),
\tag{5.62}
\]

where $h_{c,ij}$ is the coefficient vector of the error canceler for the filter $h_{ij}$ and $e_{si}[n]$ is the soft error at the $i^{th}$ output $y_i[n]$. From (5.61), $e_{si}[n]$ contains $p$ soft-error components, i.e.,

\[
e_{si}[n] = \sum_{j=1}^{p} e_{si,j}[n],
\tag{5.63}
\]

where $e_{si,j}[n]$ denotes the soft error induced by $x_j[n]$ in the VOS filtering operation $h_{ij} \otimes x_j[n]$.

Assume that the input sequences $x_j[n]$'s are zero-mean and from independent data sources. Thus, $e_{si,j}[n]$ in (5.63) is uncorrelated to $x_k[n]$ for $k \neq j$, i.e., $E(e_{si,j}[n]x_k[n]^T) = 0$. Accordingly, the solution of $h_{c,ij}$ in (5.62) can be expressed as

\[
h_{c,ij} = \frac{E(e_{si,j}[n]x_j[n]^T)}{\sigma_{x_j}^2},
\tag{5.64}
\]

where $\sigma_{x_j}^2$ is the variance of $x_j[n]$. Note that the result given by (5.64) is the same as that of a SISO filter. Hence, we can decouple the $p \times q$ error cancelers $h_{c,ij}$'s and implement each of them
Figure 5.7 The proposed MIMO-AEC technique: (a) direct-AEC and (b) MIMO-AEC with MIMO-DECOR.

independently via the energy-optimum AEC given in Section 5.3. We denote this approach as direct-AEC, as shown in Fig. 5.7(a).

While the energy-optimum AEC guarantees the minimum energy overhead for an individual error canceler, the direct-AEC scheme consisting of $p \times q$ independent error cancelers, one for each VOS filter in (5.61), may not be energy-efficient. This is due to the fact that the possible correlations among the original filters $h_{ij}$'s may introduce computational redundancies. In order to further improve energy-efficiency, we propose an algorithm transformation denoted as MIMO decorrelating (MIMO-DECOR). In contrast with the direct-AEC, the AEC technique employing MIMO-DECOR for energy optimization is referred to as MIMO-AEC.
5.5.3 MIMO-DECOR

Decorrelating (DECOR) transform [93] was studied previously for narrowband SISO filters. It employs the fact that the difference between the adjacent coefficients of a filter is typically of smaller magnitude, thereby requiring less hardware complexity and power dissipation in the implementation. MIMO-DECOR presented in this paper reduces the correlation-induced complexity in MIMO systems in favor of soft DSP. The goal of MIMO-DECOR is to shorten the critical paths for some filters in (5.61) so that they become error-free during VOS. This helps to reduce the number of error cancelers needed for error-control. Note that the proposed MIMO-DECOR differs from the previous work [93], [94] in that it is employed to reduce the correlations among the filters in a MIMO system. These filters can be wideband or narrowband, whereas the previous DECOR can only be employed for narrowband filters.

In its most general form, the MIMO-DECOR can be expressed as

\[
[\tilde{y}[n]]_{q\times 1} = T\left(\begin{bmatrix} h \end{bmatrix}_{q\times p}\right) \otimes [x[n]]_{p\times 1}
\]

\[
[y[n]]_{q\times 1} = T^{-1}\left(\begin{bmatrix} \tilde{y}[n] \end{bmatrix}_{q\times 1}\right)
\]

where \(T(\cdot)\) denotes the MIMO-DECOR transform, \([\tilde{y}[n]]_{q\times 1}\) is the output vector of the transformed system, \([h]_{q\times p}\), \([x[n]]_{p\times 1}\), and \([y[n]]_{q\times 1}\) are the short forms for the transfer matrix, inputs, and outputs, respectively, of the original MIMO system (5.61). An inverse MIMO-DECOR transform, denoted by \(T^{-1}(\cdot)\), is employed to convert the output vector \([\tilde{y}[n]]_{q\times 1}\) back to the desired \([y[n]]_{q\times 1}\).

To achieve the original goal of energy reduction, the MIMO-DECOR transform and its inverse should be simple so that the energy overhead incurred is small. In what follows, we will
derive a MIMO-DECOR transform where $\mathcal{T}$ and $\mathcal{T}^{-1}$ are $q$-by-$q$ matrices, resulting in matrix operations in (5.65) and (5.66).

Consider a general class of MIMO systems where the filters with the same input (say, filters $h_{ij}$ and $h_{kj}$ in (5.61)) have correlated time-frequency characteristics (i.e., bandwidths, impulse responses, etc.). This is typical for practical MIMO systems, e.g., Gigabit Ethernet 1000Base-T transceivers. We note that the correlated impulse responses imply a smaller precision for representing the difference between the coefficients $h_{ij}$ and $h_{kj}$ than that for $h_{ij}$ and $h_{kj}$ themselves. In addition, fewer taps might be sufficient for representing $(h_{ij} - h_{kj})$. Therefore, we can compute the outputs of these two filters alternatively by using the following filtering scheme

$$y_{ij}[n] = h_{ij} \otimes x_j[n],$$  \hspace{1cm} (5.67)

$$\Delta y[n] = (h_{kj} - h_{ij}) \otimes x_j[n],$$  \hspace{1cm} (5.68)

$$y_{kj}[n] = y_{ij}[n] + \Delta y[n],$$  \hspace{1cm} (5.69)

where $y_{kj}[n]$ and $y_{kj}[n]$ are the outputs of the filters $h_{ij}$ and $h_{kj}$, respectively. Obviously, the critical path delay of (5.68) is much smaller than that of (5.67) due to its low complexity. This also leads to additional energy savings that easily compensate for the overhead of extra computations in (5.69). Moreover, when applying VOS for further energy reduction, only (5.67) will induce soft output errors and thus require an error canceler, whereas (5.68)—(5.69) will be error-free (if their critical paths are sufficiently short, which is true for NEXT cancelers in 1000Base-T transceivers). This reduces the AEC overhead to just one error canceler as compared to two in a direct-AEC implementation, as illustrated in Fig. 5.7.

The effectiveness of the above filtering scheme is determined by the relative configuration of $h_{ij}$ and $h_{kj}$. If $h_{ij}$ and $h_{kj}$ are identical under a maximum correlation scenario, then
\( (h_{kj} - h_{ij}) = 0 \), resulting in the maximum energy savings as the computations in (5.68)–(5.69) can be avoided. In contrast, if \( h_{ij} \) and \( h_{kj} \) are uncorrelated then the complexity of (5.68) is comparable to that of (5.67) and hence no energy savings can be obtained over direct-AEC. As will be shown in Section 5.6, for practical MIMO systems such as 1000Base-T transceivers, the computations in (5.68) are typically simple enough to guarantee substantial energy savings via MIMO-AEC.

The filtering scheme given by (5.67)–(5.69) can be applied to other filters in (5.61) as well. Let \( i = 1, k = 2, \cdots, q \), and \( j = 1, \cdots, p \), we obtain the following MIMO-DECOR transform as

\[
\mathcal{T} \left( \begin{bmatrix} h_{q \times p} \end{bmatrix} \right)_{q \times p} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ -1 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ -1 & 0 & \cdots & 1 \end{bmatrix}_{q \times q} \cdot \begin{bmatrix} h_{q \times p} \end{bmatrix} = \begin{bmatrix} h_{11} & \cdots & h_{1p} \\ h_{21} - h_{11} & \cdots & (h_{2p} - h_{1p}) \\ \vdots & \ddots & \vdots \\ h_{q1} - h_{11} & \cdots & (h_{qp} - h_{1p}) \end{bmatrix}.
\]

and the corresponding inverse MIMO-DECOR transform is given by

\[
\mathcal{T}^{-1} \left( \begin{bmatrix} \tilde{y}[n] \end{bmatrix} \right)_{q \times 1} = \begin{bmatrix} 1 & 0 & \cdots & 0 \\ 1 & 1 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & \cdots & 1 \end{bmatrix}_{q \times q} \cdot \begin{bmatrix} \tilde{y}[n] \end{bmatrix} = \begin{bmatrix} \tilde{y}_1[n] \\ (\tilde{y}_2[n] + \tilde{y}_1[n]) \\ \vdots \\ (\tilde{y}_q[n] + \tilde{y}_1[n]) \end{bmatrix}, \quad (5.71)
\]

where \( \begin{bmatrix} \tilde{y}[n] \end{bmatrix}_{q \times 1} \) is given by (5.65). Obviously, \( \mathcal{T} \cdot \mathcal{T}^{-1} = I_{q \times q} \), where \( I_{q \times q} \) is an identity matrix. Thus, the outputs of inverse MIMO-DECOR transform equal the desired outputs.

From (5.70)–(5.71), the MIMO-DECOR transform involves coefficient precomputation and the inverse MIMO-DECOR transform adds up the differential outputs of the transformed system to give the desired ones. It is easy to see that both transforms incur very small overhead and
are easy to implement. In addition, there are \((q - 1) \times p\) out of \(q \times p\) filters in the transformed system (5.70) performing low-complexity filtering. As a result, the number of error cancelers needed for error-control during VOS can be reduced from \(q \times p\) for direct-AEC to only \(p\) for MIMO-AEC. In summary, the proposed MIMO-AEC technique achieves substantial energy reduction via (1) MIMO-DECOR resulting in low-complexity filtering, (2) VOS, and (3) energy-optimum AEC for restoring algorithmic performance.

5.6 Application to Gigabit Ethernet

In this section, we study the performance of the proposed MIMO-AEC technique in a Gigabit Ethernet communication system. We first give an overview of Gigabit Ethernet 1000Base-T standard and then employ the MIMO-AEC to design a low-power 1000Base-T device.

5.6.1 1000Base-T transceivers

Gigabit Ethernet is a new generation of high-bandwidth data interface over copper medium for local area networks (LAN). The 1000Base-T standard defines connections between switches (repeaters) and data terminal equipments (DTE) such as desktop terminals. As illustrated in Fig. 5.8, the 1000Base-T transmission scheme specifies a 1000-Mbit/s, full duplex data throughput achieved by using four pairs of wire in Category 5 (CAT-5) cable, each pair transmitting a 250-Mbit/s data stream encoded into a four-dimension five-level pulse amplitude modulation (4-D PAM-5) signal constellation. The interested reader is referred to [12] for a detailed discussion of 4-D PAM-5 modulation scheme.

Each 1000Base-T device contains four identical transceivers, one for each pair of physical wire. The bidirectional data transmission on the same wire is made possible by hybrid circuits. On the receive side, each receiver confronts a physical channel of minimum 100m CAT-5 cable. As shown in Fig. 5.8, the three major causes of signal distortion encountered are propag-
Figure 5.8 1000Base-T transmission scheme with signal impairments in one transceiver.

...tion loss (due to channel attenuation), echo noise (generated by a self-returned signal due to impedance mismatch in hybrid circuits), and NEXT noise (caused by near-end crosstalk between adjacent wires). The detailed description of physical mechanisms of these impairments can be found in [95]. The IEEE 802.3ab Standard [12] specifies the models for the worst-case noise environment as

\[
L_P(f) = 2.1 f^{0.529} + 0.4/f, \\
L_N(f) = 27.1 - 16.8 \log_{10}(f/100), \\
L_E(f) = \begin{cases} 
15, & 1 \leq f < 20, \\
15 - 10 \log_{10}(f/20), & 20 \leq f \leq 100, 
\end{cases}
\]

where \(1 \leq f \leq 100\) is the frequency expressed in MHz, \(L_P(f)\), \(L_N(f)\), and \(L_E(f)\), all expressed in dB/100m, are the squared magnitude of the propagation loss, NEXT, and echo transfer function, respectively.

The 1000Base-T data transmission requires a BER \(\leq 10^{-10}\). Using 4-D PAM-5 modulation scheme, the SNR at the slicer for achieving this BER is 19.3 dB. To overcome considerable
Figure 5.9 Block diagram of signal recovery scheme in 1000Base-T devices.

signal distortion caused by echo, NEXT, cable attenuation and dispersion, advanced digital signal processing and filtering techniques are needed for signal recovery. Figure 5.9 depicts the block diagram of a 1000Base-T device which consists of four identical transceivers operating simultaneously. At each receiver, the digital output of the A/D converter is first filtered by a feed-forward equalizer (FFE) to remove the intersymbol interference (ISI) introduced by the channel. As each received signal is also corrupted by one echo and three NEXT interferences from the adjacent wires, one echo canceler and three NEXT cancelers are needed correspondingly to perform interference suppression. In total, each 1000Base-T device requires four FFES, four echo cancelers, and twelve NEXT cancelers, all of which are LMS adaptive filters. This involves intensive filtering operations which necessitate effective energy reduction techniques to alleviate power dissipation.
5.6.2 Simulation results

We consider the signal recovery scheme on the receive side of a 1000Base-T device (see Fig. 5.9) as a MIMO system, which is expressed as

\[
\begin{bmatrix}
Y_1[n] \\
Y_2[n] \\
Y_3[n] \\
Y_4[n]
\end{bmatrix} = \begin{bmatrix}
h_c^1 & 0 & 0 & 0 \\
0 & h_c^2 & 0 & 0 \\
0 & 0 & h_c^3 & 0 \\
0 & 0 & 0 & h_c^4
\end{bmatrix} \otimes \begin{bmatrix}
R_1[n] \\
R_2[n] \\
R_3[n] \\
R_4[n]
\end{bmatrix} - \begin{bmatrix}
w_c^{12} & w_c^{13} & w_x^{14} \\
w_x^{21} & w_c^{22} & w_x^{23} & w_x^{24} \\
w_x^{31} & w_x^{32} & w_c^{33} & w_x^{34} \\
w_x^{41} & w_x^{42} & w_x^{43} & w_c^{44}
\end{bmatrix} \otimes \begin{bmatrix}
T_1[n] \\
T_2[n] \\
T_3[n] \\
T_4[n]
\end{bmatrix},
\] (5.75)

where \(\{Y_1[n], Y_2[n], Y_3[n], Y_4[n]\}\) is the recovered 4-D PAM-5 signal; \(T_i[n]\) and \(R_i[n]\) are the transmitted and received signals, respectively, at the \(i^{th}\) transceiver; \(h_c^i, w_c^i,\) and \(w_x^{ij}\) denote the FFE, echo canceler, and NEXT canceler (to cancel the NEXT interference generated by the \(j^{th}\) transmitter), respectively, for the \(i^{th}\) receiver. Note that the first term on the right side of (5.75) represents channel equalization that involves independent SISO filtering, whereas the second term describes the MIMO interference suppression scheme. In what follows, we employ the proposed AEC technique to reduce the power dissipation of signal recovery scheme (5.75). In particular, we apply the MIMO-AEC for the MIMO interference suppression scheme.

We assume that the SNR requirements for the FFE, echo cancellation, and NEXT cancellation are 25 dB, 28 dB, and 30 dB, respectively. This results in a 21 dB SNR at \(Y_3[n]\), which is 1.7 dB higher than the minimum of 19.3 dB necessary for achieving a BER of \(10^{-10}\). From (5.75), the FFE and echo cancellation involve independent SISO filtering operations, thus allowing direct-AEC for energy reduction. Note that these filters are LMS adaptive filters which can be implemented using the AEC-based adaptive filtering scheme presented in Section 5.4. As mentioned before, every three NEXT cancelers with the same input (e.g., \(w_x^{14}, w_x^{24}\) and \(w_x^{34}\) with \(R_4[n]\) as their input) have correlated impulse responses, thereby enabling MIMO-AEC to
further improve the energy-efficiency. In practical 1000Base-T systems, the frequency responses of NEXT interferences vary away from the bound given by (5.73) due to physical variations of CAT-5 cable. An estimate of these variations can be obtained from experiments in the field. In our simulations, we emulate these variations by introducing a disturbance $\Delta L_N(f)$ uniformly distributed between $[-L^\text{min}_N, 0]$ onto the transfer function $L_N(f)$. Thus, an instance of NEXT interference with a frequency response of $L_N(f) + \Delta L_N(f)$ is generated and utilized to calibrate the corresponding NEXT canceler.

We use a full adder with $T_a = 0.3$ ns at $V_{dd-crit} = 2.5$ V to implement these filters in a 0.25-$\mu$m CMOS technology. All the simulations employ the filter architecture shown in Fig. 5.6, where two’s complement carry-save Baugh-Wooley multipliers [96] and ripple-carry tree-style adders are being employed. It was found (see Table 5.1) that the critical path delays $T_{cp}$'s for the FFEs, echo cancelers, and NEXT cancelers are no more than $26T_a$. Thus, these filters meet the sample period requirement which is 8 ns for 1000Base-T devices. We employ a logic-level simulation [55] to detect delay violations due to VOS on every path to the filter output given a sequence of inputs. Thus, all paths and not just the critical paths are included. If the propagation delay on a path is larger than the sample period requirement, the corresponding output will not be able to settle to its new value but instead will retain its previous value, thereby resulting in an output error. The output SNR is calculated by averaging over the entire input data set. The power dissipation during steady-state filtering operation is obtained via the gate-level simulation tool MED [97] for a 0.25-$\mu$m CMOS technology.

Figure 5.10 plots the energy-performance trade-offs achieved via direct-AEC for an individual FFE, echo canceler, NEXT canceler, as well as for the 1000Base-T device consisting of four FFEs, four echo cancelers, and twelve NEXT cancelers. It is shown that in comparison with conventional implementations, energy savings of 63.1%, 65.7%, and 59.5% are achieved for the FFEs, echo cancelers, and NEXT cancelers, respectively, at the desired SNR. The overall energy
Table 5.1 Design specifications for the energy-optimum AEC-based filters.

<table>
<thead>
<tr>
<th></th>
<th>FFE</th>
<th>AEC for FFE</th>
<th>Echo Canceller</th>
<th>AEC for Echo</th>
<th>NEXT Canceller</th>
<th>AEC for NEXT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tap #</td>
<td>16</td>
<td>5</td>
<td>64</td>
<td>15</td>
<td>70</td>
<td>18</td>
</tr>
<tr>
<td>B_{INPUT}</td>
<td>8b</td>
<td>8b</td>
<td>3b</td>
<td>3b</td>
<td>3b</td>
<td>3b</td>
</tr>
<tr>
<td>B_F</td>
<td>10b</td>
<td>5b</td>
<td>12b</td>
<td>8b</td>
<td>10b</td>
<td>8b</td>
</tr>
<tr>
<td>B_WUD</td>
<td>12b</td>
<td>12b</td>
<td>14b</td>
<td>14b</td>
<td>14b</td>
<td>14b</td>
</tr>
<tr>
<td>T_{cp}</td>
<td>26T_a</td>
<td>19T_a</td>
<td>25T_a</td>
<td>17T_a</td>
<td>25T_a</td>
<td>19T_a</td>
</tr>
</tbody>
</table>

Figure 5.10 Energy savings via direct-AEC.

savings for the 1000Base-T device is found around 60.2% at 21 dB SNR. These energy savings are obtained at $k_{wor} \approx 0.6$ and $T_{a,V_{dd-sub}} \approx 0.4\,\text{ns}$. Table 5.1 provides design specifications for these filters and the associated AECs. As indicated, the energy-optimum AECs have critical path delays of less than $20T_a$, thus being error-free ($T_{cp} < 8\,\text{ns}$) at $V_{dd-sub}$.

Further energy reduction can be obtained for NEXT cancellation via the proposed MIMO-AEC, resulting in four conventional NEXT cancelers and eight low-complexity differential NEXT cancelers via MIMO-DECOR (see (5.67)–(5.69)). In addition, the number of AECs is reduced from twelve to only four. As shown in Table 5.2, a strong correlation (e.g., $L_{min} = 5\,\text{dB}$) among the NEXT cancelers enables a large reduction in the AEC overhead (44.3%); otherwise,
Table 5.2 Design specifications and energy savings for the differential NEXT cancelers using MIMO-DECOR.

<table>
<thead>
<tr>
<th>$L_N^{\text{min}}$</th>
<th>5 dB</th>
<th>10 dB</th>
<th>15 dB</th>
<th>20 dB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tap #</td>
<td>52</td>
<td>56</td>
<td>59</td>
<td>63</td>
</tr>
<tr>
<td>bit-width</td>
<td>5b</td>
<td>5b</td>
<td>6b</td>
<td>7b</td>
</tr>
<tr>
<td>$T_{cp}$</td>
<td>$18T_a$</td>
<td>$18T_a$</td>
<td>$19T_a$</td>
<td>$20T_a$</td>
</tr>
<tr>
<td>Overhead Reduction</td>
<td>44.3%</td>
<td>42.6%</td>
<td>37.1%</td>
<td>25.3%</td>
</tr>
</tbody>
</table>

Figure 5.11 Energy savings via MIMO-AEC.

the overhead reduction is small and the differential NEXT cancelers may become error-prone at VOS. This is consistent with our discussion in Section 5.5. For practical 1000Base-T transceivers where $L_N^{\text{min}}$ is typically around 10 dB – 15 dB, the MIMO-AEC leads to about 40% overhead reduction. Also shown in Fig. 5.11, a 1000Base-T device employing the MIMO-AEC can achieve energy savings of 12.6% – 22.1% over direct-AEC implementations and 64.2% – 69.1% over conventional implementations at the same output SNR.
5.7 Summary

In this chapter, we have proposed an adaptive error-cancellation (AEC) algorithm for designing low-power broadband signal processing systems. In particular, we determine the energy-optimum AEC design and derive a reduced-order least mean square (LMS) algorithm to compute the AEC coefficients adaptively. We build upon this technique by proposing an AEC-based adaptive filtering scheme and a MIMO-AEC scheme for low-power MIMO signal processing. An algorithm transformation, denoted as MIMO-DECOR, is developed to reduce complexity by exploiting correlations inherent in MIMO systems, thereby improving the energy-efficiency of AEC. Simulation results of a low-power Gigabit Ethernet 1000Base-T device show 25.2%–44.3% overhead reduction due to MIMO-DECOR and 64.2%–69.1% energy savings over optimally voltage-scaled present-day systems with no loss in algorithmic performance.
CHAPTER 6
CONCLUSIONS AND FUTURE DIRECTIONS

Power reduction is essential for high-performance computing and communication systems. Numerous low-power techniques developed so far combined with the benefits of technology scaling drive VLSI design towards integrating higher functionality, increasing throughput, extending operational life, minimizing cost, and improving reliability. With feature sizes being reduced into the deep submicron (DSM) regime, the emergence of DSM noise combined with increasingly stringent requirements on performance and aggressive design styles (such as dynamic logic, low supply voltage, using high-leakage transistors, operating with high clock-frequencies, etc.) has raised concerns about our ability to maintain reliability in an affordable manner in future CMOS technologies. This demands a new design paradigm where reliability and energy-efficiency are addressed in a cohesive manner.

6.1 Current Work

We have demonstrated that noise-tolerance is an effective method to ensure the performance and energy-efficiency trends for future VLSI systems. In particular, we address noise-tolerance issues at both the circuit and the algorithmic levels. Noise-tolerance provides a new direction for research in the design of energy-efficient VLSI computing and communication systems, whereby algorithms, architectures, and circuit properties are jointly optimized to push the limits of power reduction.

The research accomplishments presented in this dissertation are summarized as follows:

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• We proposed the metrics of average noise threshold energy (ANTE) and energy normalized ANTE (NANTE) to quantify the noise-immunity and energy-efficiency, respectively, of integrated circuit techniques. The ANTE metric is derived from the observation that each point on noise-immunity curves represents the amplitude $V_n$ and duration $T_n$ of an input noise pulse that makes a logic gate in error. Thus, a statistical measure defined as $E(V_n^2T_n)$ quantifies the average noise energy that a circuit technique can tolerate. The ANTE measure allows comparisons of noise-immunity but does not indicate the energy being involved. Thus, we proposed the energy normalized ANTE (NANTE) as a measure of the energy penalty incurred in improving noise-immunity.

• We presented a noise-tolerant, energy-efficient circuit technique referred to as the mirror technique to improve the noise-immunity of dynamic circuits. Based on the principle of the Schmitt trigger, the proposed mirror technique increases the switching threshold voltages (and thus the noise-immunity) of dynamic circuits when error-prone input patterns are present. Simulation results of NAND gates and full adders indicate that the proposed mirror technique improves the ANTE and energy normalized ANTE by about 2X and 1.4X over conventional domino circuits. In addition, the mirror technique leads to a smaller design overhead, thus having a better energy-efficiency as compared with the existing noise-tolerant techniques.

• A MAC ASIC in 0.35-$\mu$m CMOS was designed and fabricated employing the conventional domino and the proposed mirror technique. Two noise-injection circuit modules (NIC) were utilized to generate ground bounce noise (which has been identified as a major noise source in high-performance VLSI systems) into a dynamic multiplier-accumulator (dynamic MAC) and a noise-tolerant (mirror) multiplier-accumulator (mirror NT MAC). The outputs of the two MACs were compared under different operation conditions and
subject to various noise environments. Measured results demonstrate that the proposed mirror technique achieves a 27\% improvement in noise-immunity over conventional dynamic circuits.

- We investigated the leakage-induced noise-immunity degradation in deep submicron CMOS technologies. Two performance metrics, unity noise gain (UNG) and four-stage delay, were proposed to quantify the noise-immunity and speed, respectively. It was found that deep submicron CMOS technologies achieve 1.7\(X\) – 2\(X\) delay reduction but incur 60\% – 70\% degradation in noise-immunity due to the scaling of transistor threshold voltage which results in high-leakage. We proposed a leakage-tolerant circuit technique, the boosted-source (BS) technique, which is able to improve noise-immunity without incurring large speed and power penalties. Simulation results of wide fan-in OR gates designed in the Predictive Berkeley BSIM3v3 0.13-\(\mu\)m technology demonstrate 1.6\(X\) – 3\(X\) improvement in noise-immunity at the expense of minor energy overhead but no loss in delay.

- We extended the information-theoretic framework by proposing a soft-decision channel (SDC) model for deriving the lower bounds on energy dissipation of noisy digital systems. The proposed SDC model describes desired (noiseless) signals and DSM noise as binary (with a voltage level \(V_\text{dd}\) and transition probability \(t\)) and continuous (with a certain statistical distribution) random signals, respectively. Thus, all the signals and noise are captured in such a way that reflects their inherent analog nature. It was shown that the proposed SDC model is a generalized approach suitable for various digital systems. The bounds on energy dissipation derived via the SDC model are much lower than those of the previous binary symmetric channel (BSC) model. Furthermore, the proposed SDC model leads to an efficient algorithm to compute the lower bounds. The computational com-
plexity of the algorithm increases linearly with system complexity, making the proposed SDC model applicable to complex digital systems.

- We compared the energy-efficiency bounds for conventional domino and noise-tolerant circuits, and determined to what extent noise-immunity needs to be enhanced before the energy overhead starts to dominate. We proposed to employ noise-tolerance in high-speed arithmetic circuits to reduce energy dissipation subject to a specified level of algorithmic performance, thereby reducing the gap between the bounds on energy-efficiency and the actual energy dissipation. A 16-bit carry lookahead adder in the context of a CDMA communication system demonstrates 31.2% – 51.4% energy reduction over conventional systems and 1.9X reduction in the gap between the information-theoretic bounds and the actual energy dissipation without algorithmic performance loss.

- An adaptive error-cancellation (AEC) technique was proposed as a practical algorithmic noise-tolerance (ANT) approach to combat soft errors due to voltage overscaling for reducing power dissipation of integrated circuit implementations of signal processing and communication systems. The proposed AEC technique exploits the inherent dependence among soft output errors, input statistics, and arithmetic architectures for error-control. A low-complexity error canceler was employed to generate a statistical replica of the soft errors and then subtract it from the output, thereby restoring the algorithmic performance. It was shown that the proposed AEC technique is well-suited for broadband signal processing and communication systems.

- To optimize the energy-efficiency of AEC, we derived an energy-optimum AEC to mitigate the degradation in algorithmic performance while consuming minimal energy. We built upon the energy-optimum AEC by proposing a MIMO-AEC that employs an algorithm transformation, denoted as MIMO decorrelating (MIMO-DECOR) transform,
for the design of low-power MIMO signal processing systems. MIMO-DECOR reduces complexity by exploiting correlations inherent in MIMO systems, thereby improving the energy-efficiency. We employed the MIMO-AEC to design a low-power Gigabit Ethernet 1000Base-T device. Simulation results demonstrate 25.2%–44.3% overhead reduction due to MIMO-DECOR and 64.2%–69.1% energy savings over conventional implementations at the same algorithmic performance.

6.2 Future Directions

In this section, we outline some future directions based on the research presented in this dissertation.

- The noise-tolerant circuit techniques are typically developed under the assumption of a worst-case DSM noise scenario and thus induce considerable design overhead on average. Minimizing the complexity while providing more flexibility in terms of tuning the noise-immunity in the field subject to the performance constraints will improve the applicability of noise-tolerant techniques. This can be done by taking into account system and algorithmic properties (e.g., input signal statistics) along with circuit and process parameters, and reconfiguring the noise-immunity setup in real-time according to the actual noise environments and performance requirements.

- The information-theoretic framework provides an approach for determining the lower bounds on energy dissipation of integrated digital systems in the presence of noise. Accurate bounds are made possible by modeling various logic signals and noise in accordance with their inherent physical behaviors. While we have proposed a SDC model employing a general description for DSM noise, characterization of total noise contribution is still an open problem as it requires knowledge of various noise sources and consideration of
numerous factors such as temperature, circuit speed, semiconductor properties, etc. Also, determining the lower bounds analytically for complete digital systems (e.g., a sophisticated signal processing system) is a challenging topic due to the computational complexity being involved.

- Integrating noise-tolerance jointly at different levels of design hierarchy is of great importance for the design of low-power DSP and communication systems. This requires judicious considerations of algorithms, architectures, circuit techniques, and noise properties at an extended design space. An energy-optimum design methodology should address noise-tolerance and energy-efficiency issues at the circuit, architecture, and algorithmic levels in a unified manner. One can develop such design methodology by employing the existing noise-tolerant circuit and ANT techniques and generalizing a systematic determination of noise-tolerance with a properly understanding of system requirements as well as the constraints imposed by the noise-tolerant techniques.
APPENDIX A

PROOF OF THEOREM 1 IN CHAPTER 4

In this appendix, we prove that the mutual information \( I(Y_N = Y + N; X_0, X_1, \ldots, X_{n-1}) \) of an \( n \)-input, single-output noisy gate achieves the maximum when \( p_y \triangleq P(Y = 1) = 0.5 \).

From Lemma 1, we rewrite \( I(Y_N; X_0, X_1, \ldots, X_{n-1}) \) as

\[
I(Y_N; X_0, X_1, \ldots, X_{n-1})
= - \int_{-\infty}^{\infty} \left[ (p_y f_N(v - V_{dd}) + (1 - p_y) f_N(v)) \log_2 (p_y f_N(v - V_{dd}) + (1 - p_y) f_N(v)) \right.
\]
\[
- f_N(v) \log_2 f_N(v)] dv. \tag{A.1}
\]

Taking partial derivative of \( I(Y_N; X_0, X_1, \ldots, X_{n-1}) \) with respect to \( p_y \), we get

\[
\frac{\partial I(Y_N; X_0, X_1, \ldots, X_{n-1})}{\partial p_y}
= - \int_{-\infty}^{\infty} \left[ (f_N(v - V_{dd}) - f_N(v)) \log_2 (p_y f_N(v - V_{dd}) + (1 - p_y) f_N(v)) \right.
\]
\[
+ \frac{1}{\ln 2} (f_N(v - V_{dd}) - f_N(v)) \right] dv
\]
\[
= - \int_{-\infty}^{\infty} (f_N(v - V_{dd}) - f_N(v)) \log_2 (p_y f_N(v - V_{dd}) + (1 - p_y) f_N(v)) dv, \tag{A.2}
\]

where we utilize the fact that

\[
\int_{-\infty}^{\infty} \frac{1}{\ln 2} [f_N(v - V_{dd}) - f_N(v)] dv = 0. \tag{A.3}
\]
The maximum value of $I(Y_N; X_0, X_1, \ldots, X_{n-1})$ is obtained at the point where

$$\frac{\partial I(Y_N; X_0, X_1, \ldots, X_{n-1})}{\partial p_y} = 0. \quad (A.4)$$

From (A.2), this implies

$$\int_{-\infty}^{\infty} f_N(v - V_{dd}) \log_2(p_y f_N(v - V_{dd}) + (1 - p_y)f_N(v)) dv$$

$$= \int_{-\infty}^{\infty} f_N(v) \log_2(p_y f_N(v - V_{dd}) + (1 - p_y)f_N(v)) dv. \quad (A.5)$$

Obviously, (A.5) is satisfied if and only if $p_y = 0.5$. Furthermore, we have

$$\frac{\partial^2 I(Y_N; X_0, X_1, \ldots, X_{n-1})}{\partial p_y^2}$$

$$= - \frac{1}{\ln 2} \int_{-\infty}^{\infty} \frac{(f_N(v - V_{dd}) - f_N(v))^2}{p_y f_N(v - V_{dd}) + (1 - p_y)f_N(v)} dv \leq 0. \quad (A.6)$$

Thus, $I(Y_N; X_0, X_1, \ldots, X_{n-1})$ at $p_y = 0.5$ is indeed a global maximum.
APPENDIX B

PROOF OF THEOREM 2 IN CHAPTER 4

In this appendix, we derive the optimum solution \((t_0^{\text{opt}}, t_1^{\text{opt}}, \ldots, t_{m-1}^{\text{opt}})\) for the energy optimization problem (4.26)–(4.27).

Consider the mutual information for the noisy system shown in Fig. 4.4 (page 51):

\[
I_{Y_N;X}(Y_{dd}, t_0, \cdots, t_{m-1}, \sigma_{N_0}^2, \cdots, \sigma_{N_{m-1}}^2)
\]

\[
\triangleq I(Y_{N_0}, \cdots, Y_{N_{m-1}}; X_0, \cdots, X_{n-1})
\]

\[
= H(Y_{N_0}, \cdots, Y_{N_{m-1}}) - H(Y_{N_0}, \cdots, Y_{N_{m-1}}|X_0, \cdots, X_{n-1})
\]

\[
= H(Y_{N_0}, \cdots, Y_{N_{m-1}}) - H(N_0, \cdots, N_{m-1})
\]

\[
\leq \sum_{i=0}^{m-1} (H(Y_{N_i}) - H(N_i)), \tag{B.1}
\]

where the equality is achieved if the \(m\) outputs \(Y_{N_0}, Y_{N_1}, \cdots, Y_{N_{m-1}}\) are independent. Note that for typical digital systems where \(n \geq m\), there always exists certain input statistics such that the outputs are independent of each other.
We denote the mutual information \( H(Y_{N_i}) - H(N_i) \) for the \( i^{th} \) output as \( I_{Y_{N_i};X}(V_{dd}, t_i, \sigma_{N_i}^2) \).

From Lemma 1, \( I_{Y_{N_i};X}(V_{dd}, t_i, \sigma_{N_i}^2) \) is given by

\[
I_{Y_{N_i};X}(V_{dd}, t_i, \sigma_{N_i}^2) = - \int_{-\infty}^{\infty} \left[ (t_i f_{N_i}(v - V_{dd}) + (1 - t_i) f_{N_i}(v)) \log_2 (t_i f_{N_i}(v - V_{dd}) + (1 - t_i) f_{N_i}(v)) \right. \\
\left. - f_{N_i}(v) \log_2 f_{N_i}(v) \right] dv. \tag{B.2}
\]

where \( f_{N_i}(v) \) is the distribution function for the noise voltage \( N_i \).

Consider the power dissipation \( P_{\text{tot}} \) as primarily consisting of dynamic power dissipation.

Employing (B.1) and (B.2), we rewrite the optimization problem (4.26)–(4.27) as

\[
\begin{align*}
\text{minimize:} & \quad \sum_{i=0}^{m-1} t_i C_{L_i} V_{dd}^2 f_c, \\
\text{subject to:} & \quad \sum_{i=0}^{m-1} I_{Y_{N_i};X}(V_{dd}, t_i, \sigma_{N_i}^2) f_c \geq R
\end{align*} \tag{B.3}
\]

This is a standard optimization problem that can be solved using the Lagrange multiplier method [85]. Define function \( \mathcal{J}(t_0, t_1, \cdots, t_{m-1}; \lambda) \) as

\[
\mathcal{J}(t_0, t_1, \cdots, t_{m-1}; \lambda) = \sum_{i=0}^{m-1} t_i C_{L_i} V_{dd}^2 f_c + \lambda \left( R - \sum_{i=0}^{m-1} I_{Y_{N_i};X}(V_{dd}, t_i, \sigma_{N_i}^2) f_c \right), \tag{B.5}
\]

where \( \lambda \) is the sensitivity vector of the Lagrange multiplier. Differentiating \( \mathcal{J}(t_0, t_1, \cdots, t_{m-1}; \lambda) \) with respect to \( t_i \), we get

\[
\frac{\partial \mathcal{J}(t_0, t_1, \cdots, t_{m-1}; \lambda)}{\partial t_i} = C_{L_i} V_{dd}^2 f_c - \lambda f_c \frac{\partial I_{Y_{N_i};X}(V_{dd}, t_i, \sigma_{N_i}^2)}{\partial t_i}. \tag{B.6}
\]
Let (B.6) be zero, we have

\[
\frac{\partial I_{Y_N;X}(V_{dd}, t_i, \sigma_{N_i}^2)}{\partial t_i} = \beta C_i V_{dd}^2, \quad i = 0, 1, \cdots, m - 1, \tag{B.7}
\]

where \( \beta = 1/\lambda \). The optimum solution \((t_0^{\text{opt}}, t_1^{\text{opt}}, \cdots, t_{m-1}^{\text{opt}})\) to (B.3)–(B.4) is thus obtained from (B.7) at \( \lambda = \lambda_{\text{min}} \), or equivalently \( \beta = \beta_{\text{max}} \), where the information-theoretic constraint (B.4) is just met, i.e.,

\[
\sum_{i=0}^{m-1} I_{Y_N;X}(V_{dd}, t_i^{\text{opt}}, \sigma_{N_i}^2) f_c = R. \tag{B.8}
\]

This is because that \( \frac{\partial I_{Y_N;X}(V_{dd}, t_i, \sigma_{N_i}^2)}{\partial t_i} \) is a monotonically decreasing function with respect to \( t_i \) (see (A.6)). From (B.7), for any \( \beta < \beta_{\text{max}} \) (or \( \lambda > \lambda_{\text{min}} \)), \( t_i > t_i^{\text{opt}} \) making \( \sum_{i=0}^{m-1} I_{Y_N;X}(V_{dd}, t_i, \sigma_{N_i}^2) f_c > R \), which also leads to a larger power dissipation due to the increase in \( t_i \).
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VITA

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