DIGITALLY ENHANCED CMOS RF TRANSMITTER WITH INTEGRATED POWER AMPLIFIER

BY

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DISSertation

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ABSTRACT

An energy-efficient, 3.5 GHz, direct-conversion RF transmitter with integrated 23 dBm, Class-B power amplifier (PA) is fabricated in a 0.13 µm CMOS process. The TX chip is packaged using a low-cost chip-on-board (COB) technique. When 20-MHz bandwidth OFDM signals are transmitted, a high TX average power efficiency is achieved exploiting the dynamic current biasing of the Class-B PA and a low-loss output matching network using high-Q bondwire inductances in the package.

Assisted by an integrated feedback path, a two-dimensional, digital look-up table (2-D LUT) adapted by complex gradient-descent algorithms compensates the I/Q mismatch and memoryless nonlinearities of the whole transmit path, including the severe amplitude and phase distortions of the on-chip PA. Fifth-order Butterworth transmit filters with 34 MHz cutoff frequency sufficiently attenuate the aliases of the 80 MS/s digital-to-analog converters (DACs), while retaining high in-band fidelity without corrupting the predistorted signal.

When a 20 MHz, 64-QAM OFDM signal with 9.6 dB peak-to-average power ratio (PAPR) was transmitted, the measured average drain efficiency (DE) of the PA was 12.5% at 9.6 dB back-off and 17.5% at 7 dB back-off, and the
corresponding error-vector magnitude (EVM) was measured −29.6 dB and −26.3 dB with equalization, respectively. Peak DE of 55% and 25 dBm saturated output power were also measured for the same PA in a stand-alone package.
To my parents
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CHAPTER 1

INTRODUCTION

1.1 Motivation

Over the last few decades, wireless communication has dramatically developed and there have been continuing demands for performance, i.e., transmission rate, coverage range, etc., and cost reduction in recent years. High data rate is achieved not only by wide bandwidth as exemplified in Figure 1.1 [1], but also by high transmitter (TX) and receiver (RX) accuracies which allow the reliable transmission and reception of more crowded data. For example, in the 802.11a wireless local area network (WLAN) system, the transmitter constellation error spec for 54 Mbps data rate is -25 dB, which is much tighter than the spec for 16 Mbps data rate, -19 dB [2]. In addition, for the efficient use of spectrum resources, modern communication standards usually feature a high peak-to-average power ratio (PAPR), which requires high linearity and large dynamic range in tranceivers. On the other side, the demand of wide coverage in mobiles necessitates high radio-frequency (RF) TX output power.
Figure 1.1: Various wireless standards with different data rates and bandwidths [1].

The cost of mobile devices has been another major concern for the ubiquitous use of wireless communication technology. High integration in low-cost CMOS process and process scaling have enabled less discrete components and small footprints on the board. Recent system/circuit co-design facilitates minimizing the implementation complexity and optimally allocating the design resources, helping to reduce the design cost. Long-term and short-term performance variations of the devices due to temperature, environments, stress,
etc., must be addressed in order to reduce the packaging cost, improve the yield, and increase the device lifetime. Lastly, high power efficiency is crucial to reduce the implementation cost, especially for mobile devices, since it not only reduces the battery size, but also directly affects the battery lifetime. Less on-chip heat as a result of high efficiency also relaxes the packaging effort and reduces the deteriorating high temperature effects.

Power amplifiers (PAs) have become the most critical block with respect to low cost for two main reasons: (1) CMOS integration of PAs has had limited success to date, and (2) the power efficiency of PAs among various transceiver building blocks is particularly important because it significantly impacts the whole system power efficiency due to their high output power. The latter becomes more important in future generation broadband mobile communication systems (WiMAX and 4G) which adopt multi-carrier modulation schemes for reliable data transmission via severely faded, frequency-selective channels such as orthogonal frequency-division multiplexing (OFDM) channels. Due to the high PAPR of OFDM signal, high linearity is required for the RF PAs to avoid the problems of in-band intermodulation distortion and spectral regrowth in adjacent channels. However, the fact that linearity typically has a trade-off relation with power efficiency in most power amplifier topologies indicates that stringent linearity requirements make it hard to employ RF PAs with high power efficiency. In addition, high PAPR significantly degrades the average power efficiency due to
back-off. Figure 1.2 shows the typical relation between linearity and power efficiency.

One of the most popular approaches in industry for the low-cost implementation of wireless tranceivers is to integrate all other digital and analog tranceiver blocks in a single CMOS die and to use separate PA chips. Figure 1.3 shows an example of this approach, where media-access control (MAC), digital/analog baseband, and some RF blocks for several standards are integrated in a single die, but a separate chip is used for RF power amplifiers and switches in the WLAN mode [3]. Although the PA power efficiency might be high in this case by using niche technologies, e.g., GaAs, InP, etc., overall cost might increases due to high fabrication cost and large area, which is naturally driving
industry people to integrate the power amplifiers in the same CMOS die.

Figure 1.4 shows another example where the power amplifiers are integrated in the same CMOS die, moving closely toward the realization of system-on-chip (SOC). Despite the reduced cost in terms of area and fabrication cost, integrated power amplifiers suffer from low PA power efficiency owing to the low breakdown voltage and lossy passives of CMOS process. The low breakdown also poses the device reliability issue. In addition, PA integration sometimes gives rise to transmitter instability due to the coupling of PA output
back to the input or intermediate nodes through parasitics, substrates, or packages. All of these difficulties limit the success of PA integration. Furthermore, conventional Class-A or -AB PAs with large back-off to satisfy the linearity requirements of modern communication standards additionally reduce the power efficiency. This often pushes PA designers to increase the PA maximum output power beyond what is required, further worsening the stability/reliability issues especially in rugged conditions.

With this background, linearization techniques of power-efficient, nonlinear PAs—e.g., feed-forward compensation, Cartesian feedback, and digital
equalization—have been widely researched in order to (1) improve the PA power efficiency, (2) reduce the on-chip heating, and (3) relax the PA integration difficulties. While digital equalization has a long history of being used in communications, its application to nonlinear analog and RF circuits has been limited until recent years, mostly due to the complexity associated with a nonlinear formulation, and thus, a potentially high implementation cost. However, as technology downscaling continues to reduce the digital cost dramatically and the integration of RF circuits in standard CMOS process becomes commonplace, digital equalization has been increasingly investigated as a viable approach to overcome analog and RF circuit impairments in deeply scaled technology nodes. The slow feedback adaptation of digital signal processing (DSP) also renders the compensation much less susceptible to stability problems; thus, it can compensate baseband signals encompassing a broader spectrum than those that can be treated by Cartesian feedback. In the last few years, high-performance, low-power analog-to-digital converters (ADCs) error-corrected using digital adaptive techniques were successfully implemented [4]–[9]. In the RF sector, various digital algorithms for compensating the nonlinearities of RF PAs have been introduced and showcased in either stand-alone or integrated platforms [10]–[15].

Digital equalization allows the use of nonlinear, power-efficient PAs such as Class-B types that exhibit superior peak as well as average efficiency characteristics compared to Class-A or -AB PAs that are currently dominant in
real-world applications for linear amplification of high PAPR signals. Furthermore, signal preconditioning in digital domain makes it possible to treat the whole transmit signal path including the baseband building blocks, e.g., the digital-to-analog converter (DAC) and low-pass filter (LPF), and other RF blocks such as the mixer.

In practical applications, non-static operating conditions due to process, temperature, and supply voltage variations make it difficult to model the nonlinearities of RF transmitters accurately, especially in a mobile environment. The nonlinear characteristics of a PA often vary widely according to its average output power, as the heat dissipation will alter the chip temperature and hence the behavior of active devices. The variations are more significant in Class-B PAs than in Class-A PAs, owing to the dynamic nature of the Class-B operation and its ensuing severe nonlinearity. An adaptive treatment of the transmit-path distortions, such as the work described here, is therefore quite desirable from a practical standpoint as it obviates a meticulous modeling of the PA characteristics. In addition, when the adaptation is swift, the approach also provides an automatic tracking capability in time-varying operating environments, making it suitable for mobile applications.
1.2 Research Goals

The main goal of this research is to implement a linear and highly power-efficient RF transmitter with the assistance of adaptive digital equalization. The following are performed to achieve this goal:

- Designing a high-efficiency RF PA suitable for the digital equalization.
- Building the error model of Cartesian RF transmitters.
- Investigating the equalization algorithms and the adaptation schemes.
- Extracting the requirements of the system and its building blocks.
- Implementing the practical system and demonstrating its linearization performance and the consequent power efficiency enhancement.

A 5 GHz, direct-conversion RF transmitter with an on-chip 25 dBm, Class-B PA is targeted in a 0.13 μm CMOS process. A feedback path is also integrated in the same die to deliver the transmitter errors to the digital domains for the equalizer adaptation. With the support of a digital equalizer, not only is the power consumption minimized, but also the circuit complexity is relaxed in the integrated chip, satisfying the TX requirements. The main contribution of this work is that the equalized TX system is highly integrated in the chip and board levels, and no ideal block such as—ideal RX path in the test equipments, software implementation of equalization algorithm, etc.—is assumed.
The integrated chip (IC) is tested with the digital equalizer which uses a two-dimensional look-up table (2-D LUT) implemented in an FPGA. I/Q mismatch and memoryless nonlinearities of the transmitter including the baseband circuits (i.e., the DAC and LPF) and the RF blocks (i.e., the up-conversion mixer and PA) are uniformly treated in this prototype. All the issues affecting the compensation accuracy are properly dealt with in either the TX path, RX path or equalizer in an energy-efficient way.

1.3 Organization of Work

This dissertation is organized as follows:

Chapter 2 introduces the basic operation and the design procedure of an RF power amplifier with the simplest topology, and analyzes how the supplied power is delivered to the load while containing the input amplitude and phase information. In this process, the supplied power is not completely converted to the TX output power, and a significant portion of the supplied power is typically dissipated or radiated. Different PA topologies are investigated with a focus on their power efficiency, and the pros and cons of each PA topology are discussed. Trade-offs between the linearity and power efficiency are also covered in this chapter.

Since RF PAs have become the most critical block for high TX power efficiency, various TX architectures are being investigated and implemented,
accounting for the PA topologies in both industry and universities. Chapter 3 introduces different TX architectures and discusses their properties. Then, after the non-idealities of RF transmitters are described, the compensation techniques are introduced as well. Lastly, the digital equalization techniques are presented in more detail.

Chapter 4 presents a Cartesian TX system with adaptive digital equalization. After the behavioral MATLAB simulator is briefly explained, the detailed issues of this system are discussed. Based on the theory and the supporting behavioral simulation results, the solution of each issue is proposed. Whether the solution is put in TX path, RX path, or the equalizer depends on the circuit/system complexity and the effects on the TX power efficiency. Thus, in this chapter, the equalizer is designed and the design requirements of the TX and RX paths are derived. Lastly, the power control scheme and its effect on digital equalization are discussed.

Chapter 5 presents the integrated TX chip and its building blocks. A Class-B PA is designed to exploit its inherent bias adaption, thus improving the average power efficiency with the OFDM signal. The nonlinear characteristics of Class-B PAs are also suitable for digital equalization. Transmitting filters with variable cut-off frequency, building blocks with high linearity in the feedback path, and LO generation with high I/Q accuracy are presented. The issues regarding the PA integration with other small-signal blocks are also discussed.
Chapter 6 describes the measurement setup and shows the experimental results. PA output matching is designed on the board using the same stand-alone PA as the integrated PA, and Class-B PA performances are measured. Then, TX performances with and without the digital equalizer are measured and compared. The residue errors after the equalization are also analyzed. Chapter 7 summarizes the work and draws a brief conclusion.
This chapter first introduces the conventional Class-A/AB/B/C power amplifiers and their power efficiency characteristics. After the major non-idealities causing the signal distortion and spectrum corruption are introduced, the power loss mechanisms of RF PAs are analyzed. Comparison between Class-A and Class-B PAs shows the trade-off between the power efficiency and linearity. Lastly, various types of RF power amplifiers are introduced with a focus on the characteristics of their peak as well as average power efficiencies.

2.1 Class-A/AB/B/C RF PAs

Power amplifiers are traditionally classified by the conduction angle of the transconductance transistors [16]. As is well known, the conduction angle is the portion of an input sine-wave cycle during which the load current flows into the transistors. When the conduction angles are 360°, between 360° and 180°, 180°, and less than 180°, PAs are called Class-A, -AB, -B, and Class-C, respectively.
Figure 2.1 shows the schematic of a simplified RF power amplifier and its Class-A operation. Given the required maximum output power \( P_{\text{OUT, max}} \) and the supply voltage \( V_{DD} \), the load resistance \( R_L \) is calculated by

\[
R_L = \frac{V_{DD}^2}{2P_{\text{OUT, max}}}.
\]  

(2.1)

Once the load resistance is obtained, the matching network is inserted to transform the antenna impedance (typically 50 Ω) to \( R_L \). Other potential roles of the matching network are to filter the unwanted harmonics and to control the harmonic impedances at the drain node. Note that the harmonic impedances shape the drain voltage \( V_d \) and the proper shape of the drain voltage helps to reduce the...
power loss in the transconductance transistors and thus improve the power efficiency. Then, for the best power efficiency in Class-A PA, the gate bias ($V_{bias}$) of the transistor should be set as

$$V_{bias} = V_{th} + V_{i,AC,max},$$  \hspace{1cm} (2.2)

where $V_{i,AC,max}$ is the maximum AC amplitude of the input signal which is limited by either the supply voltage of the preceding stage or the gate-oxide breakdown voltage of the PA transistors. Lastly, the transistor size is chosen so that the drain current ($I_d$) for the maximum output power satisfies the following condition:

$$I_{d,AC,max} = I_{DC} = \frac{V_{DD}}{R_L}.$$  \hspace{1cm} (2.3)

Note that the transistors are assumed to be linear in this analysis for simplicity, and the analysis of the effects caused by the nonlinear transistors will follow in the next section.

With the smaller conduction angle, a portion of the drain current is clipped, which generates the harmonic components in the drain current as illustrated in Figure 2.2. Assuming that the impedances of the harmonic frequencies at the drain node are zero (the impedances are generally very low for GHz-range RF power amplifiers because of the large capacitive parasitics at the
drain node due to the bulky transistors), the harmonics are not translated to the drain voltages. Thus, the drain voltages in Figure 2.2 still stay the same in all cases. For the same maximum output power, the fundamental component of the drain current needs to be the same as the previous Class-A case with the smaller conduction angle, which requires Equations (2.2) and (2.3) to be modified although Equation (2.1) still holds. The same fundamental in the drain current can be accomplished by increasing the transistor size because the input signal cannot be further increased, as it is limited by the supply voltage of the preceding stage.

![Diagram of different PA classes](image)

Figure 2.2: Comparison of different PA classes.
Figure 2.2 also shows the efficiency improvement with the smaller conduction angle. Note that the load resistance, supply voltage, and output power are the same in all cases. Thus, the DC supplied power is proportional to the drain DC current, which is the same as the DC current from the supply. The higher efficiency of the smaller conduction angle is due to the fact that the DC current is smaller for the same fundamental as the conduction angle drops. From another point of view, the power loss in the transistor can be calculated by the product of the drain voltage and the drain current into the transistors. The average power loss of one cycle is the dissipated power in the transistors, and is smaller when PAs operate toward the Class-C condition as shown in Figure 2.2.

2.2 Power Efficiency and Linearity

2.2.1 Performance metrics

The PA power efficiency is parameterized either by drain efficiency (DE) defined as

\[ \eta_{DE} \equiv \frac{P_{OUT}}{P_{DC}} = \frac{V_{DD}}{V_{DD} I_{DC}} \]  \hspace{1cm} (2.4)

or by power-added efficiency (PAE) defined as
where $P_{OUT}$ is the PA output power, $P_{IN}$ is the PA input power, and $P_{DC}$ is the DC supplied power. Note that PAE is always less than DE, and is similar to DE when the power gain is high (>20 dB). When PAs are integrated and sophisticated linearization schemes are adopted, the DC power of the related circuits as well as the PA core circuits needs to be accounted for when referring to the power efficiency.

PAs used for constant envelope signals such as Gaussian minimum shift keying (GMSK) have relatively high drain efficiency (>50%) due to the relaxed linearity requirements. Switched-mode power amplifiers such as Class-E PAs are often used in this case. However, the high PAPR of non-constant envelope signals such as OFDM requires large power back-off to avoid signal clipping, which significantly degrades the power efficiency because the power efficiency typically drops with the output power. When the non-constant envelope signals with largely varying output power are transmitted, the average drain efficiency becomes more useful and is expressed as

$$
\eta_{DE,avg} = \int \eta_{DE}(P_{OUT}) \cdot PDF(P_{OUT}) \cdot dP_{OUT}.
$$

(2.6)
Signal probability density function (PDF) is used to calculate the average output power and the average DC supplied power. Figure 2.3 shows the typical efficiency curve against the power back-off and an example of the signal distribution. In addition to PAPR, the stringent linearity requirements further worsen the power efficiency by pushing designers to use linear, power-inefficient PAs and to introduce more back-off. This often results in PA average drain efficiency less than 10% for the standard OFDM signal.

The transmitter non-idealities are mainly characterized by the root-mean-square (RMS) error vector magnitude (EVM) and the TX output spectrum, which should satisfy the spectrum mask requirement enforced by Federal Communications Commission (FCC). EVM quantifies the constellation error and stands for the distance between the desired and actual signal vector, normalized by the signal amplitude as illustrated in Figure 2.4 (a). The RMS EVM is defined

![Figure 2.3: Typical PA drain efficiency curve and signal distribution.](image-url)
by

\[
EVM_{\text{RMS}} = \sqrt{\frac{\sum |Error|^2}{\sum |Signal|^2}}.
\] (2.7)

Figure 2.4 (b) shows the example of an RF output spectrum and the spectrum mask for 802.11a wireless local area network (WLAN). While EVM mostly concerns in-band signal distortion, the spectrum mask addresses the out-of-band spectral regrowth caused by transmitter non-idealities, e.g., transmitted nonlinearity, I/Q mismatch, etc. Adjacent channel power ratio (ACPR) is defined
as the ratio of the power in a desired channel to the power in the upper or lower adjacent channel, thus giving a number which represents the degree of the spectrum regrowth.

### 2.2.2 AM/AM and AM/PM of RF PAs

For narrowband signals, PA nonlinearities can be modeled as memoryless amplitude-to-amplitude (AM/AM) and amplitude-to-phase (AM/PM) distortion [17]. AM/AM distortion, which mainly depends on the bias voltage and the nonlinear transconductance of the transistors, causes the instantaneous output amplitude or envelope to differ in shape from the corresponding input. AM/PM distortion, which is often associated with the voltage-dependent capacitance of the transistors, causes the amplitude-dependent phase shift. AM/AM and AM/PM are illustrated with the time domain RF signal in Figure 2.5 (a). This example shows the large gain drop and the relative phase shift when the signal amplitude is large. Their impacts on the baseband I/Q plane are rotationally symmetric as shown in Figure 2.5 (b). The RF signal with the AM/AM and AM/PM distortion can be written as

\[
S_{RF_{OUT}}(t) = F[r(t)] \cdot \cos[\sigma_c t + \theta(i) + G[r(t)]]
\]  

(2.8)
where \( r(t) \) and \( \theta(t) \) are radius and angle of the modulated signal, and \( F[\cdot] \) and \( G[\cdot] \) represent AM/AM and AM/PM distortion functions, respectively. Assuming ideal down-conversion, the distorted RF signal is converted to the baseband I/Q signals as

\[
I(t) = F[r(t)] \cdot \cos[\theta(t) + G[r(t)]] ,
\]

(2.9 a)

Figure 2.5: PA nonlinearities: (a) time domain illustration of AM/AM and AM/PM, and (b) their effects on baseband complex signal plane.
\[ Q(t) = F\{r(t)\} \cdot \sin[\theta(t) + G[r(t)]] \quad (2.9\, b) \]

### 2.3 Analysis of Power Loss in RF PAs

Power loss in RF PAs occurs

- in transistors used as the transconductance devices or switches,
- in passive devices including the parasitics and lossy substrate, and
- at harmonic frequencies.

In Section 2.1, the power loss in PA transistors at the maximum output power is analyzed using the current and voltage waveforms. Two more sources of power loss are analyzed in this section in detail. In Figure 2.6, the maximum power efficiency \( \eta_{\text{max}} \) is limited by the three sources listed above, and the power efficiency additionally drops with the power back-off, as exemplified by \( \eta_i \). After

![Figure 2.6: Power efficiency versus back-off.](image)

23
the ways to improve the maximum power efficiency are examined, the power efficiency at back-off is analyzed. Lastly, how to improve the average power efficiency is also explored.

2.3.1 Power loss in the passive devices

In RF power amplifiers, passive devices such as capacitors and inductors are generally used in the inter-stage and output matching networks. In standard CMOS process, the quality (Q) factors of on-chip inductors are especially low, typically 8 to 15, due to the series metal resistance and induced currents in lossy substrate. Figure 2.7 shows an $L$-type low-pass matching network which transforms the antenna impedance, $R_{ANT}$ (typically 50 Ω), to the desired resistance at the PA output nodes, $R_L$, which is typically smaller than $R_{ANT}$. When the quality factor of the inductor is $Q_L$ at the frequency $\omega$,

![Figure 2.7: Model of an $L$-matching network with lossy inductor.](image)
\[ Q_L = \frac{\sigma a L_M}{R_{ind}}, \]  

(2.10)

\( R_{ind} \) includes the loss due to both the induced current in the substrate and the metal resistance. At the maximum output condition, the efficiency (\( \eta_{MN} \)) of the matching network can be calculated as

\[
\eta_{MN} = \frac{Q_L^2 V_{DD}^2 + R_{ANT} P_{PA} - \sqrt{R_{ANT}^2 P_{PA}^2 + 2R_{ANT} Q_L^2 V_{DD}^2 P_{PA} - Q_L^2 V_{DD}^4}}{V_{DD}^2 (Q_L^2 + 1)},
\]  

(2.11)

where \( P_{PA} \) and \( V_{DD} \) are the PA output power before the matching network and the supply voltage, respectively. As shown in Figure 2.8, the power loss in the matching network is severe at high output power and low supply voltage as well as at low Q-factor of the inductor. Intuitively speaking, low supply voltage for the same output power causes the large ratio of the impedance transformation, and thus higher current flows into the matching network, increasing the power loss in \( R_{ind} \). In this analysis, \( R_L \) is first obtained using Equation (2.1) and \( R_{ind} \) is absorbed in \( R_L \). In other words, the lossless matching network consisting of \( L_M \) and \( C_M \) transforms 50 \( \Omega \) to \( R_L-R_{ind} \). Note that using a smaller \( L_M \) may improve the efficiency of the matching network although the transformed impedance is not optimal. However, this can introduce the non-zero reactive part after the
impedance transformation and may increase the power loss in transconductance transistors due to the misalignment of the drain voltage and current waveforms.

The parasitic capacitance, inductance, and resistance more or less exist everywhere, on- and off-chip. An important source of the power loss in PAs regarding the parasitic passives is the on-chip distributed $R$-$C$ networks originating from interconnect metals, contacts, substrate, junctions in transistors, etc. To obtain insight into the power loss mechanism through the parasitics, it is first assumed that each node in the PA has one or multiple series $R$-$C$ parasitics as shown in Figure 2.9, where $C_p$ and $R_p$ are the lumped parasitic capacitance and
resistance, respectively. When the node voltage is $V_1$, the power loss at $R_p$ is expressed as

$$P_{\text{LOSS} @ R_p} = \frac{V_1^2}{2} \frac{(\sigma C_p)^2 R_p}{(\sigma C_p R_p)^2 + 1}$$  \hspace{1cm} (2.12)$$

Although this mechanism happens for all of the on-chip nodes, the power losses at the output nodes are dominant because the voltage swing ($V_i$) is the maximum and $C_p$ is typically large due to the bulky transistors. The graphs in Figure 2.9
show the power loss against the parasitic resistance with different parasitic capacitances, when $V_1$ is 2.5 V and the frequency is 5 GHz. A few important facts are observed in the graphs. First, the parasitic resistance needs to be either very small ($< 1 \, \Omega$) or very large ($> 500 \, \Omega$, not covered in the graphs). Intuitively, zero $R_P$ means the network is purely capacitive and thus lossless, and infinite $R_P$ means no current through the $R-C$ path due to the infinite impedance. Since it is difficult to implement such a large $R_P$ in practice, it is important to guarantee very small $R_P$. The second observation is that the parasitic capacitance ($C_P$) needs to be as small as possible. Large devices inevitably create large $C_P$ due to the drain-substrate junction capacitance. In this sense, PAs operating in the small conduction angle exhibit higher power loss through this mechanism because the large device is necessary for the same output power, as explained in the Section 2.1.

Lastly, the parasitic metal resistance of the main current path from the power supply to the ground also needs to be minimized in layout. When the parasitic resistance is $R_m$, the power loss is calculated as

$$P_{\text{LOSS @ } R_m} = I_{d, \text{DC}}^2 R_m + \frac{1}{2} I_{d, \text{AC}}^2 R_m.$$  

(2.13)
2.3.2 Improvement of the maximum power efficiency: Class-D and Class-F PAs

While the power loss in passive devices is mostly determined by the device and fabrication parameters, that in transistors is much more dependent on the PA topologies and input signals. As presented in Section 2.1, by reducing the transistor conduction angle from Class-A to Class-B, we can reduce the power loss in transistors by more than half. However, since large transistor size increases the power loss through the parasitic passives, reducing the conduction angle below 180° is not always desirable. The better way is probably to modify the waveforms so that the multiplication of the drain current and the drain voltage, which is the power loss in transistors, is minimized. Figure 2.10 shows three cases in which no energy is dissipated in transistors. Note that the impedances at harmonic frequencies need to be carefully designed to realize the waveform pairs. To simplify the analysis, lossless matching network and no parasitics are assumed throughout this section.

In the case of Figure 2.10(a), both drain current and voltage have finite odd harmonics, which implies finite load resistance at the corresponding harmonic frequencies. This causes the power loss at harmonic frequencies, reducing the maximum power efficiency to 81%. On the other hand, no power is lost at harmonic frequencies with the waveform pairs of Figure 2.10 (b) and (c) because half sine wave contains only the even-order harmonics while the
rectangular wave contains only the odd-order harmonics, meaning that the impedances at harmonic frequencies should be either zero or infinite. The power amplifiers exhibiting the waveforms of the case (b) are especially called Class-D, and they become Class-F when the drain voltage contains only the third-order harmonic [16]. Note that the current waveform of Class-D (or Class-F) is the same as that of Class-B. Thus, resistances at the odd harmonics need to be infinite to approximate the rectangular voltage waveforms at the drain nodes. Switches instead of transconductance transistors can also be used to generate similar waveforms, which will be explained in Section 2.4 in detail.

Figure 2.10: Examples of the waveform pair for no power loss in the transconductance transistors.
2.3.3 Power efficiency at back-off

Since modern communication standards adapt the non-constant envelope signal with high PAPR, the average power efficiency depends on the power efficiency at back-off as well as the peak power efficiency. However, the efficiency typically drops as the output power decreases because the circuit parameters are optimized at the saturated output power and are hard to change according to the output power in many PA topologies. For example, for Class-A PAs, the efficiency linearly drops with the output power because the DC supplied power in Equation (2.4) is always constant in different output powers as long as the circuit parameters and biases do not change. Thus,

\[
\eta(\text{Class } A) = \eta_{\text{max}} \frac{P_{\text{OUT}}}{P_{\text{OUT,max}}}. \tag{2.14}
\]

For Class-B PAs, on the other hand, the efficiency drops at back-off, but its slope is less steep compared to Class-A PAs. This happens because the DC supplied current is proportional to the output power when the conduction angle is half, while the supply voltage is still constant.

\[
\eta(\text{Class } B) = \eta_{\text{max}} \sqrt{\frac{P_{\text{OUT}}}{P_{\text{OUT,max}}}}. \tag{2.15}
\]
Figure 2.11 summarizes the power efficiency of different PA classes. Transconductance transistors with half conduction angle are assumed for Class-D and Class-F cases. Also note that the x-axis is linearly scaled to illustrate the difference more intuitively. Although PAs with smaller-than-half conduction angle have better shaped efficiency curves, they are generally impractical for hundreds of mW output power because the transistor size and the corresponding overhead of parasitic capacitance become too large to be used at GHz band.

One way to maintain the maximum power efficiency even at back-off is to adapt the supply voltage according to the output power. For example, since 6 dB power back-off allows the output signal swing to be reduced by half given the load resistance, there also is room to reduce the supply voltage by half. Thus, the
supply adaptation in conjunction with the Class-B bias can reduce the DC supplied power proportionally to the output power, keeping the maximum power efficiency at back-off. Table 2.1 summarizes this scenario showing that all currents and voltages are scaled by half and both the DC supplied power and the output power are scaled by the same number. However, this requires an additional expensive block in the power supply path such as DC-DC converter; not only should this block have high power efficiency, but its bandwidth should also be large enough to follow the signal. This technique is called bias adaptation or envelope tracking and will be discussed in the next chapter in more detail [16].

### 2.3.4 Example: Trade-offs between power efficiency and linearity

Figure 2.12 (c) and (d) compare the power gains and the efficiency curves of two PAs, respectively. A Class-A or -AB PA is biased in the linear region of the transconductance curve while a Class-B PA is biased near the transistor

<table>
<thead>
<tr>
<th>$I_{d,DC}$</th>
<th>$I_{d,AC}$</th>
<th>$V_{DD}$</th>
<th>$V_{d,AC}$</th>
<th>$R_L$</th>
<th>$P_{DC}$</th>
<th>$P_{OUT}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1/2</td>
<td>1/2</td>
<td>1/2</td>
<td>1/2</td>
<td>1</td>
<td>1/4</td>
<td>1/4</td>
</tr>
</tbody>
</table>
threshold where the transconductance is typically very nonlinear as illustrated in (b). This results in the nonlinear power gain (AM/AM) in the Class-B PA in the low power region in contrast to the Class-A PA. Although the Class-B PA also has the linear region in the gain curve as shown in Figure 2.12 (c), the dynamic range is typically too limited to transmit the standard OFDM signal. In addition, the amplitude-oriented phase distortion (AM/PM) is also severe in Class-B PAs due to their dynamic nature. Thus, PAs need to be biased near the Class-A operating point to achieve sufficient linearity for transmission of the non-constant envelope signal.

However, the peak power efficiency of Class-A PAs is inferior to that of Class-B PAs, and more importantly, the average power efficiency of a Class-A PA is severely degraded due to the large back-off when transmitting the signal with high PAPR, as presented in the last section. This trade-off motivates a linearization technique to be used with the Class-B PA in modern communication standards. Moreover, a successful linearization in the saturated power region will result in less back-off, and thus further improve the power efficiency of the transmitter.
Figure 2.12: Comparison between Class-A and Class-B RF PAs: (a) simplified PA circuit schematic, (b) operating points of the power transistors, (c) output power, and (d) drain efficiency.
2.4 Switched PAs

Ideal switches do not dissipate any power because either the current through the switch or the voltage across it is zero. This motivates use of the transistors as switches instead of transconductance devices in RF PAs. However, ideal switches can transfer only the phase information of an RF signal and block the amplitude information from being transferred. Thus, PAs using switches are generally used for amplifying the constant envelope signals, and there typically needs to be an additional path to deliver the amplitude information in order to use it for the non-constant envelope signals.

The current waveforms of Figure 2.10 (a) and (c) can be obtained by replacing the transconductance transistors of the conventional PAs in Figure 2.1 with switch transistors and properly controlling the output impedances at harmonic frequencies. An example to compose the waveforms of Figure 2.10 (c) is shown in Figure 2.13(a), where the impedances at harmonic frequencies are low by the ideal parallel L-C tank resonating at the fundamental frequency. Note that the matching network for the impedance transformation is not shown for simplicity. The harmonic currents from the switch are absorbed into the tank and not delivered to the load. On the other hand, the waveforms of Figure 2.10 (b) can be made by employing the normal transconductance transistors as explained in Section 2.3.2. However, it is difficult to accurately manage the impedances at harmonic frequencies to form the desired voltage waveform in this case. An
alternative way is shown in Figure 2.13 (b), where two switches and a bypass capacitor form the rectangular voltage waveform at the drain nodes and the current of each switch is a half sine wave due to the series L-C network resonating at the fundamental frequency on the output current path [18]. The harmonic contents of the drain voltage are filtered by the series L-C network.

The major drawback of switching PAs is that the transitions in either voltage or current waveform are too steep to be implemented in practice. Finite slopes introduce the region where both voltage and current are not zero, which causes the power dissipation in the switches. The fact that the sufficient condition for no power dissipation in transistors is that either voltage or current needs to be

![Figure 2.13](image-url)

Figure 2.13: Simplified schematics of (a) tuned RF switching amplifier and (b) Class-D switching amplifier.
zero in an instant gives a lot more possible waveform pairs than those in Figure 2.10. A good example is the Class-E PA [19]-[24], of which Figure 2.14 shows a typical topology. The series inductance, $L_E$, and the shunt capacitance, $C_E$, are chosen to satisfy the following Class-E operating conditions:

- The drain voltage is zero at the switching instants, and
- The first derivative of the drain voltage is zero when the switch turns on.

While the first condition minimizes the power dissipation by the stored charges in the shunt capacitor at turn-on, the second helps the circuit to be less sensitive to variations of frequency and the switching instants.

The output power of a Class-E PAs is

$$P_{OUT} = \alpha \frac{V_{DD}^2}{R_L},$$

where $\alpha$ is a constant set by Class-E topologies. Equation (2.16) shows that Class-E PAs can be used for non-constant envelope signals by modulating the amplitude information to the supply. The power efficiency at back-off is ideally sustained at 100% in this case. Thus, Class-E PAs are often used in polar transmitters and envelope elimination and restoration (EER) systems, which will be introduced in Chapter 3.
Figures 2.14 and 2.15 show the simplified schematics of a Class-E PA with a shunt capacitance load and an even-harmonic resonance load, respectively. Note that the impedance transformation network is not shown in the diagram. The design equations are also shown in the figure for the case that the conduction

\[
R_L = 0.58 \frac{V_{DD}^2}{P_{OUT}}
\]

\[
L_E = 1.15 \frac{R_L}{\omega}
\]

\[
C_E = 0.18 \frac{1}{R_L \omega}
\]

Figure 2.14: Class-E PA with shunt capacitance load.

Figures 2.14 and 2.15 show the simplified schematics of a Class-E PA with a shunt capacitance load and an even-harmonic resonance load, respectively. Note that the impedance transformation network is not shown in the diagram. The design equations are also shown in the figure for the case that the conduction

\[
R_L = 0.056 \frac{V_{DD}^2}{P_{OUT}}
\]

\[
L_E = 3.53 \frac{R_L}{\omega}
\]

\[
C_E = 0.071 \frac{1}{R_L \omega}
\]

\[
C_X = 0.23 \frac{1}{R_L \omega}
\]

Figure 2.15: Class-E PA with even-harmonic resonance load.
angle is 180°. Although the topology of Figure 2.14 is the simplest and most conventional architecture, it requires a bulky DC feed circuit such as an RF choke (RFC). On the other hand, the RF choke is replaced by a small inductance in the topology of Figure 2.15. Also note that it is often avoided to use the large ratio of impedance transformation because the large ratio increases the power loss in the matching network due to the large AC current.

Figure 2.16 shows the simplified schematic of a Class-E PA with parallel-circuit load and its design equations. The small ratio of the impedance transformation in this topology reduces the power loss in the output matching network; however, this may result in insufficient harmonic suppression. In addition, the small inductance instead of RF choke allows the fundamental current through it, causing the non-negligible power loss at the fundamental instead of DC.
The main sources of the power loss in Class-E PAs are lossy inductors in output matching networks and on-resistances of the switches. The aggregated power loss highly depends on the maximum output power and the operating frequencies. Thus, the proper load needs to be chosen according to the design and process parameters, such as the quality factors of inductances, and the transition frequency ($f_t$), output capacitances, and breakdown voltages of switch transistors.

2.5 Multi-Path RF PAs

Power amplifiers using the supply modulation, such as EER and envelope tracking PAs, require two signal paths since the amplitude information is modulated in the power supply while the phase information is transferred through the switch controls. In EER, the constant-envelope RF signal with only the phase information controls the switches. On the other hand, both phase and amplitude information is fed into the gate of the transconductance transistors in envelope tracking PAs. However, wideband DC-DC converters with high power efficiency are necessary for supply modulation, but are not readily available in CMOS process as mentioned earlier. Digitally switched multiple supplies are sometimes used to avoid the use of costly DC-DC converters, although the efficiency improvement in transistors is less due to the discrete nature of these supplies and thus their imperfect envelope tracking capability.
Modulating the load resistance instead of the power supply can also keep the maximum power efficiency at back-off, as Table 2.2 shows for an example at 6 dB back-off. This technique is called *load modulation*. For example, a *Doherty* amplifier exploits the fact that the impedance looking into one node of the identical device can be changed by inserting another current path or controlling the voltage of different nodes [25]-[26]. The well-known Miller effect in analog circuits is a good example of this impedance change. The basic principle to change the load resistance in Doherty amplifiers is to introduce another current path as shown in Figure 2.17, where the load modulation occurs when the auxiliary amplifier turns on (when the output power is $P_{\text{max}}-6\text{dB}$ in this example). When the current $I_2$ is nonzero, the impedance looking from the other path increases and thus the load resistance of the main amplifier accordingly decreases by the action of the quarter-wave transmission line. This allows the higher current $I_1$ while not increasing the drain voltage $V_{\text{d}}$, maintaining the peak power efficiency. Currents $I_1$ and $I_2$ from the main and auxiliary amplifiers and the load

<table>
<thead>
<tr>
<th>$I_{d,\text{DC}}$</th>
<th>$I_{d,\text{AC}}$</th>
<th>$V_{\text{DD}}$</th>
<th>$V_{d,\text{AC}}$</th>
<th>$R_L$</th>
<th>$P_{\text{DC}}$</th>
<th>$P_{\text{OUT}}$</th>
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<tbody>
<tr>
<td>$\frac{1}{4}$</td>
<td>$\frac{1}{4}$</td>
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<td>1</td>
<td>4</td>
<td>$\frac{1}{4}$</td>
<td>$\frac{1}{4}$</td>
</tr>
</tbody>
</table>

Table 2.2: Example of improving the power efficiency at 6 dB back-off (load modulation).
resistance, $R_L$, need to be properly designed to satisfy the operating conditions. Although the power efficiency of the main amplifier stays at peak when the output power is higher than 6 dB back-off, that of the auxiliary amplifier is lower than its peak efficiency, which causes a small dip between the two peak efficiencies. Thus, PAs with high power efficiency such as Class-C are often used as auxiliary amplifiers. A passive impedance inverter as shown in Figure 2.18 can replace the bulky quarter-wave transmission line, facilitating integration at low gigahertz frequencies [27].
Another well-known technique categorized in multi-path PAs is *outphasing* amplifiers, which decompose the non-constant envelope signal into two constant envelope signals, amplify them using two identical switched PAs, and combine the two amplified signals to restore the original signal [28]-[29]. The basic concept is illustrated in Figure 2.19, where the equivalent baseband complex expressions of two signals are

\[ V_1 = \frac{V_{O,\text{peak}}}{2} (\sin \theta - j \cos \theta), \quad \text{(2.17 a)} \]

\[ V_2 = \frac{V_{O,\text{peak}}}{2} (-\sin \theta - j \cos \theta), \quad \text{(2.17 b)} \]

respectively. Then the output voltage is
\[ V_O = V_1 - V_2 = V_{O,\text{peak}} \sin \theta, \quad (2.18 \text{ a}) \]

\[ \theta = \arcsin \left( \frac{V_O}{V_{O,\text{peak}}} \right). \quad (2.18 \text{ b}) \]

The amplitude information, \(V_O\), is temporarily carried on the phase \(\theta\) by the signal component separator (SCS) before the amplifying stage.

A Wilkinson power combiner shown in Figure 2.20 can be used as a power combiner. Although the maximum power efficiency is high by using the switched PAs, the power efficiency at back-off has similar characteristics to that of Class-A PAs because each PA’s output power is always maximal and the extra power at back-off is just dissipated in the power combiner with the Wilkinson power combiner. A lossless power combiner such as Chireix, shown in Figure 2.21, can be used to avoid the power loss at back-off; however, the lack of isolation between two paths causes impedance mismatch at the PA outputs in this

![Figure 2.20: Wilkinson power combiner.](image-url)
case. In this implementation, \( I_5 \) and \( I_6 \) are expressed as follows for the same output expression (Equation 2.18 (a)) as the previous Wilkinson implementation.

\[
I_5 = \frac{I_{O,\text{peak}}}{2} \left( \sin \theta - j \cos \theta \right), \tag{2.19 a}
\]

\[
I_6 = \frac{I_{O,\text{peak}}}{2} \left( \sin \theta + j \cos \theta \right), \tag{2.19 b}
\]

Figure 2.21: Chireix-outphasing system using two stubs.
CHAPTER 3

LINEARIZED RF TRANSMITTERS

Following the introduction of various PA topologies and their power efficiency/linearity analysis in the last chapter, this chapter opens with a variety of TX architectures regarding the employed PA topologies. The pros and cons of the architectures are also discussed considering the implementation issues. Next, the techniques to linearize the TX path including the PA and their limitations are presented. Among the linearization techniques, the digital equalization schemes and related issues are investigated in more detail.

3.1 RF TX Topologies

The basic functions of RF transmitters are digital-to-analog conversion, frequency up-conversion/modulation, and power amplification. Different architectures employing various PAs to transmit non-constant envelop signals with high PAPR are being investigated and implemented to improve the transmitter power efficiency as introduced in this section.
3.1.1 Cartesian

The Cartesian transmitter, which is the most traditional architecture, can universally transmit constant and non-constant envelope signals. Figure 3.1 shows an example of this architecture. It has fewer matching issues because two paths are identical and thus the implementation is relatively easy. The quadrature modulator up-converts the baseband signals to radio frequency and modulates the complex signals to the real signals at the same time. When the LO frequency is the same as the carrier frequency and one modulator is used for the up-conversion, this architecture is referred to as direct conversion.

To avoid the well-known drawbacks, e.g., LO feedthrough, LO pulling, etc., of the direct conversion architectures, the frequency up-conversion is

Figure 3.1: Cartesian direct-conversion RF transmitter.
sometimes performed in two steps: the baseband signal is first up-converted to the intermediate frequency (IF), and then up-converted to the RF frequency. Since the two-step up-conversion makes LO frequencies different from the carrier frequency, the LO feedthrough is located outside the signal band at TX output and thus can be filtered in the RF domain. The first up-conversion can also be done in the digital domain to circumvent the need for two LO frequencies. IF is often very low in this case to relieve the speed of digital-to-analog conversion.

Instead of using two-step up-conversion, LO feedthrough can be locally calibrated in the direct-conversion architecture by controlling the DC bias current in the mixer quad so that the DC offset is compensated [30]. The voltage-controlled oscillator (VCO) can also operate at a different frequency from the carrier frequency and create the carrier frequency using dividers and mixers to avoid pulling effects from any of the transmitters on the VCO [30].

In order to achieve the required linearity, Class-AB PAs are dominantly used in this architecture when they are integrated in the transmitter chips. Doherty amplifiers have been investigated recently to replace the inefficient Class-AB PAs. Adaptive supply bias (or envelope tracking technique) is also widely researched as discussed in the next section in more detail.
3.1.2 Envelope tracking (ET) / EER / polar

The linear PAs used in Cartesian transmitters can adopt the envelope tracking capability to improve the power efficiency. Switched PAs, typically Class-E PAs, can replace the linear PAs with the amplitude information of the switch control inputs being eliminated using the limiters. The limiter is necessary because the performance of the switched PAs is not optimal when the switch operation is imperfect because the amplitude-varying input signals degrade the power efficiency. Since the signal’s envelope is restored at the PA output, this technique is called envelope elimination and restoration (EER) [31]. Figure 3.2 (a) and (b) show the diagrams of envelope tracking (ET) and EER, respectively. An envelope detector extracts the amplitude information of the modulated RF signals and a DC-DC converter modulates it on the supply of a Class-E PA in these examples.

However, the lack of wideband DC-DC converters with high power efficiency in CMOS process undermines the advantages of the bias adaptation in ET or the supply modulation in EER. The mismatch of the two non-identical paths, the RF path and the baseband (amplitude) path, is another major concern; although the delay can be adjusted in the factory after the fabrication, the variations make it difficult to combine two paths accurately. In addition, the change of the supply according to the amplitude causes large signal-dependant capacitance at the drain nodes, resulting in large AM/PM. Class-B RF PAs are
often used for the (ideally) 100% power efficiency with the ET technique; however, their AM/AM and AM/PM distortion is known to be unacceptable in practical CMOS process.

The amplitude information can be directly provided from “digital” using a DAC instead of extracting it from the RF signal, and the phase information is transmitted on a separate path, which is called a polar transmitter [32]-[36]. The

Figure 3.2: (a) Envelope tracking (ET) and (b) envelope elimination and restoration (EER).
recent availability of extremely low power analog-to-digital interfaces has accelerated the use of this approach. By doing this, the (adaptive) compensation of the delay mismatch is more convenient in the digital domain. Figure 3.3 shows an example of this approach, where the envelope elimination is also done in the digital signal processing (DSP) and thus the limiter is removed. In this way, the below path is only for the phase modulation and frequency up-conversion. A similar approach is also possible in the ET case by using the normal complex signals and linear PAs [37].

In the case of EER, there are several different ways to implement the phase modulation path; e.g., the phase modulation can be done in the digital domain using a direct digital frequency synthesizer (DDFS) and the frequency up-
conversion is performed by one mixer as show in Figure 3.4 (a), minimizing the analog/RF complexity. One disadvantage of eliminating the amplitude information in the baseband is that the bandwidth of the phase-modulated signal is much wider than that of the baseband signals in Cartesian transmitters, which will create some overhead in the baseband analog circuits such as DAC or the reconstruction filters. Another example of phase modulation is shown in Figure 3.4 (b), where the VCO in the PLL directly produces the phase modulated RF signals, instead of using the mixer, utilizing the fact that the signal has the constant envelope. The phase information is modulated using a ΣΔ modulator in the PLL feedback path in this example. The out-of-band spurious tone is attenuated by the low-pass nature of the PLL loop, relaxing the band-pass requirements at the PA output, while the mixer approach generates lots of spurious tones at the harmonic frequencies.
3.1.3 LINC

Cartesian transmitters can be modified to employ the outphasing PAs introduced in the last chapter. According to the location of the signal component separator (SCS), several different TX topologies can be obtained as shown in Figure 3.5 [38]. Since IF as well as RF SCSs are not power efficient in the current technology, this function has typically been performed in the baseband frequency. The selection of the digital or analog SCS is determined by comparing the power consumption of the analog SCS with that of DACs; four DACs are necessary when the signal separation is done in the digital, while two DACs and analog SCS are necessary when it is done in the analog domain. An alternative proposed in the literature is to use a digital phase rotator, which receives the phase modulated
signal and rotates it according to the amplitude information as illustrated in Figure 3.5 (c) [39].

Figure 3.5: LINC RF transmitter using (a) analog signal component separator (SCS), (b) digital SCS, and (c) digital phase rotator (DPR) for the amplitude modulation.
There are two RF paths that need to be matched; although the two are identical, the high frequency of RF signals can generate significant mismatch. Note that there is only one RF path in Cartesian transmitters. The efficient power combining is another issue in this technique.

### 3.2 Linearization of Cartesian Transmitters

For PA linearization, baseband signal treatment has been heavily investigated recently in order to exploit the narrowband nature of wireless communication standards since it enables an efficient baseband model of the RF signal distortion. Although RF feed-forward can deal with very wideband signal, not only does it suffer from lack of compensation accuracy due to the high sensitivity to variations when treating signals in the GHz band, but also the additional RF circuits are typically power-hungry.

The whole transmitter system needs to be accounted for when equalizing the PA in the baseband domain. Naturally, analog/RF impairments in the TX path (before the PA) are together considered to be equalized with minimal effort. Among various TX topologies discussed in the last section, we focus on Cartesian transmitters in this section.
3.2.1 Baseband linearization

Since baseband compensation techniques correct the instantaneous output power and the phase of the fundamental tone, they can compensate only for in-band distortions; the spurious tones at RF harmonic frequencies are not cancelled since it does not correct the voltage transfer curve of the RF path.

Figure 3.6 shows (a) a TX path with a nonlinear RF PA and (b) a TX path with a linear RF PA and the baseband-equivalent nonlinear amplifier which models the AM/AM distortion of the RF PA. By comparing the two TXs, we can readily see that the envelopes of the RF output are the same although the RF waveforms are not. In the frequency domain, the in-band spectra are the same. For example, if the baseband input signal is $2 \cos(\omega_c t)$ and the PA transfer function is $a_i S_i + a_3 S_i^3$, then the PA AM/AM function is $a_i S_i + \frac{3}{4} a_3 S_i^3$. Both TX outputs have the same in-band frequency components at the frequencies of $\omega_c - 3 \omega_i$, $\omega_c - \omega_i$, $\omega_c + \omega_i$, and $\omega_c + 3 \omega_i$, whose amplitudes are $\frac{2}{4} a_i$, $a_i + \frac{3}{4} a_3$, $a_i + \frac{3}{4} a_3$, and $\frac{9}{4} a_3$, respectively. However, the spectra at the harmonic frequencies are not the same; the TX with the baseband AM/AM model and the linear RF PA does not have the spectrum components at RF harmonic frequencies, while the TX with the nonlinear RF PA does. Thus, after the in-band distortion is compensated by treating the baseband signals, the residue RF harmonics are typically attenuated by the filtering effect at the PA output and/or RF band-pass filters after the PA.
Figure 3.6: Transmit path with (a) a nonlinear RF PA and (b) its baseband AM/AM model and the linear RF PA.
3.2.2 RF feed-forward

The most common architecture of RF feed-forward linearization is shown in Figure 3.7 (a) [40]. Since there is no feedback in this technique, it guarantees unconditional stability and can handle very wide bandwidth signals. However, its power efficiency improvement is not so high because it needs an extra RF amplifier and requires precise delay and signal cancellation in the RF domain. In addition, its open-loop property makes the performance very susceptible to process and temperature variations. For these reasons, its applications are usually limited to static operation conditions, e.g., basestation PAs, and to signals with large bandwidth which is hard to handle with adaptive techniques using the

Figure 3.7: (a) RF feed-forward linearization and (b) coarse linearization of Class-AB PA by turning on the auxiliary Class-B PA in the saturated output power.
feedback loop. A similar approach is reported in [41] where an auxiliary Class-B PA is used in parallel with a Class-AB PA in order to compensate the power drop of the Class-AB PA near the power saturation as shown in Figure 3.7 (b).

### 3.2.3 Cartesian feedback

Cartesian feedback shown in Figure 3.8 performs linearization in the baseband domain by using the complex envelope of the RF signal as the feedback parameter [42]-[44]. The feedback system is inherently adaptive and can compensate for the large amount of distortion as long as the loop gain is high. The critical issue of Cartesian feedback is the system stability, which is common in analog feedback systems. With relatively large bandwidth signals, loop gain

![Cartesian feedback loop](image)

Figure 3.8: RF transmitter linearized by a Cartesian feedback loop.
should be reduced to guarantee the system stability, which limits the compensation performance.

In addition, the stability is sensitive to the phase misalignment between LO signals of an up-conversion and a down-conversion mixer since it couples the transmitting I-signal to the feedback Q-signal as shown in the red trajectory in Figure 3.8. This is effectively the cascade of the single loop, which doubles the phase response of the loop gain and thus significantly degrades the phase margin. The increased loop delay additionally worsens the system stability.

### 3.2.4 Digital equalization

Digital equalization, shown in Figure 3.9, uses digital signal processing (DSP)
instead of analog techniques [45]-[46]. The slow adaptation of DSP enables the system to be less susceptible to stability problems; thus, it can compensate a baseband signal that encompasses a much broader spectrum than what can be treated by Cartesian feedback. As CMOS technology scaling continues, it is becoming more attractive since this approach benefits from a mostly digital implementation. A side benefit of baseband digital compensation is that some nonlinearities of the transmit path other than the PA are also treated. This fact can be exploited to relax the design specs of the blocks such as DAC and transmitting filters. Different equalization and adaptation methods can be applied according to the distortion models. In general, the compensation accuracy increases while the convergence time is longer when more parameters are used. For example, an equalizer using look-up tables (LUTs) which have more parameters than an equalizer using polynomial functions typically has better compensation accuracy, but longer convergence time. The following section explores the nonidealities of the Cartesian transmitters and presents various equalization schemes to compensate them.
3.3 Digital Equalization Schemes

The errors in the TX chain can be categorized by either the memoryless errors or the memory errors depending on whether the current erroneous output is a function of only the current instantaneous input or the previous inputs as well. Thus, the equalization schemes for memoryless errors are generally much simpler than those for memory errors. Although it is known that Volterra series can model and thus compensate the nonlinear errors with the memory, its implementation cost is very high. Therefore, models using simplified Volterra series have been investigated.

Frequency-dependent error is one of the dominant memory errors; however, the resulting signal errors can be easily equalized in the receiver for multi-carrier signals such as OFDM, and they do not cause spectrum regrowth in typical transmitters. It is also reported that RF PAs can have some memory errors when the on-chip heat caused by the high output power and less-than-perfect power efficiency does not properly flow out or the bias circuits are not suitably terminated. In this work, we rule out the compensation of the memory errors because we believe it is still cheaper to treat them in the analog/RF circuit domain than by digital equalization.
The memoryless amplitude and phase errors of an RF PA are mostly amplitude-oriented [16]; thus, a complex polynomial or an amplitude-addressed, one-dimensional LUT with complex coefficients is sufficient for the compensation. In contrast, an extended treatment of the entire transmit path, including DAC, LPF, and mixer, necessitates an I- and Q-addressed, or two-dimensional, LUT. The dominant memoryless error mechanisms of a typical RF transmission process and the ensuing distortions of the baseband I/Q plane are illustrated in Figure 3.10 and explained as follows.

- The nonlinear transconductance of the PA input transistors under large-signal excitation causes the envelope of the RF output waveform to differ from the corresponding baseband input, which is known as the AM-AM effect; the signal-dependent capacitance of the transistors also leads to amplitude-dependent phase responses of the RF signal known as the AM-PM effect. Their impacts on the baseband I/Q plane are rotationally symmetric.

- The nonlinearity of the baseband I/Q paths, from the DAC to the mixer, distorts the baseband I/Q plane, which displays both phase and amplitude dependencies. The distortion pattern, as shown in Figure 3.10, can be
divided into four identical quadrants assuming that the I/Q paths are well matched and any even-order distortions are negligible.

- The gain mismatch of baseband I/Q paths, and the amplitude and phase mismatch between the quadrature LO signals, scale and rotate the baseband I/Q plane, which also displays phase as well as amplitude dependencies. Note that the delay mismatch of baseband I/Q paths is a

Figure 3.10: Distortion effects of the baseband I/Q plane due to various TX memoryless errors.
memory effect and thus is not treated in the memoryless equalizer; instead, it can be easily avoided by symmetric layout due to the low frequency of baseband signals.

### 3.3.2 Equalization schemes

The straightforward scheme is shown in Figure 3.11, where the TX memoryless errors are separately treated and the order of the equalizers is reverse to that of the TX errors. The number of coefficients can be optimized because the TX error parameters are well defined in this scheme. However, the adaptation algorithm tends to be more complicated because multiple loops are created and

![Figure 3.11: Separate equalizations of the baseband nonlinearity, I/Q mismatch, and PA distortion.](image)

Figure 3.11: Separate equalizations of the baseband nonlinearity, I/Q mismatch, and PA distortion.
each error source needs to be identified for the adaptation of each equalizer.

Instead of identifying and compensating the above three types of errors independently, they are equally (blindly) treated in a 2-D LUT, as shown in Figure 3.12, for the sake of compactness. Depending on the types and characteristics of TX errors, multiple coefficients in the 2-D LUT are identical, allowing one to reduce the number of coefficients as illustrated in Figure 3.13. When the distortion is simply amplitude dependent, the transmitted symbols are rotationally symmetric (Figure 3.13(a)); the symmetry is broken into four identical quadrants when the nonlinearities of the baseband circuits are included (Figure 3.13(b)), with the assumption that the I- and Q-paths are well matched and the even-order distortions of either path are negligible due to the matching

![Figure 3.12: Unified equalization of TX memoryless errors.](image-url)
Figure 3.13: Effects of various transmit-path memoryless impairments: (a) AM/AM and AM/PM distortions of PA, (b) baseband nonlinearity in addition to (a), and (c) I/Q mismatch in addition to (b).

accuracy and differential nature of the on-chip analog circuits; when I/Q mismatch is included, the quadrantal symmetry of the symbol map splits into a half-plane symmetry shown in Figure 3.13(c). This analysis can be carried on further, e.g., the half-plane symmetry further breaks down in the presence of an even-order nonlinearity of the baseband blocks. Thus, a full 2-D LUT can treat the even-order distortions stemming from the circuit offset, mismatch, and large-signal operation of the devices in various stages of the transmit path.
3.3.3 Example: Polynomial equalizer with LMS adaptation for PA AM/AM and AM/PM compensation

A complex polynomial filter to achieve rotation of baseband symbols as well as gain expansion is shown in Figure 3.14. The pre-compensated PA input and the RF output signals can be written as

\begin{align*}
S_{RF\_IN} &= F_p(r)\cos(\omega_c t + \theta + G_p(r)), \quad (3.1) \\
S_{RF\_OUT} &= F(F_p(r))\cos(\omega_c t + \theta + G_p(r) + G(F_p(r))), \quad (3.2)
\end{align*}

where \(r\) and \(\theta\) are the information-bearing amplitude and phase of the baseband signal, and \(F\) and \(G\) are the AM-AM and AM-PM distortion functions, respectively. To compensate for \(F\) and \(G\), the filter transfer functions, \(F_p\) and \(G_p\), should satisfy the following equations:

\begin{align*}
F(F_p(r)) &= r, \quad (3.3) \\
G_p(r) + G(F_p(r)) &= 0. \quad (3.4)
\end{align*}

The complex polynomial function \(A(r) + j \cdot B(r)\) in Figure 3.14(a) can be obtained from

\begin{align*}
rA(r) &= F_p(r)\cos(G_p(r)), \quad (3.5) \\
rB(r) &= F_p(r)\sin(G_p(r)). \quad (3.6)
\end{align*}
As the coefficients of the complex polynomial are not known up front, a least-mean-square (LMS) algorithm is chosen to adapt the filter. As shown in

![Diagram of adaptive digital filter](image)

(a)

![Diagram of filter coefficient update scheme](image)

(b)

Figure 3.14: (a) Architecture of the adaptive digital filter and (b) filter coefficient update scheme with LMS algorithm.
Figure 3.14 (b), \( \mu \) is the LMS step size, \( d \) is the loop delay, \( k \) indicates the \( k \)th-order term of the polynomial, and \( E \) is the error vector between the original and the feedback signals.
CHAPTER 4

SYSTEM DESIGN OF DIGITALLY EQUALIZED TX

Figure 4.1 shows the simplified system diagram of the digitally equalized RF transmitter. The feedback path, consisting of a down-conversion mixer, an Adaptive Digital Equalizer, and a predistortion block, allows for compensation of nonlinearities and distortions in the RF signal. The system diagram illustrates how the digital TX data is processed through the feedback loop to achieve optimal transmission performance.

Figure 4.1: System diagram of RF transmitter with adaptive baseband digital equalization.
anti-aliasing filter, and an ADC, loops the transmitted RF signal back to the
digital domain for error extraction and equalizer adaptation. In steady state, the
digital equalizer compensates the amplitude and phase distortions of the TX by
predistorting the baseband signal, forcing the error power to a minimum. As a
result, the transmit path is linearized if the feedback path is assumed linear, and
the TX gain is set by the attenuation factor of the feedback path. In this work, 2-D
LUT is employed to equalize almost all the memoryless TX errors including PA
amplitude-oriented errors, baseband nonlinearity, and LO I/Q mismatch.

Typically, the most visible effect of equalization in frequency domain is
the suppression of spectral regrowth in adjacent channels, which is exemplified by
the intermodulation products of the TX in Figure 4.1 that are cancelled out by two
sidebands with equal amplitude and opposite phase produced by the equalizer. In
this approach, the linearization performance of the equalizer is determined mostly
by three factors: the accuracy of the learned equalizer coefficients, the ideality of
the feedback path, and the severity of the TX memory effects. Design
considerations related to these aspects at the architectural level are explored in
this chapter. The design specs of each building block in the loop are also extracted
through behavioral simulations.
The target application is an 802.11a wireless LAN system. As summarized in Table 4.1, an 802.11a system uses a QAM-OFDM signal whose PAPR is typically 8 to 17 dB [2]. A challenge for PA design targeted for high PAPR OFDM signal is that the average PA power efficiency is typically very low, less than 10%, when a conventional Class-A or Class-AB PA topology is used to satisfy the required linearity. Thus, the trade-off between linearity and power efficiency can be mostly exploited with an 802.11a system. In addition, the signal bandwidth is 20 MHz, which is too large to be treated in analog feedback system because of a stability issue. The carrier frequency is 5.2 GHz and maximum output power of this system is 23 dBm. For the performance specs, EVM of the TX path should be less than -25 dB for 54 Mbps transmission and the output spectrum mask is shown in Figure 4.2 [2].

<table>
<thead>
<tr>
<th>Modulation scheme</th>
<th>QAM-OFDM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak-to-average power ratio</td>
<td>8 ~ 17 dB</td>
</tr>
<tr>
<td>Channel bandwidth</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Maximum output power</td>
<td>23 dBm</td>
</tr>
<tr>
<td>Carrier frequency</td>
<td>5.2 GHz</td>
</tr>
</tbody>
</table>

Table 4.1: Specifications of 802.11a WLAN system.
4.1 Behavioral Models

Behavioral simulations are first performed in MATLAB/SIMULINK to capture the system-level trade-offs. The concept and its mathematical proof are verified in time-domain simulations. System parameters and the specifications of various building blocks are also determined. Examining the waveforms at each critical point quantitatively in the system helped greatly in developing conceptual understanding as well as actually designing the transmitter circuits.

First, the building blocks and their dominant features are modeled accounting for their significance to the system performance, the model complexity, and the computing power available. Too-detailed models significantly increase the simulation time, undermining the purpose of a
behavioral simulation. For instance, the coexistence of digital baseband and RF signals in this work requires both small time steps and long simulation times, which significantly increase the overall simulation effort. Thus, a baseband equivalent model of RF building blocks is used to expedite the simulation in this work, e.g., the baseband AM/AM and AM/PM models are used for the nonlinear RF PA.

Next, conservative system parameters are used to verify the compensation algorithm and to obtain a reference point for the system performance. Then, more realistic system parameters are substituted using fixed-point coefficients, finite table sizes, etc., and compared with the performance of the reference design. The specifications of circuit building blocks of TX and RX—i.e., DAC and ADC resolution and sampling rate, transmit filter order and cutoff frequency, RX linearity, SNR requirements, etc.—are also modeled and optimized carefully using this design approach.

Lastly, specs of system merits and peripheral building blocks are also defined. Based on these specs/merits, a system-level picture of the test bench is derived. Error vector magnitude (EVM), adjacent-channel power ratio (ACPR), convergence time of the equalizer, TX output power, and power efficiency constitute the main elements of the system performance metrics, and are all specified and evaluated comprehensively in the behavioral simulation.
The MATLAB/SIMULINK simulator with the full features is shown in Figure 4.3. Each block is used, disabled, or bypassed depending on the simulation purpose. For example, ideal coefficients are calculated and used to see the effects of TX memory errors after all feedback blocks are disabled. In this case, “PA Output_Test” signal should be ideal because all the memoryless errors are perfectly compensated and there is no block with the memory errors in that path.

Figure 4.3: MATLAB/SIMULINK system simulator with full features.
In order to evaluate the adaptation algorithm, i.e., whether the coefficients are converged to the right values with the algorithm, an ideal feedback path is used after all non-ideal blocks are bypassed. The blocks in the feedback path can be turned on, one by one, to look at how each error affects the converged coefficients or the dynamics of the coefficient adaptation.

Figure 4.4 shows the diagram for the OFDM signal generation for 54 Mbps data transmission. (The scrambler is not used and buffers/unbuffers between the blocks are not shown.) The default sampling rate of the output signal is 80 MS/s. The output spectrum and the signal statistics are shown in Figure 4.5.

Figure 4.4: OFDM signal generation in MATLAB/SIMULINK.
and the PAPR of the signal is 9.6 dB. Over the 20 MHz bandwidth are distributed 64 sub-carriers, so the bandwidth of each is 312.5 kHz. No signal is transmitted in a few sub-carriers, including at DC. Signals with different data rates, number of sub-carriers, sampling rates, bandwidths, and PAPR can be composed by controlling the parameters of each block.

Ideal demodulation in Figure 4.3 is the reverse way of OFDM signal generation until the QAM symbols are recovered as shown in Figure 4.6; the QAM symbols are used for the EVM calculation. The fractional loop delay is first compensated for accurate performance evaluation and the analog signal (discrete-time signal with high sampling rates in MATLAB) is sampled. After the CP

Figure 4.5: (a) Spectrum and (b) distribution of the OFDM signal.
removal, FFT, and the pilot removal, data of each sub-carrier is equalized to compensate for the non-ideal frequency response in the loop. A one-tap complex number is used for the equalization of each sub-carrier in this work. For mean-square error (MSE) evaluation, the analog RX signal is time-synchronized, sampled, and compared with the original analog TX signal.

Figure 4.6: Block diagram of an ideal OFDM demodulator in MATLAB.
4.2 Transmit Path

A more detailed diagram describing the transmitting building blocks is shown in Figure 4.7. The regular direct-conversion Cartesian transmitter is used to prove the digital equalization concept. The AC coupling networks are inserted between the blocks to convert the DC bias level and block the DC offsets to be transferred to the next block. This is possible because the DC sub-channel does not generally contain the signal and the first low-frequency sub-channels for signal are ±312.5 kHz.

4.2.1 RF PA model

The PA topology is perhaps the most determining factor of the overall transmitter power efficiency due to the high output power and less-than-perfect efficiency of a typical RF PA. The average power efficiency of a Class-A PA is
usually severely degraded due to the large back-off to obtain sufficiently linear operation, especially for transmitting signals of large PAPR, which causes the PA to operate mostly in the low output power region where its efficiency is also low [16]. The trade-off between linearity and efficiency motivates the use of nonlinear PAs such as Class-B types with much higher efficiency in the low power region (owing to its dynamic bias current). Large amplitude and phase distortions stemming from Class-B operation are inevitable, which will be subsequently treated in the digital domain. Moreover, a successful linearization in the saturated power region will result in less back-off, thus further improving the power efficiency of the transmitter.

The Class-B PA is first designed in the transistor level and its AM/AM and AM/PM characteristics are extracted by the harmonic balance simulation in ADS and used in the behavioral simulation. In Figure 4.8, the solid gray curves are the AM/AM and AM/PM of the RF PA, the dashed gray curves are the calculated inverse curves, and the black curves are the cascade of the two. The EVM performance is simulated using the OFDM signal described in Figure 4.5 and the result is in Figure 4.9 (a), which shows that the EVM spec of 802.11a is not satisfied with this PA model even with the large back-off. Note that -9.6 dB back-off from the saturated output power is the largest output power in which there is no signal clipping since the signal PAPR is 9.6 dB. The output spectrum in (b) is when the back-off is -10 dB with and without the equalizer.
Figure 4.8: AM/AM and AM/PM models used in the behavioral simulation and ideal equalization to compensate them.

Figure 4.9: (a) EVM versus power back-off from the saturated output power when using the PA AM/AM and AM/PM models of Figure 4.8 and (b) output spectrum with and without equalization when the power back-off is 10 dB.
4.2.2 DAC resolution

To avoid violating the 802.11a spectrum mask requirement due to the DAC quantization noise, resolution of more than 7 bits is typically required, and 7 bit resolution causes the signal error to be below -40 dB. However, higher resolution may be required for the equalized signal since the quantization noise is amplified more than the signal; the quantization noise is amplified by the nonlinear PA while the signal is amplified by the overall (linearized) gain. When the PA AM/AM model in Figure 4.8 is used, we can easily see the quantization noise amplification is higher. Figure 4.10 compares the EVM performance of the

![Diagram](image)

Figure 4.10: EVM versus DAC resolution. (Comparison between the normal and equalized TXs.)
normal TX and the equalized TX with different resolutions. Open-loop simulation is performed with the ideal equalizer and all other transmitting blocks except DAC are bypassed. For the same EVM performance the DAC resolution of the equalized PA needs to be 1 bit higher than the normal TX; 8 bit DAC is necessary for EVM less than -40 dB.

4.2.3 Transmitting low-pass filters

In general, any memory effect of the transmit path is of concern in a memoryless compensation such as that described here. Since one major source of memory derives from the frequency response of the TX LPF, the filter type and order need to be carefully selected. The following criteria need to be satisfied in this regard:

1) The LPF needs to pass the intermodulation products and harmonics generated by the equalizer to the RF blocks in a frequency-independent manner, i.e., with a constant gain and linear phase response. Any frequency-selective response would result in a corruption of the signal preconditioning, thus impairing the compensation accuracy.

2) The filter also needs to attenuate the DAC aliases sufficiently in order to satisfy the spectrum mask.
The above design considerations boil down to a trade-off between the oversampling ratio (OSR) of the DAC and the complexity of the LPF. For example, a 4× OSR is typically employed in a practical 802.11a transmitter. Without additional oversampling, a shaper LPF cutoff is essentially required to satisfy criteria 1 and 2. Figure 4.11 summarizes the system-level simulation results for various LPF types and orders, showing the EVM performance and the maximum spectral component in the PA output spectrum of 30 MHz above and below the carrier frequency, when a standard OFDM signal with 64 subcarriers and 20 MHz bandwidth is transmitted. Measured amplitude and phase distortion curves of a stand-alone CMOS Class-B PA are used in this simulation. The results reveal that a 5th-order Butterworth filter achieves a reasonable balance between in-band and out-of-band linearity performance, displaying a better than −33 dB error-vector magnitude (EVM) while meeting the 802.11a spectrum mask with some margin. Elliptic and Chebyshev filters, especially the 5th-order ones whose results are not shown in Figure 4.11, perform worse due to their large phase variations near the cutoff frequency (0.5 dB in-band ripple and 25 dB stop-band attenuation for elliptic filters and 0.5 dB ripple for Chebyshev filters are assumed in the simulation). Lastly, Bessel filter has insufficient roll-off in spite of a relatively more linear phase response.
When the TX distortion is severe, e.g., a Class-C or even Class-E PA is used, high-order nonlinearities will need to be included in the treatment, and a larger OSR of the DAC will be necessary to accommodate the widely spread baseband spectrum due to predistortion. If the OSR is not sufficient in such a case, it will be difficult to meet the in-band and out-of-band specs simultaneously even with a higher-order LPF. Although this effect has been considered in the literature as the major limiting factor of the advocated equalization approach, we believe

![Graph showing the effects of TX filter type and order on linearization performance](image)

**Figure 4.11:** Effects of TX filter type and order on (a) out-of-band and (b) in-band linearization performance, where $\text{PD}_{\text{max}}$ is defined as the maximum spectral component in the PA output spectrum of 30 MHz above and below $f_c$ (802.11a is assumed).
that technology has evolved to a point where such a trade-off is worthwhile or even beneficial. After all, data converters have benefited from technology scaling much more than monolithic RF transmitters (with integrated PAs), especially those implemented in silicon technology.

4.2.4 Other issues

Although the non-ideal frequency response is equalized in the demodulator, the mismatch of the cut-off frequencies between the I- and Q-filters is not equalized. In addition, this is not equalized in the TX equalizer either, because this is one of the memory effects, as are most of the frequency-related errors. The simulation reveals that the mismatch needs to be less than 5% to achieve EVM below -40 dB.
4.3 Feedback Path

The feedback loop inherent to the equalizer is composed of the transmitter and a dedicated receiver (RX) cascaded. Ideally, the compensated TX can only be as linear as the RX path, which places a stringent linearity constraint on the RX circuits. In a time-division duplex (TDD) system, the normal receiver can potentially be time-shared as the feedback path. However, much simpler feedback circuits can be employed when they are dedicated for equalization, due to the relaxed requirements on the gain and noise performance. Figure 4.12 shows the block diagrams of the feedback path, including the AC coupling network.

4.3.1 RX linearity

As shown in Figure 4.12, the RF signal path is composed of passive devices such as the coupler and the RF attenuator, and thus high linearity can be

![Figure 4.12: Building blocks in the feedback path.](image-url)
efficiently achieved. Note that the blocks in the TX path and RX path are relatively well matched and those RF devices correspond to the RF power amplifier. In other words, the linearity of the TX power amplifier is efficiently achieved by exploiting the high linearity of the passive device in the RX path.

However, the nonlinearity in the I- and Q-paths does affect the TX performance. Figure 4.13 (a) is the baseband-equivalent transfer curve used in the MATLAB simulation assuming that the curves for the I- and Q-paths are identical. The simulated EVM performance against the back-off from the 1 dB compression point of RX path.

Figure 4.13: (a) Voltage transfer curve of I (or Q) channel in the RX path and (b) effects of RX linearity on the equalization performance. (EVM is measured at TX output while RX input signal is backed-off from the 1 dB compression point of RX path.)
point is shown in Figure 4.13 (b), where it is observed that 8 to 10 dB back-off in the feedback path is necessary for EVM below -35 dB at the TX output. Again, all other blocks except the RX nonlinearity are ideal.

4.3.2 RXLO I/Q mismatch

In a similar way to the linearity, the LO I/Q mismatch in the feedback affects the TX performance when the 2-D LUT is used. Since this error generates the in-band image in the spectrum, it does not generally cause violation of the spectrum mask while it causes the symbol errors. The ideal equalizers to compensate the RX I/Q mismatch are employed and the open-loop simulations are performed, with results shown in Figure 4.14. The amplitude and phase mismatch need to be below 0.1 dB and 1°, respectively, for the EVM below -40 dB with both mismatches. Note that the LO mismatch of the TX path without the equalizer also gives the same results due to the similarity of TX I/Q mismatch and the inverse of RX I/Q mismatch. Although it is true that the design cost is just moved to the RX path, it still could be efficient when the RX path with high I/Q matching accuracy is available; i.e., the normal RX path is reused for the TX equalization. Also note that it cannot compensate the LO I/Q mismatch because the effect is averaged out over one phase cycle when the amplitude-addressed equalizer is used.
4.3.3 Noise requirement

High RX sensitivity is unnecessary as the PA output is directly coupled into the feedback path, where the signal is so strong that any unwanted interferences coupled in from the antenna are essentially wiped out during the equalizer training. Even in the case when a strong interferer is present, it still tends to be averaged out in the least-mean-square (LMS) iteration loop of the equalizer, because it is uncorrelated with the transmitted symbols. In addition, the signal-to-noise ratio (SNR) and noise figure (NF) of the RX are greatly relaxed as well, since random noise tends to be averaged out in a similar manner. For example, the resolutions of the TX and RX quantization in an 802.11a system for
the EVM below -40 dB at TX output are 8 bit and 7 bit, respectively, as shown in Figure 4.10 and 4.15. Note that the ADC resolution is relaxed due to the averaging of the LMS loop and it can be further relaxed if the step-size in the LMS is getting smaller. This motivates the employment of a passive RF attenuator before the RX to decimate the down-converted signal strength and thus improve its linearity.

Although this eases the design of RX circuits, the linearity and SNR of the feedback path nonetheless need to be commensurate with the required adaptation speed and accuracy for the equalizer because the convergence time is longer and “stalling” due to the finite word length in digital is more significant with the small

![Figure 4.15: Effects of ADC resolution on the equalization performance.](image)
step-sizes. This is especially true for mobile applications (instead of base stations), in which fast convergence is highly desirable.

4.4 Power Control

Figure 4.16 shows the gain of each TX/RX block, where $G_{TXD}$, $G_{EQ,i}$, $G_{TXA}$, $G_{PA}$, $G_{A}$, and $G_{RXA}$ are the TX digital, equalizer, TX analog, PA, RF attenuator, 

![Power Control Scheme](image1)

Figure 4.16: (a) Power control scheme and (b) illustration of $G_{LTX}$. 

![Gain Illustration](image2)
and RX analog gains, respectively. The term \( i \) indicates the entry number of an LUT. Note that \( G_{TXA} \) and \( G_{PA} \) are not constant due to the TX nonlinearities. Then, the system gain, \( G_S \), and the nominal linear TX gain, \( G_{LTX} \), in the steady state can be expressed as

\[
G_S \equiv \frac{P_{OUT}}{D_{IN}} = G_{TXD}G_{LTX} = \frac{1}{G_A G_{RXA}},
\]

\[
G_{LTX} = G_{EQ,i} G_{TXA} G_{PA},
\]

respectively. The system gain (or average TX output power) is set by the receiver gain, \( G_A G_{RXA} \), similar to a conventional feedback amplifier (in which the feedback factor sets the closed-loop gain). More specifically, \( G_{RXA} \) is fixed, and the system gain is solely controlled by the RF attenuator gain, \( G_A \). The input of the active circuits in the feedback path, \( V_X \) in Figure 4.16, is thus kept constant, resulting in an optimal utilization of the RX dynamic range. In a typical setup like this, the equalizer gain, \( G_{EQ,i} \), will follow \( G_A \) when the average PA output power is varied (as the gain \( G_{TXA} G_{PA} \) is not designed to be variable). This constraint on the equalizer is undesirable as its main purpose is to handle the TX nonlinearity. An additional digital variable gain block, \( G_{TXD} \), is inserted before the equalizer and designed to track the gain variation of \( G_A \). Thus, regardless of the TX power setting, the content of the equalizer is normalized, relaxing its dynamic range requirement. The separation of (linear) power control and (nonlinear) equalization
helps to (1) minimize the equalizer coefficient variation during power control, (2) reduce the memory size needed, and (3) speed up the convergence of the equalizer.

### 4.5 Digital Equalizer

For coefficient adaptation, the equalizer should have the capability of identifying the TX memoryless errors by comparing the original data and the loopback samples (provisioned by the feedback path), which are potentially delayed, phase rotated, and even corrupted by various impairments such as memory effect, on-chip coupling, DC offset, quantization and circuit noise. The functional diagram of the digital equalizer using a gradient-descent learning algorithm is shown in Figure 4.17. The major building blocks are a 2-D multilevel LUT (2-D ML-LUT), a complex multiplier, a loop-delay compensation unit, and an LMS engine. A band-pass digital error filter $1-z^{-2}$ is also incorporated to alleviate the non-flat frequency response of the TX and RX paths due to AC coupling. The equalization algorithm, the functionalities of these blocks, and implementation details will be covered in this section.
4.5.1 Two-dimensional multilevel LUT (2-D ML-LUT)

A 2-D LUT was first employed for digital predistortion by Nagata back in 1989 [47]. Known as the mapping-LUT, it suffered from the requirement of large memory and a long training time. However, solid-state memory technology has evolved significantly since the 1980s, and nowadays the required memory size and speed of a 2-D LUT is no longer a limiting factor. On the other hand, an LUT-based compensation scheme inevitably suffers from the trade-off between convergence speed and compensation accuracy; i.e., high compensation accuracy usually requires a large table, which leads to a long training time. In this work, we introduced an ML-LUT technique to expedite the learning process by parallelizing the compensation of multiple coarse and fine tables [48]. The entries of the coarse tables are updated more frequently, which enables a fast
approximation of the desired predistortion curves as illustrated in Figure 4.18 (a 1-D LUT is shown for simplicity). The accuracy, on the other hand, is accomplished by the finer tables. The starting level and the table depth can be optimized by considering the PA characteristics, compensation accuracy, convergence speed, and implementation cost. The entries (of the multiple tables) corresponding to the same position in the baseband I/Q plane are updated at the same time by a complex LMS algorithm. It is generally known that the convergence of a 2-D table is significantly slower than that of a 1-D table, due to the squared number of total entries. The ML-LUT technique is particularly useful in such scenarios, where fast adaptation is a prominent feature of our approach compared to many alternative compensation techniques [48].

![Figure 4.18: A 1-D ML-LUT example.](image)
Each table is trained by a least-mean-square (LMS) algorithm. For the cell \(m\) of the \(n^{th}\) table, the iterative update equation is

\[
C_{n,m}[k] = C_{n,m}[k-1] + \mu V_{IN}^*[k] \left(V_{IN}[k] - V_{fb}[k]\right)
\]

where \(C\) is the coefficient, \(\mu\) is the step-size, \(k\) is the number of counting when the cell is hit, \(V_{IN}\) is the original signal, and \(V_{fb}\) is the corresponding feedback signal.

### 4.5.2 Loop-delay compensation

The baseband signal delay in the loopback path, mainly caused by a non-uniform group delay of the LPF and a sampling aperture mismatch between the DAC and ADC, will corrupt the LUT adaptation due to misaligned samples of the original data and the feedback signal [49]. Figure 4.19 shows the effect of the (fractional) delay on the EVM performance. An adaptive delay adjustment is also performed alongside the LUT correction, where the delay is spilt into an integer part and a fractional part. The integer part of the ADC/DAC sampling period, e.g., 12.5 ns for an 80 MHz sample rate, can be easily estimated (or determined in a measurement) and compensated by delaying the original data by the same amount [48].
The residual fractional loop delay ($\theta$) is located in the range of (-UI, UI) after the integer delay is corrected, and can be compensated by a 4-tap FIR interpolation filter with a modified Farrow structure [50]. The Farrow FIR filter that produces a positive delay is revised to accommodate both the positive and negative fractional delays. In either case, the nearest four neighboring samples are involved in estimating the delayed sample with the following interpolation functions:

$$y_{in}(n) = \begin{cases} 
\sum_{i=-2}^{1} a_i(\theta)x_{in}(n+i) & (\theta > 0) \\
\sum_{i=-2}^{1} a_i(1+\theta)x_{in}(n+1+i) & (\theta < 0)
\end{cases}$$

(4.4)

Figure 4.19: Effects of fractional loop delay mismatch on the equalization performance.
where,

\[ a_1(\theta) = \alpha \theta^2 - \alpha \theta, \]
\[ a_0(\theta) = -\alpha \theta^2 + (\alpha - 1)\theta + 1, \]
\[ a_{-1}(\theta) = -\alpha \theta^2 + (\alpha + 1)\theta, \]
\[ a_{-2}(\theta) = \alpha \theta^2 - \alpha \theta, \]

\( y_{in}(n) \) is the delayed sample, \( x_{in}(n) \) is the input signal, and \( \alpha \) is a design parameter between 0 and 1. When \( \alpha \) is 0, the 4-tap filter degenerates to a linear interpolator. The interpolation is actually a weighted average of 4 neighboring samples, of which the nearest 2 neighbors are more important and carry larger weights. The tap values of the interpolation filter are acquired by another LMS loop to track any time-varying fractional delays due to PVT variations [48]. When \( \theta_0 > 0 \), the update equations is

\[ \theta_{m+1} = \theta_m + \frac{\beta}{L} \sum_{j=0}^{L-1} \{x_{in}(mL + j) - x_{in}(mL + j - 1)\}e(mL + j), \quad (4.5 \text{ a}) \]

and when \( \theta_0 < 0 \),

\[ \theta_{m+1} = \theta_m - \frac{\beta}{L} \sum_{j=0}^{L-1} \{x_{in}(mL + j) - x_{in}(mL + j - 1)\}e(mL + j), \quad (4.5 \text{ b}) \]

where \( L \) is the LMS block length, and \( \beta \) is the step size and must satisfy the
requirement $0 < \beta p < 2$ to guarantee stability.

### 4.5.3 Non-flat frequency response

In this prototype design, AC coupling is used extensively in the direct-conversion TX and RX signal paths to eliminate the DC offsets of various building blocks except at the ADC output, where the signal is digital. Although the ADC offset may be small, the LMS algorithm will integrate it over time, and eventually leads to an overflow of the LUT as illustrated in Figure 4.20. This

![Figure 4.20: ADC DC offset causes the overflow of 2-D LUT because the loop is broken at DC due to the AC coupling capacitors.](image-url)
necessitates DC removal before the error is fed to the LUT. The non-flat frequency response of the loop due to the AC coupling capacitors and LPFs disrupts a normal LUT adaptation process by injecting larger-than-average errors at the low- and high-frequency ends of the signal spectrum. The overall compensation accuracy thus suffers.

A band-pass filter $1 - z^{-2}$ shown in Figure 4.17 is introduced in this work, which not only removes the ADC offset, but also mitigates the effect of any frequency-dependent errors by attenuating the low- and high-end frequency contents. The resulting band-pass shaping of the learning error is inconsequential due to the memoryless, zero-forcing nature of the equalization. Intuitively speaking, the function of this digital band-pass filter is to reject the “wrong” update information and retain only the “correct” information for the LUT learning. Since the compensation is frequency-independent by design, learned mid-band linearization curves will be automatically “propagated” to the entire 20 MHz bandwidth in steady state. The compensation accuracies of the equalizer with and without the band-pass filter are simulated and contrasted in Figure 4.21, where a high-pass filter (HPF) with a variable cutoff frequency is inserted into the feedback path to emulate the AC coupling network. As the cutoff frequency of the HPF is increased, the mean-square error (MSE) of the learning degrades dramatically when the band-pass filter is absent. In contrast, simulations also
reveal that the performance of the equalizer incorporating such a filter is immune to the stated impairments.

4.5.4 I/Q rotation

An RF-path delay in the loop or LO misalignment between the TX and RX paths can cause a constant vector rotation of the baseband I/Q plane. Figure 4.22 illustrates the two sources. First the baseband received signal due to the LO misalignment is expressed as

\[ R_{XI} + jR_{XQ} = (T_{XI} + jT_{XQ})e^{j\theta}. \]  \hspace{1cm} (4.6)
In addition, the RF delay also causes the rotation as well as the baseband delay.

\[ RXI + jRXQ = (TXI[t - \Delta t] + jTXQ[t - \Delta t])e^{-j\omega_c \Delta t}, \quad (4.7) \]

where \( \omega_c \) is the carrier frequency and other terms are defined in Figure 4.22. Note that the phase rotation is the product of the time delay and the carrier frequency expressed as \( \omega_c \Delta t \), and thus is possibly large although the RF delay is very small; i.e., 0.1 ns delay can create phase rotation of 180° with 5 GHz carrier frequency. Although the rotation can be absorbed into the AM-PM effect and thus, theoretically be compensated by the equalizer, a large rotation will at least slow down the LUT convergence, and even worse, may lead to instability of the

Figure 4.22: Complex baseband signal rotation in feedback signal due to (a) LO misalignment and (b) RF delay.
Figure 4.23 is the simulation result showing the feedback signal trajectory during the coefficient update using an LMS, where the original signal is $1 + 0j$ and the feedback signal starts from a point on the dashed line meaning different AM/AM and AM/PM distortion. The coefficients are updated using the LMS scheme.

Figure 4.23: Comparison of LMS adaptation speeds with different AM/AM and AM/PM.
algorithm so that the feedback signals are the same as the original signal, $1 + 0j$, after the convergence. The result shows that if the rotation is greater than $+90^\circ$, the feedback signal diverges, indicating that the system is unstable. It does happen with all the points in the left half-plane. Although the LMS algorithm converges if the rotation is within $\pm 90^\circ$, large rotation shows long convergence time. Especially, if the rotation is close to $\pm 90^\circ$, the convergence time is dramatically increased. Since LO misalignment and RF delay are hard to control with the GHz-range carrier frequency, the complex feedback signal is coarsely pre-rotated to compensate the constant rotation before it is used in the LMS algorithm. The pre-rotation can be inserted in either the feedback path or the original signal path.
CHAPTER 5

INTEGRATED CIRCUIT IMPLEMENTATION

The RF transmitter from the transmit filter to the power amplifier and the feedback path from the down-conversion mixer to the anti-aliasing filter are integrated in a single chip in 0.13 µm CMOS process as illustrated in Figure 5.1. This chapter describes the design procedure and the details of each building block.

Figure 5.1: Building blocks in the integrated TX chip.
Cadence Schematic Composer and SpectreRF are used as the main tools for schematic entry and simulation. Advanced Design System (ADS) is also used as a supplemental simulation tool.

Circuit topology of each block is first selected based on the system specs, linearity, circuit complexity, power consumption, etc. For example, all circuits except the power amplifier use a fully differential topology to reject any power supply or ground noise as they are sitting in the same die right next to a 23 dBm RF power amplifier whose output signal swings are more than 4 V peak-to-peak. After the circuit topologies are determined, device sizes and biases are optimized to meet the specifications such as gain, SNR, frequency response, etc., while minimizing the power consumption, using DC, AC, transient, PSS, S-parameter, and harmonic balance simulations. The sensitivities to potential process variations are also checked and proper revision is performed such that the circuit performance is least sensitive to temperature, process, and supply variations. Frequency tuning with digital programmability is widely used in RF circuits, which utilize high-Q LC tanks to obtain a high voltage gain at RF frequencies. Thus, a stable frequency response is achieved while the circuit performance is not compromised. Lastly, when each block is designed, the interfacing issues such as loading, etc., of the next stage are also estimated and asserted in the block-level schematics.
In the last stage of schematic design, all blocks are integrated and the entire chip is simulated to check the functionality and any potential side-effects due to the integration. Package and board-level models are inserted to verify the PA output power with the parasitics included in the matching network. Potential coupling of the PA output to other blocks through mutual inductance of bond-wires is also checked in simulation to avoid any potential layout mistakes. Two-dimensional E&M simulation is performed at board level to verify the microstrip/coplanar waveguide structures that are inherent to the matching network as well as the directional coupler for the feedback path.

The schematics are translated into layout using Cadence Virtuoso. Placement and pad allocation are carefully done to shorten the routing length for high frequency signals, to minimize the mutual inductance of bond-wires, and to make it easier to assemble the chip and the board. Common-centroid layout is widely adapted to improve the I/Q matching. Top metals are stacked and connected through sufficient vias for the main current path of the PA to satisfy the electromigration rules and minimize the power loss due to parasitic resistance. The large bypass capacitors inserted between the supply and ground of each power domain act as charge reservoirs and reduce any high-frequency glitches.

Parasitic capacitance and resistance are extracted for all blocks using Calibre. For the baseband filters, device sizes are adjusted to restore the cutoff frequencies and Q-factors due to the parasitics. In addition, the inductances of LC
tank loads are adjusted to get the right frequency tuning range accounting for the extracted parasitic capacitance. The whole chip is properly divided into segments with overlap and simulated with the RC-extracted netlists to reduce the overall verification time.

5.1 Class-B RF Power Amplifier

Topology Selection

The schematic of the 5 GHz, 0.13-μm CMOS, Class-B PA is shown in Figure 5.2. Targeting 25 dBm saturated output power, two-stage topology is chosen and the second stage is “Class-B” biased to achieve high average power efficiency for the OFDM signal with high PAPR. The first stage (PA driver) amplifies the mixer output to the maximum allowable swing in the second stage input. Note that the gain requirement is less as the relaxed linearity requirements throughout the TX path allow large signal swing. A cascode configuration is used in both stages to protect the input devices for reliability concerns. Thick-oxide transistors are utilized in the output stage to allow a 2.5 V supply for large output swings. According to Equation (2.11), the power efficiency of the L-type matching network increases from 80% to 90% when the supply increases from 1.2 V to 2.5 V, where the output power and the inductor Q are assumed to be 25 dBm and 20, respectively.
Transistor Sizing

The transconductance transistors of both stages (M1, M2, M5, and M6) are sized to provide the current for the necessary voltage and power gain given the bias voltages and the load impedances. On the other hand, the sizing of the cascode transistors (M3, M4, M7, and M8) is more involved. The most important rule is that the drain voltages of the transconductance transistors need to be high enough not to decrease the transconductance and low enough not to violate the reliability concern of the transconductance transistors. In addition, note that the gate bias of the cascode transistors in the second stage is provided from off-chip and thus controllable, which allows another degree of freedom in transistor sizing.
Although the low bias and large size are preferable for better current buffering capability, this is strictly limited by the parasitic capacitance; large parasitic capacitance not only increases the power loss with the series resistance as presented in Chapter 2, but also makes the values of other passive devices in the output matching network impractically small. The transistor sizes are summarized in Table 5.1.

### Table 5.1: Transistor sizes of the implemented Class-B PA.

<table>
<thead>
<tr>
<th></th>
<th>M1, M2</th>
<th>M3, M4</th>
<th>M5, M6</th>
<th>M7, M8</th>
</tr>
</thead>
<tbody>
<tr>
<td>L [μm]</td>
<td>0.12</td>
<td>0.12</td>
<td>0.12</td>
<td>0.34</td>
</tr>
<tr>
<td>W [μm]</td>
<td>280</td>
<td>320</td>
<td>1230</td>
<td>2048</td>
</tr>
<tr>
<td>W/L</td>
<td>2333</td>
<td>2667</td>
<td>10250</td>
<td>6023</td>
</tr>
</tbody>
</table>

Although the low bias and large size are preferable for better current buffering capability, this is strictly limited by the parasitic capacitance; large parasitic capacitance not only increases the power loss with the series resistance as presented in Chapter 2, but also makes the values of other passive devices in the output matching network impractically small. The transistor sizes are summarized in Table 5.1.

**Input, Inter-stage, and Output Matching**

The interface between the first and second stages is an AC coupling network consisting of the series metal-insulator-metal (MIM) capacitor and the poly resistor for the gate bias as shown in Figure 5.2. The on-chip spiral inductor load of the PA driver tunes out the parasitic capacitance in both nodes of the AC coupling capacitor at the operating frequency. The same structure is also used between the mixer output and the PA driver input; however, the inductance is large due to the lower parasitic capacitance. Therefore, the Q-factor of the tank is high at the mixer output because the larger the on-chip spiral inductance is,
typically the higher the inductor Q. To minimize the inductive coupling from the PA driver output to the mixer output, the inductors are sufficiently separated in layout. The frequency tuning capability using the switched capacitor array is only inserted at the mixer output because the high performance switch for the high swing in the PA driver output is not readily available.

By Equation (2.1), the load resistance of the second stage should be 10 Ω for 25 dBm maximum output power. However, the load-pull transistor-level simulations in ADS result in 16 Ω to 20 Ω for the optimum power efficiency in the 25 dBm saturated output power. This gap is because Equation (2.1) does not reflect the non-ideal effects due to the nonlinear transconductance, the output voltage shaping by the harmonic contents, etc. Figure 5.3 (a) shows the matching network which transforms 50 Ω to 18 Ω and two sets of component values depending on the Q of the matching network (Q_M). Note that a 2.5 pF capacitor (C_D) models the extracted parasitic capacitance at the drain nodes of M7 and M8 in Figure 5.2. This includes the capacitance from the transistor junctions, metals, and the pads. The transistor-level simulations revealed that the PA power efficiency was higher when the matching network with the small Q_M (case A) is used. This is understood by the fact that the higher impedance (Zout in Figure 5.3 (b)) of case A at the harmonic frequencies shapes the drain voltage, better reducing the power loss in the transistors. However, the large harmonic contents are less attenuated by the low-Q_M matching network as shown in AC simulation
results of Figure 5.3 (c), putting a greater burden on subsequent blocks. In this work, all the devices except $C_D$ in Figure 5.3 (a) are implemented by the bondwire

Figure 5.3: (a) Schematic of the matching network, (b) normalized impedance magnitude of the passive network, and (c) frequency response of the matching network.
inductance and the off-chip discrete capacitors and thus the values are controllable in the testing phase.

**Reliability / Coupling**

A capacitor is inserted between the gate nodes of the output cascode transistors instead of shorting the two nodes directly like the first stage, which allows the RF signal to swing at the gate nodes, enabling one to reduce the stress on the output transistors by reducing the instantaneous gate-drain voltages [51]. The saturation output power is negligibly degraded in spite of the gain drop with the capacitor. Second-order harmonics are suppressed by the series LC tanks at the common-source nodes in each stage to attenuate ground fluctuations and potential intermodulation distortions [52]-[54].

**Performance Summary (by simulation)**

With all parasitics, bondwires, and the off-chip device models, the simulated maximum saturation output power is 24.6 dBm where the drain efficiency is 49%. More than two third of the power loss is at the transconductance transistors, and the rest is mostly at the parasitic resistances. The efficiency curve against the power back-off is well matched to the Class-B behavior. The AM/AM and AM/PM curves are shown in Figure 4.8 and used in the system simulation. The PA driver is “Class-AB” biased and consumes 40 mW
in simulation. The voltage gain of the PA driver is 12 dB when the voltage swing at the second stage input is maximum. No oscillation is observed in the transient simulations under different temperatures and corner conditions with the nominal 50 Ω load, although the $K$- and $BI$-factors tell us the PA is conditionally stable.

5.2 Baseband Filters

Figure 5.4 shows the 5th-order Butterworth TX baseband LPF realized by the cascade of two 2nd-order Sallen-Key sections and an RC 1st-order section [55]-[56]. The cutoff frequency of the LPF is variable from 20 to 50 MHz, set by MIM capacitors and CMOS switches controlled by four digital bits. Besides absorbing the effect of any potential process variations, the purpose of the

![Figure 5.4: Schematic of the 5th-order tunable TX LPF.](image)
tunability is also to test the spectrum-spreading effect of the predistorted signal. The gain of the TX filter is set to unity as a large baseband input is allowed in this design due to the relaxed linearity constraint. The cutoff frequency ($\omega_c$) and the $Q$-factor of one Sallen-Key section in this design can be written as

$$\omega_c = \frac{1}{\sqrt{2R_1R_3C_1C_2}} = \frac{1}{R_1C_1\sqrt{2\alpha\beta}},$$

$$Q = \frac{\sqrt{R_1R_3}}{R_1 + R_3} \sqrt{\frac{C_2}{2C_1}} = \frac{\beta}{1 + \beta} \sqrt{\frac{\alpha}{2}},$$

where $R_3 = \beta R_1$ and $C_2 = \alpha C_1$. Equations (1) and (2) indicate that the $Q$-factor of the LPF is determined by component ratios, while the cutoff frequency can be controlled by sizing the capacitors $C_1$ and $C_2$ proportionally. In addition, by setting $\beta$ to unity, the capacitance spread $\alpha$ of the LPF is minimized given a $Q$-factor, which is desirable to accommodate a wide tuning range of the high-$Q$ section. When a parasitic capacitor ($C_p = \gamma C_1$) exists between the ground and the junction of $R_1$ and $R_3$ (similar for $R_2$ and $R_4$), the cutoff frequency and the $Q$-factor of the LPF can be revised to

$$\omega_c' = \omega_c \sqrt{\frac{\alpha}{\alpha + \gamma}},$$

(5.3)
\[ Q' = Q \frac{2^{\sqrt{\alpha + \gamma}}}{(2 + \gamma)\sqrt{\alpha}} \]  \hspace{1cm} (5.4)

where \( \beta = 1 \) is asserted. Therefore, if \( \gamma \) is assumed constant across the tuning range, the variations of the cutoff frequency and the \( Q \)-factor due to the parasitic capacitance are also constant, and thus can be factored in the design phase.

In the feedback path, a 2nd-order Butterworth LPF realized by a 2nd-order Sallen-Key section is used for anti-aliasing. Any residual DAC aliases, as well as wideband noise, will be attenuated by the RX LPF that enhances the training accuracy of the equalizer. The resistive feedback, consisting of \( R_5 \) through \( R_7 \) shown in Figure 5.4, stabilizes the gain of the amplifier used in the Sallen-Key; it also improves the linearity of the feedback path. The simulated IIP3 of the filter was 19 dBm. This filter directly drives the off-chip capacitance up to 7 pF without significant response degradation by virtue of the low output impedance, 100 \( \Omega \).

Figure 5.5 plots the schematic simulation results of the transmitting after extraction showing the frequency tuning capability. The maximum attenuation at 80 MHz, where the DAC aliasing is located, is more than -60 dB, and the in-band variation is below -0.2 dB. The estimated power consumption of the transmitting filter including the bias circuits is 8 mW to 19 mW according to the bias setting, and that of the anti-aliasing filter is 6 mW to 12 mW.
Figure 5.5: Simulated frequency response of the 5th-order tunable TX LPF.
5.3 Up-Conversion Mixer

A double balanced Gilbert-cell mixer is used for frequency up-conversion as shown in Figure 5.6 [57]. A fully differential topology is utilized to reject any potential coupling from the PA output nodes through substrate and power connections. A power-efficient stacked structure is adopted for the TX mixer, which results in a reduced output swing, and thus in degraded linearity performance, at a low supply voltage of 1.2 V. This would normally pose a problem for the transmission quality; however, as expected, it is turned into an advantage (to save power) in this design, due to a relaxed linearity constraint on

Figure 5.6: Schematic of the up-conversion mixer.
the entire TX path. The large input parasitic capacitance of the PA is tuned out by on-chip spiral inductors that also supply the DC bias current to the mixer.

A 4 bit switched-capacitor array, realized by MIM capacitors and NMOS switches, is inserted across the mixer differential output nodes for resonant frequency tuning. NMOS switches are used in the array with their contribution of parasitic capacitance minimized by biasing the drain and source nodes at the ground level through large resistors. The switched-resistor array controlled by two digital bits at the mixer output is for the purpose of gain control, and is disconnected by default. AC coupling networks are placed at the baseband and LO inputs (not shown), and the biases are provided by the circuit in Figure 5.7.

![Figure 5.7: Schematic of the bias circuits for the up-conversion mixer.](image_url)
The regular high swing bias circuit is used to maximize the allowable swing at the output [58]. The voltage gain is -1 dB to 2 dB in 1 dB steps, depending on the resistor $R_1$, when the LO swing is set to 0.8 Vpp differentially. The center frequency is tunable from 3.5 GHz to 6 GHz by controlling the switched capacitor array. The total power consumption is 5 mW to 7 mW.

### 5.4 Down-Conversion Mixer

Note that all design constraints except the linearity and I/Q mismatch are relaxed for the feedback path. Therefore, a folded structure is adapted for the down-conversion mixer to achieve high RX linearity as shown in Figure 5.8 [59]. The techniques employed to linearize the RX mixer include resistive degeneration.

![Schematic of the down-conversion mixer (I-path)](image)

Figure 5.8: Schematic of the down-conversion mixer (I-path).
of the input transistors and a folded structure that allows separate control of the bias currents of the input and output branches, and thus an improved output swing. The size of the switching quad is optimized for linearity performance given the bias current, taking into account the LO swing and the impedance looking into the load branches. A 100 Ω poly resistor is inserted between the differential RF input nodes to match to the 50 Ω impedance of the loopback signal path, which consists of a few off-chip structures, i.e., an output-matching network, a directional coupler, and an RF attenuator in this prototype. The bias circuit is shown in Figure 5.9, where the half circuit of the mixer core is extracted and scaled. The current ratio between two branches is determined by the ratio of the PMOS (M11 to M12) sizes.

![Bias Circuit for Down-Conversion Mixer Diagram](image)

Figure 5.9: Schematic of bias circuits for the down-conversion mixer.
The voltage gain is 5 dB to 8 dB in 1 dB steps, depending on the resistor $R_4$ and $R_5$, when the LO swing is set to 0.8 Vpp differentially. Although the gain is not required in the feedback path, the gain helps to improve the mixer linearity because the dominant source of nonlinearity is the input transconductance transistors. The simulated IIP3 is 12 dBm and input compression point 1 dBm. The total power consumption is 7 mW to 12 mW.

5.5 Poly-Phase Filter

On-chip poly-phase filters (PPFs), shown in Figure 5.10 (a), buffer differential LO signals from off-chip to produce the quadrature phases for the TX and RX mixers. A three-stage design is chosen to obtain a sufficient image rejection for the required magnitude and phase accuracies with a wide tuning range. This is done mostly for the sake of the RX mixer, as an I/Q mismatch can cause self-images of the loopback signal in reception and degrade the equalization performance (note that, in contrast, a similar mismatch in the TX will be compensated by the 2-D LUT).

A polyphase filter is a type of complex filter that passes the signal at a (positive) frequency while stopping the signal at its image (or negative) frequency, which makes it possible to generate the quadrature signal at the output [60]. Two ways are typically used to feed the input differential signal as shown in Figure 5.11. In the case of (a), each output is calculated as
\[
\frac{LOI +}{LO +} = \frac{1 - j\omega RC}{1 + j\omega RC} = -\frac{LOI -}{LO +}, \quad (5.5 \ a)
\]

\[
\frac{LOQ +}{LO +} = -1 = -\frac{LOQ -}{LO +}. \quad (5.5 \ b)
\]

Figure 5.10: (a) Schematic of PPF for LO generation with the component values and (b) simulated frequency response at negative frequencies. (The frequency response at positive frequencies is flat, 0 dB, and not shown here.)
Note that the equation (5.5a) becomes \(- j\) when the frequency, \(\omega\), is \(1/RC\).

On the other hand, in the case of (b), each output is expressed as

\[
\frac{\text{LOI} +}{\text{LO} +} = \frac{1}{1 + j\omega RC} = -\frac{\text{LOI} -}{\text{LO} +}, \quad (5.6\ a)
\]

\[
\frac{\text{LOQ} +}{\text{LO} +} = \frac{-j\omega RC}{1 + j\omega RC} = -\frac{\text{LOQ} -}{\text{LO} +}. \quad (5.6\ b)
\]

When the frequency, \(\omega\), is \(1/RC\), the equations become

\[
\frac{\text{LOI} +}{\text{LO} +} = \frac{1}{1 + j} = -\frac{\text{LOI} -}{\text{LO} +}, \quad (5.7\ a)
\]

\[
\frac{\text{LOQ} +}{\text{LO} +} = \frac{-j}{1 + j} = -\frac{\text{LOQ} -}{\text{LO} +}. \quad (5.7\ b)
\]

Figure 5.11: Comparison between two methods of input signaling.
Thus, the relative phase is the same as in the case of (a) while the gain magnitude is less by 3 dB because the signals are fed into only two inputs. However, the case (b) has 3 dB higher voltage gain from the source to the PPF input because the magnitude of the input impedance is twice as large as that of case (a). In other words, when the available input power is the same, the voltage amplitude at the PPF output is the same in both cases.

Another important observation is with the frequency offset from $1/RC$. If we compare Equation (5.5 a) with (5.5 b), the gain magnitude is always the same as unity at any frequency, indicating there is no gain mismatch while the quadrature phase relation is broken with the frequency offset. In contrast, Equations (5.6 a) and (5.6 b) show that the quadrature phase relation is always maintained at all frequencies, whereas the gain mismatch and thus the LO amplitude mismatch occur with the frequency offset. Thus, case (b) is preferable in sense that (1) the LO phase mismatch is typically more severe in the GHz-range LO quadrature signals, and (2) the mixers using the MOS switches are less sensitive to the LO amplitude mismatch than the LO phase mismatch. Nevertheless, the input connection of the case (a) is used in this work because (1) the frequency offset issue is systematically removed by using three-stage PPFs which sufficiently cover the frequency range of interest, and (2) a clean ground is not available in this chip, and most importantly, (3) the direct connection of any
node in the LO path to the ground is not desirable because PA-to-LO signal coupling potentially causes system instability.

Considering the I/Q mismatch of the LO signals alone, it can be estimated that the amplitude and phase mismatches need to be less than 0.1 dB and 1°, respectively, to achieve a better than −37 dB EVM, as analyzed in Chapter 4. This translates into a better than −45 dB image rejection of the PPF with some margin, and, in turn, a capacitor and resistor matching accuracy of better than 1.5% [60]. Although this matching level is not difficult to achieve in modern CMOS processes, a poor layout can still result in large mismatches for gigahertz-range operation. In this work, the last stage output nodes of the PPF are sufficiently separated in layout to minimize any potential capacitive coupling between the quadrature LO signals. In addition, the LO routings to the down-conversion mixer are well balanced to minimize any potential mismatch between the parasitic components.

5.6 Other Circuits

Bias Circuit

The bias circuit for each block, e.g., transmitting filter, up-conversion mixer, etc., is locally located to use the same ground and maximize the noise rejection. The reference currents are provided by the current-source bank as shown in Figure 5.12. One master current is from off-chip and copied to block
reference currents using the NMOS current mirrors which are also placed closely, where the current ratio is controlled by the switched transistors.

**Scan Chain**

The digital control bits are stored in the flip-flop chain using three off-chip inputs: data, clock, and load. When the load is 1, the clock is enabled and the serialized bit information is transferred to the chain. When the load is 0, the clock is disabled and the stored data is used to control each block.

**5.7 Integration**

To achieve a fully integrated operation of the transmitter with the on-chip

![Schematic of main bias circuits](image)

Figure 5.12: Schematic of main bias circuits to generate the local reference currents using one off-chip current source.
25 dBm PA, various design and layout techniques are carefully employed in this work to minimize the harmful effects of any potential coupling from the PA to the other TX and RX blocks. First, a fully differential topology is extensively utilized in the TX and RX to mitigate the effects of supply/ground fluctuations. Secondly, the power supplies and ground connections are separated into four domains, i.e., the PA, PA driver, other TX blocks, and RX. In addition, the common source nodes of the PA are isolated from the substrate and connected directly to the ground plane of the PC board through four pads. Of the four pads, one is dedicated to the second-harmonic termination (shown in Figure 5.2) to suppress any voltage fluctuations at $2f_c$ due to the large-signal operation of the PA and its potential coupling into the substrate. Thirdly, triple-well NMOS devices are used ubiquitously in the design, with their bodies split from the chip substrate to achieve better substrate isolation. Substrate taps placed between the PA and other blocks help to pick up any unwanted coupling from the PA, keeping the substrate as quiet as possible.

The test chip was fabricated in a 0.13 µm CMOS process. The die size of the chip is $4.6 \text{ mm}^2$ and its micrograph is shown in Figure 5.13. The RX blocks are placed on the opposite corner of the chip from the PA such that the RX fidelity can be maintained with minimum influence from the PA (for example, RX gain compression can result from a large instantaneous PA output coupled into the RX, which will affect the compensation accuracy of the equalizer).
A stand-alone PA chip is also fabricated in the same process. The schematic is the same as the integrated PA except that the biases for the cascode transistors are internally fixed to 2.5 V. The layout change is also minimal to obtain similar parasitic capacitance to that of the integrated PA. This stand-alone PA helps to (1) accurately characterize the PA performance, (2) estimate the integration effects, and (3) reduce the uncertainty of designing the PA matching network on the board.

Figure 5.13: Die photo of the integrated RF transmitter in 0.13 µm CMOS.
CHAPTER 6

EXPERIMENTAL RESULTS

Although the target frequency was 5 GHz, all the measurements are done at 3.5 GHz, in which the TX gave the best performance. Thus, the on-chip circuits are tuned at 3.5 GHz using the digital bits, and the matching networks on the board are also optimized at this frequency.

6.1 Board Design

Two four-layer printed circuit boards are designed using Allegro and manufactured using Rogers RO4003C; one is the PA board which is for testing the stand-alone Class-B PA and the other is the TX board for testing the digitally equalized TX system. Figure 6.1 shows the simplified schematic of the PA board where the CMOS PA chip, RF passives for the input and output matching, and RF baluns are mounted. On the other hand, the integrated chip, analog-to-digital interfaces with clock buffer chip, RF passives, and power regulators are mounted on the TX board as shown in Figure 6.2. The clock chip buffers an 80 MHz clock
from the signal generator, and provides all clock phases for the DAC, ADC, and FPGA. The TX board is connected directly to the FPGA board using a 70-pin connector, not cables, in order to minimize the clock skews. The direct connection from the DAC outputs to ADC inputs is optional to test the DACs and ADCs.

Three power/ground domains exist to provide 3.3 V for DAC and ADC, 1.2 V for on-chip baseband circuits, and 2.5 V for the PA output stage. The second and third layers are used for ground and power planes, respectively. Regulators receive 5 V input from the power supply and generate the supply voltages in each domain. The area on the top layer not used by signal routing is also used for the grounds, which are connected to the second layer using sufficient vias to provide stable ground connections to the chips. Each supply is bypassed to its corresponding ground through small and large bypass capacitors which are located close to the chips on the top and bottom layers. All RF signal paths are routed on the top layer of the board, and the digital signals use the bottom layer.

Figure 6.1: Schematic of PA board to test the stand-alone PA.
Table 6.1 shows the parameters of RO4003C. The thicknesses of the conductor and dielectric layers are 1.4 mil and 8 mil, respectively. A 50 Ω microstrip line is designed for RF signals, and its dimensions and the simulated

Figure 6.2: Schematic of TX board to test the digitally equalized TX system.
Table 6.1: Parameters of RO4003C.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dielectric Constant (Er)</td>
<td>3.38</td>
</tr>
<tr>
<td>Dissipation Factor (tanδ)</td>
<td>0.0027</td>
</tr>
<tr>
<td>Relative Permeability (Mur)</td>
<td>1</td>
</tr>
<tr>
<td>Conductivity (S/m)</td>
<td>4.1e7</td>
</tr>
</tbody>
</table>

insertion loss are shown in Figure 6.3 (a) and (b), respectively. The line width is 18 mil, which is determined by the built-in function in Allegro and the simulation using ADS Momentum. The lines are tapered near the TX chip to connect them to the small pads, thus minimizing the impedance mismatch.

Figure 6.3: 50 Ω microstrip line and its simulated insertion loss.
The integrated chip is directly mounted on the board and the on-chip pads are connected to off-chip using 1 mil gold bondwires; this is known as chip-on-board (COB) assembly. We used Westbond 747677E bonder after the attachment using a conductive epoxy. Figure 6.4 shows the top layer of the board layout for the COB assembly and TX (or PA) output matching. Multiple 0402 pads, on which RF capacitors are optionally mounted, are placed on the board at TX output for flexibility of PA output matching.

Figure 6.4: Top layer of board layout for the COB assembly and TX output matching.
6.2 Chip Assembly and Input/Output Matching

PA output matching

Figure 6.5 shows the schematic of the PA output matching network which consists of the estimated on-chip capacitances, bondwire inductances, and off-chip passive components. After S-parameters of passive devices are measured after a thru-reflect-line (TRL) calibration, the impedances looking into the board at TX chip outputs are estimated. Then, accounting for the estimated on-chip impedances, the entire matching network of Figure 6.5 is composed in ADS. Lastly, the variables such as the bondwire inductances ($L_M$ and $L_S$), series
capacitance \( (C_s) \), and shunt capacitance \( (C_M) \) are determined to transform 50 Ω to the desired impedance at operating frequencies.

A 1 inch, 50 Ω microstrip line is measured after a TRL calibration and its measured S-parameters are compared to simulated S-parameters using the parameters of Table 6.1 and Figure 6.3. As shown in Figure 6.6, the two results agree well, although the measured S-parameters are noisier; differences in the magnitudes of \( S_{11} \) and \( S_{21} \) are tolerable. Thus, the model using the parameters can safely be used in the design of a PA matching network. \( S_{12} \) and \( S_{22} \) are not shown.

Figure 6.6: S-parameters of 1 inch, 50 Ω microstrip line.
in the figure; however, they are almost the same as $S_{21}$ and $S_{11}$, respectively.

Figure 6.7 shows the model of a Murata 0.4 pF RF capacitor in the 0402 package and its simulated S-parameters, which are well matched to the measured data. A test structure is used for the measurement. The series inductance ($L_p$) and

![Circuit Diagram](image)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>3.5</td>
<td>0.4</td>
<td>0.47</td>
<td>0.3</td>
<td>0.1</td>
</tr>
</tbody>
</table>

(a)

![Graphs](image)

Figure 6.7: (a) Model for a 0.4 pF RF capacitor and (b) its S-parameters.
resistance \( (R_P) \) are from the datasheet provided by the manufacturer, and 0.1 pF shunt capacitances \( (C_P) \) are inserted on both sides to model the parasitic capacitances of pads. \( R_P \) and \( L_P \) are fairly constant across frequencies of interest and core capacitances in the 0402 package.

Two-port S-parameters of an RF balun with SMA connector are measured after terminating the unbalanced port with 50 \( \Omega \), as shown in Figure 6.8 (a). Ideally, there should be no reflection on both ports; however, imperfect interfaces

![Diagram](a)

Figure 6.8: (a) Schematic of a test structure for the S-parameter measurement of an RF balun with SMA connector (SMAs of port 1 and 2 are calibrated out) and (b) the reflection coefficients of the network through an ideal balun.
cause $S_{11}$ to deviate from the origin in the Smith chart as shown in Figure 6.8 (b).

Note that an ideal balun is inserted in ADS to realize differential signaling on balanced ports.

The variables, i.e., $L_M$, $L_S$, $C_M$, and $C_S$, in Figure 6.5 are determined in order to transform 50 Ω to 18 Ω at 3.5 GHz. Note that $C_D$ models on-chip capacitance at the PA output nodes and 2.5 pF is estimated. First, $L_S$ is set to 0.8 nH to tune $C_D$ out. There are multiple solution sets for $L_M$, $C_M$, and $C_S$, and Figure 6.9 shows the transformed impedances using one of them. In this solution, use of $C_M$ is avoided because there is a non-negligible power loss through the path, a series of reactance and resistance. The values for $L_M$ and $C_S$ are practical enough to be implemented and the sensitivity to frequency offsets is also reasonable in this solution.

Figure 6.9: Transformed impedance is $17.6 + j1.8$ Ω at 3.5 GHz. ($L_M$, $L_S$, $C_S$, and $C_D$ in Figure 6.5 are set to 0.4 nH, 0.6 nH, 2 pF, and 0 pF, respectively.)
RX and LO input matching networks

The matching network for RX input is shown in Figure 6.10 (a). The integrated chip has 50 Ω termination resistors at RX input nodes. $C_{IN}$ and $L_M$ model the parasitic capacitances at the down-conversion mixer input and bondwire inductions, respectively. An RF capacitor, $C_M$, is inserted on the board.

Figure 6.10: (a) Schematic of RX input matching network and (b) the magnitudes of reflection coefficients in dB.
to mitigate the effects of $C_{IN}$ and $L_M$, composing a Π-network. Figure 6. 10 (b) shows the measured reflection coefficients in dB at SMA input. The matching networks for LO inputs are very similar to this except that $C_{IN}$ and on-chip 50 Ω are replaced with input impedances of the polyphase filters. The magnitude of the measured reflection coefficient is below -15 dB at 3.5 GHz with the appropriate choice of $C_M$.

6.3 Test Results

For the stand-alone PA test, the RF CW signal is provided by the signal generator and fed into the PA input, and the output power and spectra are measured in the spectrum analyzer as shown in Figure 6.11 (a). On the other hand, for the TX equalization test, the baseband digital signal is downloaded into the memory on the FPGA and sent to the TX board. The experimental setup of the equalization test is shown in Figure 6.11 (b). TX output spectra and RMS EVMs are measured in the signal analyzer. (The built-in demodulator in the signal analyzer is used for the EVM calculation.) The demodulated signal is captured from the signal analyzer and more comprehensively analyzed in MATLAB.
Figure 6.11: Experimental setup for (a) the stand-alone PA and (b) the TX equalization test.
6.3.1 Stand-alone PA

Figure 6.12 shows the measured AM-AM and AM-PM curves along with the drain efficiency of the PA in a stand-alone package. The measured maximum output power was 25 dBm with a peak drain efficiency of 55%. Note that the high power efficiency is achieved at the cost of a non-flat power gain in both the saturated and low-power regions, exhibiting a typical Class-B gain characteristic. The measured peak-to-peak AM-PM error was greater than 15°. These nonlinearities will cause large in-band intermodulation distortions and out-of-band spectral regrowth in adjacent channels, which need to be treated by the digital equalizer.

Figure 6.12: Measured performance of the Class-B PA shown in Figure 5.2 in a stand-alone chip-on-board (COB) package.
6.3.2 TX equalization test

In experiment, the maximum output power of the integrated transmitter was measured at 22.8 dBm, which is 2.2 dB less than that of the stand-alone PA mainly because the on-chip supply of the upconversion mixer limits the input drive of the PA. The peak DE of the integrated PA was also reduced accordingly to 44%.

The feedback path was measured alone by disconnecting the attenuator and connecting the input to a CW source. The measured RX gain from the mixer input to the anti-aliasing LPF output was 6.5 dB; and the I/Q amplitude and phase mismatches of the RX were 0.1 dB and 1.5°, respectively, whose effects on the loopback fidelity were found negligible in experiment. Figure 6.13 shows the

![Figure 6.13: Measured signal quality of the feedback path (down-conversion mixer + anti-aliasing filter + ADC).](image)
measured signal quality of the receive path from the down-conversion mixer input to the ADC output. The peak spurious-free dynamic range (SFDR) and signal-to-noise plus distortion ratio (SNDR) at the ADC output were 50 dB and 38 dB, respectively, when the input power was −9 dBm. Since random noise tends to be averaged out in the LMS loop, the 38 dB SNDR of the feedback path attained in this work was found sufficient to train the equalizer without degrading the steady-state performance of the transmitter.

The effects of equalizer parameters such as step-size in the LMS algorithm, finest table size, and table levels were measured. Figure 6.14 shows mean-square-errors (MSEs) according to the parameters. Note that MSEs are typically a few dB

![Figure 6.14: Effects of step-size and number of tables on equalizer accuracy.](image)

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worse than EVMs because loop-back signals are used for the MSE calculation while an ideal demodulation is used for EVM calculation. When the step-size is small, i.e., 0.002 in Figure 6.14, the error tends to be large because the finite word-length effects are more significant. On the other side, MSEs worsen when both the step-size and the number of tables are large because effective step-size is proportional to the number of tables, and large step-sizes make table coefficients more sensitive to noise and memory effects on loop-back signals.

Figure 6.15 shows the effects of step-size on convergence time. In this experiment, one table of 64×64 is used. As expected, large step-size results in fast convergence; however, MSE results again show that there is an optimum step-size.
for the best steady-state compensation performance. Thus, the step-sizes and tables are chosen after balancing the adaptation speed and steady-state equalization performance.

Figures 6.16 and 6.17 show the measured EVM and ACPR of the transmitter, respectively, with and without digital equalization. The target EVM performance is −25 dB, according to the 802.11a spec. The digital equalizer was implemented in an FPGA (Altera Stratix II). A 64-QAM OFDM signal with 9.6 dB PAPR and 20 MHz bandwidth was applied; 10 bit, 80 MS/s off-chip DACs and ADCs were used; and the cutoff frequencies of the TX and RX filters were set at 34 MHz and 30 MHz, respectively. A 4-level ML-LUT consisting of 64×64,
32×32, 16×16, and 8×8 entries with 15 bit word-length was synthesized in the FPGA.

The RF attenuation, $G_A$, is set between 27 and 36 dB for 8 to 16 dBm average TX output power. Out of this, 14 dB attenuation is derived from the off-chip coupler and the RF signal-path loss, and the rest from the off-chip variable RF attenuator that supports up to 40 dB attenuation in a 0.6 dB step and exhibits a 36 dBm input third-order intercept point (IIP3). Note that the required IIP3 of this block is around 30 dBm in this test setup. We believe the RF attenuators reported in [43] and [61] are suitable for potential integration with our TX.

Figure 6.17: Measured ACPR of the TX with and without equalization.
When the gates of the input devices of the PA output stage were biased at 0.32 V (with a quiescent bias current of 5 mA), the measured EVM floor after equalization was better than −29 dB with a minimum back-off of 8 dB. The EVM was below −26 dB even with a 7 dB back-off, still satisfying the 802.11a spec with 1 dB margin. While the EVM performance stayed put with the gate bias increased toward 0.35 V (Class-AB mode), it was degraded by 1–2 dB when the bias was lowered to 0.29 V (Class-C mode). The measured average DEs with the 0.32 V bias were 12.5% and 17.5% at 9.6 dB and 7 dB back-offs, respectively, all with the same 9.6 dB PAPR OFDM signal. In addition, a 16-QAM OFDM signal with 6.5 dB PAPR and 20 MHz bandwidth was also tried in experiment. With equalization, the measured EVM floor was around −31 dB in this case.

ACPRs in Figure 6.17 are the average of the upper channel ACPR and lower channel ACPR. Although there is no specific spec for ACPR in this application, ACPR below -30 dBc is a necessary condition to satisfy the spectrum mask requirements. It is shown that ACPRs are mostly above -30 dBc without equalization, while they are below -34 dB with equalization when the back-off is more than 8 dB.
Figure 6.18: Measured TX output spectra with and without equalization, where the DAC aliases at ±80 MHz offset from the carrier frequency are clearly visible.

Figure 6.18 shows the measured PA output spectrum when the 64-QAM OFDM signal was used with a 9.6 dB back-off. It satisfies the 802.11a spectrum mask except for a center peak of LO leakage due to the direct-conversion architecture. Spectral regrowth was significantly suppressed, especially in the band offset by 10–20 MHz. Figure 6.19 shows the measured individual EVMs of the 48 data subcarriers, and Figure 6.20 shows the aggregated 64-QAM constellations with and without equalization. The same test setup as in Figure 6.17
Figure 6.19: Measured EVM of individual subcarriers with equalization: (a) for regular 64-QAM OFDM signal with 48 data subcarriers and (b) same as (a) except that a few subcarriers near DC are removed.

Figure 6.20: Measured aggregated 64-QAM constellation of 48 data subcarriers: (a) without equalization and (b) with equalization.
was used. One-tap frequency-domain channel equalization was performed before decoding the transmitted data symbols as is normally done in OFDM receivers.

Due to the extensive use of AC coupling throughout the TX and RX signal paths, the transmission of a few subcarriers around DC was garbled due to the non-flat frequency response within these sub-channels, resulting in their larger-than-average EVMs, which can also be identified in Figure 6.20 (b). Nonetheless, the overall average EVM across all 48 subcarriers was $-29.6$ dB, confirming a successful equalization in the presence of frequency-dependent (memory) errors. In addition, when the sub-channels around DC were excluded, the measured EVM floor was improved by about 1 dB. The EVM performance was otherwise quite flat and under $-30$ dB or so, indicating that the memory effects in the loop are insignificant across the rest of the 20 MHz bandwidth.

In our experiment, a 34 MHz cutoff frequency of the TX LPF and an 80 MHz DAC sample rate were found sufficient to satisfy the spectrum mask without additional oversampling. The 5th-order frequency response of the Butterworth LPF proves to be instrumental here to retain all desired spread spectrum due to predistortion and yet maintain low OSR.

Table 6.2 summarizes the measurement results of the prototype CMOS transmitter, where the reported value of power-added efficiency (PAE) accounts for the power consumption of the PA driver. The equalizer adaptation time to reach $-26$ dB EVM was 2.3 ms measured from a power-on reset with all LUT
content set to default values. In a more practical operation, the converged LUT contents can be saved as the initial condition of the next adaptation, which will significantly speed up the training as quite a few operating parameters of the TX are time invariant. In addition, the tracking of TX variations due to the output power back-off during normal operation is much faster in this prototype as the power control is separate from equalization, as explained in Chapter 4.

Table 6.2: TX performance summary.

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.13 µm CMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Frequency</td>
<td>3.55 GHz</td>
</tr>
<tr>
<td>Max. Output Power</td>
<td>22.8 dBm</td>
</tr>
<tr>
<td>Max. PA Drain Efficiency</td>
<td>44%</td>
</tr>
<tr>
<td>Max. PA PAE</td>
<td>39%</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.2 V / 2.5 V</td>
</tr>
</tbody>
</table>
| Power Consumption | TX filter + mixer: 17 mW  
                      RX filter + mixer: 12.7 mW  
                      PA driver: 60 mW |
| Die Size | 1.7 × 2.7 mm² |
| w/o EQ | w/ EQ |
| Signal Type | 64-QAM OFDM with 9.6 dB PAPR |
| Signal Bandwidth | 20 MHz |
| Avg. TX Output Power | 13.2 dBm |
| Avg. PA Drain Efficiency | 12.9%  
                          12.5% |
| EVM | -20.9 dB  
     -29.6 dB |
| Convergence Time | 2.3 ms |
CHAPTER 7

CONCLUSIONS

In this research, the CMOS integration of RF PAs and the digital treatment of TX analog/RF impairments are proposed as a cost-effective solution for wireless RF transmitters. The digital equalizer greatly relaxes the TX linearity requirements, enabling highly power-efficient RF PA to be employed. In this work, high efficiency of the RF PA is achieved by dynamic current biasing and less back-off. Thus, the PA does not need to be overdesigned to tolerate the large back-off. In addition, the relaxed linearity requirements throughout the TX path increase the TX dynamic range because the signal swing is untied from the linearity, which facilitates the CMOS integration of the RF PA. In summary, the digital equalizer not only improves the PA power efficiency but also helps the PA integration in CMOS process.

A 2-D LUT equalizer is adopted to equalize the phase as well as the amplitude-related errors; all the memoryless errors are treated in this way. TX memory errors are compensated not in the equalizer, but in the circuits. To make
the equalization be effective in practice, the adaptive coefficient update in the
equalizer is crucial not only because of the PVT variations in the chip but also the
operating environment variations. A gradient-descent algorithm updates the
coefficients in the way that the power of errors between the original signals and
the loop-back signals is minimized. The normal RX path can be reused to deliver
the TX errors in real time, but a much cheaper feedback path is dedicated in this
work. All the requirements of the normal RX path regarding gain, noise, and
memory-related errors are loose because the signal strength is large at the
feedback input and the errors are averaged out in the LMS algorithms as far as
they are uncorrelated with the original signal. However, the memoryless errors do
need to be limited so that the target TX performances are satisfied.

Convergence speed is another concern of the adaptive equalization.
Although large step sizes in the LMS are better for fast convergence, they are first
limited by the stability of the LMS loop and additionally by the quality of the
loop-back signal. Thus, SNR of the loop-back signal is maintained above 30 dB,
compromising the complexity of the feedback path with the convergence speed.
The effects of the loop’s non-flat frequency response due to the AC coupling
network and the low-pass filters are mitigated by filtering the error signal using a
digital band-pass filter. The multilevel LUT approach also aids fast convergence
by parallelizing the fast/coarse equalization path and the slow/fine equalization
path. Lastly, the power control is separated from the equalization to minimize the equalizer coefficient variation during power control.

Adaptive transmitter equalization is demonstrated in a 3.5 GHz, 0.13 µm CMOS RF transmitter with an on-chip, nonlinear power amplifier. Superior EVM performance and high peak/average PAE were achieved simultaneously in experiments by treating the memoryless nonlinearities and I/Q mismatch of the entire transmit signal path. The digital-intensive approach proves to be a viable and efficient solution to the issue of stringent power efficiency and linearity trade-offs in highly integrated CMOS transmitters for current and future radio standards.
APPENDIX A

DERIVATION OF POWER EFFICIENCY OF L-MATCHING NETWORK WITH LOSSY INDUCTOR

Figure A.1: L-matching network with lossy inductor.

It is first assumed that $R_X$ is smaller than $R_{ANT}$. In Figure A.1, $R_p$ models the source of power loss in the inductor, $L_M$, and the inductor quality factor is defined as
\[ Q_L \equiv \frac{X_S}{R_P}. \tag{A.1} \]

The quality factor of \( L \)-type matching network is defined as

\[ Q_M \equiv \frac{X_S}{R_X}. \tag{A.2} \]

To transform \( R_{\text{ANT}} \) to \( R_X \), the following two conditions need to be satisfied:

\[ X_S = -\frac{X_P R_{\text{ANT}}^2}{X_P^2 + R_{\text{ANT}}^2}, \tag{A.3} \]

\[ R_X = -\frac{X_P^2 R_{\text{ANT}}}{X_P^2 + R_{\text{ANT}}^2}. \tag{A.4} \]

By Equations (A.3) and (A.4), Equation (A.2) becomes

\[ Q_M = \sqrt{\frac{R_{\text{ANT}}}{R_X}} - 1. \tag{A.5} \]

The load resistance, \( R_L \), is determined by

\[ R_L = R_X + R_{\text{ANT}} = \frac{V_{DD}^2}{2P_{PA}}. \tag{A.6} \]

The power efficiency of the matching network is defined and expressed as

\[ \eta_{\text{MN}} \equiv 1 - \frac{P_{\text{LOSS}}}{P_{PA}} = \frac{R_X}{R_L}. \tag{A.7} \]

By Equations (A.1) and (A.2), Equation (A.7) becomes

\[ \eta_{\text{MN}} = \frac{Q_L}{Q_L + Q_M}, \tag{A.7} \]

and \( R_X \) and \( R_P \) are calculated using (A.1), (A.2), and (A.6) as
\[ R_P = \frac{V_{DD}^2}{2P_{PA}} \frac{Q_M}{Q_M + Q_M} = \frac{V_{DD}^2}{2P_{PA}} \left(1 - \eta_{MN}\right) , \quad (A.8 \text{ a}) \]

\[ R_X = \frac{V_{DD}^2}{2P_{PA}} \frac{Q_L}{Q_L + Q_M} = \frac{V_{DD}^2}{2P_{PA}} \eta_{MN} . \quad (A.8 \text{ b}) \]

By (A.8 b) and (A.5), \( Q_M \) can be written as

\[ Q_M = \sqrt{\frac{2P_{PA}R_{ANT}}{V_{DD}^2\eta_{MN}}} - 1 . \quad (A.9) \]

By substituting (A.9) into (A.7) and solving it, the power efficiency is expressed with the PA maximum output power \( (P_{PA}) \), supply voltage \( (V_{DD}) \), antenna impedance \( (R_{ANT}, \text{typically 50} \, \Omega) \), and inductor Q-factor \( (Q_L) \). 

\[ \eta_{MN} = \frac{Q_L^2V_{DD}^2 + R_{ANT}P_{PA} - \sqrt{R_{ANT}^2P_{PA}^2 + 2R_{ANT}Q_L^2V_{DD}^2P_{PA} - Q_L^2V_{DD}^2}}{V_{DD}^2(Q_L^2 + 1)} . \quad (A.10) \]
REFERENCES


AUTHOR’S BIOGRAPHY

Dae Hyun Kwon was born in Andong, South Korea, in 1976. He received the B.S. degree in electronics engineering from Korea University, Seoul, Korea, in 2002 and the M.S. degree in electrical engineering and computer sciences from Seoul National University, Seoul, Korea, in 2004. In 2005, he joined the Analog IC Group as a research assistant under Professor Yun Chiu at the University of Illinois at Urbana-Champaign. Following the completion of his Ph.D., he will begin work for Broadcom Corporation as a staff engineer in its wireless connectivity group.

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