PERFORMANCE ENHANCEMENT OF GaN-BASED HIGH-POWER HEMTS BY SELECTIVE-AREA GROWTH USING PLASMA-ASSISTED MOLECULAR BEAM EPITAXY

BY

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THESIS

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Urbana, Illinois

Adviser:

Professor Kyekyoon Kim
This thesis work presents a comprehensive study of the application of the PAMBE-SAG technique to fabrication of high-power GaN-based switching HEMTs. First, a detailed study of the efficacy of SAG was conducted by comparing it with ion-implantation, a popular technique for improving Ohmic contacts. A consistent improvement in device performance by SAG was achieved, including lower contact resistance, higher peak drain currents and higher breakdown voltages. Since the results indicated that SAG is effective in fabricating HEMTs for high power applications, it was then employed to fabricate large-periphery AlGaN/GaN HEMTs for high current operation. A high saturation current of 1.75A and low on-state resistance of 4.76mΩ cm² for a total gate width of 5.2mm were achieved. Finally, a study on enhancement of the breakdown voltage was conducted. For the first time, the use of sputtered-SiO₂ as the gate insulator was investigated. Good oxide film quality was confirmed by a low leakage current of 2.76x10⁻⁶ A/mm and a high gate breakdown voltage of 250V. A dual-SiO₂-deposition method which incorporates both PECVD-SiO₂ and sputtered-SiO₂ was then proposed to solve the problem of reduction in current caused by sputtering. The MOSHEMT fabricated using this method showed more than twofold increase in the current when compared with a regular HEMT without oxide insulation. A high breakdown voltage of 620V at 6µm gate-to-drain distance was also achieved, demonstrating that the oxide film made by our dual-SiO₂-deposition approach is a more effective gate insulator for breakdown voltage enhancement than many techniques previously reported.
ACKNOWLEDGMENTS

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Finally, I would like to extend special thanks to my parents for their constant love and support, and especially to my wife, Jing Gao, for her understanding and patience, and most importantly, her trust and willingness to spend the rest of her life with me.
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1. INTRODUCTION

1.1 Review of Gallium Nitride for Power Switching Transistors

Due to many favorable electronic properties such as high critical breakdown field, high saturation electron velocity, and good thermal conductivity, GaN has become a very promising candidate material for high-temperature, high-frequency and high-power transistors.\(^1\) GaN-based transistors also have good chemical inactivity and can be operated in harsh environments commonly encountered in satellite and military communications. Table 1.1 compares the important material properties of GaN with Si, GaAs and SiC.\(^2\)

Among the above-mentioned applications, GaN is especially suited for power transistors, which play a crucial role in the regulation and distribution of power and energy in different social areas. Power transistors used in systems can be broadly classified into two categories: power rectifiers and power switches. Silicon has long been the dominant choice for high voltage power switching devices. However, it is rapidly approaching the theoretical limits of performance. GaN offers several potential advantages over silicon like higher blocking voltage, higher operating temperature, lower power losses and faster switching speeds, and thus it can be very useful in a wide range of applications that require voltage blocking capability in the 100-1500V range, current carrying capability in the 1-10A range, ultra low on-resistance and high temperature capability. Some of the prominent applications of GaN-based high power transistors are shown in Fig. 1.1.\(^3\)
1.2 Background and Motivation

For any high-power electronic device, the challenge lies in controlling the flow of high power while keeping its power dissipation as low as possible. However, due to the wide band gap of GaN, it is difficult to achieve low-resistance Ohmic contacts, which can lead to significant power losses in GaN-based power transistors. Moreover, the most important parameters of a power switching device are the breakdown voltage $V_B$ and on-state resistance $R_{on}$, whose relationship is determined by Equation (1.1):

$$R_{on} = \frac{4V_B^2}{\varepsilon_s \varepsilon_c^3 \mu_n}$$  \hspace{1cm} (1.1)

In general, the channel doping level should be increased to provide a low $R_{on}$. But since $V_B$ is related to the double integration of the doping level along the depletion region, it drops at a square rate with the decrease of $R_{on}$. Likewise, when effort is invested in improving $V_B$, an increase in $R_{on}$ is inevitable. In order to make the power device figure-of-merit $V_B^2/R_{on}$ as large as possible, a low Ohmic-contact resistance, the dominating factor of on-resistance, is strongly desired. For decades, much effort has been placed on obtaining low Ohmic-contact resistance, utilizing techniques including ion-implantation, surface treatment and selective area growth. Selective area growth (SAG) is a very effective technique for improving the Ohmic contacts, since it deposits a highly doped GaN layer in the Ohmic contact regions which can enhance tunneling transport of electrons, as shown in Fig. 1.2.\(^4\) SAG has been achieved by metal-organic chemical vapor deposition (MOCVD)\(^5\) and hydride vapor phase epitaxy (HVPE),\(^6\) but the regrowth method by plasma-assisted molecular beam epitaxy (PAMBE) did not attract attention due to a lack of growth selectivity. However, PAMBE-SAG was realized in our previous studies, and was demonstrated to significantly improve the Ohmic contacts.
1.3 Thesis Overview

The main objective of this study is to utilize the PAMBE-SAG technique to explore the possibility of fabricating AlGaN/GaN high electron mobility transistors (HEMTs) for high-power switching applications. The experimental setups will be briefly presented in Chapter 2. In Chapter 3, PAMBE-SAG is compared with the ion-implantation technique, and the advantages of SAG are demonstrated in terms of the Ohmic contact resistance, saturation drain current density and breakdown voltage. Following this, in Chapter 4, large-periphery AlGaN/GaN HEMTs are fabricated via SAG to demonstrate a large operating current and low on-state resistance. In Chapter 5, the use of sputtered-SiO$_2$ as the gate insulator is investigated for improving the breakdown voltage, and a dual-SiO$_2$-deposition method is proposed. Finally, a summary of the work and suggestions for future work will be presented.
1.4 Figures and Table

Fig. 1.1. Applications of GaN-based power switching transistors.

Fig. 1.2. Mechanism of electron tunneling in the ohmic contact region facilitated by SAG.
Table 1.1 Semiconductor material properties at 300 K.

<table>
<thead>
<tr>
<th>Property</th>
<th>Si</th>
<th>GaAs</th>
<th>4H-SiC</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap $E_g$ (eV)</td>
<td>1.12</td>
<td>1.42</td>
<td>3.25</td>
<td>3.40</td>
</tr>
<tr>
<td>Breakdown field $E_B$ (MV/cm)</td>
<td>0.25</td>
<td>0.4</td>
<td>3.0</td>
<td>4.0</td>
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<tr>
<td>Electron mobility $\mu$ (cm$^2$/V s)</td>
<td>1350</td>
<td>6000</td>
<td>800</td>
<td>1300</td>
</tr>
<tr>
<td>Maximum velocity $v_s$ (10$^7$ cm/s)</td>
<td>1.0</td>
<td>2.0</td>
<td>2.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Thermal conductivity $\chi$ (W/cm K)</td>
<td>1.5</td>
<td>0.5</td>
<td>4.9</td>
<td>1.3</td>
</tr>
<tr>
<td>Dielectric constant $\varepsilon$</td>
<td>11.8</td>
<td>12.8</td>
<td>9.7</td>
<td>9.0</td>
</tr>
</tbody>
</table>
2. EXPERIMENTAL SETUP

2.1 Plasma-Assisted Molecular Beam Epitaxy System

The PAMBE system constructed in our laboratory is used for the growth of III-nitride semiconductor films. As shown in Fig. 2.1, the system consists of a turbomolecular pumped liquid nitrogen (LN\textsubscript{2}) coldwall chamber with base pressure of $2 \times 10^{-10}$ torr, a bottom flange with eight ports for standard effusion cells containing Ga, In, Al, Si and Mg, an inductively coupled radio-frequency (RF) plasma source and a rotatable substrate holder/heater for holding substrates of up to 3 in diameter. The substrate holder is introduced through a load-lock chamber connected to a turbomolecular pump.\textsuperscript{7}

High-purity Ga (99.99999 \%) and Si (99.99999\%) were used as the group III element and n-type doping element, respectively. To contain the source materials, high-purity refractive materials (pyrolytic boron nitride (PBN)) and water cooling systems were used to minimize contamination.\textsuperscript{8} Very large scale integration (VLSI) grade (99.9995 \%) nitrogen gas was used as the group V element, and the diatomic species was cracked by a 13.56 MHz RF power supply to generate reactive atomic nitrogen plasma at a low background pressure of $2 \times 10^{-4}$ torr. The flow rate of high purity nitrogen into the RF plasma source was controlled by a mass flow controller (MFC).

2.2 Sample Growth

MOCVD-grown AlGaN/GaN templates were used as the growth substrate. Mo block, PBN retaining ring and UNI-block tungsten substrate holder were used to mount the substrate, which was subsequently introduced into the growth chamber through the load-lock chamber. Generally,
in MBE systems, high-quality GaN films are grown under Ga-rich conditions and the growth rate is limited by the atomic nitrogen flux and, in turn, by the nitrogen flow rate. During the growth process, the nitrogen flow rate was maintained at 0.3 sccm while using an RF power of 356W. The smallest possible flow rate, which corresponds to the slowest possible growth rate (3.5 nm/min), results in the optimum surface morphology and electronic properties of the films. The temperatures of the Ga effusion cell, Si effusion cell and the substrate were set respectively at 1000°C, 1300°C and 880°C, as determined by previous studies to be the optimum conditions for SAG. During the growth, LN2 was flowed through the cooling lines attached to the MBE chamber.

2.3 Sample Fabrication and Characterization

For device fabrication (Fig. 2.2 (a)~(f)), a Karl Suss MJB-3 contact aligner was used for photolithography, and a Plasma Therm SLR-770 inductively coupled plasma reactive ion etcher (ICP-RIE) was used for dry etching of GaN and AlGaN layers. A plasma enhanced chemical vapor deposition (PECVD) system was used to deposit SiO2, and a Plasmalab Freon/O2 RIE system was used for SiO2 dry etching. In addition, a Cooke E-beam/thermal evaporator was used to deposit contact metals, a Jipelet rapid thermal processor was used for rapid thermal annealing (RTA), and a 4524 Au Wire Ball Bonder was used for wire-bonding.

For characterization, surface morphology of the films after SAG was investigated using a Digital Instruments / Veeco Dimension 3100 atomic force microscope (AFM). I-V characteristics of HEMT devices were measured by HP4155C semiconductor analyzers with ICS software. Large current and breakdown voltage measurements were conducted using a Tektronix 371 high power curve tracer via a probe-station custom-built for high-power measurements.
2.4 Figures

Fig. 2.1. Schematic diagram of PAMBE system used in this study.
Fig. 2.2. (a) Karl Suss MJB-3 contact aligner, (b) Plasma Therm SLR-770 inductively coupled plasma reactive ion etcher, (c) Plasma enhanced chemical vapor deposition system, (d) Plasmalab Freon/O2 RIE system, (e) Cooke E-beam/thermal evaporator, and (f) Jipelet rapid thermal processor.
3. ENHANCEMENT OF BREAKDOWN VOLTAGE VIA SAG OVER ION-IMPLANTATION

In developing GaN-based power transistors, there are two key challenges: achievement of a low on-state resistance (including low-resistance Ohmic contacts) and a high breakdown voltage. Among the efforts to realize the former, ion-implantation is a technology widely accepted by the semiconductor industry. Already, there are an abundance of studies involving application of ion-implantation for the GaN Ohmic contacts.\textsuperscript{9-13} Satoh et al. demonstrated an ultra-low resistive Ohmic contact with a specific contact resistivity of $1.2 \times 10^{-7} \ \Omega \text{cm}^2$.\textsuperscript{14} Recht et al. reported a contact resistance of $0.96 \Omega \text{mm}$ for non-alloyed Ohmic contacts.\textsuperscript{15} However, ion-implantation generally involves high energy radiation, which gives rise to damage at the GaN surface and a dense network of defect clusters in the doped region. Moreover, to remove damage and to activate the dopants, a post-annealing process must be performed at temperatures above $1100^\circ C$.\textsuperscript{16} Such high temperatures can cause problems including GaN film dissociation, Si dopant diffusion and surface degradation.

In an effort to resolve these difficulties, selective area growth (SAG) using highly doped $n$-type GaN can be employed. Compared to MOCVD and HVPE, PAMBE has long been ignored as an effective method for SAG. However, PAMBE-SAG has an advantage in that the growth temperature is much lower compared to MOCVD and HVPE, typically reduced by $300^\circ C$ to $400^\circ C$. In our previous studies, we were able to realize SAG with PAMBE achieving a record-low contact resistivity of $1.8 \times 10^{-8} \ \Omega \text{cm}^2$ for the Ohmic contacts to an $n$-type GaN channel of a metal-semiconductor field-effect transistor (MESFET),\textsuperscript{17} as well as an extremely low non-
alloyed contact resistance of 0.6Ω mm for the contacts to a 2-dimensional electron gas (2DEG) channel in an AlGaN/GaN high electron mobility transistor (HEMT). These results not only demonstrate the advantage of SAG over the conventional contact scheme, but also indicate that SAG may be a better choice over ion-implantation in fabricating Ohmic contacts. Furthermore, due to the damage-free nature of SAG technique, we deduce that it should yield higher breakdown voltages than by using ion-implantation, which are crucial for high-power GaN devices. The damage caused by the high implantation energy and the roughness of the resulting GaN interface due to the high activation temperature could give rise to severe current leakage, thus degrading the breakdown behavior. Compared to ion-implantation, SAG is a low-temperature process that effectively avoids damage to the device, which can lead to substantial enhancement of the breakdown voltage. In this chapter, we examine the advantages of SAG over ion-implantation for HEMTs and demonstrate that SAG not only provides better Ohmic contacts and dc characteristics, but also enables much higher breakdown voltages. Two different substrates, sapphire and silicon, are employed to prove that the effectiveness of SAG is independent of the substrate used.

3.1 Experimental Procedures

The starting material used in this study consisted of two Al$_{0.15}$Ga$_{0.85}$N(30nm) / GaN(200nm) / semi-insulating GaN(2.5µm) templates grown on sapphire(0001) substrate and two Al$_{0.28}$Ga$_{0.72}$N(20nm)/semi-insulating GaN(1.3µm) templates grown on silicon(111) substrate, both grown by MOCVD. For device isolation, 400nm thick AlGaN/GaN layers were etched using ICP-RIE with a Cl$_2$/Ar plasma. Then, out of each set of substrates, one sample was treated
via silicon implantation and the other using the SAG technique. Silicon implantation was carried out at room temperature under the condition of 80keV energy and 5x10^{14}/cm^2 dose. The sample was subsequently annealed at 1200°C for 30s in N₂ ambience using RTA to activate the implanted Si dopants. For the sample employing SAG, as shown in Fig. 3.1, a 160nm thick SiO₂ mask was deposited using plasma-enhanced chemical vapor deposition at 300°C. Photolithography and Freon RIE etching were performed to remove the SiO₂ layer in the source and drain regions. The exposed AlGaN surface was chemically cleaned using acetone, methanol and IPA. A heavily doped GaN layer (n=10^{19}cm^{-3}) was subsequently regrown on the surface using PAMBE at 880°C. During the regrowth process, 60nm thick single-crystal GaN was grown on the contact regions while polycrystalline GaN layer was formed over the SiO₂ mask simultaneously. The single-crystal GaN was grown at a rate of 3.5nm/min. The polycrystalline layer was subsequently removed using a heated 15wt% KOH solution at 75°C and the underlying SiO₂ layer was etched using a buffered oxide etchant.

After the solvent cleaning, the samples were dipped in HCl:H₂O (1:2) solution for 30 seconds, followed by a DI water rinse, to remove the surface oxide prior to contact metal deposition. The Ohmic contact metal multilayers consisting of Ti/Al/Ti/Au (30nm/90nm/30nm/60nm) were fabricated via photolithography, e-beam evaporation, and lift-off process, followed by a 30-second RTA at 830°C in N₂ ambience. Ni/Au (60nm/130nm) were then deposited as the Schottky gate contact. The gate length, width, source-to-drain and gate-to-drain distances were 2µm, 100µm, 6µm and 2µm, respectively. For illustration, cross-sectional diagrams of the HEMTs on sapphire using SAG and ion-implantation are shown in Fig. 3.2.
3.2 Results and Discussion

To compare the resulting contact resistances, transmission line method (TLM) was used. A detailed explanation of TLM can be found elsewhere. The size of the metal pads was 50x25µm² and the gap spacing between the contact pads varied from 5 to 15µm. The current was measured at voltages between −1V and +1V. The current-voltage (I-V) characteristics of the TLM pattern with 10µm pad spacing are shown in Fig. 3.3(a). Samples via both SAG and ion-implantation exhibited linear Ohmic behavior, but the contacts with SAG resulted in much higher currents, indicating that transport of electrons through the metal/AlGaN barrier is more facilitated by SAG. The specific contact resistivities and contact resistances were calculated using the plot of the total resistance as a function of gap spacing (Fig. 3.3(b)). The detailed information on each sample is provided in Table 3.1. When compared with samples via implantation, for both sapphire and silicon substrates, much smaller specific contact resistivities and contact resistances were observed when SAG was employed. The best sample, the one via SAG on sapphire substrate, exhibited a specific contact resistivity of 5.86x10⁻⁷Ω cm² and a contact resistance of 0.46Ω mm. The improvement of the Ohmic contacts may be due to the undamaged n⁺-GaN surface in contact with the metal electrodes where the bonding states and atomic arrangements are well defined, as well as the confinement of Si dopants in the n⁺-GaN region that preserves the carrier concentration. By contrast, the damage caused by implanted ions and the subsequent high temperature annealing may result in surface degradation and dopant diffusion.

To compare the DC performance, I_{ds}-V_{ds} curves were measured. As shown in Fig. 3.4, for sapphire substrate, the peak drain current of HEMT via SAG (420mA/mm) nearly doubled...
that via implantation (250mA/mm). This pattern was consistent for samples on silicon substrate, whose maximum drain currents were 370mA/mm and 320mA/mm for SAG and implantation, respectively. The increase in the peak drain current by SAG is the direct result of the better Ohmic contacts. Moreover, it has been shown that ion-implantation reduces the carrier mobility in the 2DEG, which may be attributed to the high annealing temperature for silicon activation that roughens the channel interface.\textsuperscript{19} The low temperature process of SAG maintains the interfacial sharpness, which may give rise to higher carrier mobility and peak drain current.

Finally, the breakdown behavior was examined. Figure 3.5 shows the off-state ($V_g = -10\text{V}$) breakdown voltages for all four samples. For the SAG sample on sapphire substrate, a breakdown voltage of 77V was achieved, more than twice that of the implanted sample (34V). For silicon substrate, a nearly doubled breakdown voltage was also observed, in which the sample via SAG was 56V, whereas the sample via implantation was 30V. Regardless of the substrate used, a large increase in breakdown voltage was realized when SAG was implemented.

The improvement in the breakdown behavior may be attributed to the damage-free fabrication process of SAG in comparison to implantation. In ion-implantation, an energetic ion penetrates into the GaN crystal beneath the drain region which produces a collision cascade that generates defects and vacancies, which increase the leakage current to the drain contact, either from the surface or from the GaN buffer layer. By contrast, the SAG process avoids creating defects in the doped region, thereby suppressing the drain leakage current and improving the breakdown behavior. Thus-obtained highest breakdown voltage of 77V is comparable to or better than HEMTs of the same dimension that employed a wide-bandgap AlGaN buffer layer,\textsuperscript{20} gate insulator,\textsuperscript{21} or low-density-drain structure,\textsuperscript{22} all designed to enhance the breakdown behavior.
Hence, there may still be room to further increase the breakdown voltage if we combine SAG with the other techniques mentioned above.

### 3.3 Conclusions

We have compared the impact of PAMBE-SAG and ion-implantation on the electronic properties of HEMTs on both sapphire and silicon substrates. A consistent improvement in device performance by SAG was achieved. Samples treated with SAG exhibited improved Ohmic contacts and higher peak drain currents, as well as twofold increase in the breakdown voltages compared to those processed using ion-implantation. These results indicate that SAG is effective in fabricating HEMTs for high-power applications.
Fig. 3.1. Process to regrow an $n^+$-GaN layer on only source and drain regions using PAMBE, with AFM images showing the surface morphology before and after KOH etching.
Fig. 3.2. Schematics of the HEMT structure on sapphire substrate via (a) SAG and (b) ion-implantation.
Fig. 3.3. (a) The I-V curves of TLM pattern with 10µm pad spacing, and (b) the total resistance as a function of gap spacing.
Fig. 3.4. The $I_d$-$V_d$ characteristics of samples on (a) sapphire substrate and (b) silicon substrate.
Fig. 3.5. The off-state $I_d - V_d$ curves of samples on (a) sapphire substrate, and (b) silicon substrate.
Table 3.1 Specific contact resistivity and contact resistance of each sample.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Specific Contact Resistivity $\rho_c$ (Ω cm$^2$)</th>
<th>Contact Resistance $R_c$ (Ω mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAG on sapphire</td>
<td>5.86x10$^{-7}$</td>
<td>0.46</td>
</tr>
<tr>
<td>Implantation on sapphire</td>
<td>2.83x10$^{-6}$</td>
<td>0.96</td>
</tr>
<tr>
<td>SAG on silicon</td>
<td>1.04x10$^{-6}$</td>
<td>0.58</td>
</tr>
<tr>
<td>Implantation on silicon</td>
<td>9.05x10$^{-6}$</td>
<td>2.88</td>
</tr>
</tbody>
</table>
4. HIGH-CURRENT OPERATION FOR LARGE-PERIPHERY AlGaN/GaN HEMTS

For GaN-based power transistors, although much progress has been made on microwave power devices, power switching devices are still a new and immature research area, despite the fact that they have had wide applications in inverters and power converters. Recently, some groups have demonstrated GaN-based high power switching transistors using either HEMT or metal-insulator-semiconductor (MIS)-HEMT structures, but further expectations are placed on device performance enhancement to realize higher power handling capacity, smaller footprint and reduced power loss. Since we have already demonstrated the efficacy of SAG in the improvement of high-power device characteristics, it is time to further utilize this technique to fabricate large-periphery AlGaN/GaN HEMTs for high-power operation. The term “large-periphery” refers to HEMTs with large area, or more specifically, large gate width. Since the saturation drain current of a HEMT is linearly proportional to its gate width, increasing the gate width is the most direct way to increase the operating current. However, it should be noted that it also complicates the fabrication during the photolithography and gate metal lift-off processes, since the gate can be easily broken if the aspect ratio is too high. Thus, a multi-gate design with moderate gate aspect ratio was carried out in which each device unit consists of four HEMTs \( W_g=100\mu\text{m} \) sharing the same source, drain and gate electrodes, as shown in Fig. 4.1. The total gate width of this device unit is 400 µm, with tapers at the edges of gate to prevent disconnection. Different numbers of device units were then interconnected by wire-bonding for parallel current accumulation. Longer gate widths were also investigated, as shown in Fig. 4.2, and
interconnection of 128 HEMTs ($W_g=1.28\text{cm}$) was achieved without the occurrence of gate disconnection.

4.1 New Mask for Large-Periphery HEMTs

Samples were fabricated based on a new mask designed by CAD (Fig.4.3). The blocks labeled MESA, SD and Gate stand for the masks for MESA isolation, source / drain metal contacts and gate metal contact, respectively. There are also two additional blocks, labeled Passivation and Isolation, which were used when we employed the field-plate (FP) principle in our design for breakdown voltage enhancement. The application of FP was originally proposed in the context of high voltage planar p-n junctions, and was extended to silicon MOSFETs and then to III-V MESFETs. By connecting a metal plate to the gate or source electrode and placing it in the gate-to-drain separation region over a uniform insulator, the peak electric field present at the edge of the gate can be reduced to improve the breakdown behavior. The schematic of FP structure and a simulation of the electric field distribution along the 2DEG are shown in Fig. 4.4. The HEMT structure with FP used in this study is shown in Fig. 4.5. This structure exhibits two advantages: 1. the extension of the gate into the drain side can be used for electric field relaxation; 2. the total gate area can be enlarged without increasing the actual gate length, which helps to decrease the gate aspect ratio and reduce the possibility of the gate mechanically breaking. To realize this structure, Si$_3$N$_4$ was used as the supporting dielectric material, due to its larger dielectric constant compared to SiO$_2$. A trench was etched in the gate region for deposition of a T-shaped gate. During the fabrication process, the Passivation mask was used to define the deposited Si$_3$N$_4$ layer in areas other than the source and drain regions, and the Isolation mask was used to define the trench.
4.2 Experimental Procedures

The template material in this study was an Al_{0.26}Ga_{0.74}N(25nm) / GaN(50nm) / semi-insulating GaN(2.2μm) on sapphire substrate prepared by MOCVD. The electron concentration and mobility of the 2DEG were measured by a Hall-effect measurement system at room temperature to be $1.3 \times 10^{13} \text{ cm}^{-2}$ and 1340 cm$^2$/V s, respectively. 220nm MESA isolation and 44nm recessed drain/source structures were formed by dry etching. The SAG process was then implemented in the same procedures as described previously, except that the regrown $n^+$-GaN thickness was changed to 54nm to further optimize the Ohmic contacts. Alloyed metals of Ti/Al/Ti/Au were subsequently deposited on $n^+$-GaN for the Ohmic contacts. After that, 200nm Si$_3$N$_4$ was deposited by PECVD and selectively etched in the source and drain regions. The trench with an opening window of 4μm was then made in the gate region, and the structure was confirmed by AFM (Fig. 4.6). Following this, Ni/Au metals for the Schottky gate contact were deposited over the trench. The extensions of the gate into the source and drain regions were 1 μm and 4μm, respectively. After device fabrication, different numbers of device units were interconnected by wire-bonding to achieve large current capability. A photographic flowchart of the fabrication process is shown in Fig. 4.7.

4.3 High-Current Measurement Setup

Since a reasonable target current was several amperes, the probe station that we usually use in the clean room of the ECE 444 Lab is not suited. Firstly, due to the limitations of the HP4155C semiconductor analyzers, an output power higher than the compliance ($I_{\text{max}}=100\text{mA}$ and $V_{\text{max}}=100\text{V}$) could not be measured. Consequently, a Tektronix 371 high power curve tracer was instead used, which has a power handling capacity of 3KV, 400A and 3KW. In addition, the
tungsten probes which are typically used were too sharp. As a result, during high current measurement, the current density at the probe tips would be too high, resulting in melting of the tips and destruction of the device under test (DUT). Therefore, probe modification was carried out by removing the tips and roughening the probes to make them approximately as thick as 22 gauge wire, which has a diameter of ~0.6mm and current handling capacity of 7A. Tests were then conducted by connecting wires to both ends of the probes and providing current through a power supply. The probes became hot upon reaching 10A, but were still able to operate.

In addition, the thicknesses of the metal pads of source, drain and gate regions have to be determined. Thicker metal plates than previous experimental conditions are needed as the large current flow during measurement could generate sufficient heat to cause the metal to fuse if it is too thin. In theory, thicker gold pads should lead to reduced resistance and thus reduced heat. But in practice, since the cost of gold is high, a minimal amount should be used. Different thicknesses of Au pads were fabricated and tested, and it was found that 1µm thick Au can withstand up to 4A, which is sufficient for the high current measurement. Thus, an additional step was added to the fabrication process in evaporating 1µm gold on the opening windows of source, drain and gate as the wire bonding pads.

4.4 Results and Discussion

Figure 4.8 compares the $I_{ds}$-$V_{ds}$ characteristics of two device units, one with SAG and the other without, with gate voltage ($V_{gs}$) varying from 0V to -8V in -1V steps. Good pinch-off behavior was found for both samples. The device unit processed via SAG demonstrated a maximum current of over 100mA (limited by the analyzer), which was more than twice that of the unit without SAG (41mA). The increase in current was a direct result of the improved Ohmic
contacts produced by SAG, as can be seen from the $I$-$V$ curve. Accordingly, significant improvement in the on-state resistance was also observed (2.1mΩ cm$^2$ for the device with SAG and 7.5mΩ cm$^2$ for the device without SAG).

Figure 4.9(a) shows the saturation drain current ($V_g$=0V) of five interconnected device units. The measured current was 690mA, about five times the saturation current of a single device unit. A linear relationship between the unit number and current level was found. A maximum current of 1.75A ($V_g$=0V) was achieved when thirteen device units were interconnected, as shown in Fig. 4.9(b), corresponding to a total gate width of 5.2mm. The resulting current density of 337mA/mm was higher than many of the previously reported values,$^{31-35}$ demonstrating that the same current level can be achieved by smaller device areas when SAG is employed. Larger currents can then be supported by simply interconnecting more device units in parallel, which is currently being implemented. The on-state resistance was calculated to be 4.76mΩ cm$^2$. The increased $R_{on}$ of the large-periphery device compared with a single device unit was due to the parasitic resistance of connection lines, as well as non-uniformity in the fabrication. Nevertheless, the present $R_{on}$ is better than values for many large-periphery GaN power transistors previously reported,$^{23,33,35,36}$ demonstrating that SAG is effective for achieving low on-resistance for low power-loss switching devices. However, it is difficult to pinch off the current for this large-periphery device, which may result from the increased gate leakage current. The gate leakage current is the dominant component of the off-state drain current, which may get worse due to the heat generated during large current operation. The gate leakage current was deduced to result from defects at the AlGaN surface of the templates used. This severely limited the breakdown voltage of the HEMTs fabricated, as will be discussed in Chapter 5.
4.5 Conclusions

SAG was employed to fabricate AlGaN/GaN HEMTs for large-current operation. Device units consisting of four HEMTs sharing the same source, drain and gate electrodes were made. The sample treated via SAG showed significant improvement in saturation current and on-state resistance relative to the one fabricated without SAG. Large-periphery HEMTs were realized by wire-bonding interconnection, leading to a maximum saturation current of 1.75A and an on-state resistance of 4.76mΩ cm² at a total gate width of 5.2mm. These characteristics were better than many of the previously reported values for large-periphery GaN HEMTs as power transistors.
4.6 Figures

Fig. 4.1. Schematic illustration of single device unit consisting of four HEMTs.

Fig. 4.2. Multi-gate HEMT with different gate widths (a) 400µm, (b) 800µm, (c) 1.6mm, (d) 3.2mm, (e) 6.4mm and (f) 1.28cm.
Fig. 4.3. Mask designed for large-periphery HEMT fabrication. A FP structure is included in this design.
Fig. 4.4. (a) Schematic illustration of the FP structure, and (b) simulated distribution of the electric field along the 2-DEG with and without a FP.
Fig. 4.5. Schematic illustration of a HEMT structure with FP.
Fig. 4.6. AFM images showing the 3D structure of the Si$_3$N$_4$ trench and the section analysis which confirmed the trench depth.
Fig. 4.7. Photographic images of the sample after each step of fabrication: (a) MESA etching, (b) Recessed source/drain etching, (c) SAG, (d) Ohmic metal deposition, (e) Ohmic metal annealing, (f) Si₃N₄ deposition, (g) Si₃N₄ selective etching, (h) Si₃N₄ trench etching and (i) Gate metal deposition.
Fig. 4.8. (a) I-V characteristics of AlGaN/GaN HEMT with SAG and (b) I-V characteristics of GaN HEMT without SAG. The maximum current level is limited by the Agilent 4155C semiconductor parameter analyzer.
Fig. 4.9. (a) I-V characteristics of five device units interconnected by wire-bonding and (b) I-V characteristics of thirteen device units interconnected by wire-bonding (Total $W_g=5.2\text{mm}$).
5. DUAL-$\text{SiO}_2$-DEPOSITION FOR IMPROVEMENT IN BREAKDOWN VOLTAGE

Despite the merits of high current density and low on-state resistance, the fabricated large-periphery HEMTs were not able to withstand voltage over 50V owing to the large gate leakage current as previously mentioned. The detrimental effect of gate leakage on breakdown voltage has long been observed for GaAs MESFETs.$^{37}$ The gate leakage current becomes an even larger problem as the device operating temperature increases because of the enhanced thermionic emission over the Schottky barrier. Unexpectedly, we found that the use of the FP structure did not contribute much to breakdown voltage enhancement, since premature breakdown occurs prior to the electrical field at the gate edge reaching its critical value. From the previous study, we conclude that gate leakage current is a predominant factor in determining the breakdown behavior. FP can only be used to further improve the breakdown voltage when the gate leakage current has been sufficiently suppressed.

It has been extensively reported that by employing an insulating film under the gate, the gate leakage current can be dramatically reduced. A MOS structure using $\text{SiO}_2$ was applied to GaN HEMTs, which lowered the gate leakage by 5 orders of magnitude.$^{38}$ Other insulating layers, including $\text{Al}_2\text{O}_3$, $\text{Si}_3\text{N}_4$ and high-$k$ materials like $\text{TiO}_2$, $\text{HfO}_2$ and $\text{ZrO}_2$, have also been applied. Due to the simple deposition process, low cost and good integration with silicon semiconductor, $\text{SiO}_2$ is a good choice for gate insulation. The quality of the deposited film is the main factor that determines the amount of leakage current that can flow through it. Generally, this $\text{SiO}_2$ layer is deposited by PECVD or E-beam evaporation. However, due to the unsatisfactory quality of the deposited $\text{SiO}_2$, very large gate-to-drain distance, usually 20~30µm,
has been required to achieve a breakdown voltage over 1000V. Large $L_{gd}$ not only increases the device footprint, but also reduces the operating current due to the increased channel resistance. For the first time in this study, high-vacuum magnetron sputtering was investigated as an alternative deposition method for the SiO$_2$ insulator. In a sputtering process, energetic atoms can reach the surface with large momentum due to the acceleration of the electric field from the target to the substrate, and thus can produce more compact film with better oxide quality than PECVD or E-beam evaporation.

5.1 Sole-SiO$_2$-Deposition by Sputtering

The same device template was used as in Chapter 4, in order to test the effect of the gate insulator on breakdown voltage by direct comparison. The experimental procedures for MESA isolation, recessed source/drain etching, Ohmic metals and Schottky metals deposition were the same as previously described. SAG was not included in this study for simplification. For gate insulation, 10nm SiO$_2$ was deposited by high-vacuum magnetron sputtering at the gate region prior to metal depositions. The sputtering process was done by a Lesker PVD 75 sputter system which contains two 3in sputter guns that can operate in Ar, O$_2$ or N$_2$ ambience. The computerized control system precisely controls the turbomolecular pump speed and the gas flow. A large rotating sample plate could hold sample sizes up to 12in diameter. Quartz lamps provide sample heating to 300°C. In this study, sputtering was carried out at a constant power of 300W and at a total pressure of 2mTorr in Ar:O$_2$ (85:15) plasma.

Schottky gate properties were tested after sample fabrication. The gate-to-drain distance was 6µm. $I_g$-$V_g$ characteristic showed that the gate leakage current was as low as $2.76 \times 10^{-6}$A/mm.
at $V_g = -50\text{V}$. As a result, the gate breakdown voltage measured by the curve tracer was 250V, with a low leakage current of $7.5 \times 10^{-4}\text{A/mm}$ at the breakdown voltage (Fig. 5.1). The low leakage current and the high breakdown voltage demonstrate the effectiveness of using sputtered-SiO$_2$ as the gate insulator. But unexpectedly, the current level dropped dramatically to less than 1mA after SiO$_2$ deposition, as shown in Fig. 5.2(a). The current level could not be recovered when the SiO$_2$ layer was removed, indicating that some permanent damage had been produced.

5.2 Dual-SiO$_2$-Deposition by PECVD/Sputtering

We deduced that the reason for the reduction in current could be the depletion of the 2DEG during the sputtering process. As previously mentioned, sputtering is a high energy process, in which the atoms are accelerated from the target and strike the AlGaN surface with high momentum. The bombardment of atoms may cause damage to the AlGaN surface. In AlGaN/GaN HEMTs, the source of the 2DEG is the donor-like surface states. Damage to the AlGaN surface may reduce the density of the surface states, leading to a reduction in the electron concentration in the 2DEG. This current reduction phenomenon has never been observed when using PECVD or E-beam evaporation, since these two processes are far less energetic. To prove this assumption, an additional 10nm SiO$_2$ layer was deposited by PECVD beforehand as a buffer layer. Another 10nm SiO$_2$ layer was then deposited by sputtering under the same experimental conditions. As shown in Fig. 5.2(b), there is significant improvement in the current, with the maximum current over 0.1A. This result is strong evidence for our assumption that the layer of PECVD SiO$_2$ is effective in protecting the AlGaN surface from the bombardment by sputtered
atoms. As a result, we found that the current level not only recovered, but also increased to nearly the same value as was achieved by SAG. We deduce that the increase in the current may be caused by tensile strain in the oxide layers. This tensile strain can not only increase the electron mobility, but may induce larger piezoelectric effects and band-bending at the AlGaN/GaN interface that can result in higher electron concentrations in the 2DEG. A detailed study will soon be carried out by measuring the electron concentration and mobility using a HL5500PC van der Pauw Hall measurement system, as well as the film stress after deposition using a FSM 500TC film stress measurement system.

5.3 Influence of Film Thickness on Current Level and Breakdown Voltage

To find the thicknesses of the two oxide layers which optimize the current and the breakdown voltage, different thickness combinations were tested. By increasing the thickness of sputtered-SiO$_2$ layer from 10nm to 50nm, it was found that the gate leakage current decreases dramatically, as shown in Fig. 5.3. However, it was also found that when the PECVD-SiO$_2$ thickness is much less than that of the sputtered-SiO$_2$, the current level drops due to insufficient protection by the PECVD buffer layer. For example, 4nm PECVD-SiO$_2$ / 13nm sputtered-SiO$_2$ and 15nm PECVD-SiO$_2$ / 50nm sputtered-SiO$_2$ showed maximum currents of only 3.5mA and 7.5mA respectively (Fig. 5.4). It was therefore concluded that in order to maintain a high operating current, the two oxide thicknesses should be similar.

The breakdown characteristics of the sample described in Section 5.2 were then tested with implementing 10nm PECVD-SiO$_2$ / 10nm sputtered-SiO$_2$ layers. Although the gate breakdown voltage was larger than 200V, a high leakage current of 2.5mA/mm at breakdown
was found. Such a high leakage current is not acceptable when a large on-to-off ratio is desired. To further improve the breakdown behavior, the oxide thicknesses were increased to 20nm for the PECVD-SiO$_2$ and 25nm for the sputtered-SiO$_2$. The I-V characteristic (Fig. 5.5(a)) showed an unharmed operating current, with maximum current over 0.1A. Significant improvement in the current was demonstrated when compared to the HEMT of the same dimension without any oxide insulation (Fig. 5.5 (b)). In addition, the device showed no commonly observed abnormal $I$–$V$ characteristics at positive gate biases, as seen in PECVD-grown SiO$_2$ MOSHEMTs, which are generally related to bulk or interfacial traps in the oxide film. This is another indication of the good oxide film quality achieved by our method. From the transfer characteristics, the maximum transconductance was calculated to be 43mS/mm. This value is comparable to that of the GaN HEMT or MESFET previously fabricated in our group, demonstrating that the transconductance is not significantly deteriorated by the oxide. However, there are two disadvantages caused by introduction of the oxide:

1. More negative threshold voltage. $V_T$ was -12V for the current MOSHEMT compared to -8V for the regular HEMT we previously fabricated. The larger $V_T$ resulted from the higher gate potential drop within the oxide, and can be solved by etching a portion of the AlGaN layer in order to reduce the distance from the gate to the 2DEG.

2. Larger on-state resistance. The increase in on-resistance is usually observed when a MOS structure is applied to a HEMT. This problem can be solved by incorporating SAG into the MOSHEMT structure, which will soon be studied.

The breakdown characteristics of this MOSHEMT structure were then measured. A low leakage current of $5 \times 10^{-6}$A/mm was achieved at $V_g = -130$V (Fig. 5.6) and the maximum gate breakdown voltage was measured to be 360V (Fig. 5.7). The three-terminal breakdown voltage
(source-to-drain breakdown) was also measured for this device. The maximum off-state breakdown voltage at $V_g = -12\text{V}$ was as high as 620V (Fig. 5.8). The 620V breakdown voltage with $L_{gd}=6\mu\text{m}$ is larger than the MOSFET structures using PECVD SiO$_2^{35,40}$ or E-beam SiO$_2^3$ having the same dimension, showing that the dual-SiO$_2$-deposition method is able to produce better oxide quality. This breakdown voltage is also higher than other HEMTs which utilized Al$_2$O$_3^{41}$ or high-$k$ dielectric insulators$^{21,42}$ as well as field-plate structures,$^{43,44}$ when they are scaled to the same dimension as ours, demonstrating the efficacy of our dual-SiO$_2$-deposition method for breakdown voltage enhancement.

### 5.4 Conclusions

For the first time, SiO$_2$ gate insulator by high-vacuum magnetron sputtering was studied for GaN-based HEMTs. The compact and dense oxide film deposited by sputtering resulted in low gate leakage current of $2.76\times10^{-6}\text{A/mm}$ at $V_g = -50\text{V}$ and a reverse breakdown voltage of 250V. In order to prevent current reduction caused by the sputtering damage to the AlGaN surface, PECVD SiO$_2$ was used as a buffer layer and thus a dual-SiO$_2$-deposition method was established. A MOSHEMT fabricated using this new hybrid SiO$_2$-deposition method showed significant improvement of drain saturation current, which we deduce results from the tensile strain which enhances the piezoelectric effect and causes more band-bending at the AlGaN/GaN interface. Additionally, a three-terminal breakdown voltage as high as 620V was achieved at $L_{gd}=6\mu\text{m}$. This result is not only better than the MOSHEMTs that used PECVD-SiO$_2$ or E-beam SiO$_2$, but also exceeds the values of those HEMTs which employed other dielectric materials or field-plate structures, all designed to enhance the breakdown behavior. Since these methods
increase either the fabrication cost or complexity, our simple and cost-effective dual-SiO$_2$-deposition approach is promising for fabrication of GaN-based MOSHEMTs for high-power applications.
5.5 Figures

Fig. 5.1. (a) Gate leakage current characteristics and (b) Gate breakdown characteristics.
Fig. 5.2. (a) I-V curve after 10nm SiO₂ deposition by sputtering, and (b) I-V curve after 10nm SiO₂ deposition by PECVD and 10nm SiO₂ deposition by sputtering. $V_g$ varied from 0V in -1V steps.
Fig. 5.3. Decrease of gate leakage current as a function of sputtered-SiO$_2$ thickness.
Fig. 5.4. (a) I-V curve after the deposition of 4nm PECVD-SiO$_2$ / 13nm sputtered-SiO$_2$ and (b) I-V curve after the deposition of 15nm PECVD-SiO$_2$ / 50nm sputtered-SiO$_2$. $V_g$ varied from 0V in -1V steps.
Fig. 5.5. (a) I-V curve after the deposition of 20nm PECVD-SiO$_2$ / 25nm sputtered-SiO$_2$, and (b) I-V curve for HEMT of the same dimension but without any oxide insulation. V$_g$ varied from 0V in -1V steps.
Fig. 5.6. Gate leakage current characteristics up to $V_{dg}=130$V. Breakdown did not occur at this voltage.
Fig. 5.7. Gate breakdown characteristics. The breakdown voltage shown in the figure is 360V.
Fig. 5.8. Three-terminal (off-state source-to-drain) breakdown characteristic. The breakdown voltage shown in the figure is 620V.
6. SUMMARY AND FUTURE WORK

The application of the PAMBE-SAG technique for high-power GaN-based switching HEMTs was investigated. In Chapter 3, a detailed study of the efficacy of SAG was conducted by comparing it with ion-implantation, a popular technique for Ohmic contact enhancement. A consistent improvement in device performance by SAG was achieved, including lower contact resistance, higher peak drain currents and higher breakdown voltages. Since these results indicated that SAG was effective in fabricating HEMTs for high-power applications, it was then employed to fabricate large-periphery AlGaN/GaN HEMTs in Chapter 4. A high saturation current of 1.75A and low on-state resistance of 4.76mΩ cm² at a total gate width of 5.2mm was achieved. These characteristics were better than many of the previously reported values for large-periphery GaN HEMTs. In Chapter 5, the use of sputtered-SiO₂ as gate insulator was investigated. Good oxide film quality was confirmed by a low leakage current of 2.76x10⁻⁶A/mm and a high gate breakdown voltage of 250V. A dual-SiO₂-deposition method which incorporated both PECVD-SiO₂ and sputtered-SiO₂ was then established to solve the current reduction problem caused by sputtering. The resulting MOSHEMT fabricated using this method showed more than twofold increase in the current level when compared to the conventional HEMT with no oxide insulation. A high breakdown voltage of 620V at 6µm gate-to-drain distance was also achieved, demonstrating that the oxide film made by our dual-SiO₂-deposition approach is a more effective gate insulator for breakdown voltage enhancement than many techniques previously reported.

The study of the improvement in breakdown voltage is still in progress. Associated problems such as a more negative threshold voltage and increased on-state resistance need to be
resolved. The former can be overcome by thinning the AlGaN layer of the template, and the latter can be solved when we incorporate SAG in the device fabrication. A detailed study of the reason for the current enhancement by the oxide layer remains to be performed. The stress in the films, as well as the electron concentration and mobility of the 2DEG after oxide deposition must be measured and analyzed. These experiments will soon be carried out.

The switching characteristics of the fabricated HEMTs need to be measured by RF techniques in the future. Improvements in the cutoff frequency ($f_t$) and the power-added efficiency (PAE) are expected due to the lower Ohmic contact resistance achieved using SAG. Lower current dispersion is also expected since the SiO$_2$ insulator can serve as a surface passivation layer. Finally, high-power converters using the fabricated HEMTs should be demonstrated.
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