MODELING AND SUPPRESSION OF LATCHUP

BY

FARZAN FARBIZ

DISSERTATION

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Doctoral Committee:

Professor Elyse Rosenbaum, Chair
Professor Milton Feng
Professor José E. Schutt-Ainé
Professor Shyh-Jye Jou
ABSTRACT

In this dissertation, an experimental study of latchup is conducted. A semi-physical analytical model is proposed that estimates the latchup susceptibility of a design prior to fabrication. The model can easily be implemented in a circuit simulator and be simulated together with the rest of the design.

We will show that depending on the bias conditions and layout geometry, electrons or holes can trigger latchup. Latchup hazards caused by holes and electron injection are studied.

The roles of guard rings are investigated. The impacts of N-type and P-type guard rings are reported. The guard-ring efficacy under high-level injection conditions and short injection pulse durations are also reported. We show that N-well guard rings in particular become less efficient as the amount of injection increases or when the injection-pulse duration is shortened. The effects of guard rings are incorporated into the model.

We demonstrate that whether electron injection or hole injection is the worst case, that is, has the lowest latchup susceptibility, depends on the pulse-width of the injection current. Electron injection is the worst case condition during static latchup testing, i.e., when the injection pulse-width is long. This condition is generally used for product qualification. However, real world stresses, such as cable discharges, are transient, in which case hole injection is the worst case condition.
Chapters 1 and 2 give background on latchup. They explain the difference between internal and external latchup and show that latchup can be triggered by static or transient events. A brief history of previous work on latchup is presented.

Chapter 3 focuses on internal latchup. Latchup triggering modes and characterization methods are explained.

Chapter 4 is devoted to analysis of external latchup and the standard latchup tests. The term collection efficiency is defined in this chapter to represent the number of injected carriers participating in triggering latchup. Circuit-level models are proposed to understand latchup behavior under various testing conditions. These circuit schematics provide a base for modeling latchup susceptibility later in Chapter 6.

Measurement results of the collection efficiency and external latchup trigger current are presented and investigated in Chapter 5. The effects of layout geometry are studied. Guard ring interactions and their effect on latchup resilience are explained.

A model for the external latchup trigger current is proposed and compared to the measurement results in Chapter 6. The model can be used in a circuit simulator to estimate the latchup susceptibility of a layout. The model captures the effects of the guard rings.

Transient latchup testing is discussed in Chapter 7. The worst-case testing conditions for static and transient latchup are reported. Guard rings are evaluated under transient latchup testing. Finally, conclusions are drawn and future work is suggested in Chapter 8.
To my parents and my brothers
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# TABLE OF CONTENTS

CHAPTER 1 INTRODUCTION .................................................................................................................. 1  
  1.1 Motivation ........................................................................................................................................ 1  
  1.2 Dissertation Overview ..................................................................................................................... 2  

CHAPTER 2 LATCHUP BACKGROUND .................................................................................................... 4  
  2.1 Substrate Current Injectors ............................................................................................................. 6  
  2.2 Cable Discharge Event .................................................................................................................... 7  
  2.3 Literature Review ........................................................................................................................... 8  
  2.4 Figures ............................................................................................................................................ 10  

CHAPTER 3 INTERNAL LATCHUP ....................................................................................................... 13  
  3.1 PNPN Triggering Modes ................................................................................................................. 13  
    3.1.1 Overshoot and undershoot on PNPN terminals ......................................................................... 13  
    3.1.2 Overvoltage/avalanching N-well junction .............................................................................. 13  
    3.1.3 Punchthrough ......................................................................................................................... 14  
  3.2 Latchup Characterization ............................................................................................................... 14  
    3.2.1 Two-terminal characterizations ............................................................................................ 15  
    3.2.2 Four-terminal characterizations ............................................................................................ 16  
  3.3 Figures ............................................................................................................................................ 17  

CHAPTER 4 EXTERNAL LATCHUP ..................................................................................................... 21  
  4.1 Analysis of External Latchup .......................................................................................................... 21  
    4.1.1 Negative I-test ....................................................................................................................... 22  
    4.1.2 Positive I-test ....................................................................................................................... 24  
    4.1.3 Undervoltage on V_{DDO} ..................................................................................................... 25  
    4.1.4 Considerations for the substrate current .............................................................................. 26  
  4.2 Figures ............................................................................................................................................ 28  

CHAPTER 5 MEASUREMENT RESULTS AND DISCUSSIONS .............................................................. 33  
  5.1 Test Structures ............................................................................................................................... 33  
  5.2 Collection Efficiency ...................................................................................................................... 34  
    5.2.1 Layout geometry ..................................................................................................................... 34  
    5.2.2 Temperature ......................................................................................................................... 35  
    5.2.3 Bias conditions ....................................................................................................................... 35  
    5.2.4 N-well guard rings ............................................................................................................... 37
5.2.5 Multiple detectors ........................................................................................................... 38
5.2.6 P-type guard rings ........................................................................................................... 39
5.2.7 P-well taps ....................................................................................................................... 40
5.3 Measurement Results of I_{\text{trig}} .................................................................................. 41
5.4 Figures ............................................................................................................................... 43
5.5 Tables ................................................................................................................................ 58

CHAPTER 6 MODELING THE LATCHUP TRIGGER CURRENT ........................................... 59
6.1 Collection Efficiency of a Single Detector ........................................................................ 59
6.1.1 Effects of spacing ........................................................................................................... 59
6.1.2 Effects of bias voltage .................................................................................................... 70
6.1.3 Effects of temperature .................................................................................................... 72
6.1.4 Effects of injection current ............................................................................................. 73
6.2 Effects of Guard Rings on the Collection Efficiency ......................................................... 75
6.2.1 Modeling $\alpha^{*}_{\text{NW}}$ ................................................................................................. 75
6.3 Modeling the Latchup Trigger Current ............................................................................ 81
6.3.1 Parameter extraction .................................................................................................... 83
6.4 Figures ................................................................................................................................ 84
6.5 Table .................................................................................................................................. 98

CHAPTER 7 TRANSIENT LATCHUP TESTING .................................................................... 99
7.1 Experimental Setup ......................................................................................................... 99
7.2 Results and Discussions ................................................................................................... 101
7.2.1 Pulse-width dependence ............................................................................................... 101
7.2.2 Effect of trigger source rise-time ................................................................................. 105
7.2.3 Orientation of the victim ............................................................................................... 107
7.2.4 Guard ring efficiency under TLU testing ................................................................. 109
7.2.5 Triple well technology ................................................................................................. 109
7.2.6 Negative I-test vs. positive I-test .................................................................................. 110
7.3 Modeling and Simulations ............................................................................................... 110
7.4 Figures ................................................................................................................................ 112

CHAPTER 8 CONCLUSIONS AND FUTURE WORK ......................................................... 125
8.1 Conclusions ....................................................................................................................... 125
8.2 Future Work ...................................................................................................................... 128
8.2.1 Negative I-test ............................................................................................................. 128
8.2.2 Positive injection ......................................................................................................... 129
8.2.3 Transient latchup ......................................................................................................... 129
8.2.4 Latchup and substrate noise ................................................................. 129
8.3 Figure ......................................................................................................... 130

REFERENCES ............................................................................................................ 131
1.1 Motivation

Latchup is a CMOS integrated circuit failure mechanism characterized by excessive current flow between the power supply and ground rails. It may be a temporary state that is eliminated upon removal of the exciting stimulus, a catastrophic state requiring shutdown of the system in order to clear, or a fatal state requiring that the damaged device be replaced.

Integrated circuits can be protected against latchup by use of guard rings. Guard rings are commonly used to improve the latchup resilience of CMOS chips. Efficiency of the guard rings in mitigating latchup hazards depends on the type of guard rings, i.e., P-well or N-well rings, and their design, i.e., the layout geometry. These issues are described below.

N-well and P-well guard rings are available in a design kit. The former is recommended for preventing latchup caused by electrons, and the latter for latchup by holes. Therefore, before choosing the appropriate guard rings, one must decide which type of carrier, electron or hole, is more likely to trigger latchup. This is no trivial task without having a good understanding of how latchup is triggered in the circuit.
As a general rule, wider guard rings are more effective in preventing latchup. However, wider guard rings consume more area and, hence, are more expensive. The minimum required guard ring width is always preferred to minimize cost. A model for latchup that includes the effects of the guard ring geometry can be used to design the guard rings.

These issues can be addressed by analyzing latchup and the effect of guard rings under various testing conditions. If a model for latchup were available, the designer could simulate the circuit and estimate the latchup susceptibility of the chip. If the effects of guard rings were included in the model, the designer could simulate different geometries and design the optimum guard ring.

The purpose of this work is, first, to understand how latchup is triggered in a circuit under various testing conditions. Next, it will develop a geometry-dependent physical model for latchup that can determine the latchup susceptibility of a layout prior to fabrication. With such a model in hand, layout can be analyzed to ensure that the product will pass the latchup tests [1].

1.2 Dissertation Overview

Chapter 2 gives background on latchup. It explains the difference between internal and external latchup. It shows that latchup can be triggered by static or transient events. A brief history of previous work on latchup is presented.

Chapter 3 focuses on internal latchup. Latchup triggering modes and characterization methods are explained.
Chapter 4 is devoted to analysis of external latchup and the standard latchup tests. The term *collection efficiency* is defined in this chapter to represent the number of injected carriers participating in triggering latchup. Circuit level models are proposed to understand latchup behavior under various testing conditions. These circuit schematics provide a base for modeling latchup susceptibility later in Chapter 6.

Measurement results of the collection efficiency and external latchup trigger current are presented and investigated in Chapter 5. The effects of layout geometry are studied. Guard ring interactions and their effect on latchup resilience are explained.

A model for the external latchup trigger current is proposed and compared to the measurement results in Chapter 6. The model can be used in a circuit simulator to estimate the latchup susceptibility of a layout. The model captures the effects of the guard rings.

Transient latchup testing is discussed in Chapter 7. The worst case testing conditions for static and transient latchup are reported. Guard rings are evaluated under transient latchup testing. Finally, conclusions are drawn and future work is suggested in Chapter 8.
CHAPTER 2

LATCHUP BACKGROUND

Latchup is a potential hazard in every technology that requires both kinds of MOS transistors, NMOS and PMOS, on a single substrate, meaning that both N- and P-type wells are needed. NMOS and PMOS transistors are formed by creating the N-well, P-well, P⁺ diffusion, and N⁺ diffusions shown in Figure 2-1. Unfortunately, CMOS transistors are not the only structures that exist; PNPN devices consisting of two parasitic bipolar transistors are also made. The first transistor is a PNP formed by P⁺ diffusion, N-well, and P-well. The second is an NPN transistor formed by N⁺ diffusion, P-well, and N-well. These two transistors form a PNPN that lies between V_DD and V_SS. Under normal operating conditions, the PNPN does not conduct current and remains in the off state. However, as a result of a sudden change in the supply voltage, it may switch to a low-impedance state and create a short circuit path between V_DD and the ground (Figure 2-1). The CMOS structure may be permanently damaged depending on the amount of current flowing through the short circuit path.

Figure 2-2 shows the device cross-section of a two-terminal PNPN, as well as its IV characteristics. If the voltage across the PNPN is less than the switching voltage (V_S), it remains off and, the current drawn from the power supply will be only that dissipated in the functional circuitry. However, if the voltage is higher than V_S, the PNPN switches to a low-impedance state.
When the PNPN is triggered by an undershoot or an overvoltage on one of its terminals, it is called *internal latchup* because the stress source was directly connected to the PNPN structure. Another form of latchup is when the stress source is placed away from the PNPN and is called *external latchup*. Figure 2-3 shows a substrate current injector, called *the injector*, next to a CMOS inverter. During an event, carriers may be injected to the substrate by the injector. The parasitic PNPN associated with the inverter, called *the victim* in this work, may be latched if NW (*the detector*) or PW collects enough numbers of injected carriers from the substrate. The minimum injected current at the injector that results in external latchup is denoted as the trigger current, $I_{\text{trig}}$.

Electronic products are usually required to pass static and, sometimes, transient latchup tests. In static latchup testing, the injection source has a long pulse duration (10 µs-1 s) and slow rise-time (5 µs-5 ms) [1]. It consists of I-tests and overvoltage tests. I-tests refer to injection of positive and negative current into each input, output, or I/O pin, and overvoltage tests refer to overvoltage testing of each supply pin.

The setup for static latchup testing is fairly simple. However, static latchup tests are not believed to emulate real-world transient disturbances that could trigger latchup. Such events have short pulse duration (hundreds of nanoseconds) and fast rise-time (a few nanoseconds). For example, a cable discharge event, described later in this chapter, can be as short as 100s of ns. Testing under short pulse durations is called transient latchup (TLU) testing. A variety of non-standardized procedures have been proposed for TLU testing. One such test is described in a recommended practice document published by the ESD Association [2]; in this test, the stimulus—a negative voltage pulse—is applied directly to the supply terminal of the PNPN device, placing it in the category of
static latchup testing. More relevant to this work is the transient I-test [3], [4], in which the trigger source is a current pulse with short pulse duration and fast rise-time. Details of the experimental setup for the transient I-test are given in Section 7.1.

Latchup is the result of current flow in the substrate. The current is due to carriers injected into the substrate by substrate carrier injectors, which are commonly formed as parasitic devices connected to signal pins. They are explained in the next section.

2.1 Substrate Current Injectors

Figure 2-4 shows a typical I/O circuitry. The power supply and ground rails in an I/O domain are connected to $V_{DDIO}$ and $V_{SSIO}$, respectively. Two types of substrate current injectors are found at I/O pads: bottom injectors and top injectors. A bottom injector is connected between an I/O pad and $V_{SSIO}$, while a top injector is connected between an I/O pad and $V_{DDIO}$. The bottom injector may be either an ESD protection device, e.g., a diode, or the drain/body junction of an NMOS transistor. The top injector may be either an ESD protection device or the drain/body junction of a PMOS transistor. In this work, without loss of generality, P-well and N-well diodes are used as the bottom and top injectors, respectively.

When a PN junction is forward-biased, carriers are injected from one side to the other. For instance, consider an $N^+$ diffusion forming a diode with the grounded P-substrate. This $N^+$ diffusion may be the source or drain of an NMOS transistor. Electrons are injected into the substrate when the diode is forward-biased by an undershoot on the $N^+$ diffusion.
There are several causes for such voltage undershoots. It is true that the substrate is always tied to the lowest voltage in the circuit, $V_{SS}$, and that all of the $N^+$-substrate PN junctions are reverse-biased in a CMOS device. However, capacitive coupling and cross-talk may transiently reduce the voltage of a node below $V_{SS}$. Another possible reason for forward-biasing a substrate diode is a cable discharge event (CDE). Diodes tied to the I/O pads may turn on and inject carriers into the substrate as a result of a CDE.

2.2 Cable Discharge Event

A cable discharge event (CDE) is a real reliability issue in the networking industry that may lead to permanent device malfunction [5]. A CDE occurs when charge is injected into a circuit as a result of plugging in a cable. The charge transfer from the high to the low potential causes a current flow and likely permanent damage [6]. A twisted-pair cable can store charge quite like a capacitor. The conductors inside the cable and ground are the capacitor plates, and the cable insulator acts as the dielectric. While CDE is relevant to virtually any twisted-pair cable, Ethernet cables have captured the most attention [7].

Charge may be stored in a cable from several sources. For example, dragging a cable across a carpet will result in an accumulated charge. Another example is charge induced from adjacent electromagnetic fields. Once charged, the cable may retain the charge for several hours. High-quality Ethernet cables, for instance, retain the stored charge for more than 24 hours [8].

There are several ways to prevent CDE damage at an end-user’s side. One is ensuring that the cable is discharged to ground before plugging into a circuit, preventing
the charge injection. Another is to power down the system before connecting the cable. While these methods can prevent or reduce CDE damage, they may be inconvenient or even unfeasible in some cases.

2.3 Literature Review

While latchup is typically known as a reliability issue for commercial semiconductor products, historically, it was first observed in space applications [9], [10]. The low-power advantage of CMOS technology made it the best choice for implementing space circuitry. However, these devices frequently failed when they were exposed to single-particle radiation, an unavoidable situation in space applications [11]. It was later found that CMOS devices may be triggered into a low-impedance mode in radiation environments [12].

Latchup was not considered a reliability issue for commercial semiconductor products until the mid-1970s, when scientists at Sandia National Laboratory found that there were other latchup triggering modes besides high-energy particles [13]–[17]. By dramatically scaling the channel length of transistors and progressively integrating devices in a single chip, latchup became a major issue in commercial semiconductor products in the mid-1980s [18], [19]. Several triggering modes relevant to commercial products were investigated by Troutman [20]. Based on these investigations, circuit and device techniques were proposed to eliminate the hazard [21], [22]. A few models were proposed to predict latchup susceptibility [23]–[25]. Latchup testing procedures were documented as a JEDEC standard in 1988 [26].
Years later, it was shown that plugging a charged cable into a system may trigger latchup in a circuit [5]. This triggering mode is considered as external latchup because latchup is triggered as a result of injection elsewhere in the circuit, for example in an I/O pad [27]. For example, if electrons are injected into the substrate, depending on the carrier lifetime, some of the injected carriers find the way to the devices [3]. Carrier lifetime depends on substrate doping. Low-doped substrates are now typically used to reduce noise coupling and achieve high Q for passive elements in RF applications [28].

Despite all of its advantages, using a low-doped substrate comes with increased carrier lifetime. Hence, with a low-doped substrate, minority carriers have a greater chance to survive and trigger latchup before recombining with the majority carriers. Furthermore, spacing between I/O pads and CMOS devices has been reduced with the increased focus on cost, density, and high level of integration. When I/O pads are placed closer to the core circuitry, more carriers reach CMOS devices. This is of great concern especially in flip chip technologies where I/O pins are placed very close to the core circuitry. Therefore, the technology trend has increased the susceptibility of CMOS devices to external latchup.

Latchup can be investigated by performing device simulations [29], [30]. The device parameters such as doping levels must be well calibrated in order to get predictive results. The calibration procedure is complicated and performing the simulations is always time consuming.

Ever since latchup was identified as a concern for commercial electronic devices, the need for a model that predicts susceptibility of a circuit has emerged [31]. In [6], a simple model is proposed that estimates the number of carriers in the substrate at a
distance $r$ from the injection source. The model is entirely empirical and incapable of capturing the effects of layout geometry. The effects of guard rings are not incorporated in the model, which makes it impractical for most real design situations, where guard rings are always used.

Electrons or holes can trigger latchup in a circuit. Kontos claims that electrons are more likely to trigger latchup [4]. We will show that this is too general a claim. Latchup triggered by electrons or holes could be the worst case, depending on the layout and bias conditions.

Kontos and Domanski report that $I_{\text{trig}}$ of transient latchup is a decreasing function of the pulse-width of the injection current [3], [4]. Nevertheless, they do not explain why this is so. We will mathematically show why $I_{\text{trig}}$ is a decreasing function of the pulse-width. We will also show that the pulse-width dependence depends on whether latchup is triggered by electrons or holes.

2.4 Figures

![Diagram of CMOS device showing parasitic bipolar transistors](image)

Figure 2-1: Device cross-section of a CMOS device showing the parasitic bipolar transistors.
Figure 2-2: (a) PNPN device cross-section and (b) its IV characteristics.
Figure 2-3: Device cross-section of a CMOS inverter next to a substrate current injector. The carriers in the substrate may reach the CMOS inverter and trigger latchup. The N-well of the victim is where the electrons are collected and is called the detector.

Figure 2-4: A typical I/O circuitry. The diodes are for ESD protection and could be replaced by other ESD clamps.
CHAPTER 3

INTERNAL LATCHUP

Internal latchup is studied in this chapter. This type of latchup is called *internal latchup* because the stimulus is connected directly to the victim, the parasitic PNPN.

3.1 PNPN Triggering Modes

3.1.1 Overshoot and undershoot on PNPN terminals

The voltage on an output node may temporarily exceed the supply voltage as a result of a signal reflection at a mismatched interface. This could trigger latchup if a parasitic PNPN is connected to the output node. When this transient overshoot is on a P* diffusion, holes are injected into the N-well. The injected carriers are collected by the substrate contact and produce a voltage drop across the substrate. If the voltage drop across the base-emitter junction of the NPN is high enough, the parasitic NPN is turned on. The collector current of this NPN builds up a voltage drop across the base-emitter junction of the PNP. Latchup is triggered when both transistors are on [20].

Latchup can also be triggered when the output node falls below ground. In this case, electrons are injected into the substrate and leave a voltage drop as they are collected by an N-well.

3.1.2 Overvoltage/avalanching N-well junction

Since both parasitic bipolar transistors in a parasitic PNPN are normally off, the supply voltage appears across the reverse-biased N-well/P-substrate PN junction. When
the supply voltage is raised, e.g., because of a power supply glitch, the resulting avalanche current may forward-bias one of the base-emitter junctions and trigger latchup [20].

3.1.3 Punchthrough

The depletion region of the reverse-biased N-well/P-substrate junction may spread into a closely spaced N⁺ diffusion in the substrate, causing a punchthrough current that may bias either of the parasitic transistors. Similarly, punchthrough current flows when the depletion region spreads into a closely spaced P⁺ diffusion in the N-well. Although silicon devices are engineered to ensure that punchthrough does not occur at the nominal supply voltage, since the depletion width of a PN junction is an increasing function of the voltage, punchthrough current flows when the supply voltage exceeds the nominal voltage. Depending on the device characteristics, either avalanche or punchthrough current may trigger latchup at a lower voltage [20].

3.2 Latchup Characterization

The aim of latchup characterization is to find the minimum allowable N⁺-to-P⁺ spacing and maximum allowable diffusion-well tap spacing in a given technology by extracting the key latchup parameters, such as the internal latchup trigger current. The main idea is to trigger one of the parasitic bipolar transistors by an external voltage or current excitation. Once one of the transistors is on, it provides enough current to turn on the other transistor.
Depending on how the PNPN terminals are biased, characterization methods fall into one of two groups: two-terminal characterizations and four-terminal characterizations.

### 3.2.1 Two-terminal characterizations

A two-terminal PNPN is formed and biased by tying the P$^+$ diffusion and N-well taps to $V_{DD}$ and grounding the N$^+$ diffusion and substrate taps. The PNPN is triggered by either a voltage or current stress.

**Supply overvoltage stress**

Voltage across the terminals is slowly raised, and the current through the device is recorded, as shown in Figure 3-1. Current compliance of the tester is set low enough to prevent permanent damage to the device. This method does not capture the negative resistance region of the PNPN I-V curve unless resistance is added in series with the voltage source.

**Supply overcurrent stress**

A supply overcurrent stress test is used to get the complete I-V curve of the PNPN, including holding current and voltage. Unlike the previous test, in this test, shown in Figure 3-2, a current source is connected to one of the terminals. The PNPN snaps back and switches into its low-impedance regime when the current is raised. The difficulty of this test is that the injection current needed to forward-bias either of the parasitic transistors is typically much larger than the typical leakage current of the N-well/P-substrate PN junction. Therefore, a relatively large voltage is induced across the device when the current is raised, which may cause a failure before triggering latchup.
3.2.2 Four-terminal characterizations

In these methods, the PNPN terminals are individually connected to the curve tracer, and the current or voltage of each terminal is separately measured.

Voltage excitation at $P^+$ diffusion

Referring to Figure 3-3, while the N-well voltage is fixed at $V_{DD}$ and $N^+$ diffusion and the substrate tap are grounded, the voltage at the $P^+$ diffusion is raised from $V_{DD}$ to forward-bias the base-emitter junction of the PNP. Latchup is triggered when the collector current of the PNP is high enough to forward-bias the base-emitter junction of the NPN.

Current source excitation at substrate or well contact

There are two ways to do this test. First, a current source is connected to the N-well tap, the $P^+$ diffusion is tied to $V_{DD}$, and the substrate tap and $N^+$ diffusion are grounded (Figure 3-4 (a)). The PNP is turned on when the voltage drop across the N-well is high enough to forward-bias the base-emitter junction.

In the second test, shown in Figure 3-4 (b), latchup is triggered by turning on the NPN. A current source provides current at the substrate tap to forward-bias the base-emitter junction of the NPN. The $N^+$ diffusion is grounded, and the N-well tap and $P^+$ diffusion are tied to $V_{DD}$ (Figure 3-4 (b)).

Current source excitation at $P^+$ or $N^+$ diffusion

Latchup may be triggered by injecting current into the $P^+$ diffusion, as depicted in Figure 3-5. Unlike a two-terminal supply overcurrent stress, the N-well tap is tied to $V_{DD}$.
and current is only injected into the diffusion. Alternatively, latchup can be triggered by sinking current from the N\textsuperscript{+} diffusion (Figure 3-5 (b)).

3.3 Figures

Figure 3-1: Supply overvoltage stress test.

Figure 3-2: Supply overcurrent stress test.
Figure 3-3: Voltage excitation at P+ diffusion.
Figure 3-4: Current excitation at (a) N-well tap and (b) substrate tap.
Figure 3-5: Current excitation at (a) P+ diffusion and (b) N+ diffusion.
CHAPTER 4

EXTERNAL LATCHUP

4.1 Analysis of External Latchup

External latchup is the result of the substrate current flow. Substrate current may consist of majority carriers (holes) and/or minority carriers (electrons). To understand how $I_{\text{trig}}$ is related to layout parameters, the type of carrier that triggers latchup must first be determined.

Figure 4-1 shows the cross-section of a parasitic PNPN. The terms $I_{\text{coll,n}}^{\text{crit}}$ and $I_{\text{coll,p}}^{\text{crit}}$ are the minimum amount of collected current that turn on the parasitic PNP and NPN, respectively. Latchup will be triggered if the minority carrier current collected by the N-well of the PNPN ($I_{\text{coll,n}}$) exceeds $I_{\text{coll,n}}^{\text{crit}}$ or if the majority carrier current collected by the P-well of the PNPN ($I_{\text{coll,p}}$) exceeds $I_{\text{coll,p}}^{\text{crit}}$.

Standards have been developed to establish methods for determining latchup characteristics and to define latchup failure criteria. The testing procedure outlined in the JEDEC standard is designed to trigger latchup between a supply rail and its ground (i.e., $V_{\text{DDx}}$ and $V_{\text{SSx}}$) [1]. It consists of I-tests and overvoltage tests, with the former referring to injection of positive and negative current into each input, output, or I/O pin, and the latter referring to overvoltage testing of each supply pin. Each test associated with
external latchup is examined in the following sections. In each case, the roles of substrate majority and minority carriers in triggering latchup are elucidated.

4.1.1 Negative I-test

The carrier injector is a substrate diode placed near a parasitic PNPN device, shown in Figure 4-2 (a). Figure 4-3 shows a circuit model corresponding to the cross-section of Figure 4-2 (a), for the case of a negative transient at the I/O pad. In Figure 4-3, Q_{PNP1} and Q_{NPN1} represent the cross-coupled bipolar transistors that form the PNPN, and Q_{NPN2} represents the lateral NPN formed by the N^+ cathode of the diode, the P-substrate, and the N-well.

Most of the electrons injected into the substrate by the diode will recombine with holes, but some will be collected by the N-well of the PNPN. The resulting N-well current will flow through R_{NW}. The corresponding \( I \cdot R \) drop forward-biases the base-emitter junction of Q_{PNP1}. However, turning on Q_{PNP1} is not sufficient to induce latchup. The collector current of Q_{PNP1} must be large enough to forward-bias the base-emitter junction of Q_{NPN1}. Due to current flow through \( R_{diode} \), the substrate in the vicinity of the undershooting I/O is at a lower potential than \( V_{SS} \); the resulting majority-carrier substrate current through \( R_{PW1} \) and \( R_{SUB} \) tends to reverse-bias the base-emitter junction of Q_{NPN1}. In order for latchup to occur, \( I_{C,PNP1} \) must be large enough to counteract the substrate current flowing from PW\(_1\) to the diode. Latchup is triggered if the current collected by the N-well is large enough to result in forward-biasing both bipolar transistors. The necessary current \( I_{coll,n}^{crit} \) is given by
The first term on the right side of (4.1) counts for the required collected current to trigger \( Q_{PNP1} \), and the second term counts for forward-biasing the base-emitter junction of \( Q_{NPN1} \).

The nodal equation at the base of \( Q_{NPN1} \) gives the following:

\[
\frac{(R_{\text{diode}} + R_{\text{sub}})I_{\text{crit}}^{\text{PNP1}} - R_{\text{diode}} \frac{I_{\text{trig}}}{\beta_{PNP1}}}{R_{\text{diode}} + R_{\text{sub}} + R_{PW1}} - \frac{V_{BE,\text{on},N}}{R_{PW1}} = 0. \tag{4.2}
\]

In (4.2), \( V_{BE,\text{on},P} \) and \( V_{BE,\text{on},N} \) represent the base-emitter voltage drops of \( Q_{PNP1} \) and \( Q_{NPN1} \), respectively, at the PNPN triggering point. The common-emitter current gains of \( Q_{NPN2} \) and \( Q_{PNP1} \) are represented by \( \beta_{NPN2} \) and \( \beta_{PNP1} \), respectively. The current collected by the N-well, \( I_{\text{coll},n} \), may be related to the substrate current injected by the diode \( I_{\text{inj}} \), as follows:

\[
I_{\text{coll},n} = \alpha_{NPN2} \cdot I_{\text{inj}}, \tag{4.3}
\]

where \( \alpha_{NPN2} \) is the common-base current gain of \( Q_{NPN2} \). From (4.3), one finds

\[
I_{\text{trig}} = \frac{I_{\text{coll},n}}{\alpha_{NPN2}}. \tag{4.4}
\]

Equations (4.1), (4.2), and (4.4) may be solved for the external latchup trigger current:

\[
I_{\text{trig}} = \frac{R_{\text{diode}} + R_{\text{sub}} + R_{PW1}V_{BE,\text{ON},N} + R_{\text{diode}} + R_{\text{sub}}}{R_{PW1}} - \frac{R_{PW1}}{\beta_{PNP1} + 1} \frac{V_{BE,\text{ON},P}}{R_{NW}}. \tag{4.5}
\]

If \( R_{SUB} > R_{PW1} \) and \( R_{SUB} > R_{\text{diode}} \), then (4.5) reduces to
\[ I_{\text{trig}} = \frac{V_{BE,ON,N}}{R_{PW1}} + \beta_{PNP1} \frac{V_{BE,ON,P}}{R_{NW}} \]
\[ \frac{\beta_{PNP1}\beta_{PNP2}}{\beta_{PNP2} + 1} = \frac{1}{\alpha_{NPN2}} \left( \frac{V_{BE,ON,N}}{\beta_{PNP1}R_{PW1}} + \frac{V_{BE,ON,P}}{R_{NW}} \right). \] (4.6)

On the far right-hand side of (4.6), the expression inside the parentheses is equal to \( I_{\text{crit, coll, n}} \) and is a function of only the PNPN geometry. From studies of internal latchup, e.g., [20], it is known that \( V_{BE,ON,P} \) and \( V_{BE,ON,N} \) are functions of the PNPN anode-to-cathode spacing (i.e., P⁺-to-N⁺ spacing). Specifically, for a larger anode-to-cathode spacing, the current gains of the bipolar transistors inside the PNPN are reduced, and so a larger forward-bias is needed on each transistor to reach the triggering point. Small well resistances, \( R_{PW1} \) and \( R_{NW} \), will increase the trigger current for both internal and external latchup; \( R_{PW1} \) and \( R_{NW} \) are layout-dependent parameters. Clearly, the expression inside the parentheses, \( I_{\text{crit, coll, n}} \), is correlated with the internal latchup trigger current.

In contrast, \( \alpha_{NPN2} \) of (4.6) is relevant only for external latchup. The symbol will be shortened to \( \alpha_{NW} \), and this quantity will be referred to as the collection efficiency.

### 4.1.2 Positive I-test

In a positive I-test, a positive current source is connected to an I/O pin, and the top diode of Figure 4-2 (b) will inject substrate current. The corresponding circuit model for latchup analysis is shown in Figure 4-4. The PNP transistor \( Q_{PNP2} \) is formed by the P⁺ diffusion of the diode, NW₂, and the P-substrate. During a positive I-test, \( Q_{PNP2} \) injects holes into the substrate. These majority carriers will forward-bias the base-emitter junction of \( Q_{NPN1} \) as they are collected by PW₁. In contrast, the minority carrier substrate
current injected by Q_{NPN2} has the wrong polarity to turn on Q_{PNP1}. Therefore, for a positive I-test, majority carriers trigger latchup.

For the circuit of Figure 4-4, one can show

\[ I_{\text{trig}} \approx \frac{I_{\text{crit}}^{\text{coll,p}}}{\alpha_{PNP2}}. \]  

(4.7)

The term \( I_{\text{crit}}^{\text{coll,p}} \) can be approximated as

\[ I_{\text{crit}}^{\text{coll,p}} \approx \frac{V_{BE,\text{on}} - N}{R_{PW}} + \frac{V_{BE,\text{on}} - P}{\beta_{NPN} \cdot R_{NW}} - I_{C,PNP3}. \]  

(4.8)

Note that the base-width and, hence, the current gain of Q_{PNP3} are independent of d_{det}. This means that I_{C,PNP3} is also independent of d_{det}. Therefore, none of the parameters in (4.7) or (4.8) are functions of d_{det}, and thus one expects that for a positive I-test, I_{trig} will be insensitive to injector-to-detector spacing. Note that I_{C,PNP3} is a function of I_{inj} and, hence, (4.7) or (4.8) cannot estimate I_{trig}. Instead, one has to simulate circuit schematics of Figure 4-4 to find I_{trig}.

4.1.3 Undervoltage on V_{DDIO}

The top N-well diode of Figure 4-2 (c) will also provide substrate current if an undervoltage event causes V_{DDIO} to dip below the voltage on the I/O pin; analysis of the corresponding circuit in Figure 4-5 shows that this can result in latchup on a separate V_{DD} line. In this case, I_{trig} is defined as the current flowing through power supply V_{DDIO} just before latchup is triggered.
In the circuit of Figure 4-5, $Q_{PNP2}$ injects majority carriers into the substrate. The collector current of $Q_{PNP2}$ may turn on $Q_{NPN1}$; the corresponding condition is

$$R_{PW1} \cdot I_{C,PNP2} \geq V_{BE,on_{P}}.$$  

In this case, latchup is the result of majority carrier collection. However, the collector current of $Q_{PNP2}$ may also turn on $Q_{NPN2}$; the condition for this to occur is

$$R_{PW1} + R_{SUB} \cdot I_{C,PNP2} \geq V_{DDIO} + V_{BE}.$$  

$Q_{NPN2}$ injects minority carriers into the substrate, which may trigger latchup. Although this analysis indicates that latchup can be triggered by either majority or minority carriers, for any specific case, one can easily determine the underlying cause of latchup. One simply examines whether $I_{trig}$ varies with $d_{det}$; $I_{trig}$ is a decreasing function of $d_{det}$ only when minority carriers trigger latchup.

If $Q_{NPN1}$ turns on before $Q_{NPN2}$, the latchup condition is simply

$$I_{trig} \approx \frac{I_{crit}}{\beta_{PNP2}}.$$  \hspace{1cm} (4.9)

A comparison of (4.7) and (4.9) shows that an undervoltage on $V_{DDO}$ can be more hazardous than positive current injection at the I/O, because $\beta > \alpha$.

4.1.4 Considerations for the substrate current

In Figure 4-4 and Figure 4-5, the inclusion of $Q_{PNP3}$ (the parasitic PNP formed by the P-substrate, NW1, and PW1) might seem unnecessary, but, as will be shown in Section 5.3, it is required to achieve agreement between measurement and simulation results. The activity of $Q_{PNP3}$ is highlighted by the experiment sketched in Figure 4-6 (a). The $N^+$ diffusion of an N-well diode was tied to $V_{DD}$, the $P^+$ diffusion in PW1 was grounded, and positive current was applied to the I/O. All other terminals were left floating, unless otherwise indicated. The current at the $P^+$ diffusion $I_{PW1}$ was measured
two times, once with NW\(_1\) floating and once with NW\(_1\) connected to V\(_{DD}\). Biasing NW\(_1\) increases I\(_{PW,1}\), as shown in Figure 4-6 (c). This result can be understood by considering the effect of Q\(_{PNP3}\). Referring to Figure 4-6 (b), when NW\(_1\) is floating, Q\(_{PNP3}\) remains off. I\(_{PW,1}\) is initially an increasing function of I\(_{inj}\), but eventually levels off when Q\(_{PNP2}\) is driven into saturation and the voltage drop across the substrate becomes roughly constant. In contrast, when NW\(_1\) is biased at V\(_{DD}\), I\(_{PW,1}\) does not level off. After Q\(_{PNP2}\) is driven into saturation, the emitter voltage of Q\(_{PNP3}\) becomes larger than its base voltage, thus forward-biasing this junction and turning on Q\(_{PNP3}\). The forward-bias on the emitter-base junction is a result of the following relations that are valid when Q\(_{PNP2}\) operates in saturation: V\(_{E,PNP3}\) = V\(_{C,PNP2}\) > V\(_{B,PNP2}\) = V\(_{DD}\); V\(_{B,PNP3}\) < V\(_{DD}\). When Q\(_{PNP3}\) turns on, I\(_{C,PNP3}\) adds to I\(_{PW,1}\). Even though the current through R\(_{SUB}\) becomes almost constant when Q\(_{PNP2}\) is driven into saturation, I\(_{PW,1}\) remains an increasing function of I\(_{inj}\) as long as Q\(_{PNP3}\) is not saturated. Therefore, the inclusion of Q\(_{PNP3}\) is necessary to accurately model the majority carrier collection by PW\(_1\).
4.2 Figures

Figure 4-1: Cross-section of a parasitic PNPN. $I_{\text{coll,n}}$ and $I_{\text{coll,p}}$ are the minority carrier and majority carrier substrate currents, respectively, collected by this structure.
Figure 4-2: Setups for (a) a negative I-test, (b) a positive I-test, and (c) an undervoltage test.
Figure 4-3: Circuit-level model of a substrate current injector (bottom diode) and victim (PNPN) for a negative I-test.

Figure 4-4: Circuit-level model of injector (top diode) and victim (PNPN) for a positive I-test.
Figure 4-5: Circuit-level model of injector (diode) and victim (PNPN) for an undervoltage on $V_{DDO}$ with a top N-well diode.
Figure 4-6: (a) Experiment setup. (b) Circuit-level model. (c) $I_{PW,1}$ vs. $I_{inj}$ with and without biasing NW$_1$. SmartMOS technology. Room temperature.
CHAPTER 5

MEASUREMENT RESULTS AND DISCUSSIONS

5.1 Test Structures

Test structures were fabricated in four different technologies: 0.25-μm SmartMOS [32], 0.18-μm RF-CMOS, 0.13-μm CMOS, and 90-nm CMOS. Figure 5-1, Figure 5-2, and Figure 5-3 show the test structure. In the SmartMOS test structures, the injector has 25 N⁺-stripes, each 25 μm wide (25 × 25 μm), the N-well detector is 60 μm wide, and \( d_{TAP} = 30 \) μm. In the RF-CMOS test structures, the injector is a 15 μm wide, single-stripe diode, the victim contains a 15 μm wide N-well, and \( d_{TAP} = 5 \) μm. In the 130-nm and 90-nm CMOS test structures, the injector has four N⁺-stripes, each 20 μm wide (4 × 20 μm), and the detector is 20 μm wide. In these structures, \( d_{TAP} = 40 \) μm, and \( d_{victim} = 5 \) μm. Guard rings are 1 μm wide and \( d_{PGR} = d_{NGR} = 2 \) μm.

Referring to Figure 5-1, the collection efficiency \( \alpha_{NW} \) was measured with the anode grounded, a negative current source of magnitude \( I_{inj} \) connected to the cathode, the NW terminal connected to \( V_{DD} \), and all other terminals floating. Since the guard rings are almost always used in a design, they were added to the test structures but were left floating when \( \alpha_{NW} \) was measured. We found that the induced voltage on a floating NGR is negative. Since the P-wells are grounded, the P-well/NGR junctions are forward-biased and do not block the carrier flow.
In advanced CMOS technologies, different supply voltages are used with I/O and core transistors. The supply voltage varies from 2.5 V to 5 V for the I/O and from 1 V to 1.8 V for the core for the technologies used in this work. Parasitic PNPNs are found in both I/O and core logic circuits, meaning that the victims of Figure 5-1 and Figure 5-2 could have \( V_{DD} \) in the range of 1 V to 5 V. However, latchup will be sustained after the removal of the trigger source only if \( V_{DD} > 1.2 \) V [33]. We know that \( I_{trig} \) is a decreasing function of \( V_{DD} \), but we will show that the effect is small (Section 5.2.3). In this work, \( V_{DD} \) was set to 1.5 V for the 130-nm CMOS and 90-nm CMOS devices and to 2 V for the 0.25-\( \mu \)m SmartMOS and 0.18-\( \mu \)m RF-CMOS devices. \( V_{DDIO} \) was also set equal to \( V_{DD} \), arbitrarily, because \( I_{trig} \) is insensitive to \( V_{DDIO} \).

A semiconductor parameter analyzer is used to ramp the injection current and provide \( V_{DD} \). It has four SMUs (source-measure units), which can simultaneously provide voltage and measure current.

5.2 Collection Efficiency

5.2.1 Layout geometry

As evident from the data of Figure 5-4 and Figure 5-5, collection efficiency is a decreasing function of \( d_{det} \) because more electrons recombine within the substrate as \( d_{det} \) increases.

As shown in Figure 5-6 and Figure 5-7, \( \alpha_{NW} \) is an increasing function of \( W_{det} \) and \( L_{det} \) because more carriers are collected as the area of the victim increases. Note that \( W_{det} \) is set equal to the width of the N-well, rather than the width of the \( N^+ \) diffusion inside the well, because measurement data show that \( \alpha_{NW} \) is a far stronger function of the former
Data also indicate that the width and the length dependences are nonlinear.

5.2.2 Temperature

The data of Figure 5-4 and Figure 5-5 also show that the collection efficiency is an increasing function of temperature. This dependence is expected when $\alpha_{NW}$ is interpreted as the common-base current gain of a bipolar transistor,

$$\alpha = \gamma \cdot \beta_T,$$

(5.1)

where $\gamma$ is the emitter injection efficiency and $\beta_T$ is the base transport factor. For an ordinary, vertical bipolar transistor, $\alpha_{NW}$ is dominated by the emitter injection efficiency, which is an increasing function of temperature [35], in agreement with the data of Figure 5-4 and Figure 5-5. Moreover, the NPN lying between the injector and the detector, $Q_{NPN2}$, has a very long base and, thus, the base transport factor significantly affects the value of $\alpha_{NW}$. The base transport factor is also an increasing function of temperature because, in the range 0–125 °C, carrier lifetime is an increasing function of temperature [36]; base recombination is thus reduced as temperature increases. Therefore, the experimental results for $\alpha_{NW}(T)$ are consistent with theory.

5.2.3 Bias conditions

Let $V_{det}$ denote the bias voltage of the N-well of the victim. Then $\alpha_{NW}$ is an increasing function of the bias voltage of the detector $V_{det}$, as shown in Figure 5-8. This behavior is consistent with the Early effect in bipolar transistors.
Physically, however, the observed voltage dependence is not due to the Early effect. If the $V_{\text{det}}$ dependence were a result of the Early effect, then the extracted Early voltage, $V_A$, would be an increasing function of $d_{\text{det}}$. The data in Figure 5-9 and Figure 5-10 show that the extracted Early voltage is fairly insensitive to $d_{\text{det}}$. Furthermore, the extracted values of $V_A$ are much smaller than would be expected for the true Early effect. It is further noted that $V_A$ is insensitive to temperature.

We claim that the change in the area of the detector $A_{\text{col}}$ is the reason for the voltage dependence of $\alpha_{NW}$. One should note that $A_{\text{col}}$ is larger than what is extracted from the layout because the depletion region of the N-well/substrate junction extends the detector into the substrate, as illustrated by the dashed lines in Figure 5-11. The area of the extended detector is defined as $A_{\text{col}}$ and is equal to

$$A_{\text{col}} = W_{\text{det}} + 2X_{D, PW} \cdot L_{\text{det}} + 2X_{D, PW} + 2W_{\text{det}} + 2X_{D, PW} \cdot X_j + X_{D, SUB} (5.3)$$

In (5.3), $X_{D, PW}$ and $X_{D, SUB}$ are the width of the N-well/P-well and N-well/substrate depletion regions, respectively. They are functions of the P-well, substrate, and N-well doping levels ($N_{PW}$, $N_{SUB}$, and $N_{NW}$, respectively) as well as $V_{\text{det}}$, as indicated in (5.4).

$$\left\{ \begin{array}{l} X_{D, PW} = \left( \frac{2\varepsilon_s}{q} \left( \frac{1}{N_{NW}} + \frac{1}{N_{PW}} \right) \varphi_i + V_{\text{det}} \right)^{1/p} \\ X_{D, SUB} = \left( \frac{2\varepsilon_s}{q} \left( \frac{1}{N_{NW}} + \frac{1}{N_{SUB}} \right) \varphi_i + V_{\text{det}} \right)^{1/p} \end{array} \right. (5.4)$$
In (5.4), \( \phi_i \) is the built-in voltage of the N-well/substrate junction, and \( n \) depends on the gradient of the change in the doping profiles at the N-well/P-well or N-well/substrate junctions. For an abrupt junction, \( n = 2 \). From (5.3) and (5.4), one concludes that \( A_{\text{col}} \) is an increasing function of \( V_{\text{det}} \). We know that \( \alpha_{\text{NW}} \) is an increasing function of the collector area. Therefore, one expects \( \alpha_{\text{NW}} \) to be an increasing function of \( V_{\text{det}} \). Equation (5.3) predicts that the relative increase in \( A_{\text{col}} \) will be more pronounced for smaller detector geometries. Therefore, one should expect \( V_{A} \) to be an increasing function of \( W_{\text{det}} \) and \( L_{\text{det}} \). This expectation is borne out by the data of Figure 5-12 and Figure 5-13.

Figure 5-14 shows that \( \alpha_{\text{NW}} \) is a function of the injection current \( I_{\text{inj}} \). This observation is consistent with the behavior of bipolar transistors under high-level injection conditions. As \( I_{\text{inj}} \) increases, the electron density in the substrate increases. At some point, the electron density exceeds the substrate doping density, and the density of the majority carriers then starts to increase to maintain charge neutrality in the substrate. Therefore, similarly to the current gain of a bipolar transistor, one expects \( \alpha_{\text{NW}} \) to be a decreasing function of \( I_{\text{inj}} \) under high-level injection conditions.

### 5.2.4 N-well guard rings

The term \( \alpha_{\text{NW}}^{*} \) denotes the collection efficiency of the detector measured with the N-well guard rings (NGRs) tied to the positive voltage supply. As shown in Figure 5-15, wide guard rings that are placed close to the injector are most effective in reducing current collection by the detector. At moderate current levels, guard rings reduce carrier collection by the detector by 90% or more (Figure 5-15); however, this does not imply that the latchup trigger current is increased by about an order of magnitude. A measure of
guard ring efficiency is \( \alpha_{NW}^* / \alpha_{NW} \) which is between 0 and 1. Measurement results show that guard rings are less efficient at the high current levels typically needed to trigger latchup (Figure 5-16).

### 5.2.5 Multiple detectors

In this experiment, \( \alpha_{NW}^* \) is measured with the secondary detector rather than with the NGRs activated (Figure 5-17). The primary and secondary detectors are equidistant from the injector. Note that unlike a guard ring, a secondary detector is not a ring and does not surround the injector. It simply represents the N-well of another victim. One might expect that the presence of an identical second detector will lower \( \alpha_{NW}^* \) by a factor of one-half relative to \( \alpha_{NW} \), but this is contradicted by the data of Figure 5-18, which show a smaller effect. A 2-D device simulation provides insight. The simulated electron current flow is shown in Figure 5-19. In Figure 5-19 (a), only the primary detector is active, whereas both detectors are active in Figure 5-19 (b). The effect of the second detector diminishes as the spacing increases, as shown by the measurement data in Figure 5-20. These effects may be understood as follows.

For the case of a single detector, some of the electron flux that initially flows leftward from the injector (labeled Group II in Figure 5-19 (a)) will be collected by the primary detector on the right side of the injector. When both detectors are activated, the carriers in Group II are collected by the second detector (see Figure 5-19 (b)), which explains the reduced collection efficiency (\( \alpha_{NW}^* < \alpha_{NW} \)); however, the effect is limited because the flux contained in Group II is less than that in the Group I. Furthermore, the data of Figure 5-20 indicate that the effect of the second detector diminishes as \( d_{detL} \) is
made larger. This is because at large $d_{\text{det},R}$, the secondary victim collects the carriers that otherwise recombine in the substrate. Therefore, as $d_{\text{det},L}$ increases, $\alpha_{NW}^*$ approaches $\alpha_{NW}$. The effect of the second detector is also reduced when NGR is active (Figure 5-21).

Table 5-1 lists $\alpha_{NW,R}^*$ measured when the primary and secondary detectors are not equidistant from the injector. When $d_{\text{det},R} << d_{\text{det},L}$, activating NW$_R$ has only a small effect on carrier collection at NW:

$$\alpha_{NW,R}^* \simeq \alpha_{NW,R}.$$  \hspace{1cm} (5.5)

In fact, (5.5) provides a reasonable, albeit conservative, estimate of $\alpha_{NW,R}^*$, except for the case of small $d_{\text{det}}$, where small means that $d_{\text{det}}$ is much less than the electron diffusion length in the substrate (tens of $\mu$m [34]). For small $d_{\text{det}}$, $\alpha_{NW,R}^*$ may be significantly less than predicted by (5.5), especially for the case $d_{\text{det},L} < d_{\text{det},R}$.

5.2.6 P-type guard rings

The collection efficiency of the primary detector when the P-well guard ring (PGR) is grounded (i.e., activated) is $\alpha_{NW}^+$. In this experiment, the NGR and secondary detector are inactive. Since PGRs collect majority carriers, whereas this experiment measures minority carrier collection, one might expect the PGRs to have no effect. However, the PGRs increase the collection efficiency of the detector (Figure 5-22), and the effect worsens as the PGR is moved closer to the detector (Figure 5-23). Device simulation results are shown in Figure 5-24. Figure 5-24 (a) and Figure 5-24 (c) are for the case that the PGRs are inactive, and Figure 5-24 (b) and Figure 5-24 (d) are for an
activated PGR. In Figure 5-24 (c), the current density along the injector PN junction is highly non-uniform; it is highest at the edges and lowest near the middle of the bottom surface of the junction. This indicates there is a non-uniform potential along the PN junction. The potential varies due to IR drops caused by the laterally directed hole current, analogous to the non-uniform base resistance effect in bipolar junction transistors (BJTs) [37]. Current crowding at the edges of the junction causes high-level injection effects to occur at a lower current level than they would if the current density were uniform. In Figure 5-24 (d), the current density along the injector PN junction is more uniform because more of the hole current (base current) is flowing vertically. Therefore, for a fixed injection current, high-level injection effects are reduced when the PGR is active. The PGR increases collection efficiency by delaying the onset of high-level injection, as is evident from the data of Figure 5-22. Note that $\alpha_{NW}^+ = \alpha_{NW}$ at low $I_{\text{inj}}$.

The deleterious effect of PGR is especially pronounced when NGR is active (Figure 5-25). The deleterious effect of PGR is also observed if one measures the latchup trigger current instead of the minority carrier collection efficiency.

5.2.7 P-well taps

Similarly to PGRs, an active P-well tap (PT) increases the collection efficiency (Figure 5-26). A PT on the same side of the injector as the detector has a bigger impact than does one on the opposite side (Figure 5-27). This is because $PT_R$ increases current uniformity on the right side of the junction, which increases the number of electrons injected toward the detector.
5.3 Measurement Results of $I_{\text{trig}}$

Figure 5-28 shows $I_{\text{trig}}$ as a function of $d_{\text{det}}$ for a positive I-test (Figure 5-1 (b)). The device dimensions are given in Section 5.1. The resistors $R_{\text{NW ext}}$ and $R_{\text{PW ext}}$ are external resistors optionally added in series with the N$^+$ and P$^+$ diffusion in NW$_1$ and PW$_1$ (Figure 5-1 (b)), respectively, in order to emulate the effect of a large well tap spacing.

Figure 5-28 shows that $I_{\text{trig}}$ is insensitive to $d_{\text{det}}$; this is expected from Section 4.1.2 because latchup is triggered by majority carriers during a positive I-test. For a fixed $R_{\text{NW1}}$, increasing $R_{\text{PW1}}$ lowers $I_{\text{trig}}$ as predicted by (4.8). In contrast, for a fixed $R_{\text{PW1}}$, $I_{\text{trig}}$ is an increasing function of $R_{\text{NW1}}$. One may notice that the first two terms of (4.8) indicate that $I_{\text{crit}}^{\text{coll,p}}$ is a decreasing function of $R_{\text{NW1}}$. However, increasing $R_{\text{NW1}}$ will also lower $I_{\text{B,PNP3}}$, which in turn lowers $I_{\text{C,PNP3}}$. As a result, increasing $R_{\text{NW1}}$ lowers the current through $R_{\text{PW1}}$, requiring a higher $I_{\text{inj}}$ in order to forward-bias the base-emitter junction of Q$_{\text{NPN1}}$ and trigger latchup. Although increasing the N-well resistance was shown here to provide increased resistance against positive external latchup, it is not recommended as a latchup prevention method because it increases the susceptibility to negative external latchup [38], and also increases susceptibility to internal latchup.

Figure 5-29 shows $I_{\text{trig}}$ as a function of $d_{\text{det}}$ for an undervoltage test, as shown in Figure 5-1 (c). As discussed in Section 4.1.3, either majority or minority carriers can trigger latchup during an undervoltage test. The data of Figure 5-29 show that $I_{\text{trig}}$ is an increasing function of $d_{\text{det}}$. Therefore, latchup was triggered by minority carriers in these experiments.
Table 5-2 summarizes the results of measuring $I_{\text{trig}}$ on a variety of test structures at an elevated temperature of $125 \, ^\circ\text{C}$. The $I_{\text{trig}}$ values of both the positive and negative I-tests are decreasing functions of temperature; this is supported by previous works [3], [38]. For example, in the positive I-test, raising the temperature decreases $I_{\text{trig}}$ by a factor of $\sim 3.5$. Because of the positive temperature dependence of the N-well and P-well resistances, $I_{\text{trig}}$ is a decreasing function of temperature. In addition, $I_{\text{trig}}$ of a negative I-test is a decreasing function of temperature because of the positive temperature dependence of $\alpha_{\text{NW}}$ [34].

The data in Table 5-2 show that $I_{\text{trig}}$ is a decreasing function of $d_{\text{TAP}}$ for both a positive I-test and an undervoltage test. $R_{\text{PW1}}$ and $R_{\text{NW1}}$ are increasing functions of $d_{\text{TAP}}$. For a positive I-test, increasing $R_{\text{PW1}}$ lowers $I_{\text{trig}}$, while increasing $R_{\text{NW1}}$ increases $I_{\text{trig}}$. The data shown in the table indicate that the effect of $R_{\text{PW1}}$ is dominant; $I_{\text{trig}}$ is a decreasing function of $d_{\text{TAP}}$. Furthermore, the data indicate that $I_{\text{trig}}$ of an undervoltage test is a stronger function of $d_{\text{TAP}}$ than is $I_{\text{trig}}$ of a positive I-test. We expect $I_{\text{trig}}$ to be an especially strong function of $d_{\text{TAP}}$ when latchup is triggered by minority carriers, as in this undervoltage experiment. Increasing $d_{\text{TAP}}$ not only increases the well resistances, it also increases $\alpha_{\text{NW}}$, which further lowers $I_{\text{trig}}$. The value of $\alpha_{\text{NW}}$ is an increasing function of $d_{\text{TAP}}$ because structures with increased $d_{\text{TAP}}$ have larger $L_{\text{det}}$. Therefore, $I_{\text{coll,n}}$ becomes an increasing function of $d_{\text{TAP}}$ which means that smaller $I_{\text{inj}}$ can trigger latchup.
5.4 Figures

Figure 5-1: Test structure cross-sections for (a) a negative I-test, (b) a positive I-test, and (c) an undervoltage test. The victims are oriented 180°.
Figure 5-2: Test structure cross-sections for (a) a negative I-test and (b) a positive I-test. The victims are oriented 0°.

Figure 5-3: Top view of a test structure with a single-finger injector.
Figure 5-4: $\alpha_{NW}$ vs. $d_{det}$ and temperature. RF-CMOS technology.

Figure 5-5: $\alpha_{NW}$ vs. $d_{det}$ and temperature. SmartMOS technology.
Figure 5-6: $\alpha_{NW}$ vs. $W_{\text{det}}$. 90-nm CMOS technology. Room temperature.

Figure 5-7: $\alpha_{NW}$ vs. $L_{\text{det}}$. 90-nm CMOS technology. Room temperature.
Figure 5-8: $\alpha_{NW}$ as a function of detector voltage $V_{det}$ and $d_{det}$. RF-CMOS technology. Room temperature.

Figure 5-9: $V_A$ as a function of $d_{det}$. $V_A$ is fairly insensitive to spacing. 90-nm CMOS technology. Room temperature.
Figure 5-10: $V_A$ as a function of $d_{det}$ and temperature. $V_A$ is fairly insensitive to spacing and temperature. RF-CMOS technology.

Figure 5-11: Device cross-section of the detector. The dashed lines show the boundaries of the depletion region formed around the detector. $A_{col}$ is the area of the region enclosed by the dashed lines.
Figure 5-12: $V_A$ as a function of $W_{\text{det}}$. 90-nm CMOS technology. Room temperature.

Figure 5-13: $V_A$ as a function of $L_{\text{det}}$. 90-nm CMOS technology. Room temperature.
Figure 5-14: Measured $\alpha_{NW}$ vs. $I_{inj}$. $\alpha_{NW}$ decreases at high currents. P-well type injectors. SmartMOS technology. Room temperature.

Figure 5-15: Ratio of $\alpha_{NW}^*$ to $\alpha_{NW}$ for different NGR layouts. $\alpha_{NW}$ and $\alpha_{NW}^*$ are extracted at the current level that gives the highest $\alpha_{NW}^*$ ($= 0.11$). $d_{det} = 49 \, \mu m$. 130-nm CMOS technology.
Figure 5-16: $\alpha_{NW}^{*}/\alpha_{NW}$ vs. current injected at the I/O. $L_{NGR} = 1 \, \mu m$ and $d_{det} = 49 \, \mu m$. 90-nm CMOS technology.

Figure 5-17: Device cross-section of the test structures designed to investigate the effect of a secondary detector.
Figure 5-18: $\alpha_{NW,R}$ and $\alpha^*_{NW,R}$ as a function of $I_{inj}$. The NGRs and PGRs are inactive. $d_{det,R} = d_{det,L} = 49 \mu m$. 130-nm CMOS technology. The presence of a second detector slightly reduces carrier collection by the primary one.

Figure 5-19: Electron current flow lines when (a) only NW$_R$ (primary victim) is active, and (b) both NW$_R$ and NW$_L$ (secondary victim) are active. NW$_L$ collects the electrons from Group II and leaves fewer electrons for NW$_R$, the primary detector.
Figure 5-20: $\alpha_{NW,R}^*/\alpha_{NW,R}$ vs. injector-to-detector spacing. $d_{det,R} = d_{det,L}$. $\alpha_{NW,R}$ and $\alpha_{NW,R}^*$ are extracted at $I_{inj}$ corresponding to the highest $\alpha_{NW,R}$. 130-nm CMOS technology.

Figure 5-21: $\alpha_{NW,R}$ and $\alpha_{NW,R}^*$ vs. $I_{inj}$. NGR is activated. Data obtained from device simulation. The effect of a second detector is less noticeable when NGR is used (compare with Figure 5-18).
Figure 5-22: $\alpha_{NW}^+$ and $\alpha_{NW}$ vs. $I_{inj}$. $d_{det} = 49 \mu m$ and $d_{PGR} = 6.5 \mu m$. 130-nm CMOS technology. Collection efficiency increases when PGR is active, increasing the latchup hazard.

Figure 5-23: $\frac{\alpha_{NW}^+ - \alpha_{NW}}{\alpha_{NW}} \times 100$ as a function of the relative placement of the PGR. Data obtained from device simulation. The effect of PGR is heightened when they are placed closer to the detector.
Figure 5-24: Current flow lines for (a) inactive PGR ((c) zoomed-in view), and (b) active PGR ((d) zoomed-in view). In (a), hole current is injected only from the injector P$^+$ diffusions; but in (b), the current is also injected from the PGR.

Figure 5-25: Collection efficiency vs. $I_{inj}$. NGRs are active. $d_{NGR} = 3.5 \ \mu m$, $d_{PGR} = 4.5 \ \mu m$, and $d_{det} = 50 \ \mu m$. 130-nm CMOS technology. Active PGR increases minority carrier collection by the detector.
Figure 5-26: Collection efficiency vs. $I_{\text{inj}}$ with and without an active PT on the right side. NGRs, PT$_L$, and the secondary detector are inactive. $d_{\text{det}} = 49 \, \mu m$ and $d_{\text{PGr}} = 5 \, \mu m$. 90-nm CMOS technology.

Figure 5-27: Collection efficiency with PT$_L$ and PT$_R$ individually activated. Data obtained from device simulation.
Figure 5-28: $I_{\text{trig}}$ is plotted as a function of injector-to-PNPN spacing for a positive $I$-test with an N-well injector. 180º victim orientation. SmartMOS technology. Room temperature.

Figure 5-29: $I_{\text{trig}}$ is plotted as a function of injector-to-PNPN spacing for an undervoltage test (see Figure 4-5). An external resistor ($R_{\text{NW_ext}} = 10 \, \text{kΩ}$) is connected to the N-well contact of the PNPN to increase $R_{\text{NW}}$. Without $R_{\text{NW_ext}}$, $I_{\text{trig}}$ is outside the range of the measurement equipment (>100 mA). 180º victim orientation. SmartMOS technology. Room temperature.
5.5 Tables

Table 5-1: \( \alpha_{NW,R}^* \) as a function of both \( d_{det,R} \) and \( d_{det,L} \). \( \alpha_{NW,R} \) and \( \alpha_{NW,R}^* \) are extracted at the injection current corresponding to the highest \( \alpha_{NW} \). 130-nm CMOS technology.

<table>
<thead>
<tr>
<th>( d_{det,R} ) (µm)</th>
<th>( d_{det,L} ) (µm)</th>
<th>( \alpha_{NW,R} )</th>
<th>( \alpha_{NW,L} )</th>
<th>( \alpha_{NW,R}^* )</th>
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</thead>
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<tr>
<td>5</td>
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<td>0.34</td>
<td>0.23</td>
<td>0.29</td>
</tr>
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<td>0.34</td>
<td>0.11</td>
</tr>
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<td>0.11</td>
<td>0.09</td>
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</tr>
<tr>
<td>57</td>
<td>49</td>
<td>0.09</td>
<td>0.11</td>
<td>0.077</td>
</tr>
</tbody>
</table>

Table 5-2: Measured \( I_{trig} \). 125 °C. 180° victim orientation. SmartMOS technology. All PNPN dimensions are held constant in the experiments, except \( d_{TAP} \). Injectors are N-well diodes. \( d_{det} \) scales with \( d_{TAP} \) in the test structures.

<table>
<thead>
<tr>
<th>Positive I-test</th>
<th>Undervoltage test</th>
</tr>
</thead>
<tbody>
<tr>
<td>( d_{TAP} = 30 ) µm</td>
<td>3.7 mA</td>
</tr>
<tr>
<td>( d_{TAP} = 50 ) µm</td>
<td>2.2 mA</td>
</tr>
</tbody>
</table>
CHAPTER 6

MODELING THE LATCHUP TRIGGER CURRENT

The purpose of this chapter is first to provide a semi-physical analytical model for the collection efficiency of a detector, $\alpha_{NW}$. Then, with a model for $\alpha_{NW}$ in place, $I_{trig}$ is obtained by simulating the proposed circuit models.

6.1 Collection Efficiency of a Single Detector

First, the case of a single minority carrier detector is studied. This occurs when other N-well regions except the primary detector are floating or non-existent. Therefore, carriers that are injected to the substrate either recombine with the majority carriers or are collected by the single detector.

6.1.1 Effects of spacing

Collection efficiency $\alpha_{NW}$ is a decreasing function of $d_{det}$, as explained in Section 5.2.1. This section proposes a semi-physical analytical model for $\alpha_{NW}$ as a function of $d_{det}$.

To find the current collected by the detector, the electron distribution in the substrate must be first determined by solving the diffusion equation,

$$\nabla^2 n_p = \frac{n_p}{L_n^2}.$$ (6.1)
In (6.1), $L_n$ is the electron diffusion length in the substrate. Given the electron distribution, one may calculate the current crossing the boundary of the detector by solving

$$J_n = qD_n \nabla n_p.$$  \hspace{1cm} (6.2)

A closed-form, analytic solution to (6.1) does not exist for the geometry of the test structures [39]. A closed-form solution may be obtained only by simplifying the problem geometry. Two sets of approximations are used: one when $d_{det}$ is smaller than or close to $L_n$ and the other when $d_{det} >> L_n$. The former is called the *near spacing* model and the latter the *far spacing* model.

**The near spacing model**

If the injector width, $W_{inj}$, is much less than $d_{det}$, then the injector may be modeled as a point source, and (6.1) should be solved using spherical coordinates. Conversely, if $W_{inj} >> d_{det}$, then the injector may be modeled as an infinitely long line source, and a cylindrical coordinate system is used. Neither inequality is valid for all values of $W_{inj}$ and $d_{det}$ used in this work; nevertheless, good results are obtained using the line-source model [40].

For an infinitely long line source of minority carriers, centered at the origin of the coordinate system, (6.1) may be rewritten as

$$r^2 \frac{\partial^2 n_p}{\partial r^2} + r \frac{\partial n_p}{\partial r} = r^2 \frac{n_p (r)}{L_n^2}, \quad r > 0.$$  \hspace{1cm} (6.3)

A Neumann boundary condition is taken at the silicon surface, i.e., the normal component of the current is zero. Below the silicon surface, for a finite-sized detector, the
boundary condition for (6.3) will be spatially non-uniform. Further simplification of the
problem geometry is needed in order to obtain a closed-form solution.

**Case I: No detector**

First, (6.3) is solved for the case that there is no detector. In this case, one
boundary condition is

$$\lim_{r \to \infty} n_p(r) = 0.$$  \hfill (6.4)

The solution to (6.3) is thus

$$n_p(r) = C_1 K_0 \left( \frac{r}{L_n} \right),$$  \hfill (6.5)

where $K_0(x)$ is the modified Bessel function of the second type and order zero.

Define $I_{inj}^\ast$ as the current injected into the substrate per unit length. $C_1$ in (6.5) is
found by substituting (6.5) into (6.2) and setting

$$J_n(0) = \gamma \lim_{r \to 0} \frac{1}{\pi r} I_{inj}^\ast.$$  \hfill (6.6)

One thus obtains

$$C_1 = \frac{\gamma I_{inj}^\ast}{\pi q D_n},$$  \hfill (6.7)

where $\gamma$ is the electron injection efficiency, defined as the ratio of the injected electron
current to the total injected current.

$$\gamma = \frac{I_{inj}}{I_{inj} + I_{inj}}.$$  \hfill (6.8)

From (6.2), (6.5) and (6.7), one obtains
\[
\left| J_n^{*} \right| = \frac{\gamma I_{\text{inj}}^{*}}{\pi L_n^{*}} K_1 \left( \frac{r}{L_n^{*}} \right),
\]
where \( K_1(x) \) is the modified Bessel function of the second type and order one.

**Case II: Radially uniform detector**

Next, (6.3) is solved for the case that one boundary condition is \( n_p \left( r = d_{\text{det}} \right) = 0 \).

Indeed, \( n_p = 0 \) is the boundary condition at the edge of the depletion region outside the real detector, provided the carrier velocity inside the N-well is not saturated [41]. The solution to (6.3) is

\[
n_p(r) = C_1 K_0 \left( \frac{r}{L_n} \right) + C_2 I_0 \left( \frac{r}{L_n} \right), \quad r > 0,
\]

where \( I_0(x) \) and \( K_0(x) \) are the modified Bessel functions of the first and the second type, respectively, and order zero.

Using (6.6) as the boundary condition at \( r = 0 \), one obtains

\[
C_1 = \frac{\gamma I_{\text{inj}}^{*}}{\pi q D_n^{*}}.
\]

The value of \( C_2 \) is found by satisfying the boundary condition \( n_p \left( r = d_{\text{det}} \right) = 0 \):

\[
C_2 = -C_1 \frac{K_0 \left( \frac{d_{\text{det}}}{L_n} \right)}{I_0 \left( \frac{d_{\text{det}}}{L_n} \right)}.
\]

Current density is found using (6.2), (6.10), (6.11), and (6.12):
where $I_1(x)$ is the modified Bessel function of the first type and order one.

**General solution**

The device simulation results of Figure 6-1 indicate that the diffusion current in the substrate follows two main trajectories. Group I flow lines leave the injector as if there were no detector. Some of these lines bend in the vicinity of the detector, but the carrier density is given to the first order by (6.5). Group I carriers are primarily collected by the bottom plate of the reverse-biased N-well/P-substrate junction.

Group II flow lines leave the injector as if there were a radially uniform detector. The carrier density is given by (6.10). Group II carriers are primarily collected by the N-well detector sidewall that lies closest to the injector.

For Group I, the collected current may be written using (6.9):

\[
I_{col,I} = G_{det,I} \frac{\gamma}{\pi L_n} \frac{I_{inj}^*_{det}}{I_{inj} W_{inj}} = \alpha I_{inj}.
\]  

For Group II, the collected current may be written using (6.13):

\[
I_{col,II} = G_{det,II} \frac{\gamma}{\pi L_n} \left( K_1 \left( \frac{d_{det}}{L_n} \right) + \frac{K_0 \left( \frac{d_{det}}{L_n} \right)}{I_0 \left( \frac{d_{det}}{L_n} \right)} \right) \frac{I_{inj}^*_{det}}{I_{inj} W_{inj}} = \alpha I_{inj}.
\]
Above, $W_{inj}$ is the injector width. $G_{det,I}$ and $G_{det,II}$ are the geometric factors that model the effective collection areas.

Assuming that some fraction $\rho$ of the minority carriers in the substrate falls into Group I and the rest into Group II, the total collected current may be written as

$$I_{coll} = \rho I_{col,I} + (1 - \rho) I_{col,II} = \rho \alpha_I + (1 - \rho) \alpha_{II} I_{inj}.$$  \hspace{1cm} (6.16)

In Figure 6-2 and Figure 6-3, measurement results for both technologies are compared with the model in Equation (6.16). $G_{det,I}$, $G_{det,II}$, and $\rho$ are treated as fitting factors to get the best overall fit. As expected for a physics-based model, the extracted values of $L_n$ are the same order of magnitude, 55 $\mu$m and 25 $\mu$m for RF-CMOS and SmartMOS technologies, respectively. Furthermore, the fit of the model to data is good. Note that for multi-stripe devices, each finger is considered as a separate injector. The solution is then found using the superposition principle, as a sum of solutions for each single-finger injector. In the results of Figure 6-2 and Figure 6-3, $\rho$ is treated as a fitting factor. We found that $\rho$ is independent of the layout parameters as long as $d_{det}$ is less or slightly greater than $L_n$.

**The far spacing model**

A different approach is needed to model the collection efficiency when $d_{det} >> L_n$. Equation (6.16) fails because the current flow lines cannot be divided into Group I or II unless $\rho$ is modeled as a function of $d_{det}$. Instead, a different set of approximations is sought to solve the diffusion equation in the substrate.
The carrier collection over the surface of the detector is not uniform. The parts of the detector that are closer to the injector collect most of the carriers, whereas those that are farther away collect fewer. However, when \( d_{\text{det}} \gg L_{\text{det}} \), we can assume that the carriers are uniformly collected over the surface of the detector; i.e., \( J_{\text{col}} \) is the same over the surface. As will be shown, this will let us use a boundary construction approach to solve (6.1). Similarly to the near spacing model, further approximations are needed to simplify the geometry.

**Spherical coordinate system**

The injector is taken as a point source \( n_{\text{inj}} \) in the spherical coordinate system, and the detector as a full sphere (Figure 6-4 (a)). Note that only the carriers collected by the bottom half of the sphere contribute to \( \alpha_{\text{NW}} \). In the case of Figure 6-4 (a), by removing the detector and inserting an image sink \( n_{\text{im}} < 0 \), one can always construct a second case that gives the same solution for \( n_{p} \) everywhere in the substrate. This is shown in Figure 6-4 (b). One can see that the current flow lines of Figure 6-4 (a) and Figure 6-4 (b) have the same form. This occurs only with careful choice of \( n_{\text{im}} \).

In the case of Figure 6-4 (b), the electrons in the substrate originate from either \( n_{\text{inj}} \) or \( n_{\text{im}} \). Those from the former have the density of

\[
 n_{p,s} \frac{r}{r_1} = n_{\text{inj}} \frac{e^{\frac{r_1}{R}}}{r_1},
\]

and those from the latter
\( n_{p,im} \frac{r_2}{r_2} = n_{im} \frac{r_1}{L_n} \).  

(6.18)

In (6.17) and (6.18), \( r_1 \) and \( r_2 \) are the distance from \( n_{inj} \) and \( n_{im} \), respectively. The final solution can be found using the superposition principle

\[ n_p \frac{r_1, r_2}{r_1, r_2} = n_{p,s} + n_{p,im}. \]  

(6.19)

Here, \( n_{im} \) must be determined before using (6.19). Although the detector is removed from the geometry of the case of Figure 6-4 (b), it is useful to consider the dashed sphere in Figure 6-4 (b) as a virtual detector. We define the current collected by the virtual detector as the integral of the current density over the surface of the dashed sphere. The solutions for \( n_p \) in the case of Figure 6-4 (a) and Figure 6-4 (b) are identical if the boundary conditions at the surface of the detector and virtual detector are the same.

For the case of Figure 6-4 (a), \( n_p = 0 \) over the surface of the detector. Hence, \( n_{im} \) must be chosen to enforce \( n = 0 \) along the surface of the virtual detector in the case of Figure 6-4 (b). At \( r_1 = d_{det} \) and at \( r_2 = L_{det}/2 \), the surface of the virtual detector, (6.19) gives

\[ n_p \left( d_{det} \frac{L_{det}}{2} \right) = n_{inj} \frac{d_{det}}{L_n} + n_{im} \frac{L_{det}}{2L_n}. \]  

(6.20)

To have \( n_p = 0 \) along the surface of the virtual detector,

\[ n_{im} = -\frac{L_{det}}{2d_{det}} e^{\frac{L_{det} - 2d_{det}}{2L_n}} n_{inj}. \]  

(6.21)

Therefore, the current density along the surface of the virtual detector is
\[
J_{col} = qD_n \nabla n_{p,s} + \nabla n_{p,im} \bigg|_{r = r_{det}} = qD_n \left( 1 + \frac{L_{det}}{2L_n} e^{-\frac{L_{det}}{2L_n}} \right) n_{im} \cdot \frac{L_{det}}{4}.
\] (6.22)

When \(n_{mj}\) and \(n_{im}\) satisfy (6.21), the solutions for \(n_p\) in the case of Figure 6-4 (a) and Figure 6-4 (b) are identical. Hence, the current collected by the detector and the virtual detector are the same, and (6.22) represents the current collected by either of them.

Collection efficiency is found as

\[
\alpha_{NW} = \gamma \cdot \frac{\int J_{col} dS}{I_{mj}} = \frac{\gamma}{2} \left( 2 + \frac{L_{det}}{L_n} \right) \cdot \frac{1}{d_{det}} \cdot e^{-\frac{d_{im}}{L_n}} = \gamma \cdot G_{det} \cdot \frac{1}{d_{det}} \cdot e^{-\frac{d_{im}}{L_n}},
\] (6.23)

where \(G_{det}\) is a geometry factor. The fit of the model to the measurement results is shown in Figure 6-5 (dashed line). The model closely follows the measurement results.

**Cylindrical coordinate system**

If the injector and the detector widths are large and comparable to \(d_{det}\), then the spherical coordinate system cannot be used because the injector can no longer be represented by a point source. The cylindrical coordinate system is a better approximation for these cases. The injector is taken as an infinitely long line source and the detector as a cylinder. Similarly to the approach presented in the previous section, the detector is replaced with an image \(n_{im}\) with opposite polarity. To have \(n_p = 0\) along the surface of the virtual detector, \(n_{mj}\) and \(n_{im}\) must satisfy the following equation
\[ n_{im} = - \frac{K_0 \left( \frac{d_{det}}{L_n} \right)}{K_0 \left( \frac{L_{det}}{2L_n} \right)} \cdot n_{inj}, \]

(6.24)

It can be shown that collection efficiency has the following form,

\[ \alpha_{NW} = \gamma G_{det}' K_1 \left( \frac{d_{det}}{L_n} \right), \]

(6.25)

where \( G_{det}' \) is a geometry factor. Figure 6-5 compares the fit of the models in the spherical and cylindrical coordinate systems to the measurement results. Both models accurately predict the results.

**The general model**

Previous sections suggest that two models for \( \alpha_{NW} \) are needed, one for near spacing and the other for far spacing. The former is used when \( d_{det} \) is smaller or around \( L_n \), while the latter is used when \( L_n \ll d_{det} \). Occasionally, one may need to try both to decide which one to use. Another problem with the proposed models is the difficulty of implementation in circuit simulators. For example, use of the Bessel functions in circuit simulators may be computationally inefficient.

The need to have two separate models for \( \alpha_{NW} \) can be eliminated by using a generalized model that gives a reasonable estimate of \( \alpha_{NW} \) at all \( d_{det} \). We propose an exponential-based equation in the from of

\[ \alpha_{NW} = \gamma \cdot G_{det}' \cdot e^{-\frac{d_{det}}{L_n}}. \]

(6.26)
In (6.26), $\tilde{G}_{\text{det}}$ and $\tilde{L}_n$ are fitting factors and are different from $G_{\text{det}}$ and $L_n$, respectively.

Physical estimates of $G_{\text{det}}$ and $L_n$ can be used as initial guesses for extracting $G_{\text{det}}$ and $\tilde{L}_n$. Figure 6-6 shows that the fit to the measurement results is reasonably good. Note that the fitting factors are chosen to minimize the absolute mean square error, which explains why the fit is much better for higher $\alpha_{\text{NW}}$. Error in calculating $\alpha_{\text{NW}}$ at very far spacing is acceptable because the latchup hazards at such spacing are minimal. Equation (6.26) can be easily implemented in circuit simulators.

**Multi-finger injectors**

Collection efficiency when the injector has more than one stripe can be modeled in two ways. In the first, the multi-finger injector is treated as a single-finger injector placed at a distance $d_{\text{det},s}$ from the detector; then, $d_{\text{det},s}$ is taken as a fitting parameter and $d_{\text{det}} < d_{\text{det},s} < d_{\text{det}} + L_{\text{inj}}$, where $L_{\text{inj}}$ is the length of the injector. In the second, each finger is treated as a separate injector, and the collection efficiency is obtained as

$$\alpha_{\text{NW}} = \sum_{i=1}^{m} \alpha_{\text{NW},i}.$$  \hspace{1cm} (6.27)

In (6.27), $m$ is the number of fingers, and $\alpha_{\text{NW},i}$ is the fraction of the carriers injected by the $i^{th}$ finger that is collected by the detector. The results of both methods are similar. The second method is preferred and used in this work because it has one fewer fitting factor, $d_{\text{det},s}$, which simplifies the model extraction procedure.
6.1.2 Effects of bias voltage

The collection efficiency is an increasing function of \( V_{\text{det}} \) (refer to Section 5.2.3). Empirically, this can be well modeled using an Early voltage construct, as indicated in (6.28).

\[
\alpha \ V_{\text{det}} = \alpha _0 \left( 1 - \frac{V_{\text{det}}}{V_A} \right). \quad (6.28)
\]

The fit of the model to the measurement results is shown in Figure 6-7. Section 5.2.3 shows that, although insensitive to \( d_{\text{det}} \), \( V_A \) is a function of \( W_{\text{det}} \) and \( L_{\text{det}} \). Hence, a model for \( V_A \) as a function of \( L_{\text{det}} \) and \( W_{\text{det}} \) should accompany equation (6.28).

The area of the detector is a function of the depletion width of the N-well/P-well and N-well/substrate junctions \( X_{D,\text{PW}} \) and \( X_{D,\text{SUB}} \), respectively (refer to (5.3)). Here for simplicity, we assume \( X_{D,\text{PW}} \simeq X_{D,\text{SUB}} = X_D \). The terms \( A_{\text{col}}^0 \) and \( A_{\text{col}}^{V_{\text{DD}}} \) denote the detector area for \( V_{\text{det}} = 0 \) and \( V_{\text{det}} = V_{\text{DD}} \), respectively, and are equal to

\[
A_{\text{col}}^0 = W_{\text{det}} + 2X_D^0 \cdot L_{\text{det}} + 2X_D^0 + 2W_{\text{det}} + 2X_D^0 \cdot X_j + X_D^0 \nonumber + 2 \ L_{\text{det}} + 2X_D^0 \cdot X_j + X_D^0, \quad (6.29)
\]

and

\[
A_{\text{col}}^{V_{\text{DD}}} = W_{\text{det}} + 2X_D^{V_{\text{DD}}} \cdot L_{\text{det}} + 2X_D^{V_{\text{DD}}} + 2W_{\text{det}} + 2X_D^{V_{\text{DD}}} \cdot X_j + X_D^{V_{\text{DD}}} \nonumber + 2 \ L_{\text{det}} + 2X_D^{V_{\text{DD}}} \cdot X_j + X_D^{V_{\text{DD}}}. \quad (6.30)
\]

In (6.29) and (6.30), \( X_D^0 \) and \( X_D^{V_{\text{DD}}} \) denote the depletion width of the detector/substrate junction for \( V_{\text{det}} = 0 \) and \( V_{\text{det}} = V_{\text{DD}} \), respectively. It can be shown that...
The data of Figure 6-8 indicate that $\alpha_{NW}$ is an increasing function of $A_{col}$, and that the dependence can be modeled by

\[ \alpha_{NW} \simeq C_1 A_{col} + C_2. \]  

(6.35)

Therefore,

\[ \frac{\alpha_{NW}}{\alpha_{NW}} \frac{V_{DD}}{0} \simeq \frac{C_1 A_{col}^{V_{DD}} + C_2}{C_1 A_{col}^{0} + C_2}, \]  

(6.36)

Which can be simplified to

\[ \frac{\alpha_{NW}}{\alpha_{NW}} \frac{V_{DD}}{0} \simeq \frac{A_{col}^{V_{DD}}}{A_{col}^{0}}, \]  

(6.37)

if
The condition in (6.38) is met, because the change in the detector area is relatively small, for a voltage change from 0 to $V_{DD}$. By substituting (6.37) in (6.34), one gets

$$V_A = \frac{V_{DD}}{\frac{A_{col}^{V_{DD}}}{A_{col}^0} - 1}. \quad (6.39)$$

Equation (6.39) together with (6.33) can be used to estimate $V_A$ as functions of $W_{det}$ and $L_{det}$. The terms $\Delta X_D$ and $X_j$ can be taken as fitting parameters to get the best results. The model is compared to the measurement results in Figure 6-9 and Figure 6-10. Extracted values of $\Delta X_D$ and $X_j$ (0.2 µm and 5 µm, respectively) are within their expected ranges from the process technology.

6.1.3 Effects of temperature

The two key temperature-dependent parameters in the model for $\alpha_{NW}$ are diffusion length $L_n$ and electron injection efficiency $\gamma$. It has been shown that, over the range 25–100 °C, $L_n$ is an increasing function of temperature [36]. The injection efficiency $\gamma$ is analogous to the emitter injection efficiency of an NPN bipolar transistor, which is an increasing function of temperature [35]. Therefore, both $L_n$ and $\gamma$ contribute to the positive temperature dependence of $\alpha_{NW}$. From electrical measurements of the test structures employed in this work, it is not possible to separately extract the temperature dependence of $L_n$ and that of $\gamma$. Therefore, for simplicity, all of the temperature
dependencies are modeled inside $\gamma$. It is found that a linear model well represents $\gamma(T)$.

This linear model was employed in Figure 6-2 and Figure 6-3.

6.1.4 Effects of injection current

So far in this chapter, $\alpha_{NW}$ is assumed to be independent of $I_{inj}$; however, the measurement data of Section 5.2.3 show that $\alpha_{NW}$ decreases at high currents. This high-level injection (HLI) effect is addressed by modeling the injection efficiency as a decreasing function of the current density [42]. We know that $\gamma$ is defined as:

$$\gamma = \frac{I_{E,n}}{I_E} = \frac{I_{E,n}}{I_{E,n} + I_{E,p}} = \frac{1}{1 + \frac{I_{E,p}}{I_{E,n}}}. \tag{6.40}$$

In (6.40), $I_{E,n}$ and $I_{E,p}$ are the currents carried by electrons and holes, respectively, at the emitter-base junction. To find $I_{E,p}$, the diffusion equation in the emitter is solved. The high background doping density of the emitter permits the use of the low-level injection (LLI) assumption. Hence,

$$I_{E,p} = 2\pi qD_p p_{E0} \left( \frac{qV_{BE}}{e^{kT}} - 1 \right). \tag{6.41}$$

$D_p$ is the hole diffusion constant, and $p_{E0}$ is the equilibrium hole density in the emitter region. To find $I_{E,n}$, the minority carrier distribution in the substrate, $n_p$, is given in (6.10). Under HLI, the boundary conditions are

$$\begin{cases} n_p (r = L_{inj \_ det}) = 0, \\ n_p (r = 0) = \frac{n_p^2 (r = 0)}{N_{SUB}} \left( \frac{qV_{BE}}{e^{kT}} - 1 \right), \end{cases} \tag{6.42}$$
and these are applied to find $C_1$ and $C_2$ in (6.10). In (6.42), $N_{SUB}$ is the substrate (base region) doping density. The base region of $Q_{NPN2}$ is not uniformly doped; nevertheless, the assumption of uniform doping in the base region significantly simplifies the analyses. The results are later parameterized, which corrects for any error introduced by this assumption. At high currents, the substrate majority carrier density increases to maintain neutrality, and this gives rise to an electric field. Therefore, under HLI, $I_{E,n}$ has both diffusion and drift components. Carrying out the algebra and making a few simplifications, one obtains

$$I_{E,n} = \frac{\pi q D_n n_i^2 \left( \frac{q V_{gh}}{kT} - 1 \right)}{N_{SUB} K_0 \left( \frac{X_E}{L_n} \right) \left( 1 + \ln \left( \frac{d_{det}}{X_E} \right) \cdot I_{inj} \right) \cdot \frac{q D_n N_{SUB}}{W_{inj}}}.$$  (6.43)

In (6.43), $X_E$ is the depth of the $N^+$ diffusion region of the injector, $D_n$ is the electron diffusion constants, and $W_{inj}$ is the width of the injector. Finally, $\gamma$ is found by substituting (6.41) and (6.43) in (6.40):

$$\gamma = \frac{1}{1 + 2 \frac{D_p N_B}{D_n N_E} K_0 \left( \frac{X_E}{L_n} \right) \left( 1 + \ln \left( \frac{d_{det}}{X_E} \right) \cdot I_{inj} \right) \cdot \frac{q D_n N_B}{W_{inj}}}.$$  (6.44)

In (6.44), $N_E$ is the doping density of the $N^+$ diffusion region of the injector. Hence, $\alpha_{NW}$ can be approximately written as
\[ \alpha_{NW} \approx \frac{\alpha_0}{1 + \frac{I_{inj}}{I_K}}. \]  

Above, \( \alpha_0 \) is given in Section 6.1.1, and \( I_K \) is defined as

\[ I_K = \frac{2qN_e W_{inj} D_n^2}{D_p \ln \left( \frac{d_{det}}{X_E} \right) K_0 \left( \frac{X_E}{L_n} \right)} \approx \frac{I_{K0}}{\ln d_{det}}. \]  

From (6.46), \( I_K \) is a decreasing function of \( d_{det} \) and may be treated as a fitting parameter. The fit of the model to the data is demonstrated in Figure 6-11 and Figure 6-12 for RF-CMOS and SmartMOS technologies.

### 6.2 Effects of Guard Rings on the Collection Efficiency

The NGR lowers the collection efficiency of the detector by collecting some of the electrons in the substrate. The term \( \alpha^*_{NW} \) denotes the collection efficiency of the detector when NGR is present and is obviously smaller than \( \alpha_{NW} \). Referring to Section 5.2.4, \( \alpha^*_{NW} \) is a function of the injection current \( I_{inj} \), the guard ring length \( L_{NGR} \), and the NGR distance from the injector \( d_{NGR} \) (Figure 6-13 (a)). The collection efficiency of the NGR when other carrier detectors are absent is denoted by \( \alpha_{NGR} \). The modeling approach in Section 6.1 can be used to model \( \alpha_{NGR} \) as a function of \( d_{NGR}, L_{NGR}, \) and \( I_{inj} \). However, a new model for \( \alpha^*_{NW} \) must be developed.

#### 6.2.1 Modeling \( \alpha^*_{NW} \)

The modeling approach presented in Section 6.1 assumes that the injected electrons either recombine in the substrate or get collected by the detector. This
assumption is false when NGR is active, and, hence, the previous models cannot be
directly used to model $\alpha_{\text{NW}}^*$. The goal of this section is to build a model for $\alpha_{\text{NW}}^*$ based
on the existing models for $\alpha_{\text{NW}}$ and $\alpha_{\text{NGR}}$.

Figure 6-13 (b) and Figure 6-13 (c) show two device cross-sections, one with and
one without NGR, respectively. Let us assume that the number of electrons injected per
cm$^2$ into the substrate of the devices shown in Figure 6-13 (b) and Figure 6-13 (c) are
different and denoted by $N_{\text{inj}}^*$ and $N_{\text{inj}}$, respectively. Similarly, the injected electron
densities in Figure 6-13 (b) and Figure 6-13 (c) are denoted as $n_{\text{inj}}^*$ and $n_{\text{inj}}$, respectively.
In Figure 6-13, $S_1$ is a hypothetical box that separates the injector and the NGR from the
substrate. In Figure 6-13 (b), where NGRs are present, $n_{\text{inj, sub}}^*$ and $N_{\text{inj, sub}}^*$ denote the
number of electrons along the edges of $S_1$ per cm$^3$ and per cm$^2$, respectively. Similarly in
Figure 6-13 (c), where NGR is absent, $n_{\text{inj, sub}}$ and $N_{\text{inj, sub}}$ denote the number of electrons
along the edges of $S_1$ per cm$^3$ and per cm$^2$, respectively. The number of electrons
collected by the detectors in Figure 6-13 (b) and Figure 6-13 (c) are denoted by $N_{\text{col}}^*$ and
$N_{\text{col}}$, respectively.

Obviously, $N_{\text{col}}^*$ and $N_{\text{col}}$ are functions of $N_{\text{inj}}^*$ and $N_{\text{inj}}$, respectively. We will
show that there exists a constant $C_1$ such that $N_{\text{col}}^* = N_{\text{col}}$ when $N_{\text{inj}} = C_1 N_{\text{inj}}^*$. For these
choices of $N_{\text{inj}}^*$ and $N_{\text{inj}}$,

$$
\alpha_{\text{NW}}^* \equiv \frac{N_{\text{col}}^*}{N_{\text{inj}}^*} = \frac{N_{\text{col}}}{N_{\text{inj}}^*} = \frac{N_{\text{inj}}}{N_{\text{inj}}^*} \frac{N_{\text{col}}}{N_{\text{inj}}} = \frac{N_{\text{inj}}}{N_{\text{inj}}^*} \alpha_{\text{NW}} = C_1 \alpha_{\text{NW}}. \quad (6.47)
$$
Equation (6.47) indicates that if \( C_I \) were known, one could construct a model for \( \alpha_{NW}^* \) using the model presented earlier in this chapter for \( \alpha_{NW} \) together with (6.47). An expression for \( C_I \) is obtained below.

Referring to Figure 6-13 (a), the X and Y directions are horizontal and vertical, respectively; \( X = 0 \) is the surface of the silicon and \( Y = 0 \) is the center of the injector. Therefore, the injector lies between \(-L_{inj}/2 \) and \( L_{inj}/2 \), where \( L_{inj} \) is the length of the injector. The number of electrons per \( \text{cm}^3 \) is related to the number of electrons per \( \text{cm}^2 \) by

\[
N_{inj\_sub}^* = \int_{S_1} n_{inj\_sub}^* \cdot dr = \int_{S_1} n_{inj\_sub}^* \cdot dx \quad \left| \begin{array}{c}
X=X_{pw} \\
X=0
\end{array} \right| 
+ \int_{X=0}^{X=X_{pw}} n_{inj\_sub}^* \cdot dx \\
+ \int_{Y=Y_{inj}}^{Y=Y_{inj}} n_{inj\_sub}^* \cdot dy
\]

and

\[
N_{inj\_sub} = \int_{S_1} n_{inj\_sub} \cdot dr = \int_{S_1} n_{inj\_sub} \cdot dx \quad \left| \begin{array}{c}
X=X_{pw} \\
X=0
\end{array} \right| 
+ \int_{X=0}^{X=X_{pw}} n_{inj\_sub} \cdot dx \\
+ \int_{Y=Y_{inj}}^{Y=Y_{inj}} n_{inj\_sub} \cdot dy
\]

in Figure 6-13 (b) and Figure 6-13 (c), respectively. The first two terms in the right-hand sides of (6.48) and (6.49) are the integrals along the right and the left (vertical) edges of \( S_1 \), and the last terms are the integrals along the bottom (horizontal) edge of \( S_1 \). The length of the left and the right edges of \( S_1 \) is \( X_{pw} \), and the length of the bottom edge is \( L_{inj} + 2d_{NGR} + 2L_{NGR} \). We found that the first two terms in the right-hand sides of (6.48)
and (6.49) can be neglected. This is a reasonable approximation because $X_{PW} \ll L_{\text{inj}} + 2d_{\text{NGR}} + 2L_{\text{NGR}}$ in most designs. Therefore, (6.48) and (6.49) are simplified to

$$N_{\text{inj}_{\sub}}^+ \approx \int_{Y=-\frac{L_{\text{inj}}}{2} - d_{\text{NGR}} - L_{\text{NGR}}}^{X=X_{PW}} n_{\text{inj}_{\sub}}^+ \cdot dy,$$

and

$$N_{\text{inj}_{\sub}}^- \approx \int_{Y=-\frac{L_{\text{inj}}}{2} - d_{\text{NGR}} - L_{\text{NGR}}}^{X=X_{PW}} n_{\text{inj}_{\sub}}^- \cdot dy.$$

We need $n_{\text{inj}_{\sub}}^+$ and $n_{\text{inj}_{\sub}}^-$ to calculate the integrals of (6.50) and (6.51). Figure 6-14 (a) shows that the electrons near the injector are almost uniformly distributed when NGRs are absent. Therefore, we can assume that the electron density along the bottom surface of $S_1$ is approximately constant when guard rings are absent, which gives

$$N_{\text{inj}_{\sub}} = \int_{-\frac{L_{\text{inj}}}{2} - d_{\text{NGR}} - L_{\text{NGR}}}^{\frac{L_{\text{inj}}}{2} + d_{\text{NGR}} + L_{\text{NGR}}} n_{\text{inj}_{\sub}} \cdot dy \approx n_{\text{inj}_{\sub}, 0} \cdot L_{\text{inj}} + 2d_{SGR} + 2L_{SGR},$$

where $n_{\text{inj}_{\sub}, 0}$ is the electron density at $X = X_{PW}$ and is related to $n_{\text{inj}}$ by

$$n_{\text{inj}_{\sub}, 0} = 1 - B \cdot n_{\text{inj}}.$$

In (6.53), $0 < B < 1$ represents the fraction of injected electrons that has recombined in the P-well. It is a function of the P-well background doping and depth. From (6.52) and (6.53), one obtains
\[ N_{\text{inj\_sub}} = n_{\text{inj}} \cdot \left( 1 - B \cdot L_{\text{inj}} + 2d_{NGR} + 2L_{NGR} \right) . \] (6.54)

For two reasons, \( N_{\text{inj\_sub}}^{*} \) is different from \( N_{\text{inj\_sub}} \) in (6.52). First, the NGRs collect some of the electrons in the P-well that would cross into the substrate otherwise. Second, the N-well/substrate junction forces the electron density to be near zero, which means that there should be almost no electrons beneath the NGRs. Figure 6-15 shows \( n_{\text{inj\_sub}}^{*} \) along the bottom edge of \( S_1 \). Note that the electron distribution near the injector is non-uniform in the \( Y \) direction when NGRs are present. The value of \( n_{\text{inj\_sub}}^{*} \) is highest right below the injector \( (0 < \left| Y \right| < \frac{L_{\text{inj}}}{2}) \) and becomes almost zero below the NGRs. In (6.50), the integral of \( n_{\text{inj\_sub}}^{*} \) is needed to calculate \( N_{\text{inj\_sub}}^{*} \). Because of its complicated shape, the exact profile is approximated by the dashed curve showed in Figure 6-15, where \( n_{\text{inj\_sub}}^{*} \) is assumed constant for \( 0 < \left| Y \right| < Y_0 \) and equal to zero for

\[ Y_0 < \left| Y \right| < \frac{L_{\text{inj}}}{2} + d_{NGR} + L_{NGR} . \]

The value of \( Y_0 \) is chosen to ensure that the areas under the solid and the dashed curves are equal.

By integrating the approximated electron density profile, \( N_{\text{inj\_sub}}^{*} \) can be found:

\[
N_{\text{inj\_sub}}^{*} = n_{\text{inj\_sub}}^{*} \cdot \left. \frac{L_{\text{inj}}}{2} + d_{NGR} + L_{NGR} \right|_{Y = \frac{L_{\text{inj}}}{2} - d_{NGR} - L_{NGR}} \bigg|_{X = X_{pg}} = n_{\text{inj\_sub}_0}^{*} \cdot 2Y_0 , \tag{6.55}
\]

where
In (6.57), it is assumed that the collection efficiency of the NGR is independent of the detector, which is usually true because $d_{\text{NGR}} \ll d_{\text{det}}$ and $\alpha_{\text{NGR}} >> \alpha_{\text{NW}}$. Equation (6.55) can be rewritten as

$$N_{\text{inj}_{\text{sub}}}^* = n_{\text{inj}}^* \cdot 1 - B - \alpha_{\text{NGR}}^* \approx n_{\text{inj}}^* \cdot 1 - B - \alpha_{\text{NGR}}^*.$$  \hspace{1cm} (6.58)

From (6.54) and (6.58), one concludes that if $N_{\text{inj}_{\text{sub}}}^*$ and $N_{\text{inj}_{\text{sub}}}^*$ were equal, one would hypothesize that the total number of electrons that leave $S_1$ is the same in both cases, and, hence, the number of the electrons collected by the detectors in Figure 6-13 (b) and Figure 6-13 (c) would be approximately equal. This condition is met when $N_{\text{inj}_{\text{sub}}}^*$ and $N_{\text{inj}_{\text{sub}}}^*$ from (6.54) and (6.58) are equal:

$$n_{\text{inj}}^* = \frac{n_{\text{inj}}^* \cdot 1 - B - \alpha_{\text{NGR}}^* \cdot L_{\text{inj}} + 2A \cdot d_{\text{NGR}}}{1 - B \cdot L_{\text{inj}} + 2d_{\text{NGR}} + 2L_{\text{NGR}}} = n_{\text{inj}}^* \cdot A{^*} B{^*} - \alpha_{\text{NGR}}^*.$$  \hspace{1cm} (6.59)

where

$$\begin{align*}
A{^*} &= \frac{L_{\text{inj}} + 2A \cdot d_{\text{NGR}}}{1 - B \cdot L_{\text{inj}} + 2d_{\text{NGR}} + 2L_{\text{NGR}}} \\
B{^*} &= 1 - B - \alpha_{\text{NGR}}.
\end{align*}$$ \hspace{1cm} (6.60)

Therefore, one can find $C_1$ as

$$A = \frac{Y_0 - \frac{L_{\text{inj}}}{2}}{d_{\text{NGR}}},$$ \hspace{1cm} (6.56)
\[ C_I = \frac{N_{inj}}{N_{inj}^*} = A' B' - \alpha_{NGR} \cdot \alpha_{NW}. \]  

(6.61)

Therefore, using (6.47), it can be shown that \( \alpha_{NW} \) and \( \alpha_{NW}^* \) are related by

\[ \alpha_{NW}^* = C_I \cdot \alpha_{NW} = A' B' - \alpha_{NGR} \cdot \alpha_{NW}. \]  

(6.62)

Analytical models for \( \alpha_{NW} \) and \( \alpha_{NGR} \) are constructed according to Section 6.1.

Therefore, one can use (6.62) to estimate \( \alpha_{NW}^* \) as a function of the layout geometry.

Parameters \( A' \) and \( B' \) can be taken as fitting factors to get the optimum results.

Figure 6-16 and Figure 6-17 show the fit of the model to the measurement results. The model is capable of capturing the effects of guard ring design parameters, \( L_{NGR} \) and \( d_{NGR} \), as well as \( I_{inj} \).

6.3 Modeling the Latchup Trigger Current

The circuit-level models presented in Chapter 4 are used to predict \( I_{trig} \) for a given layout and bias condition. They are shown in Figure 6-18, Figure 6-19, and Figure 6-20.

To model the effect of the PGR, \( R_{PGR} \) is added to the schematics.

In Section 4.1.2, we showed that latchup in a positive I-test is triggered when

\[ I_{coll,p} = I_{PW}^{crit}. \]  

The current collected by the P-well of the victim, \( I_{coll,p} \), can be written as

\[ I_{coll,p} = f I_{inj} \alpha_{P+P2} d_{victim} L_{PGR} d_{PGR}. \]  

(6.63)

The device cross-section of Figure 6-21 shows the substrate resistive network formed between the injector and the grounded \( P^+ \) and \( N^+ \) diffusions of the victim. Function \( f \) in (6.63) can be implemented by modeling and extracting the resistive network of Figure
A complete model of the substrate network can be constructed only by numerical techniques such as those presented in [43]. However, in this work, we seek a method that is computationally efficient. Therefore, a simplified resistive network shown in Figure 6-19 is proposed. Assuming \( Q_{\text{PnP2}} \) does not enter into the saturation mode,

\[
I_{\text{coll,p}} = \frac{R_{\text{PGR}}}{R_{\text{PGR}} + R_{\text{SUB}} + R_{\text{PW}}} \alpha_{\text{PnP2}} I_{\text{inj}} - \frac{\alpha_{\text{PnP2}} I_{\text{inj}}}{f_1(L_{\text{PGR}}, d_{\text{PGR}})}
\]

(6.64)

Above, \( f_1 \) is a weakly increasing function of \( d_{\text{victim}} \), and \( f_2 \) is a decreasing function of guard ring length, \( L_{\text{PGR}} \), and an increasing function of \( d_{\text{PGR}} \). In [44], a similar approach is used for modeling the substrate for evaluating the substrate noise hazards. Analytical models for \( f_1(d_{\text{victim}}) \) and \( f_2(L_{\text{PGR}}, d_{\text{PGR}}) \) are presented in [44]. The extraction of the fitting parameters of the model requires test structures that, unfortunately, were not available. In this work, \( R_{\text{SUB}} \) and \( R_{\text{PGR}} \) are extracted from measurement results of \( I_{\text{trig}} \) vs. \( L_{\text{PGR}} \) (consult Figure 6-25) as well as the measured base resistance of \( Q_{\text{NPN1}} \) (\( R_{b,\text{NPN1}} \)) [45], which gives the sum of \( R_{\text{SUB}} \) and \( R_{\text{PGR}} \) as

\[
R_{\text{PGR}} + R_{\text{SUB}} = \frac{R_{\text{PW}} R_{b,\text{NPN1}}}{R_{\text{PW}} - R_{b,\text{NPN1}}}.
\]

(6.65)

Simulations are done in Spectre and the results are shown in Figure 6-22 and Figure 6-23 for the positive I-test and the undervoltage test, respectively, when guard rings are inactive. The effect of guard rings are simulated and compared to the measurement results as shown in Figure 6-24 and Figure 6-25. A good fit between the model and the measurements is observed for all cases.
6.3.1 Parameter extraction

Parameter extraction must be done before one can simulate the circuit schematics. The Gummel–Poon model is used for all the transistors except Q_{NPN2}. For the other transistors, except Q_{PNP3}, saturation current (I_S) and current gain are extracted from a plot of I_C vs. V_{BE} and a Gummel plot, respectively [45]. The model parameters for Q_{PNP3} cannot be extracted using these procedures because its terminals are inaccessible. Instead, its parameters are extracted from substrate current measurements, such as the one in Figure 4-6. The values of R_{NW1} and R_{PW1} are functions of well-tap spacing and are extracted from collector resistance measurements on Q_{PNP1} and Q_{NPN1}, respectively [45].

We cannot model Q_{NPN2} well with standard, compact BJT models due to its highly non-uniform geometry and boundary conditions. Instead, the models presented in Sections 6.1 and 6.2 are used. The model presented in Section 6.2 is used when NGRs are active. A few test structures, described below, have to be fabricated to extract the fitting factors of the model, I_{K0}, A, B, \tilde{G}_{det}, and \tilde{L_n}.

Table 6-1 lists the test structures needed for extracting the fitting parameters of the model for \alpha_{NW} and \alpha_{NW}^*. The test structures consist of an injector and a victim, similar to those shown in Figure 5-1 (a). The test structures with at least three different injector-to-victim spacings, d_{victim,1}, d_{victim,2}, and d_{victim,3}, must be used to extract the fitting factors. We recommend that d_{victim,1} be taken as the minimum spacing between the injector and victim allowed in the technology, and that d_{victim,2} and d_{victim,3} be a typical, relatively large injector-to-victim spacing, respectively. We recommend to take d_{NGR,1} and L_{NGR,1} as the minimum allowed in the technology, and to take d_{NGR,2} and L_{NGR,2} as a typical guard ring spacing and length, respectively. By measuring the collection
efficiency of structures T_1, T_2, and T_3, and finding the best fit-to-measurement results, one can extract $\tilde{G}_{\text{det}}$ and $\tilde{L}_u$. Structures T_1 and T_4 are needed to extract parameters A and B in order to construct a model for $\alpha^*_{\text{NW}}$. Measurement of $\alpha_{\text{NW}}$ vs. $I_{\text{inj}}$ on structures T_1, T_2, and T_3 can be used to extract $I_{\text{K0}}$.

As presented in Section 5.2.1, $\tilde{G}_{\text{det}}$ is a function of detector width and length, $W_{\text{det}}$ and $L_{\text{det}}$. We found that models for the geometry factors are best implemented using lookup tables, where $\tilde{G}_{\text{det}}$ is recorded for different combinations of $W_{\text{det}}$ and $L_{\text{det}}$. Data of Figure 5-6 and Figure 5-7 indicate that a line could result in a good fit for $L_{\text{det}} > 20 \, \mu\text{m}$ and $W_{\text{det}} > 5 \, \mu\text{m}$. Therefore, test structures with only two different $L_{\text{det}}$ and two different $W_{\text{det}}$ are enough for constructing a model for $\tilde{G}_{\text{det}}$. These structures are labeled as T_5 and T_6 in Table 6-1. Additional test structures may be needed for modeling small detector geometries.

### 6.4 Figures

![Diagram](image)

Figure 6-1: Current density in a test structure was simulated using DESSIS. The injector diode is forward-biased, and the detector N-well is reverse-biased.
Figure 6-2: $\alpha_{NW}$ vs. $d_{det}$ and temperature. RF-CMOS technology. Markers are measurement data, and solid lines are the model. Model parameter $L_n = 55$ $\mu$m.

Figure 6-3: $\alpha_{NW}$ vs. $d_{det}$ and temperature. SmartMOS technology. Markers are measurement data, and solid lines the model. Model parameter $L_n = 25$ $\mu$m. For these multi-finger injectors, $d_{det}$ is measured from the injector finger closest to the detector.
Figure 6-4: Current flow lines in the substrate. The injector is a point source $n_{inj}$ at the left side of the figures. At the right side, the detector is a sphere in (a) and a point sink $n_{im}$ in (b). $n_{im}$ is chosen in a way to recreate the current flow lines of (a). The dashed lines in (b) represent the virtual detector. The current collected by the detector in (a) and the virtual detector in (b) are the same when $n_{im}$ is chosen according to (6.21).
Figure 6-5: $\alpha_{NW}$ as a function of $d_{det}$. Markers show the measurement data, the solid line the spherical model, and the dashed line the cylindrical model. 90-nm CMOS technology. Room temperature.

Figure 6-6: $\alpha_{NW}$ as a function of $d_{det}$. Markers show the measurement results, and the line shows the model. 90-nm CMOS technology. Room temperature.
Figure 6-7: $\alpha_{NW}$ as a function of detector voltage $V_{det}$ and $d_{det}$. Markers show the measurement data, and solid lines show the model. RF-CMOS technology. Room temperature.

Figure 6-8: $\alpha_{NW}$ as a function of the detector area. 90-nm CMOS technology. Room temperature.
Figure 6-9: $V_A$ as a function of $W_{\text{det}}$. Markers show the measurement results, and the solid curve shows the model. 90-nm CMOS technology. Room temperature.

Figure 6-10: $V_A$ as a function of $L_{\text{det}}$. Markers show the measurement results, and the solid curve shows the model. 90-nm CMOS technology. Room temperature.
Figure 6-11: $\alpha_{NW}$ vs. $I_{inj}$. Markers show the measurement data, and solid lines show the model. RF-CMOS technology. Room temperature. The injector is a single-finger P-well diode.

Figure 6-12: $\alpha_{NW}$ vs. $I_{inj}$. Markers show the measurement data, and solid lines show the model. SmartMOS technology. Room temperature. The injector is a 25-finger P-well diode.
Figure 6-13: Device cross-section of an injector near a detector. In (a) and (b) NGRs are present and in (c) NGRs are absent. $n_{\text{inj}}$ and $n_{\text{inj}}$ are the injected electron density in (b) and (c), respectively. $n_{\text{col}}$ and $n_{\text{col}}$ are the collected electron density by the detectors of (b) and (c), respectively. $S_1$ is a hypothetical box that encloses the injector and NGRs.
Figure 6-14: Contours of electron density near the injector when (a) NGRs are absent and (b) NGRs are present. Injector is a P-well diode with five fingers. Note that there is only one contour line in (a), while there are several in (b), which means that the electron distribution near the injector is less uniform when NGRs are present (b). This is caused by the boundary condition at the depletion regions of the NGR/substrate and the NGR/P-well junctions. The detector is at the far right side of the injector (not shown in the diagrams).
Figure 6-15: $n_{\text{inj, sub}}$ along the bottom (horizontal) edge of $S_1$, underneath the injector and the NGR (at $X = X_{\text{PW}}$). The solid curve is extracted from the device simulation results of Figure 6-14(b), and the dashed line is an approximated curve for estimating the area under the solid curve. $Y_0$ is chosen to ensure that the areas under the solid and the dashed curves are equal.

Figure 6-16: $\alpha^+_{\text{NW}}$ as a function of $I_{\text{inj}}$. NGRs are biased at $V_{\text{DD}}$. Markers show the measurement results, and the solid lines show the model. 130-nm CMOS technology. Room temperature.
Figure 6-17: $\alpha_{NW}^*$ as a function of $I_{inj}$. NGRs are biased at $V_{DD}$. Markers show the measurement results, and the solid lines show the model. 130-nm CMOS technology. Room temperature.

Figure 6-18: Circuit-level model of a substrate current injector (P-well diode) next to a victim (PNPN), for a negative I-test.
Figure 6-19: Circuit-level model of a substrate current injector (N-well diode) next to a victim for a positive I-test.

Figure 6-20: Circuit-level model of a substrate current injector (N-well diode) next to a victim for an undervoltage test on $V_{DDIO}$. 
Figure 6-21: Substrate resistive network formed between the injector and P+ and N+ diffusions of the victim.

Figure 6-22: $I_{\text{trig}}$ vs. $d_{\text{det}}$ for a positive I-test with an N-well injector (see Figure 4-4). Markers are measurement data, and solid lines are the model. The injector is a 25-finger P-well diode. Victim orientation is 180°. SmartMOS technology. Room temperature.
Figure 6-23: $I_{\text{trig}}$ vs. $d_{\text{det}}$ for an undervoltage test. An external resistor ($R_{\text{NW,ext}} = 10$ kΩ) is connected to the N-well contact of the PNPN to increase $R_{\text{NW}}$. Victim orientation is 180º. SmartMOS technology. Room temperature.

Figure 6-24: $I_{\text{trig}}$ of a negative I-test as a function of the NGR length. Markers are measurement data, and solid lines are the model. The leftmost data point belongs to an unbiased NGR. Victim orientation is 0º. 130-nm technology. Temperature is 100 ºC.
Figure 6-25: $I_{\text{trig}}$ of a positive I-test as a function of the PGR length. Markers are measurement data, and solid lines are the model. The leftmost data point belongs to an unbiased PGR. Victim orientation is 0º. 130-nm technology. Room temperature.

6.5 Table

Table 6-1: The necessary test structures for extracting the fitting parameters for modeling $I_{\text{trig}}$ of a negative I-test. Device cross-sections of the test structures are shown in Figure 5-1 (a).

<table>
<thead>
<tr>
<th>Test Structure</th>
<th>$d_{\text{victim}}$</th>
<th>$d_{\text{NGR}}$</th>
<th>$L_{\text{NGR}}$</th>
<th>$L_{\text{det}}$</th>
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CHAPTER 7

TRANSIENT LATCHUP TESTING

7.1 Experimental Setup

Figure 7-1 and Figure 7-2 illustrate the experimental setup and the test structures used to study TLU in this work. A high-power pulse generator, with output impedance of 50 Ω, is connected to the signal pad of the test structure, labeled I/O, via a rise-time filter (RTF) and a 50-Ω resistive matching network. The RTF sets the rise-time of the pulse, $t_r$, to the desired value, which is 7 ns, unless otherwise noted. The pulse-width, $T_{PW}$, is variable. The use of the matching network results in cleaner pulse waveforms by eliminating reflections [46]. The current injected into the signal pin, $I_{inj}$, is calculated by measuring the voltage drop across $R_s$ of the matching network (refer to Figure 7-1). The current provided by the power supply connected to the PNPN, or victim, is denoted by $I_{DD}$. Latchup is said to have been triggered if $I_{DD}$ exceeds 2 mA after the trigger source has been removed.

The length of the ground connection between the power supply and the pulse generator is important. Because of the fast rise-time of the pulse, one has to ensure that the voltage drops across the parasitic inductances are not significant enough to alter the measurement results. Litz cables, which have very small inductance, are used everywhere a ground jumper is needed, for example, to connect the grounds of the pulse generator.
and the dc supply. It is best to connect the N⁺ and P⁺ diffusions inside the P-well of the victims on silicon. This helps to minimize the inductance between the diffusions.

In the setup for the positive I-test TLU, the current injected into the I/O pin has its return path. The inductance of the cable that connects the power supply to the device under test degrades the quality of the injection waveform, as shown in Figure 7-3. In a real chip, the on-chip decoupling capacitors connected to V_{DDIO} provide an alternative current path for the injection current, which bypasses the dc power supply. The test structures that have on-chip capacitors are highly recommended if measurements with a pulse-width of less than 50 ns are done. Unfortunately, such test structures were not available in time for this work. Therefore, results with T_{PW} less than 50 ns are not reported.

It is important to note that during a negative [positive] I-test, the PN junction injects minority [majority] carriers into the substrate. It is normal practice to surround a minority carrier injector with an N-well guard ring (NGR), to prevent the electrons from reaching the victims. Similarly, majority carrier injectors are surrounded by P-type guard ring (PGR), which is comprised of a P⁺ diffusion inside a P-well. The guard ring efficacy may be assessed by measuring I_{trig} both with and without the guard ring activated. An inactive guard ring is left floating; in this work, an active NGR is connected to V_{DD}, and an active PGR is connected to V_{SS}.  

100
7.2 Results and Discussions

7.2.1 Pulse-width dependence

The pulse-width dependence of \( I_{\text{trig}} \) is investigated by changing the \( T_{\text{PW}} \) of the trigger source. The measurement results are shown in Figure 7-4 and Figure 7-5. The results shown in Figure 7-4 confirm previous observations [3], [4]: negative \( I_{\text{trig}} \) is a decreasing function of \( T_{\text{PW}} \). These data also show that for a fixed spacing between substrate current injector and victim (\( d_{\text{victim}} \)), negative \( I_{\text{trig}} \) is virtually identical for 90- and 130-nm CMOS technologies. The data of Figure 7-5 reveal that positive \( I_{\text{trig}} \) is also a function of pulse-width; a comparison of Figure 7-4 and Figure 7-5 indicates that \( I_{\text{trig}} \) becomes independent of \( T_{\text{PW}} \) on a significantly shorter time scale under positive test conditions than under negative test conditions. The different time dependencies observed under positive and negative test conditions suggest that these time dependencies are not intrinsic to the victim. This hypothesis is confirmed by applying a pulsed overvoltage to the \( V_{DD} \) terminal of the victim so as to trigger internal latchup. The measurement results of Figure 7-6 show that the latchup trigger voltage is independent of \( T_{\text{PW}} \) on a time scale ranging from less than 100 ns up to 100 \( \mu \text{s} \).

The pulse-width dependence of negative \( I_{\text{trig}} \) is attributed to the non–quasi-static behavior of the parasitic NPN transistor \( Q_1 \), formed by the \( N^+ \) region of the injector, the P-substrate, and \( NW_1 \) (refer to Figure 7-1). This is confirmed by an experiment. The potential at the emitter of \( Q_{\text{NPN2}} \) is pulled below zero, resulting in a non-zero emitter current. The steady-state value of \( I_{E} \) is just a little bit less than the value of \( I_{\text{trig}} \) obtained from the static I-test. The measured rise-time for \( I_{E} \) is 7 ns. The collector current \( I_{C,\text{NPN1}(t)} \) is monitored. As shown in Figure 7-7, \( I_{C,\text{NPN2}} \) approaches steady state far more slowly.
than does $I_E$. We know from Section 4.1.1 that latchup is triggered when $I_{C,NPN2}$ is large enough to forward-bias the base-emitter junction of the victim, i.e., when

$$I_{C,NPN2} = I_{NW}^{crit}.$$  (7.1)

In (7.1), $I_{NW}^{crit}$ is the minimum amount of current that has to be collected by NW$_1$ to trigger latchup. Based on Figure 7-7, if the current injected at the I/O pad is just slightly higher than the static $I_{trig}$, it will take about 10 $\mu$s for $I_{C,NPN2}$ to reach $I_{NW}^{crit}$. Therefore, $I_{trig}$ should be a decreasing function of $T_{PW}$ for $T_{PW} \leq 10$ $\mu$s, which is consistent with the data of Figure 7-4.

Slowly, $I_{C,NPN2}$ increases as a result of the large transit time for minority carriers in the substrate. The transit time is affected by recombination in the base region of Q$_{NPN2}$. One may show this mathematically by solving the diffusion equation in the base region of Q$_{NPN2}$ to obtain an analytical expression for $I_{C,NPN2}(t)$. A closed-form solution cannot be obtained if one attempts to model the non-uniform, three-dimensional geometry of Q$_{NPN2}$. Here, we formulate and solve the diffusion equation for a simplified NPN transistor that has uniform geometry in two dimensions. This transistor is shown in Figure 7-8. The base length in the x-direction is $d_{base}$. Under low-level injection conditions, the continuity equation in the base is written as

$$\frac{\partial n_p}{\partial t} = \frac{1}{q} \frac{\partial J_n}{\partial x} - \frac{n_p}{\tau_n}.$$  (7.2)

In (7.2), $J_n$ and $\tau_n$ are the current density and the carrier lifetime, respectively, of electrons in the substrate (base of Q$_{NPN2}$). Neglecting any drift component, the electron current in the base region may be written as
\[ J_n = qD_n \frac{\partial n_p}{\partial x}, \]  

(7.3)

where \( D_n \) is the diffusion constant for electrons in the substrate. Substituting this expression for \( J_n \) into (7.2), one obtains the diffusion equation,

\[ \frac{\partial n_p}{\partial t} = D_n \frac{\partial^2 n_p}{\partial x^2} - \frac{n_p}{\tau_n}. \]  

(7.4)

The partial differential equation (7.4) is solved by the Laplace transform method. Taking the Laplace transform of (7.4) and solving for \( N_p(s,x) \), one gets

\[ N_p(s,x) = C_1 e^{-\frac{s+1}{D_n \tau_n} D_n \tau_n x} + C_2 e^{-\frac{s+1}{D_n \tau_n} D_n \tau_n x}, \]  

(7.5)

and

\[ J_n(s,x) = qD_n \frac{\partial N_p(s,x)}{\partial x} = qD_n \left[ C_2 e^{-\frac{s+1}{D_n \tau_n} D_n \tau_n x} - C_1 e^{-\frac{s+1}{D_n \tau_n} D_n \tau_n x} \right]. \]  

(7.6)

One may set \( C_2 \) to zero, as long as the solution will not be used to find the current in devices with \( d_{base} << \sqrt{D_n \tau_n} \), the diffusion length for electrons in the substrate. \( C_1 \) is found by considering the boundary condition at the base edge \( x = 0 \),

\[ J_n(t,0) = J_E \cdot u(t), \]  

(7.7)

where \( u(t) \) is the unit step function and \( J_E \) is the emitter current density. A unit step function is used in (7.7) because the source driving the emitter has a very fast rise-time,
justifying the step function approximation, which greatly simplifies the algebra. Equation (7.7) can be rewritten in the Laplace domain,

\[ J_n(s, 0) = \frac{J_E}{s}. \]

(7.8)

Equation (7.8) is substituted in (7.6), yielding

\[ C_1 = -\left(\frac{1}{s + \frac{1}{\tau_n}}\right) \cdot \frac{J_E}{s}. \]

(7.9)

The final expression for \( J_n(s) \) thus becomes

\[ J_n(s, x) = \frac{J_E}{s} e^{-\frac{1}{\tau_n} \cdot \frac{x}{D_n}}. \]

(7.10)

The collector current density, \( J_C(t) \), is calculated by setting \( x = d_{base} \) in (7.10) and then taking the inverse Laplace transform:

\[ J_C(t) = J_E \frac{d_{base}}{2\sqrt{\pi D_n}} \int_0^t e^{-\frac{\tau_n}{t^*} \cdot e^{-\frac{d_{base}^2}{4D_n t}}} dt. \]

(7.11)

Finally, one may write an expression for the common base current gain, \( \alpha \):

\[ \alpha(t) = \frac{J_C}{J_E} = \frac{I_C}{I_E} = \frac{d_{base}}{2\sqrt{\pi D_n}} \int_0^t e^{-\frac{\tau_n}{t^*} \cdot e^{-\frac{d_{base}^2}{4D_n t}}} dt. \]

(7.12)

From (7.1), latchup is triggered when the current collected by NW\(_1\) of the victim is equal to \( I_{NW}^{crit} \). This N-well region is analogous to the collector region of the transistor.
in Figure 7-8. We know that $I_{\text{trig}}$ is related to $I_{\text{crit}}^{\text{NW}}$ by the NW collection efficiency, $\alpha_{\text{NW}}$.

Reasonably assuming that $\alpha_{\text{NW}}$ has the same functional form as does $\alpha$ derived above, one obtains the following expression for the pulse-width-dependent $I_{\text{trig}}$:

$$I_{\text{trig}} = \frac{I_{\text{crit}}^{\text{NW}}}{\int_{0}^{\tau_{\text{PW}}} e^{-\frac{t}{\tau_n}} \cdot e^{-\frac{I_{\text{trig}}}{4D_n \cdot t} \cdot t^{1.5}} dt}$$  \hspace{1cm} (7.13)

In (7.13), the constant C is a function of the emitter and collector areas, and other material and geometric constants. Equation (7.13) is plotted in Figure 7-9 with $D_n = 30 \text{ cm}^2\text{s}^{-1}$ and $\tau_n = 3 \mu\text{s}$, reasonable values for 90- and 130-nm technologies. The model predicts that $I_{\text{trig}}$ should be a decreasing function of $T_{\text{PW}}$ for $T_{\text{PW}} \leq 10 \mu\text{s}$, which is consistent with the measurement data. Generally, in a technology with a moderate or high resistivity substrate, $\tau_n$ will be large and a negative $I_{\text{trig}}$ will be a strong function of $T_{\text{PW}}$.

The pulse-width dependence of a positive $I_{\text{trig}}$ (see Figure 7-5) may be understood by considering current conduction through $Q_{\text{PNP2}}$ (refer to Figure 7-2 (c)). Figure 7-10 shows that $I_{\text{C,PNP2}}$ saturates after 200 ns, which is consistent with the behavior of $I_{\text{trig}}$ in Figure 7-5. The value of $I_{\text{C,PNP2}}$ reaches steady state much faster than does $I_{\text{C,NPN1}}$ because of the short base-width of $Q_2$. Therefore, the pulse-width dependence of a negative $I_{\text{trig}}$ is more pronounced than that of a positive $I_{\text{trig}}$.

**7.2.2 Effect of trigger source rise-time**

During transient test conditions, displacement current will augment the carrier injection into the substrate. Recall that the PN junction current injectors have an associated capacitance. Displacement current is a majority carrier current. Referring to
Figure 7-4, let $I_{\text{disp}}$ denote the amount of displacement current injected into the I/O when the pad voltage is raised [lowered] from $V_{\text{DDIO}}$ to $V_{\text{inj}}$ [0 to $-V_{\text{inj}}$] with a rise-time [fall-time] of $t_{\text{edge}}$. Because $I_{\text{disp}}$ is a decreasing function of $t_{\text{edge}}$, fewer carriers are injected into the device as $t_{\text{edge}}$ increases. Therefore, one might expect $I_{\text{trig}}$ to be an increasing function of $t_{\text{edge}}$. However, both positive and negative $I_{\text{trig}}$ are insensitive to $t_{\text{edge}}$ (Figure 7-11 and Figure 7-12). These results are explained below.

During a negative I-test, latchup is triggered by electrons, whereas the displacement current in the substrate is a hole current. In fact, based on the analysis in Section 4.1.1, during a negative I-test, substrate hole current has the wrong polarity to trigger latchup. Thus, negative $I_{\text{trig}}$ is insensitive to $t_{\text{edge}}$, as was shown in Figure 7-11.

Figure 7-13 shows parasitic PNP $Q_{\text{PNP2}}$, which controls substrate current injection during a positive I-test. The substrate current is equal to the collector current of $Q_{\text{PNP2}}$, $I_{C,\text{PNP2}}$. The displacement current component of $I_{C,\text{PNP2}}$ is denoted as $I_{C,\text{PNP2,disp}}$. By solving KCL at the base of $Q_2$, we get

$$I_{\text{disp}} = \frac{C_{BE}}{t_r} \left( \frac{t_r}{t_r + R_{NW2} C_{BC}} + C_{BE} \right) V_{\text{inj}}.$$  \hspace{1cm} (7.14)

By solving KCL at the emitter of $Q_2$,

$$I_{C,\text{PNP2,disp}} = \frac{R_{NW} C_{BC} C_{BE}}{t_r} \left( \frac{t_r}{t_r + R_{NW} C_{BC} + C_{BE}} \right) V_{\text{inj}}.$$  \hspace{1cm} (7.15)

The resistor $R_{NW2}$ is a few ohms and $C_{BC}$ is not more than 1 pF. Since the product of $R_{NW2}$ and $C_{BC}$ is much less than $t_{\text{edge}}$,
\[
\frac{I_{C,PNP2,disp}}{I_{disp}} = \frac{R_{NW2}C_{BC}}{t_r + R_{NW2}C_{BC}} \ll 1, \tag{7.16}
\]

which means that only a small fraction of the displacement current at the I/O pin is injected into the substrate. This is why positive \(I_{\text{trig}}\) is insensitive to \(t_{\text{edge}}\).

### 7.2.3 Orientation of the victim

In previous work, it was claimed that a 0\(^\circ\) victim orientation (Figure 7-2 (a)) provides the lowest value of negative \(I_{\text{trig}}\) [3], [4]. Figure 7-14 and Figure 7-15 indicate that this is generally not a correct assertion. It is true only under static test conditions in the absence of guard rings. In most cases, the 180\(^\circ\) oriented victim (Figure 7-2 (b)) has the lower trigger current; this can be attributed to the smaller base-width of \(Q_{\text{NPN2}}\), \(d_{\text{base}}\).

The device simulation results of Figure 7-16 may be used to further understand the effects of orientation. The value of \(I_{\text{trig}}\) depends both on the fraction of current injected at the I/O pad that gets collected by NW\(_1\) of the victim (i.e., \(\alpha_{\text{NW}}\)) and on the direction of current flow within NW\(_1\). The current must be directed such that it lowers the N-well potential in the vicinity of the P\(^+\) diffusion, thus forward-biasing the PN junction, a necessary step to trigger latchup. When NGRs are used (Figure 7-16 (a)), current flows vertically through NW\(_1\), regardless of orientation, and the 180\(^\circ\) oriented victim always has lower \(I_{\text{trig}}\) due to the smaller \(d_{\text{base}}\) and consequently larger \(\alpha_{\text{NW}}\). Figure 7-16 (b) and Figure 7-16 (c) illustrate current flow in structures without guard rings. For the 180\(^\circ\) oriented victim (Figure 7-16 (b)), the portion of the current that flows laterally between the injector and NW\(_1\) does not assist in lowering the N-well potential in the vicinity of the P\(^+\) diffusion (see Figure 7-16 (d)). For the 0\(^\circ\) oriented victim (Figure 7-16 (c)), all of the current in NW\(_1\) helps to lower the potential near the P\(^+\) diffusion (see Figure 7-16 (e)).
Thus, for the case of no NGRs and long $T_{PW}$, $I_{trig}$ of the 0° oriented victim is lower than that of the 180° oriented victim. However, as the stress pulse-width is made small, (7.13) indicates that the number of carriers collected by NW$_1$ of the 0° oriented victim (long $d_{base}$) becomes a decreasing fraction of the number collected by NW$_1$ of the 180° oriented victim (shorter $d_{base}$). Therefore, for short stress durations, the 180° oriented victim has the lowest $I_{trig}$, as shown in Figure 7-14.

Figure 7-17 examines the effect of orientation on positive $I_{trig}$. For the positive I-test, the 180° victim orientation (Figure 7-2 (d)) provides the lower $I_{trig}$, regardless of $T_{PW}$; only the active guard ring case is examined. In Section 4.1.2, it is shown that in a positive I-test,

\[ I_{trig} = \frac{1}{\alpha_{PW}} \cdot \frac{V_{BE, on, P}}{R_{PW, 1}}, \quad (7.17) \]

where $\alpha_{PW}$ is the common-base current gain of Q$_2$, $R_{PW, 2}$ is the P-well resistance, and $V_{BE, on}$ represents the on-state base-emitter voltage drop of Q$_2$. Equation (7.17) seems to suggest that $I_{trig}$ of a positive I-test will be independent of both spacing ($d_{victim}$) and orientation; the first of these predictions is consistent with measurement data (refer to Section 5.3). The orientation effect seen here (Figure 7-17) is an artifact of the test structure design. Since the test structures contain guard rings, (7.17) is modified to account for their presence:

\[ I_{trig} = \frac{1}{\alpha_{PW}} \cdot \frac{1}{f_{PGR}} \cdot \frac{V_{BE, on, P}}{R_{PW, 1}}, \quad (7.18) \]
where \( f_{\text{PGR}} \) is the fraction of injected carriers that is collected by the PGRs. Note that \( I_{\text{trig}} \) is a decreasing function of \( R_{\text{PW},1} \). In the test structures with a 0° oriented victim, the PGRs are placed in the same well as is the victim (PW\(_1\)). In these test structures, the PGRs not only increase \( I_{\text{trig}} \) by collecting some of the excess holes from the substrate, they also increase \( I_{\text{trig}} \) by decreasing \( R_{\text{PW},1} \).

### 7.2.4 Guard ring efficiency under TLU testing

The N-well [P-well] guard rings increase negative [positive] \( I_{\text{trig}} \), thus improving latchup resilience; however, Figure 7-18 shows that the relative benefit of NGRs decreases for short stress durations. In the earlier dataplots, e.g., Figure 7-4, it was shown that \( I_{\text{trig}} \) is higher for short \( T_{\text{PW}} \); we have shown in Section 5.2.4 that NGR efficiency drops under high-level injection conditions. Taken together, these two observations explain why NGRs raise \( I_{\text{trig}} \) by a smaller percent as \( T_{\text{PW}} \) decreases. Data of Figure 7-18 indicate that the benefit of PGRs is insensitive to \( T_{\text{PW}} \).

### 7.2.5 Triple well technology

Triple well technology can be used to reduce the latchup hazard due to substrate hole injection, which occurs during a positive I-test. In the 130-nm technology, placing the victim inside a deep N-well was found to increase \( I_{\text{trig}} \) by almost a factor of two (280 mA vs. 590 mA at 150 °C). However, a comparison of the data in Figure 7-4 and Figure 7-19 shows that placing the victim inside a deep N-well enhances its susceptibility to negative TLU. A similar observation was made about static latchup [38]. Triple well technology raises the latchup threat because the deep N-well provides an additional collection area for electrons.
7.2.6 Negative I-test vs. positive I-test

Previously, it had been reported that the negative I-test provides the lowest $I_{\text{trig}}$; that is, it is the worst-case test condition [4]. However, the data of Figure 7-20 and Figure 7-21 show that this is too general a claim. These figures compare the values of $I_{\text{trig}}$ obtained from positive and negative I-tests, both when the guard rings are inactive (Figure 7-20) and when they are active (Figure 7-21). If $T_{PW}$ is large, as is the case for static latchup testing, the negative I-test does yield the smallest $I_{\text{trig}}$. However, for stress durations less than about 500 ns, the positive I-test yields a lower value of $I_{\text{trig}}$.

7.3 Modeling and Simulations

We know from Section 4.1.1 that $I_{\text{trig}}$ of a negative I-test is related to $\alpha_{NW}$ by the following equation:

$$I_{\text{trig}} = \frac{I_{\text{trig}}^{\text{crit}}}{\alpha_{NW}}.$$  \hspace{1cm} (7.19)

In Chapter 6, a model for $\alpha_{NW}$ is presented as functions of layout geometry, temperature, and bias conditions. Data of Figure 7-22 indicate that $\alpha_{NW}$ is frequency dependent; this dependence is important in modeling the transient effects. We can express the current gains in the frequency domain by

$$\alpha_{NW}(f) = \frac{\alpha_{NW}^{dc}}{1 + j \frac{f}{f_{3dB,NPN2}}},$$  \hspace{1cm} (7.20)
where \( \alpha_{NW}^{dc} \) and \( f_{3dB,NPN2} \) are the common-base current gain at low frequencies (dc) and the 3-dB bandwidth of \( Q_{NPN2} \), respectively. One can take the inverse Fourier transform of (7.20) and insert it into (7.19) to get

\[
I_{trig} \sim \frac{I_{NW}^{crit}}{\alpha_{NW}^{dc} \left( 1 - e^{-2\pi f_{3dB,NPN2} T_{PW}} \right)}.
\] (7.21)

The model presented in Chapter 6 for the collection efficiency is used for \( \alpha_{NW}^{dc} \) in (7.21). The value of \( f_{3dB,NPN2} \) can be extracted from dataplots such as in Figure 7-22. The data from this figure suggest that \( f_{3dB,NPN2} \) is well below 300 kHz, the minimum frequency limit of the network analyzer used in this work. To show that (7.21) is capable of modeling \( I_{trig} \) of a negative I-test, \( f_{3dB,NPN2} \) is treated as a fitting parameter. Results are shown in Figure 7-23. The model fits well with the measurement results. The extracted \( f_{3dB,NPN2} \) is 20 kHz.

The value of \( I_{trig} \) of a positive I-test can be similarly modeled using the presented single-pole model. The terms \( \alpha_{NW}^{dc}, I_{NW}^{crit}, \) and \( f_{3dB,NPN2} \) in (7.21) are replaced with \( \alpha_{PW}^{dc}, I_{PW}^{crit}, \) and \( f_{3dB,PNP2} \), respectively.
Figure 7-1: TLU experimental setup. The rise-time filter adjusts the rise-time of the pulse that reaches the device under test. $I_{\text{inj}}$ is calculated from the measured voltage drop across the matching network. $I_{\text{DD}}$ is the current through the dc power supply.
Figure 7-2: The setup and structures for performing negative, (a) and (c), and positive, (b) and (d), I-tests. The victims in (a) and (c) are 0° oriented, which means that the P-well of the victim (PW₁) is closer to the injector than is its N-well (NW₁). (b) and (d) show 180° oriented victims, in which the relative positions of PW₁ and NW₁ are reversed.
Figure 7-3: (a) The setup for the positive I-test showing the cable that connects the dc supply to $V_{DDIO}$ with its parasitic inductance $L_{par}$. (b) The injection current as a function of time during a transient positive I-test.
Figure 7-4: Negative I-test. 0° oriented victims. $I_{trig}$ is a decreasing function of $T_{PW}$ and $d_{TAP}$. 90-nm and 130-nm CMOS technologies. NGRs are inactive.

Figure 7-5: $I_{trig}$ from positive I-test. Guard rings are inactive. 0° oriented victim. 130-nm CMOS technology.
Figure 7-6: $V_{\text{trig}}$ for internal latchup vs. $T_{PW}$. The victim is shown in Figure 7-1. The terminals of the substrate injector are left floating. A trigger source with pulse-width of $T_{PW}$ and rise-time of 7 ns is placed in series with the dc supply, $V_{DD}$. 130-nm CMOS technology.

Figure 7-7: Collector and emitter current of $Q_{\text{NPN2}}$ during a negative I-test for a 0° oriented victim. 130-nm CMOS technology.
Figure 7-8: A 1-d NPN is used to simplify the derivation of the diffusion equation.

Figure 7-9: $I_{\text{trig}}$ vs. $T_{PW}$ as predicted by (7.13). $D_n = 30 \text{ cm}^2\text{s}^{-1}$ and $\tau_n = 3 \mu\text{s}$, which are reasonable values for 90- and 130-nm technologies. $I_{\text{trig}}$ becomes constant for $T_{PW} \geq 10 \mu\text{s}$, which is similar to the data of Figure 7-4.
Figure 7-10: Collector current of Q_{PNP2} during a positive I-test for a $0^\circ$ oriented victim. 130-nm CMOS technology.

Figure 7-11: Negative I-test. $I_{trig}$ is insensitive to $t_{edge}$. $T_{PW} = 500$ ns. $0^\circ$ oriented victims. 130-nm CMOS.
Figure 7-12: Positive I-test. $I_{\text{trig}}$ is insensitive to $t_{\text{edge}}$. $T_{PW} = 1 \, \mu\text{s}$. $0^\circ$ oriented victims. 130-nm CMOS.

Figure 7-13: Parasitic PNP $Q_{PNP2}$ is the substrate current injector during a positive I-test (see Figure 7-2 (c) and (d)). $R_{NW2}$ is the N-well resistance. $C_{BE}$ and $C_{BC}$ are the base-emitter and the base-collector junction capacitances, respectively. Only the P+ diffusion of the victim is shown.
Figure 7-14: Negative I-test with inactive NGRs. Only for large $T_{PW}$ does the $0^\circ$ oriented victim have smaller $I_{trig}$ than the $180^\circ$ oriented victim. 130-nm CMOS technology.

Figure 7-15: Same experiment as for Figure 7-14, except that the NGRs are active. The $180^\circ$ oriented victim has the smallest $I_{trig}$, regardless of $T_{PW}$. 
Figure 7-16: Simulated current flow during a negative I-test for (a) a 180° oriented victim with active NGRs, (b) a 180° oriented victim without NGR, and (c) a 0° oriented victim without NGRs. Figures (d) and (e) show potential contours for cases (b) and (c), respectively. I_{inj}= 100 mA/µm in all simulations.

Figure 7-17: Positive I-test with active PGRs. The 180° oriented victim has the lower I_{trig}. 130-nm CMOS technology.
Figure 7-18: $\Delta I_{\text{trig}} / I_{\text{trig}}$ (guard rings inactive) where $\Delta I_{\text{trig}} \equiv I_{\text{trig}}$ (guard ring active) - $I_{\text{trig}}$ (guard ring inactive). $0^\circ$ oriented victims. Circular data markers are for a negative I-test; square ones are for a positive I-test. 130-nm CMOS technology.

Figure 7-19: Negative I-test on $0^\circ$ oriented victims built using triple well technology, which lowers the latchup trigger current. 130-nm CMOS technology.
Figure 7-20: $I_{\text{trig}}$ from positive and negative I-tests. Guard rings are inactive. 0° oriented victims. 130-nm CMOS technology.

Figure 7-21: Same experiment as for Figure 7-20, except the guard rings are active.
Figure 7-22: Common-base current gain of $Q_{\text{NPN2}}$ vs. frequency. A network analyzer is used to perform the measurement. 130-nm CMOS technology.

Figure 7-23: Model vs. measurement for the negative I-test. Guard rings are inactive. 130-nm technology. Room temperature.
CHAPTER 8

CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

A parasitic PNPN device will be triggered on, resulting in latchup, if current larger than a critical value is injected into the substrate. The key factors of external latchup are (i) the critical current that is needed to trigger the PNPN, (ii) the amount of current injected into the substrate ($I_{\text{inj}}$), and (iii) the amount of current collected by the wells ($I_{\text{col}}$). A model for the critical current can be developed along the lines of existing models for the (internal) latchup trigger current. A semi-physical analytical model for the collection efficiency was presented in this work. It predicts that the collection efficiency is a function of device geometry, temperature, bias conditions, and the presence of guard rings and other detectors. Model parameters are extracted from measurements performed on a limited number of test structures. Subsequently, latchup hazards can be identified in any layout.

Either minority or minority carrier injection to the substrate can trigger latchup. Which type of carrier triggers latchup depends on the substrate current injector, the bias conditions, and the layout. When latchup is triggered by majority carriers, $I_{\text{trig}}$ is relatively insensitive to injector-to-PNPN spacing. This highlights the key role of P-type rings and substrate taps in preventing external latchup, since spacing does little to
mitigate the latchup hazard. On the other hand, when latchup is triggered by minority carriers, $I_{\text{trig}}$ is an increasing function of injector-to-PNPN spacing.

High-level injection effects greatly reduce the efficacy of NGRs for preventing latchup; thus, guard rings should be evaluated under high-current conditions. In most cases, the collection efficiency of an isolated detector is not very different from that in the presence of multiple detectors.

P-well guard rings, which are required to prevent latchup triggering by positive current injection and for substrate noise reduction, increase minority carrier collection efficiency and the latchup hazard from negative current injection.

Negative current injection is the worst-case condition during static latchup testing, which is generally used for product qualification. However, real world stresses, such as cable discharges, are transient, in which case positive current injection is the worst-case condition.

The circuit schematics presented in this work can be used to simulate the value of $I_{\text{trig}}$ for various bias conditions. A good fit is observed between the model and simulation for the latchup tests described in the JEDEC standard.

Based on the results of this work, we recommend the following design guidelines for minimizing the latchup hazards.

Identify the victims. Skip those that are located in the domains with supply voltages below 1.2 V. Pay special attention to the victims that are biased at voltages
higher than 1.5. These victims are more likely to latchup. Be careful with victims biased at voltages between 1.2 V and 1.5 V. Some of them may latchup.

Identify the injectors. They are usually PN junctions connected to signal pins. Determine which of them inject electrons and which ones inject holes. Add appropriate guard rings to the injectors. The guard ring lengths larger than 6 µm do not improve latchup hazards. Keep the guard ring-injector spacing minimum. Expect a factor of 4-6 improvement by using NGRs and a factor of 7-9 by using PGRs. To decrease latchup hazards from minority carriers, increase the spacing between the injectors and the victims, or use NGRs. When latchup is triggered by majority carriers, using PGRs is the only option. Avoid adding PGRs to minority carrier injectors. If PGRs must be added for noise issues, place the P-well ring inside the N-well ring. NGRs can be safely connected to \( V_{SS} \) instead of \( V_{DD} \) to ease the layout routing.

If the product has to pass only the static latchup tests, guarding minority carrier injectors has priority over majority carrier injectors, because the negative injection is the worst testing condition. On the other hand, if the product has to pass only the transient latchup tests, majority carrier injectors must be given a higher priority.

Do the latchup testing at evaluated temperatures. A product that passes the latchup tests at room temperature may fail at evaluated temperatures. The latchup trigger current at 100°C is usually a factor of 2-3 smaller.
8.2 Future Work

8.2.1 Negative I-test

We showed in Section 5.26 that PGRs have an adverse effect on latchup triggered by electrons, because the PGRs increase the collection efficiency of the victim. This effect is not captured by the model presented in Chapter 6.

Lookup tables are proposed to model the effect of detector geometry in Section 6.1. Lookup tables are computationally inefficient. One can further investigate these effects and construct a physical based model that includes the effect of detector geometry.

A computer program can be written that automatically extracts the model parameters. This program speeds up the extraction procedure needed for developing the model.

Figure 8-1 illustrates four victims with different orientations near an injector. We only studied the 180° and 0° victim orientations in this work, Victims B and D, respectively. Victim C is not studied in any of the previous publications. Among A, B, and D, the orientation of Victim A is claimed to be the worst case in [3] and [4]. However, these structures did not have guard rings worst case victim orientation. The injector-to-detector spacing in Victims A, B, and C are the same, but the directions of the current flow are different. Unfortunately, test structures with orientations of Victims A or C were not available in time to draw a conclusion. New test structures or 3-D device simulations can be done to understand how latchup is triggered in victim orientations other than 0° and 180°.
8.2.2 Positive injection

We showed that the circuit schematics in Figure 6-19 can be used to estimate the $I_{trig}$ of a layout. A sophisticated extraction method has yet to be developed for extracting $R_{PGR}$ and $R_{SUB}$ for various layout geometries, i.e., functions $f_1$ and $f_2$ in Section 6.3. The model can be based on existing work such as [44].

8.2.3 Transient latchup

The setup for the transient latchup testing can be improved to perform measurements for $T_{PW} < 50$ ns. Adding on-chip capacitors to test structures is one way to improve the quality of the injection current waveform.

The single-pole model presented in Section 7.3 for predicting the $I_{trig}$ in TLU testing is promising; however, it has not been verified for various conditions. For example, the 3-dB band width of $Q_{NPN2}$, $f_{3dB,NPN2}$, is a function of injector-to-victim spacing. Furthermore, activating guard rings may also change $f_{3dB,NPN2}$. This dependence is important and not yet incorporated in the model.

8.2.4 Latchup and substrate noise

In addition to preventing latchup triggering by positive injection, PGRs and P-taps are commonly used for suppressing the substrate noise. However, Section 5.2.6 shows that PGRs and P-taps increase the collection efficiency of the detector and the latchup hazard from negative current injection. For example, we showed in Section 5.2.6 that when NGRs are active, activating PGRs may lower $I_{trig}$ by a factor of ~ 30%. Therefore, a tradeoff exists between suppressing the substrate noise and the latchup hazards; a design practice that improves one may degrade the other. New design techniques that could simultaneously improve both hazards should be investigated.
Figure 8-1: Victims near an injector at different orientations. Victims B and D are 180° and 0° oriented, respectively.
REFERENCES


[39] Prof. J. Jin, University of Illinois at Urbana-Champaign, private communication, Nov. 2006.


