BER-OPTIMAL ANALOG-TO-DIGITAL CONVERTERS FOR COMMUNICATION LINKS

BY

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THESIS

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Abstract

In this thesis, we propose BER-optimal analog-to-digital converters (ADC) where quantization levels and thresholds are set non-uniformly to minimize the bit-error rate (BER). This is in contrast to present-day ADCs which act as transparent waveform preservers. We define the ADC shaping gain metric in order to quantify the improvements. Simulations for various communication channels show that the BER-optimal ADC achieves shaping gains that range from 2.5 dB for channels with low intersymbol interference (ISI) to more than 30 dB for channels with high ISI. Moreover, a 3 bit BER-optimal ADC achieves at least as low a BER as a 4 bit uniform ADC. For flash converters, this corresponds to a power reduction by 2×. Look-up table based equalizers compatible with BER-optimal ADCs are shown to reduce the power up to 47% and the area up to 66% in a 45 nm CMOS process. The shaping gain due to BER-optimal ADCs can be exploited to lower peak transmit swings at the transmitter or decrease power consumption of the ADC.

To my family for their unconditional support and love

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List of Abbreviations

ADC	analog-to-digital converter
AWGN	additive white Gaussian noise
BER	bit error rate
BPSK	binary phase shift keying
CDR	clock data recovery
DAC	digital-to-analog converter
DFE	decision feedback equalizer
ENOB	effective number of bits
FIR	finite impulse response
FEC	forward error correction
FOM	figure of merit
ISI	intersymbol interference
LE	linear equalizer
LMS	least mean square
LS	least square
LUT	look-up table
MLSE	maximum likelihood sequence estimation
MMSE	minimum mean square error
PDF	probability density function
PLL	phase-locked loop

RTL	register-transfer level
RX	receive
SAR	successive-approximation register
SNDR	signal-to-noise-plus-distortion ratio
SNR	signal-to-noise ratio
SQNR	signal-to-quantization-noise ratio
TX	transmit

List of Symbols

B_X	Number of bits per sample
D	Overall delay in the channel and equalizer
$h[n]$	Sampled time impulse response of the communication channel
$\mathbf{r}$	Vector containing ADC quantization levels
$\mathbf{t}$	Vector containing ADC quantization thresholds
$\mathbf{w}$	Vector containing coefficients of a linear equalizer
μ	Update step size
$\mathbf{p}$	Composite channel coefficients obtained by convolving the channel and the equalizer
V_{max}	Maximum input value expected by the ADC
$v[n]$	Additive white Gaussian noise
$x[n]$	ADC output at time index n
$y[n]$	Output of the equalizer at time index n

Chapter 1

Introduction

1.1 Overview

Traditional analog-to-digital converter (ADC) design is based on a fidelity criterion, attempting to reconstruct the input subject to constraints such as circuit power and process technology. The metric to be optimized, the error between input and output, is captured by signal-to-quantization-noise ratio (SQNR) and signal-to-noise-plus-distortion ratio (SNDR). Most ADCs today employ uniform quantization; that is, the levels and thresholds are placed uniformly within the signal dynamic range. As the SQNR depends strongly on the number of bits B_X of the ADC, system design leads one to determine B_X required to meet a specific SQNR or other performance specification. Unfortunately, large values of B_X lead to high power consumption, large area, and increased input capacitance. In high-speed systems, low-power ADCs are particularly difficult to design, and the effective number of bits (ENOB) usually does not exceed 6 [1–3].

As uniform quantization does not take into account statistics of the input signal other than the range, it does not maximize SQNR or minimize bit error rate (BER). In the context of an ADC-based communication link in Fig. 2.1(a) on page 10, we show the eye diagram of the received signal $x_c(nT)$ prior to quantization (Fig. 2.1(b)) along with its probability density function (PDF) (Fig. 2.1(c)). Signal statistics can be exploited to assign thresholds and levels in the ADC to improve system performance. The problem of determining the optimal set of quantization levels and thresholds was solved in [4] and [5]. The Lloyd-Max algorithm was proposed to iteratively determine the optimal levels $\mathbf{r}$ and thresholds $\mathbf{t}$ of a quantizer. We show in this thesis that the Lloyd-Max algorithm improves SQNR in communication links but does not necessarily reduce BER.

Hence, we propose an ADC in which the levels and the thresholds are set to minimize the BER. We term this a BER-optimal or BER-aware ADC because it employs a detection criterion and, instead of SQNR, maximizes the probability of detecting a transmitted bit correctly. The idea of BER-optimal components is not novel, as BER-optimal equalizers [6,7] and sampling phase [7] have been determined. However, this is the first work which addresses the issue of designing BER-optimal ADCs. BER-optimal ADCs differ from various digitally assisted ADCs [8, 9] as the latter maximize SQNR.

Before delving into BER-optimal ADCs, this thesis will elaborate more on the current state-of-art ADC designs. The detailed literature survey intends both to illustrate critical issues in the area and to place this work in context.

1.2 Literature Survey

1.2.1 The High Speed I/O Backplane Environment

This thesis was initially motivated by the difficulty of ADC design in modern-day high speed I/O links, links which have become bottlenecks in chip-to-chip communication.

Due to the restriction on pin counts and the density constraints on the number of transmission wires that can run between chips, most links are serial in nature and operate at high frequencies. As a result, I/O links are plagued by a variety of factors that compromise signal integrity in the multi-gigabits-per-second regime. For example, consider the backplane link shown in Fig. 1.1 [10]. Skin effect and dielectric loss become increasingly evident at high frequencies; the growing resistance contributes to the lossy nature and bandwidth limitation of the backplane traces. Additionally, via stubs and parasitic capacitances at both the transmitter and the receiver present impedance discontinuities to the signal. This will cause multiple reflections. To observe the combined effects of all the non-idealities, the sampled impulse response of one such backplane channel is plotted in Fig. 1.2. When sent over this link, a narrow pulse becomes attenuated and dispersed (widened), with previously transmitted symbols interfering with the current symbol in a phenomenon termed "intersymbol interference" (ISI). Furthermore, because high-speed links do not provide much functionality, it is undesirable to allo-

cate too much power to these data links. This stringent power budget makes reliable communication (BER$< 10^{-12}$) even more difficult.

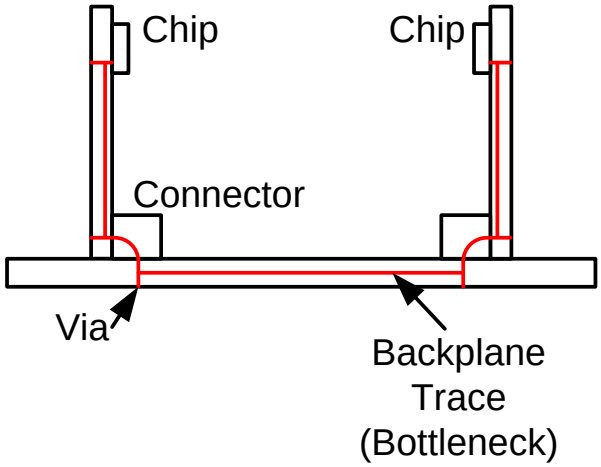


Figure 1.1: The backplane environment.

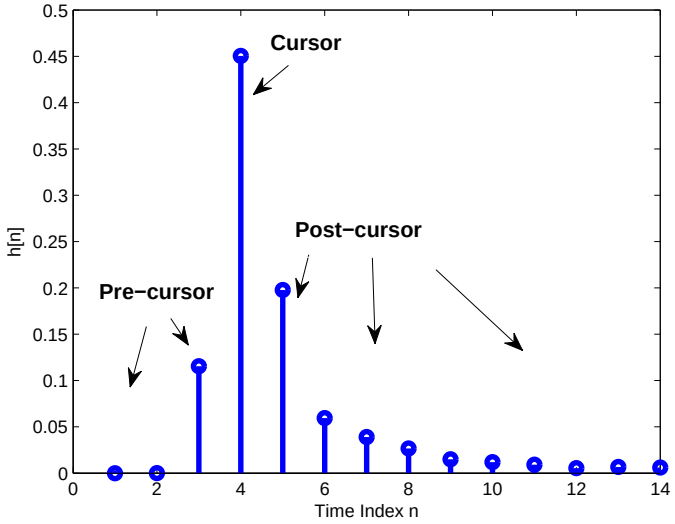


Figure 1.2: Sampled impulse response of a 10 Gb/s backplane channel.

Current designs often operate in the high signal-to-noise ratio (SNR) and ISI-dominated region. To equalize the channels, the links employ pre-emphasis at the transmitter (TX) to cancel pre-cursor taps and decision-feedback equalization (Fig. 1.3) at the receive (RX) side to eliminate post-cursor ISI. Payne et al. in [11] implemented a 6.25 Gb/s binary transceiver

in 0.13 μm that compensates for signal loss and crosstalk in legacy backplane channels. A programmable 4-tap finite impulse response (FIR) filter followed by a 4 bit digital to analog converter (DAC) takes care of the transmit equalization, while the receiver uses a half-baud-rate adaptive decision feedback equalizer (DFE). Total power consumed is 438 mW for the transmitter and 210 mW for the receiver.

Another work by Krishna et al. [12] presented a 0.6 to 9.6 Gb/s binary backplane transceiver core in 0.13 μm process technology. The transmitter has a tunable 2-tap equalizer. The receiver has an adaptive DFE that employs loop-unrolling to eliminate the tight timing constraint on the feedback path. Furthermore, a bandwidth adapting loop at the RX side adjusts the bandwidth based on whether the primary channel impairment is loss or high frequency crosstalk. The core occupies 0.56 mm^2 and consumes only 150 mW of power at 6.25 Gb/s.

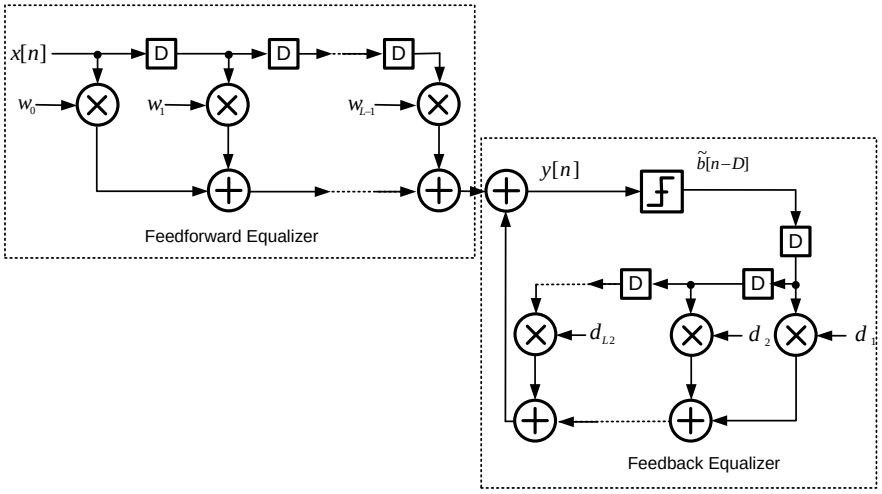


Figure 1.3: Structure of a decision-feedback equalizer with both feedforward and feedback taps.

A key figure of merit (FOM) for high speed I/O links is the power consumption per data rate, for which numbers as low as 10 mW/Gb/s have been reported. The greater power efficiencies of these analog, discrete time transceivers are one of the reasons that links migrated from designs based on analog-to-digital converters. However, as some of the recent papers indicate, interest in ADC-based links is once again growing.

1.2.2 High Speed ADCs

Though many transceivers in the past avoided the use of an ADC, ADC-designs are still attractive for several reasons. First, they allow flexibility in the data processing circuitry, which can be easily made programmable. Second, unlike analog components that have to be re-designed for each new process technology, digital circuits can be ported from one technology node to another with relative ease. Both power and area scale with newer processes. Third, an ADC-based receiver eliminates the troublesome analog feedback loop in high speed DFEs.

Bae et al. [1] introduced a maximum likelihood sequence estimation (MLSE) receiver to compensate for dispersion in OC-192 fiber links. The receiver incorporates a 12.5 Gb/s, 4 bit ADC, a phase-locked loop (PLL) that tolerates dispersion, a 1:8 multiplexer, and the digital circuitry for the MLSE algorithm. The chip was fabricated in a combination of CMOS technology and SiGe BiCMOS. Total power dissipation was 4.5 W, with 1 W consumed by the ADC. The digital data processing was much more sophisticated than previous high speed link designs.

Harwood et al. from TI [2] implemented a 12.5 Gb/s SerDes in 65 nm CMOS. It also diverged from the transceivers of past years by using a pair 4.5 bit baud rate flash ADCs. Both equalization and clock data recovery (CDR) are done via digital signal processing. The worst case power of one TX/RX lane is 330 mW/lane and the area is 0.45 mm^2 per lane.

An even more recent joint work from Nortel and STMicroelectronics reported fabricating a 24 GS/s, 6 bit ADC in 90 nm CMOS. ENOB is more than 4.1 up to 8 GHz and more than 3.5 up to 12 GHz. The ADC core consumes 1.2 W under 1 V and 2.5 V power supplies. The total area occupied is 4×4 mm^2.

One of the challenges of ADC-based high speed link designs is reducing power dissipation.

1.2.3 BER-Optimal Components

The idea of BER-optimal components is not new, as engineers long ago recognized the sub-optimality of the minimum mean squared error (MMSE) metric in communication links. In the case of equalization, one of the first

papers to consider minimum error probability DFE was [13]. However, the work was theoretical in nature and did not present any algorithm to compute the equalizer coefficients, nor did it compare the performance of the new equalizer with the standard MMSE DFE. Yeh and Barry in [6] developed an algorithm no more complex than the well-known least mean squares (LMS) to adapt the coefficients of minimum-BER equalizers. The algorithm, which was named "approximate minimum bit error rate" and abbreviated as AMBER, was applied to several channels to show that minimum-BER equalizers outperform conventional MMSE equalizers.

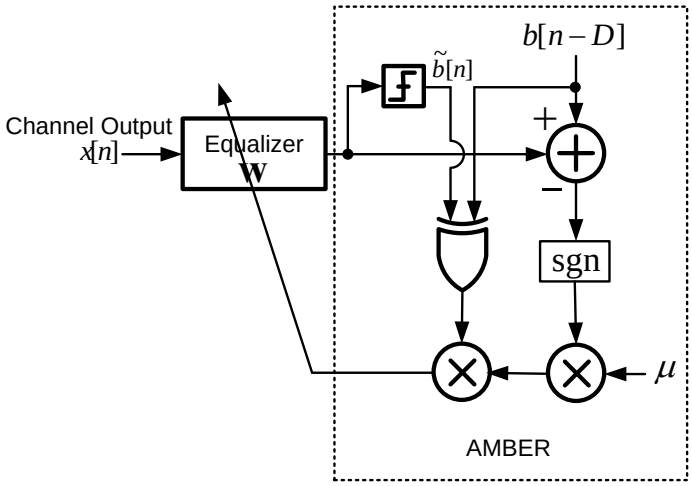


Figure 1.4: The AMBER algorithm.

According to AMBER, the coefficients of a minimum-BER equalizer should be updated as follows:

$$\mathbf{w}_{n+1} = \mathbf{w}_n - \mu I_n \,\mathrm{sgn}\{e_n\}\mathbf{x}_n \tag{1.1}$$

where n refers to the nth iteration of the update process, $\mathbf{w}$ the vector containing L equalizer coefficients, μ the update stepsize, I_n the error indicator function, and $\mathbf{x}_n$ the corresponding vector containing current and past equalizer inputs $[x[n], x[n-1], x[n-2] \ldots x[n-L+1]]^T$. The AMBER algorithm is depicted pictorially in Fig. 1.4, where D is the combined delay of the channel and the equalizer.

A quick comparison shows that AMBER only differs from the standard signed-LMS by the presence of an error indicator I_n. In other words, this

minimum-BER algorithm only updates the equalizer coefficients when an decision error has been made at the slicer. Mathematically, I_n can be expressed as $I_n = \frac{1-\tilde{b}[n]b[n-D]}{2}$, where $\tilde{b}[n]$ is the decision bit and $b[n-D]$ is the original transmitted bit.

Chen et al. [7] implemented a 90 nm test chip to verify an adaptation algorithm that minimizes the BER instead of MMSE. The so-called minBER algorithm steps the coefficients in three directions (increase, decrease or no change), measures the resulting BER, and chooses one direction based on majority vote. Because desired link BERs are usually low, accurate measurement could take a long time, thereby leading to slow convergence. To quicken the process, a target BER is specified, and a comparator with adaptive offset samples the DFE outputs. Whenever BER decreases during a change in the coefficients, the offset of an adaptive sampler is increased. The output of this adaptive sampler is XORed with the outputs of the standard data sampler to produce a BER metric, which is then fed into the adaptive macro. In other words, increasing the adaptive sampler offset creates more errors to help speed up the algorithm convergence. The paper admits that the BER metric from the XOR operation is a "pseudo BER" because output of the data sampler is not absolutely error free. However, since the pseudo BER has been shown to consistently follow true BER, it is considered to be an equivalent measure for adaptation. The minBER algorithm was applied to find the optimal Tx pre-emphasis taps, Rx-DFE taps, as well as the sampling-phase of CDR. The chip confirmed Yeh's theoretical results. Application of the said adaptation method to Tx-FIR leads to voltage margin improvement of $> 50\%$. When applied to Rx-DFE, the improvement can go up to 10%. The paper mentioned briefly the possibility of the adaptation strategy stalling because of a local minimum.

A separate 65 nm test chip from Chen et al. [14] demonstrated an ADC-based SerDes receiver that adapts the clock phase based on a degraded BER measurement, modified from the implementation in [7] . Because the true BER is low and difficult to measure in real time, [14] uses the errors at the DFE output when there is a static offset. In addition to the clock phase, this implementation adapts the ADC full scale range by making the observation that signal values which are too large or too small occur infrequently, so use of extreme digital code can be avoided. The paper reported a 1.5 bit reduction in the ADC. Chen et al.'s approach to the ADC is still rather different

from what is proposed in this thesis, because it only avoids overdesigns that result when ADCs are configured to digitize the entire dynamic signal range (specifically infrequently occurring extreme values), thereby decreasing the quantization error. It does not perform as effectively as the BER-optimal ADCs proposed in this thesis, or even the Lloyd-Max algorithm.

1.2.4 Digitally Assisted ADCs

Similar to BER-optimal ADCs, works in this category use digital techniques to correct for static and dynamic errors in the ADC circuitry. Unlike BER-optimal ADCs, many only take a component level view. In addition, they maximize SQNR instead of minimizing BER. However, many digitally assisted ADC works include circuit-level models that can be incorporated into the future research on BER-optimal ADCs.

W. Liu et al. [15] implemented a successive-approximation register (SAR) ADC array that, by extensive use of digital techniques, maintains 7.5 ENOB and a 65 dB SFDR at 600 MS/s while only consuming 23 mW of power. The design contains 10 parallel ADC lanes, every one consuming little power and clocked at only 60 MS/s. The output of each path is processed by a 10-tap adaptive digital linear filter. A reference ADC updates these adaptive digital filters via LMS algorithm at a much lower frequency. This adaptation allows the ADC to track process, voltage, and temperature variations. By effectively treating the path-mismatch problem among the time-interleaved ADC arrays and by correcting for nonlinearities, the ADC is able to achieve very good SFDR.

Nikaeen and Murmann also attacked errors and nonlinearities in ADCs [9], but they focused mainly on dynamic acquisition at the A/D front-end. The paper first presented a compact model of the nonidealities and then proceeded to derive an inverse model to correct them. Training signals and the least square (LS) algorithm are used to obtain the coefficients of the said inverse model. It was shown by Matlab simulations that more than 40 dB of improvement in SFDR can be achieved. When the algorithm was tested in a commercial 14 bit ADC, SFDR exceeded 83 dB up until 470 MHz.

1.3 Thesis Organization

The rest of this thesis is organized as follows. Chapter 2 presents an algorithm for computing BER-optimal levels and thresholds. Section 2.4 compares the performance of the BER-optimal and traditional ADCs via simulations for different channels. Chapter 3 presents a partial implementation of a BER-Optimal ADC Receiver. Chapter 4 concludes the thesis by outlining future research directions.

Chapter 2

BER-Optimal ADC

2.1 System Description

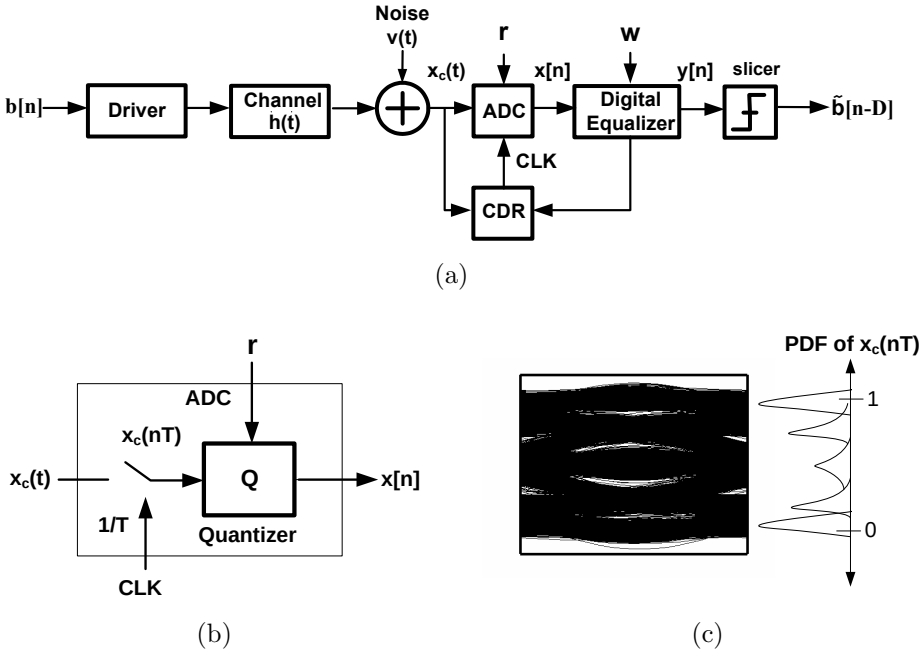


Figure 2.1: Role of an ADC in a communication link: (a) block diagram of a communication link, (b) functional diagram of an ADC, and (c) eye diagram and PDF of the sampled received signal $x_c[nT]$.

Figure 2.1(a) illustrates an equalized communication link. Assuming binary phase shift keying (BPSK) modulation, the transmitter sends pseudo-random sequence of bits $b[n] \in \{\pm 1\}$ through the channel. At the receiver, the ADC quantizes the signal, and the outputs are subsequently processed by a digital equalizer to eliminate ISI that results from the bandlimited channel. A slicer following the equalizer makes a hard decision on which bit has been transmitted. With a slight abuse of notation, we refer to the BPSK

symbols as bits in the sequel. As shown in Fig. 2.1(b), the ADC consists of a baud-rate sampler followed by a quantizer.

ADCs convert a continuous-time, continuous-amplitude signal $x_c(t)$ to discrete-time, discrete-amplitude $x[n]$ so that it can be processed later by digital hardware. As such, it involves both sampling and quantization (Fig. 2.1(b)). The sampling operation is represented by $x_c(t)|_{t=nT}$, where T is the sampling period, and $x_c(nT)$ the continuous-amplitude, discrete-time value. However, since sampling is not the topic of this thesis, we assume it to be perfect and focus on determining BER-optimal quantizer parameters.

At a given sampling instant $t = nT$, assuming a sampler with sufficient bandwidth, the input $x_c[n] = x_c(nT)$ to the ADC is given by

$$x_c[n] = \sum_{i=0}^{M-1} h[i]b[n-i] + v[n], \tag{2.1}$$

where $b[n]$ is the transmitted bit, $h[i]$ the baud-rate sampled impulse response of the channel with memory M, and $v[n]$ is modeled as additive white Gaussian noise with variance σ^2.

The ADC has N levels r_k $(k = 1, \ldots, N)$ and $N-1$ thresholds t_k $(k = 1, \ldots, N-1)$, where N is equal to 2^{B_X}. The mapping between $x_c[n]$ and the quantized signal $x[n]$ is

$$\begin{aligned} x[n] &= r_1 \text{ if } x_c[n] \epsilon (-\infty, t_1] \\ &= r_N \text{ if } x_c[n] \epsilon (t_{N-1}, \infty) \\ &= r_k \text{ if } x_c[n] \epsilon (t_{k-1}, t_k] \text{ for } k = 2, \ldots, N-2. \end{aligned} \tag{2.2}$$

Following the ADC is a L-tap linear equalizer. Its output will be the convolution of ADC outputs and equalizer coefficients $\mathbf{w}$, i.e.,

$$y[n] = \sum_{j=0}^{L-1} w[j]x[n-j]. \tag{2.3}$$

The slicer is a symbol-by-symbol memoryless device. Therefore, the estimate of the transmitted symbol $b[n-D]$ is $\tilde{b}[n-D] = \text{sgn}(y[n])$. Here D is introduced to account for delay in the channel and equalizer; it must be chosen carefully to achieve a good BER.

2.2 ADC Based on Fidelity Criterion

The ADC approximates its continuous-amplitude, discrete-time input $x_c(nT) = x_c[n]$ with a finite set of levels according to (2.3). In doing so, it introduces quantization error. Let

$$x[n] = x_c[n] + q[n] \tag{2.4}$$

where $x[n]$ is the ADC output, $x_c[n]$ the continuous-amplitude, discrete-time input, and $q[n]$ the quantization error.

From [16], as long as quantization step-size $\Delta = \frac{2V_{max}}{N}$ is small, the following three assumptions can be made regarding $q[n]$:

1. $q[n]$ is a sample sequence from a stationary random process.

2. $q[n]$ is uncorrelated with the input signal sequence $x_c[n]$.

3. $q[n]$ is an uncorrelated sequence.

If we define $\sigma_x^2 = E[(x[n] - E[x[n]])^2]$ to be signal power and $\sigma_q^2 = E[q^2[n]]$ to be variance of quantization noise, then the signal-to-quantization-noise ratio (SQNR), a commonly used performance metric for quantizers, is given by

$$SQNR = 10 \log_{10} (\frac{\sigma_x^2}{\sigma_q^2}). \tag{2.5}$$

ADCs designed today act as transparent waveform preservers, which minimize $E[q^2[n]]$ (i.e., maximize SQNR) subject to constraints such as circuit power and process technology. Such ADCs are designed based on a fidelity criterion.

2.2.1 Uniform ADC

In a uniform ADC, the quantization levels and thresholds are spread evenly within the signal dynamic range. The minimum and maximum input amplitudes expected by this ADC are expressed as $-V_{max}$ and V_{max}, respectively. The quantizer step-size is $\Delta = \frac{2V_{max}}{N} = \frac{2V_{max}}{2^{B_X}}$ [16]. For sufficiently small quantization error, $q[n] = x_c[n] - x[n]$ is assumed to be a uniformly distributed random variable, bounded between $-\frac{\Delta}{2}$ and $+\frac{\Delta}{2}$ and

independent of input (Figure 2.2). In the following, we drop the time-index n because quantization is done in a memoryless fashion. Quantization noise power $\sigma_q^2 = E[q^2[n]]$ is given by

$$\begin{aligned} E[q^2] &= \int_{-\frac{\Delta}{2}}^{\frac{\Delta}{2}} q^2 \frac{1}{\Delta} dq \\ &= \frac{\Delta^2}{12}. \end{aligned} \tag{2.6}$$

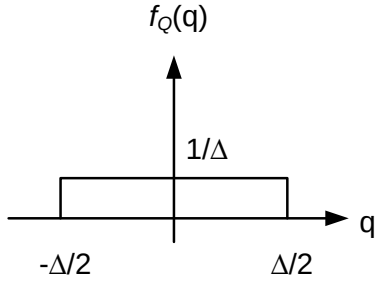


Figure 2.2: Probability density function of quantization error. Q is the random variable representing quantization error $q[n]$, and $f_Q(q)$ is its PDF.

Combining (2.5) and (2.6), SQNR can be calculated as

$$SQNR(dB) = 6.02B_X + 4.8 - 20\log_{10}\frac{V_{max}}{\sigma_x}, \tag{2.7}$$

where each additional bit increases SQNR by 6 dB.

2.2.2 Nonuniform ADC Lloyd-Max Quantizer

A Lloyd-Max Quantizer [4,5] minimizes the distortion measure known as the mean-squared error $E(q^2)$ (MSE), given by

$$\begin{aligned} E(q^2) &= E[(x_c - r_k)^2] \\ &= \sum_{k=1}^{N} \int_{t_{k-1}}^{t_k} (x_c - r_k)^2 f_{Xc}(x_c) dx_c, \end{aligned} \tag{2.8}$$

where X_c is the random variable representing input x_c, $f_{X_c}(x_c)$ is its PDF, and t_0 and t_N equal $-\infty$ and $+\infty$, respectively.

Stationary points of the MSE $E(q^2)$ in terms of $\mathbf{r}$ and $\mathbf{t}$, where $\mathbf{r}$ and $\mathbf{t}$ are ADC quantization levels and thresholds, can be found by setting the gradient of 2.8 with respect to $\mathbf{r}$ to zero, i.e.,

$$\frac{\partial E(q^2)}{\partial r_k} = 0. \tag{2.9}$$

Because $f_{X_c}(x_c)$ is independent of the quantizer parameters, $r_{k,opt}$ can be readily calculated:

$$\frac{\partial E(q^2)}{\partial r_k} = -2\int_{t_{k-1}}^{t_k}(x_c - r_k)f_{Xc}(x_c)dx_c \tag{2.10}$$

Setting $\frac{\partial E(q^2)}{\partial r_k}$ to zero,

$$\int_{t_{k-1}}^{t_k} x_c f_{X_c}(x_c)dx_c = r_k\int_{t_{k-1}}^{t_k} f_{X_c}(x_c)dx_c$$

$$r_k = \frac{\int_{t_{k-1}}^{t_k} x_c f_{X_c}(x_c)dx_c}{\int_{t_{k-1}}^{t_k} f_{X_c}(x_c)dx_c}. \tag{2.11}$$

$$\tag{2.12}$$

Given r_ks, the optimal t_ks minimizes squared error $(x_c - r_k)^2$. In other words, each input x_c should be mapped to the closest r_k,

$$t_k = \frac{r_k + r_{k+1}}{2}. \tag{2.13}$$

Thus, $r_{k,opt}$ and $t_{k,opt}$ are

$$r_{k,opt} = \frac{\int_{t_{k-1,opt}}^{t_{k,opt}} x_c f_{X_c}(x_c)dx_c}{\int_{t_{k-1,opt}}^{t_{k,opt}} f_{X_c}(x_c)dx_c}, \tag{2.14}$$

$$t_{k,opt} = \frac{r_{k,opt} + r_{k+1,opt}}{2}. \tag{2.15}$$

Equation (2.15) implies that $t_{k,opt}$ lies halfway between adjacent optimal quantization levels, and $r_{k,opt}$ is the conditional mean of X_c conditioned on the event that input $x_c[n]$ lies between t_{k-1} and t_k.

Equation (2.14) is difficult to solve analytically. The Lloyd-Max algorithm is an iterative procedure used to determine $\mathbf{r}$ and $\mathbf{t}$. It alternatively optimizes thresholds $\mathbf{t}$ for a given set of levels $\mathbf{r}$, and then re-computes the levels for the new set of thresholds. Until the MSE converges, this process is

repeated. Figure 2.3(a) shows quantization levels $\mathbf{r}$ obtained via the Lloyd-Max algorithm for the outputs of an artificial channel, superimposed on top of the PDF of the channel outputs. In accordance with (2.15), more levels are placed around "peaks" in the PDF, and fewer are needed in other regions. The improvement in SQNR is shown in Figure 2.3(b).

Although this algorithm improves SQNR, we find that it is not the same as minimizing BER. For channels with high ISI, it provides less SQNR gain (Figure 2.4).

2.3 BER-Optimal ADC

In a communication link, the Lloyd-Max algorithm is still suboptimal, because the ADC is based on a fidelity criterion. While SQNR is improved, such a scheme ignores the fact that the ADCs are part of a detection process, thereby leading to over-designs that are power-hungry. Hence, we propose an ADC in which the levels and the thresholds are set to minimize the BER. We term this a BER-optimal or BER-aware ADC because it employs a detection criterion and, instead of SQNR, maximizes the probability of detecting a transmitted bit correctly.

We will motivate BER-optimal ADCs using two examples before considering the entire communication link.

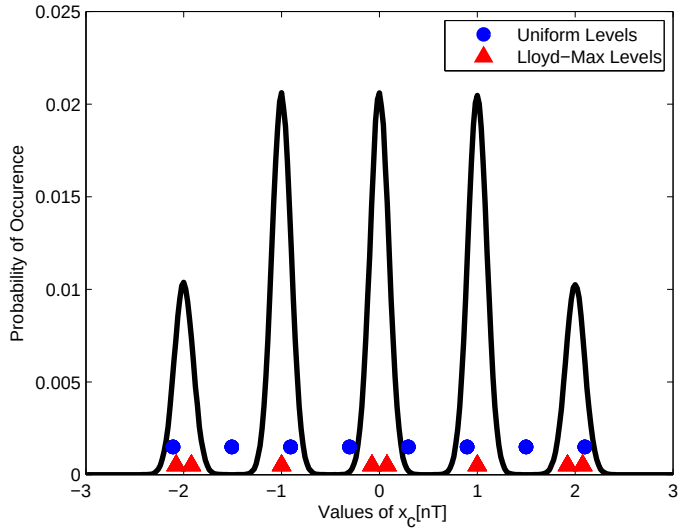
2.3.1 AWGN Channel, ADC Only

The first system to be analyzed is presented in Fig. 2.5, which differs from 2.1(a) by the absence of the equalizer and the slicer.

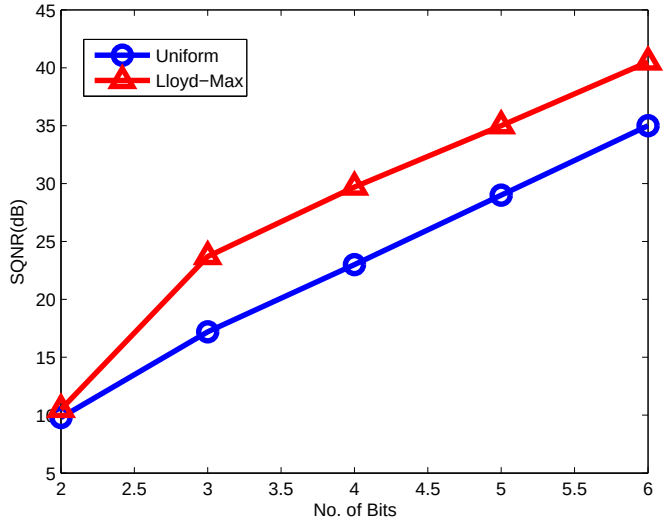
Let the channel be a simple AWGN channel. That is, $\mathbf{h} = [1]$, and $D = 0$. We wish to choose $\tilde{b}[n]$ that has the larger *a posteriori* probability, i.e.,

$$\begin{aligned} \tilde{b}[n] &= 1 \text{ if } \mathbb{P}\{b[n] = 1 \mid x_c[n]\} > \mathbb{P}\{b[n] = -1 \mid x_c[n]\} \\ &= -1 \text{ otherwise.} \end{aligned} \tag{2.16}$$

$\mathbb{P}\{\bullet\}$ signifies the probability of an event, and $\mathbb{P}\{b[n] \mid x_c[n]\}$ is the *a posteriori* probability of $b[n]$ conditioned on having observed the received signal

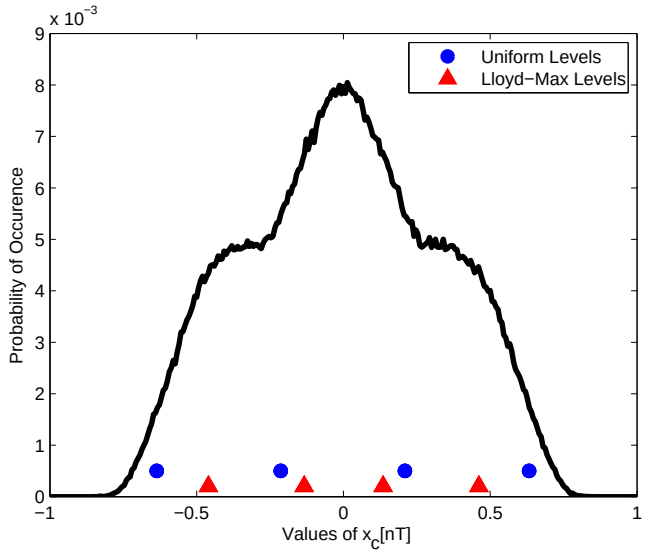


(a)

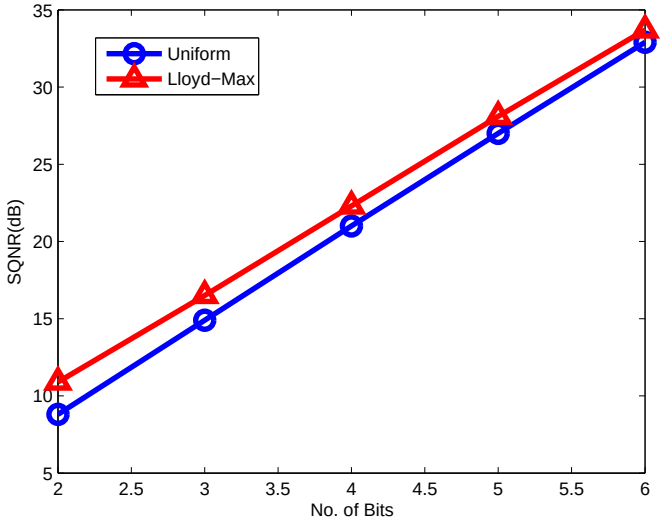


(b)

Figure 2.3: Lloyd-Max vs. uniform ADC: (a) placement of levels for 3 bit uniform and Lloyd-Max ADCs, and (b) improvement in SQNR by Lloyd-Max over uniform quantization. BPSK signal is sent through channel $[-0.5\ 1\ -0.5]$. Noise is modeled as AWGN.



(a)



(b)

Figure 2.4: Lloyd-Max vs. uniform ADC: (a) placement of levels for 2 bit uniform and Lloyd-Max ADCs, and (b) improvement in SQNR by Lloyd-Max over uniform quantization. BPSK signal is sent through a FR4 backplane channel. Noise is modeled as AWGN.

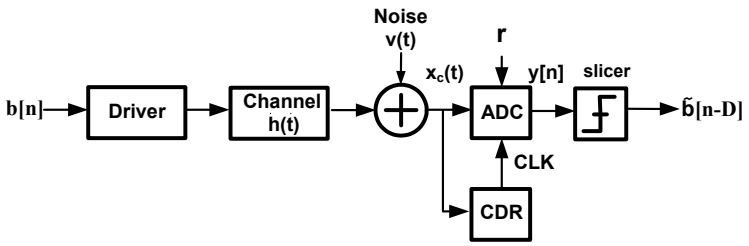


Figure 2.5: Simplified artificial communication link.

$x_c[n]$.

Using Bayes rule,

$$\begin{aligned}
\mathbb{P}\{b[n]=1 \mid x_c[n]\} &= \frac{\mathbb{P}\{x_c[n] \mid b[n]=1\}\mathbb{P}\{b[n]=1\}}{\mathbb{P}\{x_c[n]\}} \\
\mathbb{P}\{b[n]=-1 \mid x_c[n]\} &= \frac{\mathbb{P}\{x_c[n] \mid b[n]=-1\}\mathbb{P}\{b[n]=-1\}}{\mathbb{P}\{x_c[n]\}}. \quad (2.17)
\end{aligned}$$

Under the original assumption that the transmitted bits are i.i.d. and using (2.17), (2.16) simplifies to

$$\begin{aligned}
\tilde{b}[n] &= 1 \text{ if } \mathbb{P}\{x_c[n] \mid b[n]=1\} > \mathbb{P}\{x_c[n] \mid b[n]=-1\} \\
&= -1 \text{ otherwise.} \quad (2.18)
\end{aligned}$$

$\mathbb{P}\{x_c[n] \mid b[n]=1\}$ and $\mathbb{P}\{x_c[n] \mid b[n]=-1\}$ are dependent on statistical knowledge of the channel noise, which is modeled as additive white Gaussian. Thus, (2.16) can be re-written as

$$\begin{aligned}
\tilde{b}[n] &= 1 \text{ if } \frac{1}{\sqrt{2\pi\sigma_1^2}} e^{-\frac{(x_c[n]-1)^2}{2\sigma_1^2}} > \frac{1}{\sqrt{2\pi\sigma_2^2}} e^{-\frac{(x_c[n]+1)^2}{2\sigma_2^2}} \\
&= -1 \text{ otherwise.} \quad (2.19)
\end{aligned}$$

To stay general, σ_1^2 and σ_2^2 are not assumed to be equal. The inequality can be solved analytically.

When $\sigma_1^2 = \sigma_2^2$, (2.19) becomes

$$\begin{aligned}
\tilde{b}[n] &= 1 \text{ if } x_c[n] > 0 \\
&= -1 \text{ otherwise.} \quad (2.20)
\end{aligned}$$

Therefore, the ADC threshold should be set to 0.

When $\sigma_1^2 \neq \sigma_2^2$, the optimal ADC threshold should be set to

$$\frac{\sigma_1^2+\sigma_2^2+\sqrt{4\sigma_1^2\sigma_2^2+2\sigma_1^4\ln(\frac{\sigma_1}{\sigma_2})\sigma_2^2-2\sigma_2^4\ln(\frac{\sigma_1}{\sigma_2})\sigma_1^2}}{-\sigma_1^2+\sigma_2^2}$$
or
$$\frac{\sigma_1^2+\sigma_2^2-\sqrt{4\sigma_1^2\sigma_2^2+2\sigma_1^4\ln(\frac{\sigma_1}{\sigma_2})\sigma_2^2-2\sigma_2^4\ln(\frac{\sigma_1}{\sigma_2})\sigma_1^2}}{-\sigma_1^2+\sigma_2^2}, \tag{2.21}$$

whichever value that lies between $+1$ and -1.

2.3.2 Channel with ISI and Additive White Gaussian Noise, ADC Only

We again consider Figure 2.5, but now the channel has a memory of M symbols. Without any loss of generality, we assume $D = 0$ in order to simplify notation. Again, we wish to choose $\tilde{b}[n]$ that has the larger *a posteriori* probability, i.e.,

$$\begin{aligned}\tilde{b}[n] &= 1 \text{ if } \mathbb{P}\{b[n]=1 \mid x_c[n]\} > \mathbb{P}\{b[n]=-1 \mid x_c[n]\} \\ &= -1 \text{ otherwise.}\end{aligned} \tag{2.22}$$

Using Bayes rule and under the original assumption that the transmitted bits are i.i.d. and using (2.17), (2.22) simplifies to

$$\begin{aligned}\tilde{b}[n] &= 1 \text{ if } \mathbb{P}\{x_c[n] \mid b[n]=1\} > \mathbb{P}\{x_c[n] \mid b[n]=-1\} \\ &= -1 \text{ otherwise.}\end{aligned} \tag{2.23}$$

$\mathbb{P}\{x_c[n] \mid b[n]=1\}$ and $\mathbb{P}\{x_c[n] \mid b[n]=-1\}$ are dependent on statistical knowledge of the channel noise, which is modeled as additive white Gaussian, and on the previous $M-1$ transmitted bits. Thus,

$$\begin{aligned}\mathbb{P}\{x_c[n] \mid b[n]=1\} &= \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x_c[n]-h[0]-\sum_{i=1}^{M-1} h[i]b[n-i])^2}{2\sigma^2}} \\ \mathbb{P}\{x_c[n] \mid b[n]=1\} &= \frac{1}{\sqrt{2\pi\sigma^2}} e^{-\frac{(x_c[n]+h[0]-\sum_{i=1}^{M-1} h[i]b[n-i])^2}{2\sigma^2}}.\end{aligned} \tag{2.24}$$

Previously $M-1$ transmitted bits $b[n-(M-1)], b[n-(M-2)], \ldots, b[n-1]$ are unavailable. However, because each bit assumes values of $+1$ and -1 with probability $\frac{1}{2}$, there are the 2^{M-1} possible equally likely values of $\sum_{i=1}^{M-1} h[i]b[n-i]$.

Therefore, (2.24) can be written as

$$\begin{aligned}\tilde{b}[n] &= 1 \text{ if } 2^{-M+1} \sum_{b[n-1]\in\{\pm 1\}} \cdots \sum_{b[n-M+1]\in\{\pm 1\}} \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{(x_c[n]-\sum_{i=0}^{M-1} h[i]b[n-i])^2}{-2\sigma^2}} > \\ &\quad 2^{-M+1} \sum_{b[n-1]\in\{\pm 1\}} \cdots \sum_{b[n-M+1]\in\{\pm 1\}} \frac{1}{\sqrt{2\pi\sigma^2}} e^{\frac{(x_c[n]+h[0]-\sum_{i=1}^{M-1} h[i]b[n-i])^2}{-2\sigma^2}} \\ &= -1 \text{ otherwise.} \end{aligned} \tag{2.25}$$

Since the channel has M terms, it will generate 2^M number of possible noiseless outputs. Let $\{q_1, q_2, q_3, \ldots, q_{2^{M-1}}, \ldots, q_{2^M}\}$ be the set of channel outputs. $\mathbf{Q_1} = \{q_1, q_2, q_3, \ldots, q_{2^{M-1}}\}$ correspond to $b[n]$ being 1, and $\mathbf{Q_0} = \{q_{2^{M-1}+1}, q_{2^{M-1}+2}, \ldots, q_{2^M}\}$ correspond to $b[n]$ being -1; then (2.25) can be expanded to be a summation of 2^{M-1} exponential terms on either side of the inequality.

$$\begin{aligned}\tilde{b}[n] &= 1 \text{ if } 2^{-(M-1)} \frac{1}{\sqrt{2\pi\sigma^2}} \left(\sum_{q\in\mathbf{Q_1}} e^{-\frac{(x_c[n]-q)^2}{2\sigma^2}} \right) > \\ &\quad 2^{-(M-1)} \frac{1}{\sqrt{2\pi\sigma^2}} \left(\sum_{q\in\mathbf{Q_0}} e^{-\frac{(x_c[n]-q)^2}{2\sigma^2}} \right) \\ &= -1 \text{ otherwise.} \end{aligned} \tag{2.26}$$

With Max-Log approximation, (2.26) becomes a comparison between

$$\min\left((x_c[n]-q_1)^2, (x_c[n]-q_2)^2, \ldots, (x_c[n]-q_{2^{M-1}})^2\right)$$

and

$$\min\left(x_c[n]-q_{2^{M-1}+1})^2, (x_c[n]-q_{2^{M-1}+2})^2, \ldots, (x_c[n]-q_{2^M})^2\right).$$

In other words, this is the comparison between the Euclidean distances

from the received voltage $x_c[n]$ to the nearest noiseless channel outputs corresponding to $b[n]$ being -1 and $+1$, respectively.

Therefore, Equation (2.25) shows that in the case of no equalization, when the PDF of the received signal is known, the optimal thresholds of the ADC should be set to where $b[n]$ transitions from 1 to -1 or vice versa, in the middle between the appropriate adjacent noiseless channel outputs. The number of required thresholds to achieve minimum BER is dictated by the number of such transitions. Contrasts this with the Lloyd-Max algorithm. It often places thresholds between adjacent modes but makes no distinction for transition of bits; furthermore, it is rather ambiguous with the placement of thresholds for optimal BER. In cases where the aforementioned 1 to -1 and -1 to 1 transitions are few, ADCs based on detection criterion would show a distinct advantage.

To illustrate (2.25), consider a channel with taps $\mathbf{h} = [0.6, 1, 0.6]^T$, which results in the PDF shown in Figure 2.6. For this channel, $\mathbf{Q_1} = \{-2.2, -1, 0.2\}$ and $\mathbf{Q_0} = \{-0.2, 1, 2.2\}$. ADC optimal thresholds are therefore set at -0.6, 0, and 0.6. Only three thresholds are sufficient.

Figure 2.6 plots additionally uniform and Lloyd-Max thresholds. They are quite different from the optimal ADC thresholds.

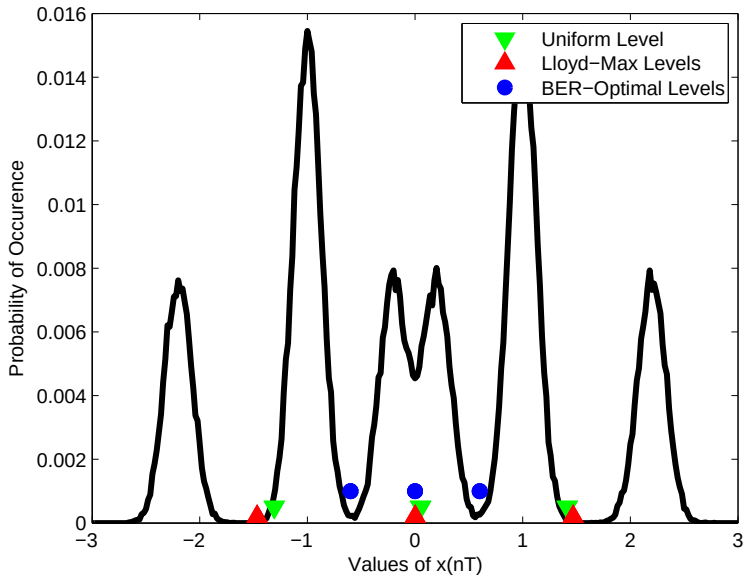


Figure 2.6: Output PDF of channel $[0.6, 1, 0.6]$.

Unfortunately, in real communication links where ISI can be quite severe and channel memory is large, post-processing after the ADC is required. This impacts the assignment of levels and thresholds. Channels that require equalization are the main interest and will be discussed for the rest of the thesis.

2.3.3 Channel with ISI and Additive White Gaussian Noise, ADC and Linear Equalizer

We propose quantization based on the detection criterion, by setting the levels $\mathbf{r}$ and thresholds $\mathbf{t}$ non-uniformly using the BER metric. In the system presented in Fig. 2.1(a), an error is made when $\tilde{b}[n] \neq b[n]$ (assuming $D = 0$), so BER is computed by averaging over all possible values of equalizer output $y[n]$ and hence all equalizer input vectors $\mathbf{x}_n = [x[n], x[n-1], ..., x[n-L+1]]$ such that $\tilde{b}[n] = \text{sgn}(y[n]) = \text{sgn}(\mathbf{w}^T\mathbf{x}_n)$ produces an error at the slicer. To this end, we define an error indicator $\left(\frac{1-b[n]\tilde{b}[n]}{2}\right)$. It is 1 when the slicer makes an error and 0 otherwise. Thus, BER is computed by summing the probability of all $y[n]$ corresponding to non-zero error indicator (2.27):

$$\begin{aligned} BER &= \mathbb{P}\{b[n] \neq \tilde{b}[n]\} \\ &= \sum_{y[n]} \left[\mathbb{P}\{y[n]\} \left(\frac{1 - b[n]\tilde{b}[n]}{2} \right) \right] \qquad (2.27) \\ &= \sum_{\mathbf{x}_n} \left[\left(\prod_{j=0}^{L-1} \mathbb{P}\{x[n-j] = r_k\} \right) \left(\frac{1 - b[n]\tilde{b}[n]}{2} \right) \right] \qquad (2.28) \end{aligned}$$

where $\mathbb{P}\{x[n-j] = r_k | x_{c0}[n-j]\}$ is given by

$$Q\left(\frac{t_{k-1} - x_{c,0}[n-j]}{\sigma} \right) - Q\left(\frac{t_k - x_{c,0}[n-j]}{\sigma} \right), \qquad (2.29)$$

$\mathbb{P}\{\bullet\}$ was defined before, $Q(\bullet)$ is the Gaussian Q function, and $x_{c0}[n]$ is noiseless channel output $\sum_{i=0}^{M-1} h[i]b[n-i]$. The equalizer output $\tilde{b}[n]$ is given

by

$$\tilde{b}[n] \;=\; \mathrm{sgn}\left(\sum_{j=0}^{L-1} w[j]x[n-j]\right). \tag{2.30}$$

A BER-optimal ADC is one where $\mathbf{r}$ and $\mathbf{t}$ are chosen to minimize (2.27).

2.3.4 Gradient Descent

A closed form expression for the BER optimal parameters $\mathbf{r}$ and $\mathbf{t}$ of the ADC is difficult to obtain due to the highly non-linear objective function (2.27). Therefore, we employ the gradient descent algorithm to determine the parameters. The following update equations are used to compute $\mathbf{r}$ iteratively. For the ith iteration of the algorithm, we have

$$BER \;=\; f(\mathbf{h}, \mathbf{r}, \mathbf{t}, \mathbf{w}, \sigma) \tag{2.31}$$

$$\begin{aligned} \mathbf{r_i} \;&=\; \mathbf{r_{i-1}} + \mu\left(\frac{\partial BER}{\partial \mathbf{r}}\right)|_{\mathbf{r}=\mathbf{r_{i-1}}} \\ &\approx\; \mathbf{r_{i-1}} + \mu\left(\frac{\Delta BER}{\Delta \mathbf{r}}\right). \end{aligned} \tag{2.32}$$

The placement of $\mathbf{t}$ remains the same as given by (2.15) to reduce search complexity. To avoid differentiating the sign function, the gradient is computed by finite differences—each entry in the gradient vector is obtained by perturbing the r_k's one at a time and computing the change in BER due to this perturbation [17].

The algorithm can be summarized as follows:

Step 1. Initialize the ADC parameters $\mathbf{r}$ and $\mathbf{t}$ appropriately.

Step 2. Estimate the gradient vector by computing finite differences.

Step 3. Update $\mathbf{r}$ using (2.32).

Step 4. Repeat Steps 2 and 3 until BER converges, i.e. when the difference in the BER between adjacent runs is less than a specified value.

We demonstrate next through simulations that the BER-optimal ADC outperforms the uniform and Lloyd-Max quantization approaches.

2.4 BER-Optimal ADC Simulation Results

This section presents simulation results for several channels with different levels of ISI.

2.4.1 Methodology

The process is described pictorially by Fig. 2.7.

First, given a sampled channel impulse response, a minimum mean squared error (MMSE) linear equalizer with three taps is obtained assuming a uniform ADC. Next, (2.32) was used to iteratively approximate the minimum BER thresholds and representation levels for the ADC. Equation (2.27) was then used to compute the BER analytically. We verified our expressions via Monte Carlo simulations and error counting for BER down to 10^{-7}. In order to isolate the effect of nonuniform quantization, the equalizers in all setups are MMSE linear equalizers with 3 taps. In addition, only equalizer inputs are quantized; the equalizer itself has infinite precision. Receiver signal-to-noise ratio (SNR) was computed by $\text{SNR} = \sum_{i=0}^{M-1} \frac{h[i]^2}{\sigma^2}$.

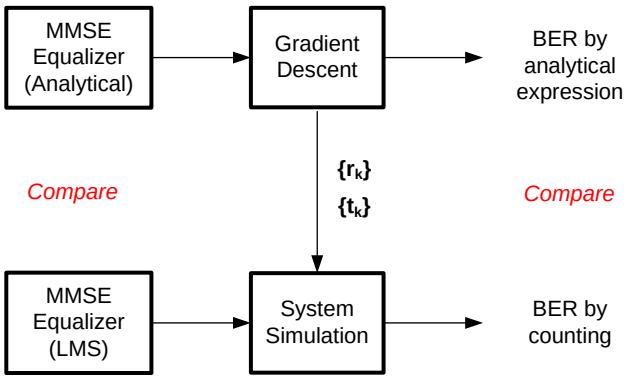


Figure 2.7: Simulation setup and verification of results.

To quantify the reduction in SNR achieved via the BER-optimal techniques, we define the *ADC shaping gain* S_G at a given BER as

$$S_G(BER) = \text{SNR}_{old}(BER) - \text{SNR}_{new}(BER). \tag{2.33}$$

ADC shaping gain is defined in the same fashion as coding gain, which measures the difference between uncoded system SNR and coded system

SNR needed to achieve the same BER.

In the case of channels with large memory M, small taps are truncated to reduce complexity of gradient search (the term "small" is being defined as less than 10% of the magnitude of the main channel tap). The initialization point for the algorithm is the uniform quantizer for low signal SNR, and the resulting new quantizer serves as the initialization point for higher SNRs to avoid suboptimal local minimum points.

2.4.2 Results

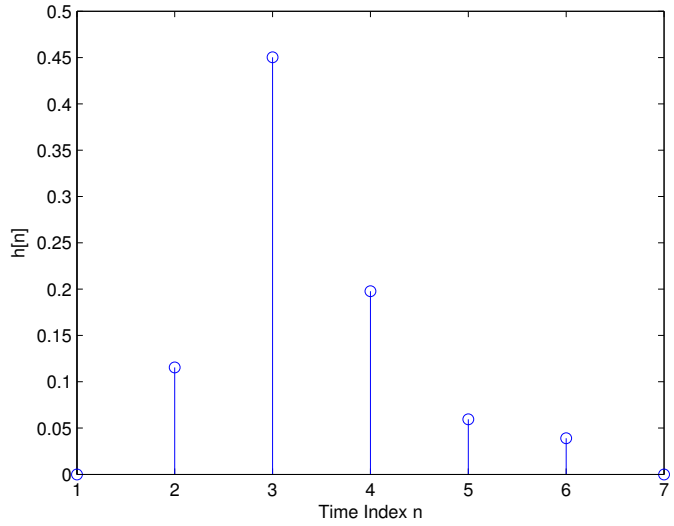
BER-Optimal ADC vs. Uniform ADC

Figures 2.8, 2.9, and 2.10 demonstrate the algorithm of (2.32) applied to a variety of channels, all of which were derived from models provided by the IEEE standard 802.3ap and Intel. The plots are arranged in the order of increasing intersymbol interference, characterized by the ratio $I = \frac{h_{i_{max}}^2}{\sum_{i=0, i\neq i_{max}}^{M-1} h_i^2}$, where $h_{i,max}$ is the cursor tap (Fig. 1.1). Large values of I imply low ISI. In all runs, the equalizer is an MMSE FIR filter with 3 taps, derived assuming an uniform ADC with the indicated number of bits in the front.

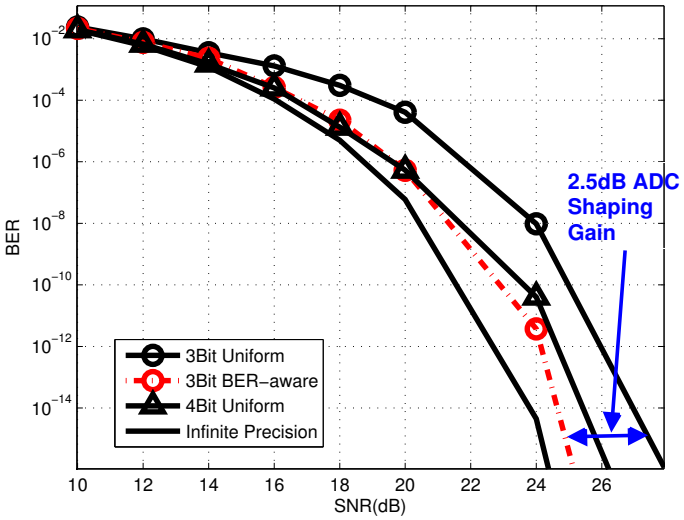
1) Channel with low level of ISI (Fig. 2.8(a)): Fig. 2.8(b) shows that a 3 bit BER-optimal ADC performs better than a 3 bit uniform ADC. Furthermore, a 3 bit BER-optimal ADC is at least as effective as a 4 bit uniform ADC. The BER curve for an infinite precision ADC, infinite precision equalizer is also displayed for comparison purposes. In both the low and high SNR regimes (BER=10^{-4} and 10^{-15}, respectively), the shaping gain S_G achieved by the BER-optimal ADC is 2.5 dB.

2) Channel with medium level of ISI (Fig. 2.9(a)): Fig. 2.9(b) shows that a 3 bit BER-optimal ADC is at least as effective as a 4 bit uniform ADC. Compared to a 3 bit uniform ADC, ADC shaping gain S_G is 3 dB at $BER = 10^{-4}$ and increases to 4.5 dB at $BER = 10^{-15}$.

3) Channel with high level of ISI (Fig. 2.10(a)): When channels with high levels of ISI are employed for testing, the 3 bit BER-optimal ADC is significantly better than the 3 bit uniform ADC as shown in Fig. 2.10(b). In this case, performance of the 3 bit uniform ADC does not improve with

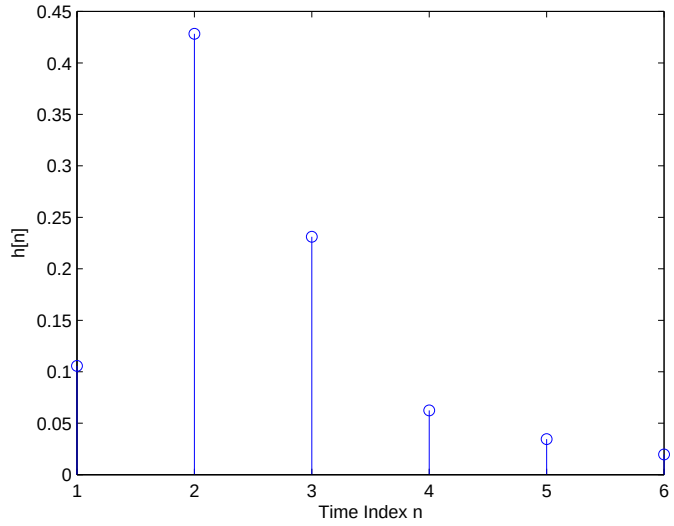


(a)

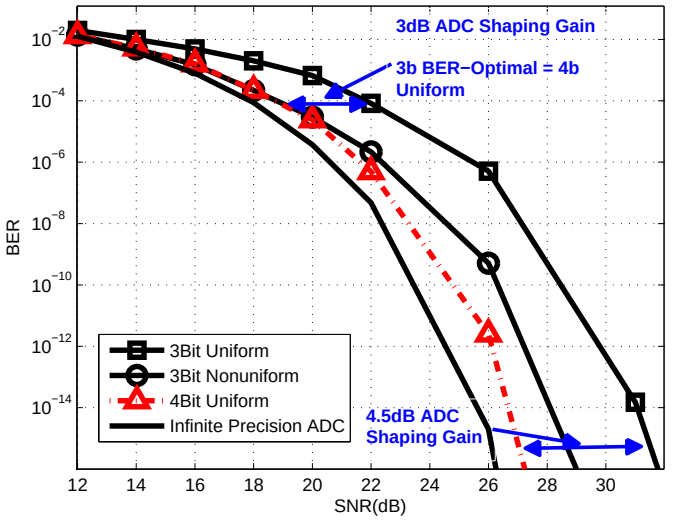


(b)

Figure 2.8: Performance for a low-ISI channel, I=3.5: (a) trimmed sampled impulse response of an FR4 backplane channel, and (b) BER vs. SNR curves for a 3 bit uniform, 3 bit BER-optimal, 4 bit uniform, and infinite-precision ADC, respectively.

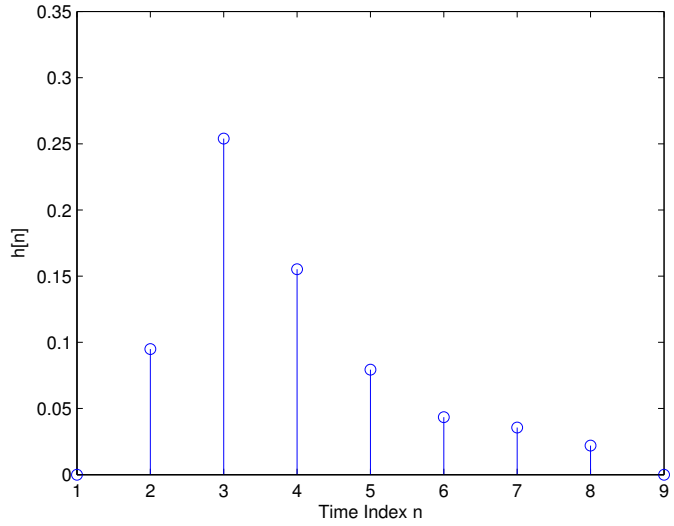


(a)

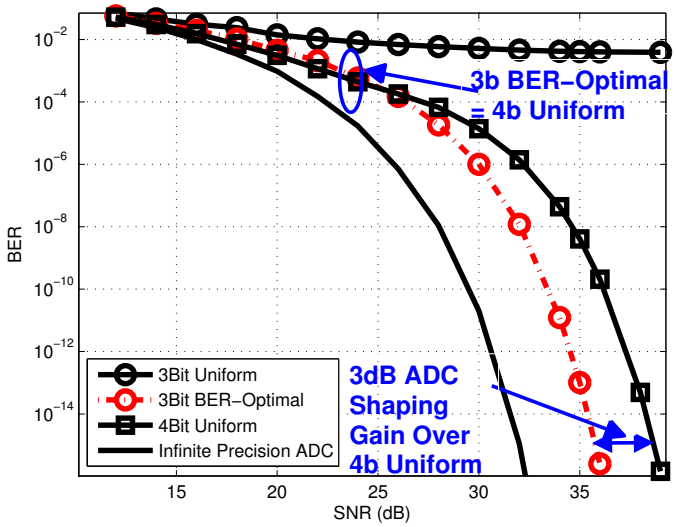


(b)

Figure 2.9: Performance for a medium-ISI channel, I=2.55: (a) trimmed sampled impulse response of an FR4 backplane channel, and (b) BER vs. SNR curves for a 3 bit uniform, 3 bit BER-optimal, 4 bit uniform, and infinite-precision ADC, respectively.



(a)



(b)

Figure 2.10: Performance for a low-ISI channel, I=1.5: (a) trimmed sampled impulse response of an FR4 backplane channel, and (b) BER vs. SNR curves for a 3 bit uniform, 3 bit BER-optimal, 4 bit uniform, and infinite-precision ADC, respectively.

increasing SNR due to severe quantization noise. Compared to a 3 bit uniform ADC, ADC shaping gain S_G is too large to be quantified; compared to a 4 bit uniform ADC, $S_G(BER = 10^{-15}) = 3$ dB.

The data are summarized in Table 2.1.

Table 2.1: Shaping gain of BER-optimal ADC for I/O channels with different ISI

ISI Level I	BER $= 10^{-4}$	BER $= 10^{-15}$
3.5	2 dB	3 dB
2.55	3 dB	4.5 dB
1.5	> 30 dB	> 30 dB

BER-Optimal ADC vs. Lloyd-Max ADC

The BER-optimal ADC is based on the detection criterion, while uniform and Lloyd-Max ADCs are both based on the fidelity criterion. Although a Lloyd-Max ADC can improve SQNR, Fig. 2.11 shows that a 2 bit Lloyd-Max ADC followed by a MMSE linear equalizer results in little improvement in BER when compared with a 2 bit uniform ADC followed by a MMSE LE. This observation indicates that SQNR is not the best metric when the goal is to reduce BER. In contrast, a receiver based on the detection criterion (2 bit BER-optimal ADC followed by min-BER linear equalizer, where the equalizer coefficients are computed in a similar manner as in (2.32) using gradient descent algorithm) results in significant improvement, surpassing even a 3 bit uniform ADC for SNR > 16 dB. This clearly demonstrates that the detection criterion is a more effective metric than the fidelity criterion in communication links.

BER as a Function of B_X

This section examines two relationships: improvement achievable by BER-optimal nonuniform quantization versus number of quantization bits and BER improvement versus signal SNR. Figure 2.12 shows the simulation results. 18 dB and 24 dB are the two chosen signal SNRs because they cor-

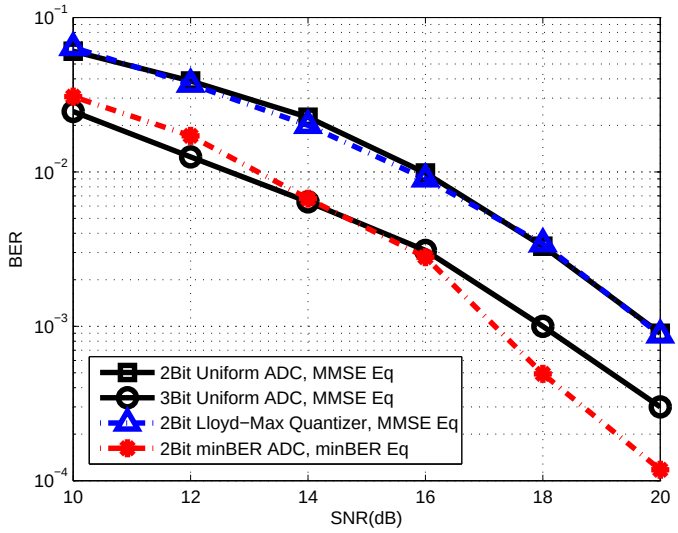


Figure 2.11: Performance comparison between the BER-optimal and Lloyd-Max ADC for a synthetic channel $h = [0.1\ 0.7\ 0.4]$.

respond to BER ranges needed for satisfactory operation in FEC-based and non-FEC high I/O links, respectively.

In the case of too few bits, BER-optimal quantization and uniform quantization are equally ineffective. A large amount of quantization noise prevents the receiver from correctly detecting the transmitted bit. When resolution is high, the BER gap closes. It is in the intermediate region that the BER improvement by using BER-optimal quantization is the greatest. Also, Figure 2.12 shows that BER can be greatly reduced when the signal is not as corrupted by noise. To quantify this improvement, a ratio $\frac{BER_{uniform}}{BER_{nonuniform}}$ is defined, and the values are presented in Table 2.2

Table 2.2: Log $\frac{BER_{uniform}}{BER_{nonuniform}}$ as a function of quantization bits and SNR

Bits	Signal SNR of 18 dB	Signal SNR of 24 dB
1	0	0
2	***1.4***	3.3
3	1.1	***3.4***
4	0.1	1.9

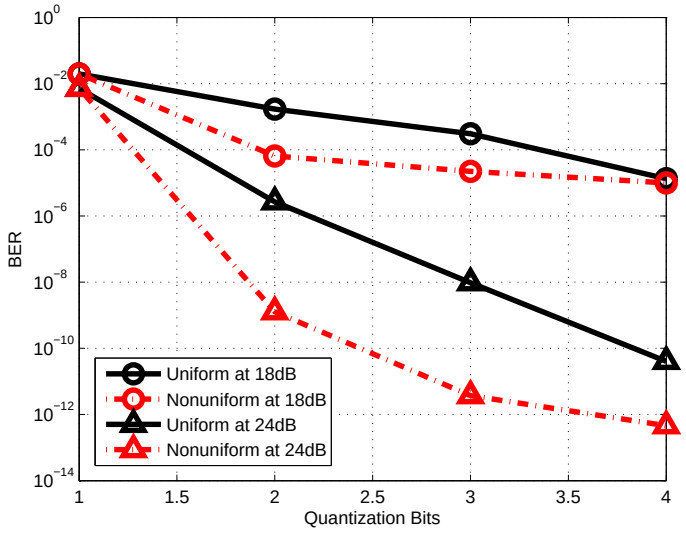


Figure 2.12: BER-optimal vs. uniform quantization for different numbers of bits and SNRs.

Predicting Conditions for Maximal Reduction in BER

To predict conditions for maximal BER reduction, this subsection analyzes noise that contributes to errors in a communication link.

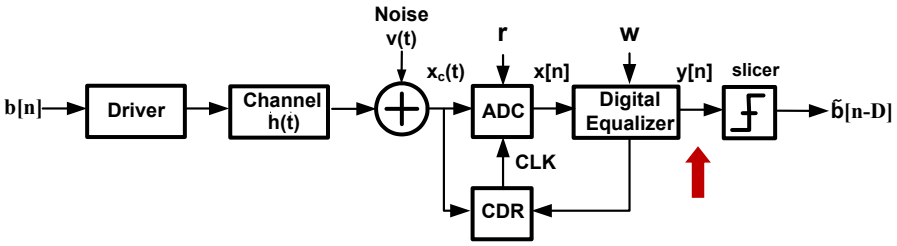


Figure 2.13: Noise sources at the slicer of a communication link.

There are three noise sources at the slicer, indicated by the thick arrow in Fig. 2.13: additive Gaussian noise that has been amplified by the linear equalizer, residual ISI, and quantization noise introduced by the ADC, also amplified by the equalizer. They are assumed to be independent of one another. We denote the respective noise variances as $\sigma^2_{v,slicer}$, $\sigma^2_{I,slicer}$, and $\sigma^2_{q,slicer}$ and compute them as follows:

$$\sigma^2_{v,slicer} = \sigma^2 \sum w_j^2,$$
$$\sigma^2_{I,slicer} = \sigma_s^2 \sum p^2_{j,j\neq max},$$
$$\sigma^2_{q,slicer} = \frac{V^2_{max}}{12\times 2^{2B_X-2}} \sum w_j^2, \tag{2.34}$$

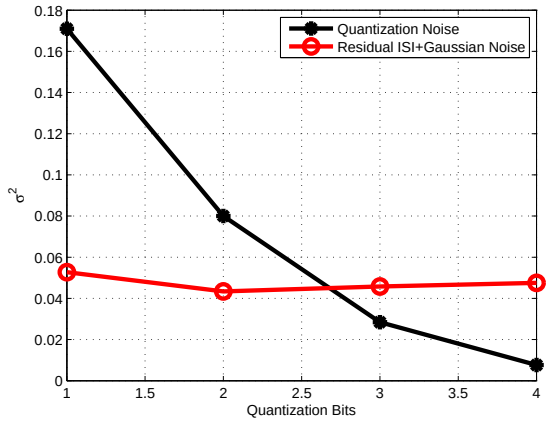
where w_js are MMSE linear equalizer coefficients, σ^2 the additive Gaussian noise variance before the receiver, σ_s^2 the signal power as set by the transmitter swing, p_js the composite channel coefficients obtained by convolving the channel and the equalizer, $p_{j,j\neq max}$s are all taps of the composite channel except for the largest, and V_{max} is the maximum value expected by the ADC.

Noise analysis is done accordingly for two channels (Fig. 2.8(a) and 2.10(a)); the variances are plotted as a function of ADC quantization bits in Fig. 2.14 and 2.15. For Channel 1, quantization noise is dominant when ADC has less than 2.5 bits and signal SNR is 18 dB. At 24 dB, this crossover point between quantization noise and the total sum of Gaussian noise plus residual ISI shifts to 3 bits. Similar trend is observed for Channel 2.

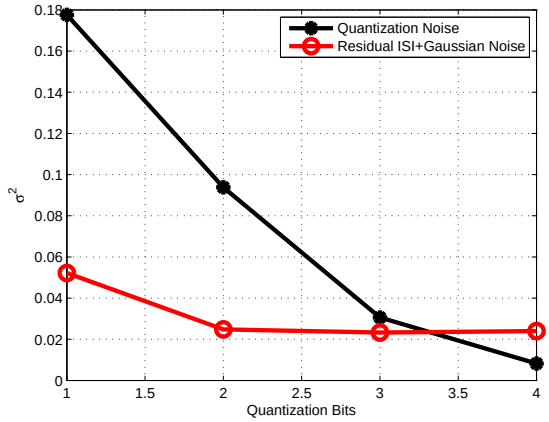
BER-optimal quantization should be most effective when the quantization error is the dominant noise source. Maximal BER reduction in theory occurs in low noise regions, where because of the waterfall nature of the Q-function, increasing signal-to-noise ratio by either using more signal power or reducing noise power exponentially decreases the probability of error. Tables containing $\frac{BER_{uniform}}{BER_{nonuniform}}$ numbers (Tables 2.2 and 2.3) for different quantization bits and SNRs show that this is indeed the case. The maximum improvement in BER occurs at the largest integer number of bits not greater than the x-axis coordinate of the crossover point between the noise variances.

Table 2.3: Log $\frac{BER_{uniform}}{BER_{nonuniform}}$ as a function of quantization bits and SNR for channel in Fig. 2.10(a)

Bits	Signal SNR of 18 dB	Signal SNR of 28 dB
0	0	0
2	***0.6***	1
3	0.4	***2.5***
4	0.04	1.6

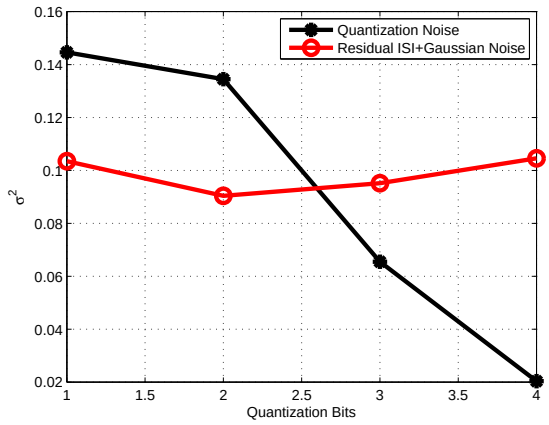


(a)

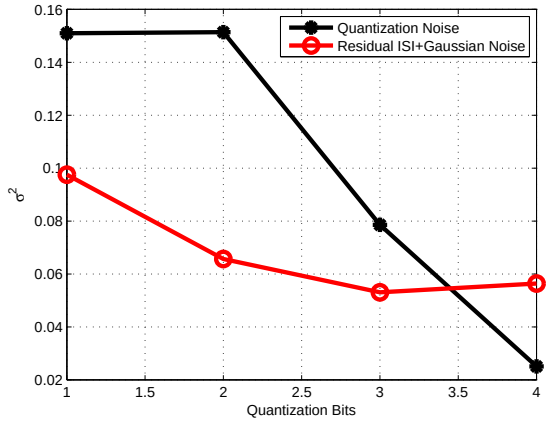


(b)

Figure 2.14: Noise sources at the slicer of a communication link: (a) SNR = 18 dB, and (b) SNR = 24 dB.



(a)



(b)

Figure 2.15: Performance for a medium-ISI channel, I=2.55: (a) trimmed sampled impulse response of an FR4 backplane channel, and (b) BER vs. SNR curves for a 3 bit uniform, 3 bit BER-optimal, 4 bit uniform, and infinite-precision ADC, respectively.

Chapter 3

Implementation of a BER-Optimal ADC Receiver

Implementation of the BER-optimal ADCs is not straightforward. Once the optimal $\mathbf{r}$ and $\mathbf{t}$ are obtained, the crucial issue that must be addressed is the representation of the output values. Since the quantization levels are no longer equidistant, a change in digital output will correspond to different changes in analog input. The equalizer cannot operate directly on such digital outputs.

To interface the BER-optimal ADCs and the digital equalizer, we must perform some digital linearization; i.e., we must represent the ADC outputs with more bits, or modify the equalizer. Unfortunately, either introduces more circuit blocks that must be carefully designed for high speed operation. Furthermore, in case of digital linearization, more data bits would increase the gate count as well as critical path delay of the equalizer.

To avoid these design problems, one option is to replace the standard digital equalizer with a look-up table (LUT). This is done by mapping the ADC bits in the tapped-delay line directly to a binary value corresponding to the detected bits. The result therefore has the same function of an equalizer and slicer.

We synthesized the digital equalizer following the BER-optimal ADC and compared its complexity to that of the standard linear equalizer (Fig. 3.1). Not only does the LUT occupy less area and consume less power, it also avoids the interface problem between the BER-optimal ADCs and digital equalizers.

The channels are those presented in Section 2.4.1; for each channel, two design points in the plots, corresponding to low and high input SNRs, are synthesized and compared. The BER-optimal ADCs have 3 bits, while the benchmark is a 4 bit uniform ADC, 3-tap linear equalizer, with sufficient bits assigned to equalizer coefficients to ensure no BER degradation due to coefficient quantization at BER of 10^{-4}. From Table 3.1, we see that

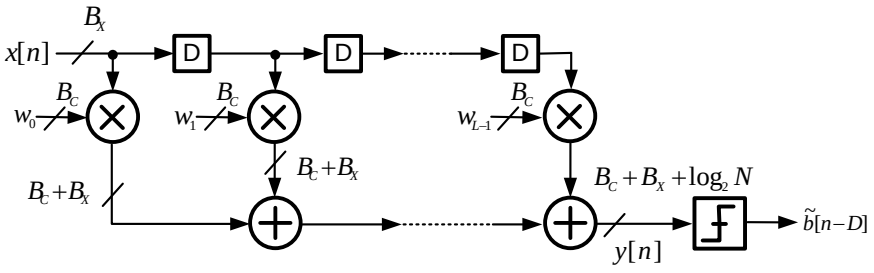


Figure 3.1: Finite precision FIR filter.

the LUT-based equalizer is in fact much simpler than the conventional FIR filter, indicating that BER-optimal ADCs are superior. The area and power numbers are provided by synthesis reports from Nangate's Open 45 nm Cell Library. At low SNR design point for the high ISI channel, the standard LE occupies 269.7 μm^2 , while area of the LUT-based equalizer is only 91.5 μm^2. This is a reduction of 66%. To summarize, for low SNRs, the area of the LUT-based equalizer is reduced by 55% to 66%, and power is reduced by about 45%. For high SNRs, the area of the LUT-based equalizer is reduced by 39% to 56%, and power reduction is around 24% to 32%. Global voltage of 0.95 V and clock frequency of 400 MHz are used.

Table 3.1: Comparing complexity of LUT-based equalizer with LE

Low ISI Channel	**Fig. 2.8**	
SNR (dB)	**Cell Area (μm^2)**	**Power (μW)**
10 (LUT)	108	22.2
10 (LE)	244.4	40.5
18 (LUT)	106	22.7
18 (LE)	177	29.9
High ISI Channel	**Fig. 2.10**	
SNR (dB)	**Cell Area (μm^2)**	**Power (μW)**
12 (LUT)	91.5	22.6
12 (LE)	269.7	43.0
24 (LUT)	93	23.1
24 (LE)	209	34.4

Chapter 4

Conclusion

This thesis introduced the novel idea of BER-optimal ADCs, which unlike past ADC designs, use a detection criterion instead of a fidelity criterion. An analytical expression for bit error rate was presented for a communication link in which the receiver consists of an ADC, LE/DFE, and slicer. Subsequently a gradient-descent algorithm was developed to numerically determine levels and thresholds that minimize bit error rate.

BER-optimal quantization is applied to several channel models with varying degrees of ISI. The results all demonstrate the efficacy of an ADC based on a detection criterion, indicating a promising direction for future designs. In all cases, a 3 bit BER-optimal ADC achieves at least as low a BER as a 4 bit uniform ADC. Shaping gains achieved by the BER-optimal ADC range from 2.5 dB for channels with low ISI to more than 30 dB for channels with high ISI. For high speed flash architecture, a 1 bit reduction corresponds a power reduction by $2\times$. Additionally in the second half of Chapter 2, noise sources at the slicer were analyzed in order to predict the conditions under which the new approach would bring maximum BER reduction.

Chapter 3 presents a feasibility study for the BER-optimal ADCs. Look-up table based equalizers compatible with BER-optimal ADCs are shown to reduce the power up to 47% and the area up to 66% in a 45 nm CMOS process.

4.1 Future Work

There are many interesting directions to explore.

One direction would extend the concept of BER-optimal ADC to link systems with decision feedback equalizers and channels with "notches" or nulls (channel whose amplitude spectrums evidence a dip). Moreover, to

prove the concept of BER-optimal ADCs, all equalizers in this work are fixed MMSE equalizers. To achieve optimal performance, however, equalizer and ADC should be ideally jointly adapted.

Thus far, the work has only concerned itself with quantization and not sampling. The next logical step would be to include bandwidth limitations and nonlinearity in the track-and-hold circuitry of the ADC. The models of [9], for example, can account for nonlinearity arising from switch resistances and memory caused by a dependency on the signal slope.

As the current objective function is highly nonlinear, finding an alternative function that closely approximates the original but is highly differentiable can help to improve the gradient descent algorithm.

Finally, though the LUT-based equalizer is much simpler than conventional finite precision equalizers, it is not adaptable. Making it reconfigurable or adaptable would increase its practicality.

Appendix

Channel Sampled Time Impulse Responses

Following are tap coefficients of FR4 backplanes sampled at 10 Gb/s.

Channel 1 Sampled Time Impulse Response

Following is a FR4, 1.25 in, middle layer stripline. The linecards are made from Nelco 4000-13 routed in top and middle layers. Frequency response data are provided by IEEE802.3ap Standard.

0.1154 0.4503 0.1977 0.0595 0.0390 0.0021 0.0267 0.0149 0.0120 0.0092 0.0044 0.0012 0.0055 0.0022 0.0068 0.0027 0.0021 0.0024 0.0061 0.0020 0.0025 0.0026 0.0015 0.0003 0.0016 0.0025 0.0015 0.0011 0.0005 0.0005 0.0013 0.0009 0.0004 0.0006 0.0013 0.0005 0.0012 0.0009 0.0011 0.0011 0.0007 0.0004 0.0006 0.0001 0.0002 0.0003 0.0001 0.0002 0.0002 0.0002 0.0004 0.0002 0.0001 0.0001 0.0001 0.0001 0.0001 0.0001 0.0001 0.0001 0.0001 0.0001 0.0001 0.0000 0.0001 0.0001

Channel 2 Sampled Time Impulse Response

Following is a FR4, 1.25 in, bottom layer stripline. The linecards are made from Nelco 4000-13 routed in middle and bottom layers. Frequency response data are provided by IEEE802.3ap Standard.

-0.0000 -0.0001 -0.0001 -0.0001 -0.0001 -0.0001 -0.0001 -0.0001 -0.0001 -0.0001 -0.0001 -0.0001 -0.0000 -0.0001 -0.0000 0.0000 0.0096 -0.0016 -0.0055 -0.0019 0.0000 0.0001 0.1057 0.4283 0.2312 0.0625 0.0346 0.0196 0.0147 0.0308 -0.0077 0.0100 -0.0081 0.0041 0.0019 0.0109 0.0021 0.0028 0.0025 -0.0034 -0.0006 0.0100 0.0030 -0.0031 0.0018 0.0015 0.0020 -0.0019 -0.0023 0.0051 0.0006 0.0006 0.0018 -0.0002 0.0001 0.0013 0.0007 -0.0003 0.0007 0.0005 -0.0010 0.0016 0.0003 -0.0001 0.0008 0.0005 -0.0004 0.0006 0.0008 -0.0006

0.0009 -0.0005 0.0003 0.0000 0.0004 -0.0009 0.0005 0.0010 -0.0004 -0.0002 0.0009 0.0003 -0.0003 -0.0001 0.0008 -0.0008 0.0006 0.0002 -0.0006 0.0000 0.0007 -0.0002 -0.0002 0.0005 0.0001 -0.0000 0.0001 -0.0000 -0.0002 0.0003 0.0001 -0.0003 0.0002 0.0003 0.0002 -0.0002 -0.0000 0.0003 0.0001 -0.0001 -0.0001 0.0004 -0.0001 0.0000 0.0001 0.0000 0.0001 0.0000 -0.0002 -0.0001 0.0002 -0.0005 -0.0002 0.0003 -0.0002 -0.0002 0.0003 0.0002 -0.0002 -0.0000 0.0001 -0.0000 0.0001 -0.0001 -0.0003 0.0001 0.0002 -0.0001 -0.0002 0.0001 0.0001 0.0000 -0.0000 -0.0000 -0.0000 0.0001 0.0001 -0.0002 -0.0001 0.0001 0.0002 0.0000 -0.0000 -0.0001 0.0001 0.0002 0.0000

Channel 3

Following is a "high ISI," 20 in, FR4 backplane channel.

0.0006 0.0007 0.0008 0.0010 0.0012 0.0015 0.0020 0.0027 0.0041 0.0072 0.0171 0.0949 0.2539 0.1552 0.0793 0.0435 0.0356 0.0220 0.0126 0.0112 0.0099 0.0097 0.0076 0.0072 0.0065 0.0060 0.0066 0.0142 0.0032 -0.0025 0.0019 0.0010 0.0025 0.0075 0.0037 0.0001 0.0008 0.0017 0.0020 0.0017 0.0028 0.0048 -0.0000 -0.0024 0.0008 0.0030 0.0023 0.0015 0.0023 0.0016 0.0011 0.0014 0.0014 0.0013 0.0014 0.0014 0.0017 0.0031 0.0037 0.0007 -0.0007 -0.0004 -0.0003 0.0012 0.0021 0.0010 0.0002 0.0000 0.0003 0.0005 0.0005 0.0005 0.0009 0.0014 0.0017 0.0018 0.0017 0.0015 0.0013 0.0013 0.0014 0.0016 0.0016 0.0014 0.0012

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