ELECTRICAL AND THERMAL CHARACTERIZATION TECHNIQUES FOR CARBON NANOTUBE TRANSISTORS AND NETWORKS

BY

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ABSTRACT

In this study, pulsed measurement techniques to suppress hysteresis in carbon nanotube (CNT) field-effect transistor (CNTFET) transfer characteristics are demonstrated. As hysteresis is reduced, both forward and backward gate voltage sweeps move toward a common, unique central transfer characteristic that reveals the “true” device mobility. Time constants associated with environmental charge trapping, at various ambient temperatures from 80 to 453 K are extracted. Hysteresis dependence of pulsed measurements is compared under air, high-temperature, and vacuum conditions. Using such measurements we investigate the error on carrier mobility associated with mobility extractions from forward and backward DC gate voltage sweeps. A pulsed electrical breakdown technique to increase the $I_{\text{ON}}/I_{\text{OFF}}$ ratio of carbon nanotube random network transistors is also demonstrated. The ratio is increased by three orders of magnitude, with minimal reduction in $I_{\text{ON}}$ (< 50%). It is shown that adsorbed water rather than oxygen promotes nanotube breakdown. Finally, the design of an electrical thermometry platform for measuring the thermal properties of nanoscale films is presented, with possible application to single-walled CNT random networks and perfectly aligned arrays. The platform is freely suspended to confine heat flow to one dimension, leading to challenging stress patterns in the constituent SiO$_2$ membrane. Using sputtered SiO$_2$ reduces stress by a factor of 20 and results in a “flatter,” more robust membrane for thermal measurements. Methods of incorporating CNT networks in the device fabrication process are discussed. As a calibration step, the thermal conductivity for a 320 nm freestanding thin film of RF sputtered SiO$_2$ is found to be 0.45 Wm$^{-1}$K$^{-1}$ at 300 K, in agreement with previous measurements of thin SiO$_2$ films on bulk Si.
To my wife and son, for their love and support.
ACKNOWLEDGMENTS

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CHAPTER 1: POWER DISSIPATION AND RELIABILITY IN NANOELECTRONICS

1.1 Power Dissipation in Nanoelectronics: The “Top-Down” Picture

The typical PC and server waste more than 30 percent of their input power in the form of heat. This wasted energy has yet to be harnessed to perform work, such as switching transistors or storing data in a memory bit. To compound the problem, the amount of waste heat generated requires advanced thermal management techniques and increases demands on auxiliary systems such as air conditioning, which results in higher energy requirements and cost [1]. Figure 1.1 illustrates the amount of computer-related energy use reported in the United States for the year 2007. When cooling is added to the energy use of data centers, PCs, and displays, computer-related energy consumption accounted for 5 percent of the nationwide power budget in 2007. If current trends continue, it is expected that computer-related energy use would require one-third of the national power budget in the year 2025 [2].

Additionally, computer processes that may appear to be computationally inexpensive at the local level, such as filtering email spam, require enormous amounts of energy at the global scale. It has recently been estimated that, globally, 33 billion KWh are required annually to create, send, receive, store, and view email spam. Coal is estimated to have an energy density of 6.67 KWh/kg. Assuming the thermodynamic efficiency of converting coal to electricity is roughly 30%, spam email consumes approximately 16.5 billion kg of coal annually [3, 4]. This accounts for the power generation of 4 new coal power plants and 0.2 percent of the total global CO₂ emissions [3].
One of the major influences on the increased power dissipation in computers is an exponential increase in the power density of computer processors (Fig. 1.2). Current computer processor technology has a power density of about 100 Wcm$^{-2}$, approximately equal to that of an incandescent light bulb. Power density in integrated circuits is a result of leakage currents in transistors, $P_{\text{STATIC}} = I_{\text{LEAK}} \cdot V_{DD}$, and increased dynamic power consumption, $P_{\text{DYN}} = f \cdot C \cdot V_{DD}^2$. Here, $f$ is the clock frequency, $C$ is the load capacitance, $V_{DD}$ is the operating voltage. While transistor scaling has lowered the required operating voltages, faster switching speeds and increased leakage currents continue to dominate the resultant power densities. If current trends continue, the power densities of future processors would exceed the power density of the Sun’s surface, 6000 Wcm$^{-2}$. The maximum operating temperature of silicon-based integrated circuits is approximately 125 °C. Therefore, future scaling for increased transistor density will be limited by the rate at which heat can be removed from the integrated circuit [5]. Hence, using known heat removal technologies, the power density of integrated circuits is limited to several hundred Wcm$^{-2}$ at best [5].

While reducing power dissipation is a fundamental challenge for continued scaling of nanoelectronics, it may be possible to enhance integrated circuit performance by introducing novel, high-mobility/high-thermal-conductivity materials as devices, interconnects, or back-end heat sinks. Among these, carbon nanotubes (CNTs) are 1-dimensional (1-D) materials with extraordinary electrical and thermal properties: $\sim 10^9$ A/cm$^2$ current density and thermal conductivity up to 3500 Wm$^{-1}$K$^{-1}$ for freely suspended CNTs [6]. However, such 1-D materials and devices must be connected to the surrounding 3-D world, giving rise to boundary resistance, density-of-states mismatch,
and atomic-scale surface roughness effects. Furthermore, much work remains to be done to understand the fundamental behavior of dimensionally mismatched electron devices and thermal-electrical materials.

1.2 Carbon Nanotubes and Nanotube Devices

Carbon nanotubes are one-dimensional conductors with excellent electron mobility ($\approx 20 \times \mu_{\text{Si}}$) [7] and lattice thermal conductivity ($\approx \kappa_{\text{DIAMOND}}$) [6]. CNTs are an allotrope of carbon in a cylindrical nanostructure. Each nanotube wall is an atomic monolayer of $sp^2$-bonded carbon atoms in a honeycomb lattice. The orientation of the carbon atoms with respect to the CNT’s longitudinal axis, i.e., the CNT chirality, determines many of its properties, particularly its conductance (Figs. 1.3, 1.4). A CNT is considered metallic if the difference between the chiral vector indices is divisible by three ($n - m = 3i$, where $i$ is an integer). Hence, two-thirds of CNTs grown with random $n$ and $m$ are semiconductors and one-third are metallic. The band gap of a semiconducting single-walled CNT is inversely proportional to the diameter, $0.84 \text{ eV}/d$ [8, 9].

The excellent electrical, mechanical, and thermal properties of CNTs have prompted their use as circuit elements, such as transistors or interconnects. CNTs have also been investigated as thermal heat sink components and thermal interface materials. Because of the high electric field or temperature gradients associated with these applications, it is important to fully characterize CNTs’ fundamental properties, and their reliability under such stress. In research labs, carbon nanotube field effect transistors (CNTFETs) are often back-gated, with the CNT exposed to the ambient environment (Fig. 1.4) [10]. CNTFETs are possible candidates for future nanoelectronics because of
their ability to carry large current densities and their high carrier mobility, greater than $10^9 \text{A/cm}^2$ and $10^4 \text{cm}^2/\text{V}\cdot\text{s}$ respectively [7, 11]. Anti-clockwise hysteretic behavior in the drain-to-source current ($I_{DS}$) and gate-to-source voltage ($V_{GS}$) transfer characteristics is common and will vary depending on sweep direction, sweep rate, and environmental conditions (Fig. 1.5). Therefore, it is often unclear which of the transfer curves, forward or reverse, should be used to extract carrier mobility and threshold voltage, leading to large discrepancies (>10×) in reported values.

In addition to single-connected CNTFETs, random networks of single-wall carbon nanotubes (SWCNT) (Fig. 1.3) have been demonstrated as semiconductors for applications in small- to medium-scale integrated circuits on flexible or transparent substrates [1]. Typical mobilities for these types of films can be of the order 20 – 40 cm$^2$V$^{-1}$s$^{-1}$, up to two orders of magnitude greater than other conformal electron devices. One of the major challenges in applying such nanoscale thin films to electron devices has been enhancing the semiconducting properties of the film. Typically, the metallic percolative pathways in the network result in poor ON/OFF ratios, which are detrimental to static power dissipation as well as to clear logic transitions between ones and zeros. Geometric striping of random network CNT films can enhance their ON/OFF ratio by reducing metallic percolative pathways in the film [1]. Previous work suggests that current-induced defect formation, and oxidation induced by pulsed electrical stress also selectively remove metallic pathways from CNT bundles and low-density CNT thin films [2, 3]. It would be beneficial to find a method of eliminating metallic pathways in situ, which could lead to the development of programmable integrated circuits on conformal substrates.
1.3 Measuring Heat Transfer at the Nanoscale

The use of nanoscale devices and materials in current and future integrated circuit technology is problematic in that the length scales of the electron devices are approaching the wavelengths and mean free paths of the carriers responsible for heat transport in the device. This requires the development of new and accurate metrology methods to further understanding of heat flow at the nanoscale, enabling the development of novel materials and devices to better transport the generated heat [12]. A simple yet versatile approach to measuring thermal properties at the nanoscale is by steady-state electrical thermometry. Electrical thermometry techniques can provide novel and non-destructive approaches to measure the thermal and electrical behavior of nanostructures. This particularly includes dimensionally mismatched materials and devices, such as those formed by 1D CNTs or 2D graphene with their 3D environment. Other existing thermometry techniques such as scanning thermal microscopy and thermoreflectance thermometry offer nanometer or sub-nanosecond resolution, respectively, but at the expense of each other. In addition, they cannot be applied in situ to nanostructures under real operating conditions, because they require a surface view of the sample, or are partially destructive [13].

Steady-state electrical thermometry induces a temperature rise on one side of the sample by flowing current through a metallic heater, generating Joule heating. Temperature gradients across the sample are sensed by measuring calibrated changes in the resistance of a nearby metallic sensor. This technique has been used to measure the lateral thermal conductivity (κ) of suspended thin films for over two decades [14]. Since then, advances in microfabrication technology have enabled the use of suspended membranes and steady-state electrical thermometry to measure the lateral κ of various
thin films, thin film stacks, and nanostructures [15-20]. Figure 1.6 illustrates a typical electrical thermometry platform with one heater and two sensors.

In this study, metrology methods for investigating the thermal and electrical properties of CNTs are developed. A pulsed technique to suppress hysteresis in CNTFET transfer characteristics is demonstrated. As hysteresis is reduced, both forward and backward gate voltage sweeps move toward a common, unique central transfer characteristic that reveals the “true” device mobility. A pulsed electrical breakdown technique to increase the $I_{ON}/I_{OFF}$ ratio of carbon nanotube random network transistors is also demonstrated. Finally, the design of an electrical thermometry platform for measuring the thermal properties of nanoscale films is presented, and it is shown how it can be applied to CNT random networks and perfectly aligned arrays.
### 1.4 Figures

**2007 Power Consumption (GW)**

- Work displays: 7 GW
- Work PCs: 3.2 GW
- Home displays: 2.6 GW
- Home PCs: 6.5 GW
- Data Centers: 1.3 GW

**Figure 1.1:** Total U.S. computer-related power consumption separated by computer sector for 2007. In 2007 computer-related energy use accounted for 5% of the national power budget.

**Figure 1.2:** Power density vs. time for major computer processors manufactured over the past two decades. The exponential trend in power density has limited transistor scaling and is the main source for computer-related energy consumption.
Figure 1.3: Scanning electron micrograph of randomly grown CNT network grown by chemical vapor deposition. Two-thirds of the CNTs in the network are thought to be semiconductors. One-third are thought to be metallic.

Figure 1.4: Typical back-gated CNTFET. The CNT lies on a gate dielectric exposed to the ambient from above, and is contacted by a source and drain electrode. The highly doped substrate acts as a back gate electrode [10].
Figure 1.5: Typical transfer characteristics for a back-gated CNTFET. The arrows indicate the direction of the hysteresis and the $V_{GS}$ sweep. Hysteresis is defined as the difference between the threshold voltages extracted from the forward (–10 to 10 V) and reverse (10 to –10 V) sweeps.

Figure 1.6: Optical image of an electrical thermometry platform with one heater and sensor strips. The device active region is a suspended thin film, which allows for a 1-D heat flow approximation. The thermal properties of nanoscale materials/devices can be measured by monitoring calibrated changes in the resistance of the sensors.
1.5 References


CHAPTER 2: REDUCTION OF HYSTERESIS IN CARBON NANOTUBE FIELD EFFECT TRANSISTOR MOBILITY MEASUREMENTS

2.1 Hysteresis in Carbon Nanotube Field Effect Transistors

As stated in Chapter 1, carbon nanotube field effect transistors (CNTFETs) are possible candidates for future nanoelectronics because of their ability to carry large current densities and their high carrier mobility, greater than $10^9$ A/cm$^2$ and $10^4$ cm$^2$/V·s respectively [1, 2]. In research labs, CNTFETs are often back-gated, with the CNT exposed to the ambient environment. Hysteretic behavior in the drain-to-source current ($I_{DS}$) and gate-to-source voltage ($V_{GS}$) transfer characteristics is common and will vary depending on sweep direction, sweep rate, and environmental conditions. This is typically attributed to charge trapping by surrounding water molecules or charge injection into the substrate [3, 4]. Thus, it is often unclear which electrical characteristics should be used to extract carrier mobility and threshold voltage, leading to large discrepancies (>10×) in reported values, as both the forward[1] and backward[2] $I$-$V$ sweeps have been used (Table 2.1).

In this study, a pulsed measurement technique to suppress hysteresis in CNTFET transfer characteristics is presented. As hysteresis is reduced, both forward and backward sweeps move toward a common, unique central transfer characteristic that reveals the “true” device mobility. By varying the pulse width and duty cycle in this measurement over a wide range (1ms–10 s), the time constants associated with environmental charge trapping are extracted at various ambient temperatures from 80 to 453 K. A greater reduction in hysteresis at higher temperature ($\approx 2 \times$ at 453 K) is reported. Hysteresis dependence of pulsed measurements is compared under air and vacuum conditions. Using
such measurements we investigate the error on carrier mobility associated with mobility extractions from forward and backward DC gate voltage sweeps.

2.2 Experimental Setup

Approximately thirty single-wall nanotube devices were used in this study. The results presented here are a representative sample. Single-wall nanotube devices were grown by chemical vapor deposition (CVD) from Fe catalyst on 70 nm SiO$_2$. The highly doped (p++) silicon substrate serves as a back gate, and the CNTs were exposed to ambient from above, as shown in Fig. 2.1. The Ti/Pd electrodes are fabricated using standard lithographic techniques. CNT diameter ($d$) and length ($L$) are measured by atomic force microscopy and scanning electron microscopy (inset Fig. 2.1a). The transfer characteristics were measured by keeping the drain-to-source voltage ($V_{DS}$) constant at 50 mV, while performing a pulsed-linear sweep of $V_{GS}$ between ±10 V. The gate voltage pulse period was varied over a wide range (~1 ms–10 s) with the pulse width held constant at 1 ms (no significant dependence of pulse width was found in the range of 250 µs to 1 ms). Measurements are made using a Keithley 2612 dual source measurement unit under varying ambient conditions and temperatures. The devices in this study have diameters ranging from 1.6 nm to 3.8 nm and channel lengths of approximately 2 µm to 7.5 µm.

2.3 Hysteresis Reduction

The hysteresis gap ($\Delta V_{TH}$) is defined as the difference in threshold voltage between the forward and backward gate voltage sweeps, as determined by the linear
extrapolation method (Fig. 2.2a). Hysteresis dependence of pulsed measurements is compared under air and vacuum conditions (10^{-5} torr) at room temperature (Figs. 2.2a–d). At room temperature in air and under vacuum, hysteresis is reduced by increasing the length of the pulse off time (t_{OFF}). Under ambient conditions, hysteresis is reduced by up to 75% (Fig. 2.2a), while under vacuum, hysteresis is nearly eliminated (Fig. 2.2d) as t_{OFF} is increased from 1 ms to 10 s. Furthermore, hysteresis reduction due to vacuum is more pronounced at shorter off times for the device with d = 2.1 nm, indicating that charge injection into the substrate affects hysteresis less than charge trapping by surrounding water molecules for this device. However, for the device with d = 1.7 nm, vacuum has no effect on the hysteresis at shorter off times, possibly because of the reduced surface area for water adsorption. For this device, charge injection into the substrate is most likely the dominant cause of hysteresis. Hystereses from the DC V_{GS} sweeps are compared for CNTFETs of varying d and L (Fig. 2.3). It is shown that hysteresis does not depend on CNT d or L. Measurements made in air at ambient temperatures from 293 to 453 K indicate the rate of hysteresis reduction with t_{OFF} increases with increased temperature (Fig. 2.4a). This suggests reduced charge trapping by the surrounding water molecules and a faster relaxation rate of trapped charge at high temperature. It is rather intuitive that higher temperature evaporates water from the SiO_{2} surface and that thermally excited carriers will escape trap sites faster than those with less thermal energy. At low temperature hysteresis becomes nearly constant, at approximately 1.5 V, with increasing t_{OFF}, in agreement with the findings of Vijayaraghavan et al.[21].

Figure 2.4a illustrates the dependence of ΔV_{TH} on t_{OFF} under varying temperature in air. Figure 2.4b illustrates the dependence of ΔV_{TH} on t_{OFF} at room temperature in air
and under vacuum. In both cases, at short $t_{\text{OFF}} (< 100 \text{ ms})$, there is not a significant
dependence of $\Delta V_{\text{TH}}$ on $t_{\text{OFF}}$. However, at higher $t_{\text{OFF}}$ there is a rapid decrease in
hysteresis with increased $t_{\text{OFF}}$. This indicates that the relaxation time of injected charge
into the substrate is greater than 100 ms. The corresponding trap depths can then be found
by using the tunneling front model:

$$x = \frac{1}{2k} \ln \left( \frac{t}{\tau_0} \right)$$

(2.1)

where

$$k = \frac{\sqrt{2m^*(\Phi - E)}}{\hbar}$$

(2.2)

and $m^*$ is the effective mass in SiO$_2$, $\Phi$ is the barrier height, $E$ is the energy up to which
the traps are filled, and $\tau_0$ is a characteristic tunneling constant [5–7].

2.4 Mobility Extraction

Finally, the effective mobility $\mu_{\text{EFF}} = GL/[C'(V_{\text{GS}}-V_{\text{TH}})]$ extracted from the
forward and backward DC $V_{\text{GS}}$ sweeps is compared to the extracted $\mu_{\text{EFF}}$ from pulsed $V_{\text{GS}}$
sweeps with $t_{\text{OFF}} = 10 \text{ s}$ under vacuum. This is done for devices with similar $L$, and $d =
1.7 \text{ nm}, 2.1 \text{ nm}$ (Fig. 2.5). Here $G = I_{DS}/(V_{DS}-I_{DS}R_C)$ is the drain conductance at $V_{DS} = 50$
mV, $C'$ is the capacitance per unit length, and $R_C$ the contact resistance. The $R_C$ is
determined using the devices’ low-bias resistance, $R_{LB}$. The contact resistance is written
as $R_C = R_{LB} - R_0$, where $R_0$ is the intrinsic resistance of the CNT, which depends on $L$ and
the acoustic phonon mean free path, $\lambda_{\text{AC}} \approx 280 d$. The $V_{\text{TH}}$ used in calculating $\mu_{\text{EFF}}$ is
determined by finding the gate voltage at a specified threshold drain current ($I_{\text{TH}}$), such
that $I_{\text{TH}} \approx G/G_0 < 0.001$. Here, $G_0$ is the quantum conductance for four CNT channels.
We find that at longer pulse off times there is less discrepancy between forward and backward sweep, and the extracted mobility approaches a common value (Figs. 2.4c,d). Moreover, we find $\mu_{\text{EFF}}$ varies by approximately a factor of two between the forward and backward DC $V_{GS}$ sweeps. However, when measured with a pulsed technique under vacuum, the error between the extracted $\mu_{\text{EFF}}$ between the forward and backward $V_{GS}$ sweep is reduced to less than 10% for the device with $d = 2.1$ nm and completely eliminated in the case of the device with $d = 1.7$ nm. The detailed MATLAB code for the mobility extraction is included as Appendix A. It is interesting to note the extracted $\mu_{\text{EFF}}$ from the pulsed measurement technique lies between the extracted $\mu_{\text{EFF}}$ from the forward and reverse DC sweeps. This indicates that coulombic scattering due to trapped charge has less of an effect on the $\mu_{\text{EFF}}$ than acoustic phonon scattering.

2.5 Conclusions

In conclusion, the dependence of hysteresis in the $I_{DS}$-$V_{GS}$ characteristics of CNTFETs at varying ambient conditions has been experimentally observed. Hysteresis in air and under vacuum conditions can be reduced by increasing $t_{\text{OFF}}$ of the $V_{GS}$ pulse. The relaxation time of the trapped charge, which affects hysteresis, is found to be $\approx 100$ ms. The effect of hysteresis on mobility extraction from the forward and backward DC $V_{GS}$ sweeps is determined, and it is shown that long pulse intervals at high temperature and under vacuum result in the extraction of a more consistent, “true” mobility value for CNTFETs.
### Table 2.1. Reported $\mu_h$ Values for CNTFETs

<table>
<thead>
<tr>
<th>Mobility</th>
<th>cm² V⁻¹ s⁻¹</th>
<th>$d$ (nm)</th>
<th>$L$ (μm)</th>
<th>$V_{GS}$ Sweep</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\mu_h$</td>
<td>Ballistic</td>
<td>3</td>
<td>0.3</td>
<td>PMMA Passivated</td>
<td>[8]</td>
</tr>
<tr>
<td></td>
<td>79,000 ± 8,000</td>
<td>3.9</td>
<td>325</td>
<td>Reverse</td>
<td>[1]</td>
</tr>
<tr>
<td></td>
<td>5,000 - 20,000</td>
<td>&lt;5</td>
<td>4000</td>
<td>NR</td>
<td>[9]</td>
</tr>
<tr>
<td></td>
<td>16,000</td>
<td>4</td>
<td>4</td>
<td>Forward</td>
<td>[2]</td>
</tr>
<tr>
<td></td>
<td>4,000</td>
<td>3</td>
<td>3</td>
<td>PMMA Passivated</td>
<td>[8]</td>
</tr>
<tr>
<td></td>
<td>2,500</td>
<td>1.5</td>
<td>10</td>
<td>Forward</td>
<td>[2]</td>
</tr>
<tr>
<td></td>
<td>1,000 - 4,000</td>
<td>1 to 4</td>
<td>1 to 3</td>
<td>Vacuum</td>
<td>[10]</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>1.6</td>
<td>0.3</td>
<td>NR</td>
<td>[11]</td>
</tr>
</tbody>
</table>
Figure 2.1: (A) Top view optical image of a typical nanotube device. Metal pads are Ti/Pd (0.5/40 nm). Nanotubes were grown by chemical vapor deposition using Fe catalyst on top of ~70 nm of SiO₂. The devices are back-gated with the highly doped (p+) Si wafer beneath. Semicircular electrodes are used for tighter control of nanotube device length. (Inset) SEM image of typical device (B) and schematic illustration of a device, with one active connection. The test configuration for electrical characterization is shown.
Figure 2.2: (A) Typical $I_{DS}-V_{GS}$ transfer curves for a device with diameter = 2.1 nm in air and (B) under vacuum conditions. $\Delta V_{TH}$ is defined as the difference between the forward sweep and reverse sweep $V_{TH}$. The hysteresis is always anticlockwise, indicative of charge trapping. (C) Typical $I_{DS}-V_{GS}$ transfer curves for a device with diameter = 1.7 nm in air and (D) under vacuum conditions. In all cases hysteresis is reduced by increasing $t_{OFF}$ of the applied $V_{GS}$ pulse.
Figure 2.3: (A) $\Delta V_{TH}$ from DC $V_{GS}$ sweep vs. CNT diameter and (B) $\Delta V_{TH}$ vs. normalized CNT length. No obvious $\Delta V_{TH}$ dependence is found on CNT diameter or CNT length.
Figure 2.4: (A) $\Delta V_{TH}$ vs. $t_{OFF}$ for the device in Fig. 2.2a at varying temperatures. At high temperature the rate of hysteresis reduction increases dramatically. At low temperature, for a different device (inset), hysteresis is found to be nearly constant at 1.5 V. (B) $\Delta V_{TH}$ vs. $t_{OFF}$ for the devices in Fig. 2.2a,b. Vacuum has a more pronounced effect of reducing hysteresis on the large-diameter device. In both (A) and (B) the rate of hysteresis reduction is greatest for $t_{OFF} > 100$ ms, indicative of the trap relaxation rates.
Figure 2.5: (A) Typical DC $I_{DS}-V_{GS}$ transfer curves for a device with diameter = 2.1 nm in air (dashed) pulsed $I_{DS}-V_{GS}$ and under vacuum conditions (solid). (B) Typical DC $I_{DS}-V_{GS}$ transfer curves for a device with diameter = 1.7 nm in air (dashed) and pulsed $I_{DS}-V_{GS}$ under vacuum conditions (solid). (C) Corresponding mobility extraction for the device in Fig. 2.5a. (D) Corresponding mobility extraction for the device in Fig. 2.5b. Rightward arrows indicate mobility extracted from the forward sweep, and leftward arrows indicate mobility extracted from the reverse $V_{GS}$ sweep. Solid arrows correspond to DC $V_{GS}$ sweeps, and open arrows correspond to pulsed $V_{GS}$ sweeps.
2.7 References


CHAPTER 3: PULSED ELECTRICAL BREAKDOWN OF CARBON NANOTUBE NETWORK TRANSISTORS

3.1 Carbon Nanotube Network Transistors

Random networks of single-wall carbon nanotube (CNT) films have been demonstrated as semiconductors for applications in small- to medium-scale integrated circuits on flexible or transparent substrates [1]. Typical mobilities can be of the order 20–40 cm²V⁻¹s⁻¹, up to two orders of magnitude greater than other conformal electron devices. Geometric striping of random network CNT films can enhance their on/off ratio by reducing metallic percolative pathways in the film [22]. Previous works suggest that current-induced defect formation, and oxidation induced by pulsed electrical stress, also selectively remove metallic pathways from CNT bundles and low-density CNT thin films [2, 3]. In this study, it is shown that pulsed electrical sorting of CNT thin films can be used to enhance the on/off ratios of random networks of CNTs to levels comparable with geometrically striped CNT thin films, without the need for additional process steps. This offers the possibility of reconfigurable integrated circuits on conformal substrates. Furthermore, this is the first report on the effects of high temperature and vacuum (10⁻⁵ Torr) ambient on CNT pulsed electrical burnout. The findings suggest that water-assisted oxidation is the dominant breakdown mechanism when electrically sorting CNTs under ambient conditions.
3.2 Experimental Setup

Figure 3.1 shows a schematic representation of the typical CNT devices considered in this work. The CNT films are grown from Fe catalyst using a chemical vapor deposition process at 900 °C. The CNTs are on 100 nm of SiO₂, exposed to the ambient environment from above, and back-gated with a highly doped (p⁺) Si substrate. Ti/Pd (1/40 nm) electrodes are patterned using standard lithographic techniques and deposited by electron beam evaporation. The CNT film is patterned by oxygen reactive ion etching (RIE) at 20 sccm, 100 mTorr, 100 W, for 45 seconds [4]. The devices have a channel width (W) of 1 mm and channel lengths (L) of ~15 µm, 20 µm, and 25 µm. Electrical measurements are performed using the Keithley 2612 dual-source measurement unit and the Keithley 4200 semiconductor characterization system. High-temperature measurements are made in air, with the substrate temperature controlled by a Signatone hot chuck. Vacuum measurements are made at room temperature using a Janis variable temperature probe station with pressure ~10⁻⁵ Torr.

The devices were stressed in cycles by applying a pulsed linear voltage sweep, $V_{DS} = 0$ to -40 V, under a constant gate bias, $V_{GS} = +15$ V. We note that as-grown semiconducting CNTs exposed to ambient are oxygen-doped and p-type [5]. These bias conditions reduce the probability that semiconducting CNTs conduct current during electrical stress under ambient conditions. The duty cycle ($t_{ON}$ vs. period $t_{ON} + t_{OFF}$) was held constant during each stress cycle at 50%. Initially, the pulse width was varied between 1 ms and 50 ms with increasing stress cycle. A stress cycle is defined as a completed pulsed linear $V_{DS}$ sweep. However, we found no significant difference on the
number of stress cycles required to electrically sort the CNT films when we held the pulse width constant at 45 ms for all applied stress cycles.

3.3 Improving the On/Off Ratio

Figure 3.2 shows an SEM image of the typical CNT density before (a) and after (b) electrical sorting. The circled area highlights the reduced density in the CNT film near the drain (negative) electrode. The lower density is a result of energy loss and Joule heating by the hole carriers to the lattice near the negative electrode. This raises the CNT film temperature more near the drain, resulting in Joule breakdown of metallic percolating pathways. We can estimate the temperature to be near 600 °C based on the oxidation temperature of CNTs under ambient conditions [6].

Figure 3.3 illustrates the transfer characteristics of a device with \( L \approx 15 \) µm before (solid line) and after (dashed line) pulsed electrical breakdown. The corresponding increase in the \( I_{\text{ON}}/I_{\text{OFF}} \) ratio is shown in Fig. 3.4 as a function of the applied stress cycle. We find the \( I_{\text{ON}}/I_{\text{OFF}} \) ratio increases from 30 to \( 2 \times 10^4 \), by three orders of magnitude. The Fig. 3.4 inset shows the corresponding \( I_{\text{ON,Fresh}} \) to \( I_{\text{ON,Stress}} \) ratio (ON-current before and after stress). The overall \( I_{\text{ON}} \) of the device is degraded by less than 50%. These results are comparable to those obtained by geometrically striping CNT networks with 2 µm wide stripes [1], but without the need for additional lithography or process steps. The poststress \( I_D-V_{DS} \) characteristics indicate the final saturation current is approximately 500 nA/µm channel width (Fig. 3.5).

Finally, we repeat our measurements in vacuum and at high temperature (100 °C) to analyze the effects of water vs. ambient oxygen on the pulsed electrical breakdown
effectiveness (Figs. 3.6 and 3.7). In both cases we find the $I_{ON}/I_{OFF}$ ratio decreases with increasing stress cycles. This suggests that water-assisted oxidation is the dominant breakdown mechanism of metallic pathways in randomly oriented CNT films under electrical stress and ambient conditions. While oxygen was naturally available for the high-temperature breakdown, water was removed from the SiO$_2$ surface both at high temperature and under vacuum conditions [5]. We also note that modification of the Schottky barrier height at the metal/nanotube junctions results from oxygen desorption at the contacts under vacuum conditions [5, 7]. Therefore, water removal and barrier height modification may change the conductive nature of the CNT film, adding to the inefficiencies of the CNT film breakdown under high-temperature and vacuum conditions [5, 7, 8].

3.4 Conclusions

In summary, this work represents the first systematic study of pulsed electrical breakdown of CNT thin films under varying ambient conditions. This technique increases the device $I_{ON}/I_{OFF}$ ratio by three orders of magnitude, while only showing a reduction in $I_{ON}$ of < 50%. These results are comparable to geometrically striping random CNT networks, which have been demonstrated as comparatively high-performance semiconductors for circuits on flexible substrates. Therefore, pulsed electrical stress of CNT thin films may enable advances in conformal consumer electronics, including reconfigurable medium-scale integrated circuits.
3.5 Figures

**Figure 3.1:** Schematic illustration of a three-terminal CNT network device used in the experiments. The terminal biases are as labeled, with $V_{GS}$ held constant at +15 V and $V_{DS}$ swept in a pulsed linear sweep from 0 to -40 V.

**Figure 3.2:** Scanning electron micrograph (SEM) illustrating typical CNT random film density (a) before pulsed electrical stress and (b) after pulsed electrical stress. The circled area highlights where film density is affected by breakdown.
Figure 3.3: Typical transfer characteristics for a device with $L \approx 15 \, \mu m$ before (solid) and after (dashed) pulsed electrical stress. The $I_{ON}/I_{OFF}$ ratio is increased by three orders of magnitude.

Figure 3.4: $I_{ON}/I_{OFF}$ ratio as a function of pulsed electrical stress sweep cycle for the device in Fig. 3.3. The $I_{ON}/I_{OFF}$ ratio is increased from 30 to $2 \times 10^4$. The corresponding degradation in the $I_{ON}$ (inset) is less than 50%.
Figure 3.5: $I_D-V_{DS}$ characteristics for the corresponding device in Figs. 3.3 and 3.4 following pulsed electrical stress of the CNT film. $V_{GS}$ is stepped from 0 to -20 V in -5 V increments. The maximum saturation current is approximately 500 nA/µm channel width.

Figure 3.6: $I_{ON}/I_{OFF}$ ratio vs. sweep cycle for a device of $L \approx 25$ µm. The stress is applied at $T = 100^\circ$C. The $I_{ON}/I_{OFF}$ ratio is decreased from 31 to 12. The corresponding $I_D-V_{GS}$ (inset) curves show an increase in $I_{OFF}$ following breakdown, likely due to a change in the doping of the film induced by water desorption [8].
Figure 3.7: $I_{ON}/I_{OFF}$ ratio vs. pulsed electrical stress sweep cycle for a device of $L \approx 25$ µm in vacuum ($\sim 10^{-5}$ Torr). The $I_{ON}/I_{OFF}$ ratio is decreased from 110 to 21. The corresponding $I_D-V_{GS}$ (inset) curves begin to exhibit an ambipolar behavior due to oxygen desorption at the contacts [7]. This change reduces the effectiveness of pulsed electrical stress.
3.6 References


CHAPTER 4: ELECTRICAL THERMOMETRY PLATFORM FOR CARBON NANOTUBE ARRAYS AND NETWORKS

4.1 Electrical Thermometry of Thin Films

Reducing power dissipation is a major challenge for the continued scaling of nanoelectronics. In the case of microprocessors, high clock frequencies and large transistor densities have increased power dissipation to approximately 100 Wcm\(^{-2}\). Future designs must now consider a joint electro-thermal design to limit or reduce power dissipation, or the heat generated will certainly affect device reliability. Therefore, a greater understanding of the fundamental physics governing heat flow at the nanoscale is needed to better engineer materials and devices which will facilitate the continuation of Moore’s law. Along the way, accurate metrology tools are also required to investigate the thermal properties of nanoscale films, interfaces, nanowires, and nanotubes.

In this work, the thermal properties of nanoscale thin films and carbon nanotube (CNT) networks are addressed. A simple yet versatile approach to measuring thermal properties at the nanoscale is by steady-state electrical thermometry. This method induces a temperature rise on one side of the sample by flowing current through a metallic heater, generating Joule heating. Temperature gradients across the sample are sensed by measuring calibrated changes in the resistance of a nearby metallic sensor. This technique has been used to measure the lateral thermal conductivity (\(\kappa\)) of suspended thin films for over two decades. Völklein’s experiment of measuring thin (<500 nm) bismuth films illustrated how suspending a sample enabled highly sensitive \(\kappa\) measurements of a conductive film by steady-state electrical thermometry [1]. In his experiment a low-\(\kappa\) organic foil (thickness, \(d = 40\) nm) was suspended between two copper electrodes. One
electrode acted as a Joule heater and the other as a heat sink. Heat flow in the direction of
the film thickness was confined by freely suspending the sample, and a constant
temperature ($T$) was assumed along the width of the sample. Heat flow was thus
restricted along the lateral direction, and a temperature rise across the sample was
extracted by monitoring calibrated changes in the resistance of the bismuth film.

Since then, advances in microfabrication technology have enabled the use of
suspended membranes and steady-state electrical thermometry to measure the lateral $\kappa$ of
various thin films, thin film stacks, and nanostructures. Typically, these suspended
thermal test structures use SiN membranes because of the robustness of the suspended
film even at ~100 nm thickness. This is attributed to its high tensile strength, which
allows it to be “stretched” over trenches etched into the Si substrate [2–7]. Other
microfabricated test structures have used thicker membranes (on the order of µm) with a
second film on top of the membrane for mechanical stability [8]. However, large
membrane thickness could be detrimental to measurements requiring high sensitivity.
Furthermore, microfabricated test structures have not utilized free-standing low-stress
SiO$_2$ films (<400 nm), which benefit from lower surface roughness than SiN films. Such
a thermometry platform could find applications in measuring the $\kappa$ of thin single-walled
CNT films—e.g., perfectly aligned CNT arrays that are grown on quartz substrates—but
cannot be transferred to SiN due to surface roughness (Fig. 4.1a).

### 4.2 Thermal Properties of CNTs and CNT Networks

CNTs and CNT films are of great interest in the scientific community as possible
solutions to reducing power dissipation in nanoelectronics. CNTs are a 1-dimensional
(1D) system with extraordinary electrical and thermal properties. They have the capability to carry approximately $10^9$ A cm$^{-2}$ current, and their thermal conductivity has been reported as high as 3500 Wm$^{-1}$K$^{-1}$ for individual freely suspended CNTs at room temperature [9]. However, when coupled with other CNTs the reported values of $\kappa$ are as low as 8 Wm$^{-1}$K$^{-1}$ for metal coated vertical arrays, and 35 Wm$^{-1}$K$^{-1}$ for randomly oriented films [10–12]. Values for perfectly aligned arrays (Fig. 4.1a) of CNTs have not yet been reported. Inter-tube coupling is thought to play a significant role in reducing the thermal conductivity of vertical arrays and random films (Fig. 4.1b), but this effect has also not been quantified experimentally in monolayer CNT films. Table 4.1 further emphasizes the wide range of thermal conductivities reported for various CNTs and CNT networks.

In this study, a measurement platform and technique with 0.001 K temperature resolution is developed to explore the thermal and mechanical coupling between CNTs and their dielectric environment. It is proposed this device can be applied to investigate the thermal properties of aligned CNT arrays and random CNT networks (Fig. 4.1a–c). Experimentally, the parallel arrays are grown on a quartz substrate and then transferred through a microcontact printing process onto a Si wafer with a thin (300 nm) SiO$_2$ top layer [13]. Metal heater and sensor strips are patterned on top, as shown, and the wafer is back-etched to suspend the SiO$_2$ membrane (Fig. 4.1c). A heating current (~200 µA) is passed through the middle electrode, while the temperature is sensed by monitoring calibrated changes in the electrical resistance of the two sensors. One side of the measurement platform provides the thermal conductance of the CNTs and substrate, while the other measures only the supporting substrate film. The effective thermal conductance of the CNT sample is thus obtained by subtraction. Comparison of the
parallel CNT arrays (Fig. 4.1a) can be made with randomly aligned CNT networks (Fig. 4.1b) and with deliberately imperfect (damaged) CNT films, which will elucidate the role of the nanostructure (dis)order on their thermal, electrical, and mechanical properties.

4.3 Electrical Thermometry Platform Fabrication Process

It is common for random networks and aligned arrays of CNTs to be grown by chemical vapor deposition (CVD) on thermal SiO$_2$ or sapphire substrates, respectively. The CNT arrays can then be transferred to thermal SiO$_2$ via a microcontact printing method [13]. However, the use of thermal SiO$_2$ as a membrane for a suspended electrical thermometry platform is problematic. A suspended membrane of thermally grown SiO$_2$ tends to warp from the large compressive stress in the film [14, 15]. Therefore, to achieve a “flat” membrane for thermal measurements of CNT films a low-stress SiO$_2$ film that is compatible with the transfer process is desirable. The fabrication for an electrical thermometry platform with such a film is described below.

**Step 1. Wafer preparation, etch stop layer, and low-stress SiO$_2$ deposition:** 275 ± 25 μm Si wafers were cleaned in a Piranha solution (5:1 H$_2$O$_2$ to H$_2$SO$_4$) at 120 °C for 15 min followed by a 5 min rinse in deionized water. The wafers were then dried under an N$_2$ flow, and the native oxide etched in a 10:1 buffered oxide etch (BOE) prior to atomic layer deposition (ALD) of a thin Al$_2$O$_3$ etch stop layer. A 5 nm layer of Al$_2$O$_3$ was deposited using a Cambridge Nanotech ALD system. The silicon wafer was heated to 250 °C in the reaction chamber, and trimethyl aluminum (TMA) and water vapor were pulsed into the chamber to deposit Al$_2$O$_3$ with atomic layer precision. Next, approximately 300 nm of SiO$_2$ was deposited using a Lesker PVD 75 sputter system. The system was
evacuated to a base pressure of $1 \times 10^{-6}$ Torr, and deposition was performed in a 5:1 Ar:O$_2$ environment. The sputtering pressure and power were held constant at 5 mTorr and 300 W respectively [16]. The substrate temperature was controlled by a quartz lamp and held at 200 °C during sputtering (Fig. 4.2a).

**Step 2. Electrode patterning and deposition:** The heater and sensor electrodes were patterned using standard lithographic techniques. NR5-8000 photo resist was spun onto the wafer at 3000 RPM for 30 s. Exposure was done through a bright field mask, and the patterns were developed using RD6 developer. The sample was then placed in electron-beam evaporators for deposition of 20 nm of SiO$_2$, 1 nm titanium (Ti), and 40 nm of palladium (Pd). Evaporators were evacuated to a base pressure of $8 \times 10^{-7}$ Torr before deposition. Liftoff was performed by placing the sample in Remover PG at 80 °C. A similar lithographic process was performed to increase the metal thickness of the pads and heat sinks to 300 nm. The extra thickness on the pads aided in wirebonding but also served as a spacer for the device active region during backside processing (Fig. 4.2b).

**Step 3. Backside patterning and membrane suspension:** Prior to backside processing, the topside structures of the wafer were protected by applying a thin layer of photoresist. The backside was patterned by spin-coating NR5-8000 at 3000 RPM for 40 s. Alignment to topside features was done using an infrared (IR) through-wafer backside alignment tool. Backside patterns were developed using RD6 developer. The wafer was attached to a carrier wafer for backside etching in an anisotropic deep silicon etching system. A Bosch 2 process was used to etch completely through the wafer. Both wafers were immersed in solvent, releasing the sample and suspending the SiO$_2$ membrane (Fig. 4.2c). A schematic cross section of the final device structure is shown in Fig. 4.2d.
4.4 Fabrication and Measurement Results

Film stress was measured using a FSM 500TC film stress measurement system, and surface roughness was measured by atomic force microscopy (AFM) (Fig. 4.3a–c). Results for the stress and surface roughness, $R_q$, of sputtered SiO$_2$ films are compared to thermal SiO$_2$ in Table 4.2. The stress in sputtered SiO$_2$ without a 5 nm Al$_2$O$_3$ etch stop layer is negligible compared to thermal oxide. However, the $R_q$ is too high for transfer printing of CNT films. The stress in sputtered SiO$_2$ with a 5 nm Al$_2$O$_3$ etch stop layer is 5 times lower than that in thermal SiO$_2$, and the low $R_q$ is as good as that of thermal SiO$_2$. The high selectivity of the Bosch2 process for Si over Al$_2$O$_3$ facilitates increased yield in the process. The Al$_2$O$_3$ prevents any etching of the thin SiO$_2$ membrane, which could occur as a result of variance in the wafer thickness. Therefore, thermal analysis of this film stack is detailed in subsequent paragraphs.

The heater and sensor of the device under test (DUT) were wirebonded to a Kyocera leaded ceramic chip carrier, prior to being placed in a Janis vacuum probe station for measurement. The probe station is capable of reaching vacuum levels down to $10^{-5}$ Torr and has a temperature range of 25 – 650 K. The experimental setup is shown in Fig. 4.4. The heater and sensor resistances were calibrated as a function of temperature from 200 K to 400 K (Fig. 4.5). This was done using a 4-point Delta Mode technique and the Keithley 6221/2182A current source and nanovoltmeter combo. When power was applied to the heater, resistance of the sensor was monitored by a 4-point Delta Mode technique, and heater power was monitored with a 4-point current-voltage measurement using a Keithley 4200-SCS. The ambient temperature is controlled with a Lakeshore model 377 temperature controller. Because our measurements are done under vacuum,
heat loss due to convection is negligible. The maximum heat loss due to radiation is approximately 5% at 400 K.

Heat flow in the direction of the film thickness is confined by suspending the membrane, and the 10:1 aspect ratio of the device allows for the assumption of a constant $T$ along the width of the membrane. Hence, the temperature variation due to conduction can be approximated by a 1D problem. Fourier’s law for heat conduction in 1D is

$$q = -\kappa \frac{dT}{dx}$$

(4.1)

The heat flux, $q$, depends only on the $\kappa$ and temperature profile along the length of the membrane. Solving for $\kappa$:

$$\kappa = \frac{\dot{Q} \Delta x}{A \Delta T}$$

(4.2)

where $\dot{Q}$ is the power supplied to the center electrode by Joule heating, $A$ is the cross sectional area for heat flow, $\Delta x$ is the membrane length between the heater and sensor, and $\Delta T$ is the temperature difference between heater and sensor.

Simultaneously measuring both the temperature of heater and the sensor with 0.001 K resolution requires a rather complicated and expensive experimental setup. A simpler alternative approach is to monitor the electrical resistance of the sensor as a function of the power applied to the heater, $R_{\text{EL}}(P)$ [17]. If this is done with nanovolt sensitivity, the temperature of the sensor, $T_{\text{SENSOR}}$, can be extracted from the calibrated electrical resistance, $R_{\text{EL}}(T)$, with mK resolution. After measurements, $R_{\text{EL}}(T)$ and $R_{\text{EL}}(P)$ are both known. Therefore, the thermal resistance of the membrane can be found by the chain rule:
\[
\frac{dR_{EL}}{dP} = \frac{dR_{EL}}{dT_{SENSOR}} \frac{dT_{SENSOR}}{dP} = \alpha R_{TH} \tag{4.3}
\]

The results of this measurement are shown in Fig. 4.6 for varying ambient temperatures. The relationship found for \(R_{EL}(T)\) is of the quadratic form:

\[
R_{EL}(T) = -1.4 \times 10^{-3} T^2 + 2.9T + 5.4 \times 10^2 \tag{4.4}
\]

\(T_{SENSOR}\) can then be found by solving for the roots of (4.4) with the quadratic formula.

The results for the \(T_{SENSOR}\) calculations as a function of heater power are shown in Fig. 4.7. The slope of the linear fits corresponds to \(R_{TH}\) for the varying ambient temperatures.

Using \(R_{TH}\) and the membrane dimensions for 1D heat flow, \(\kappa\) can be expressed as:

\[
\kappa = G_{TH} \frac{\Delta x}{A} \approx \frac{1}{R_{TH} \frac{\Delta x}{A}} \tag{4.5}
\]

Dimensions for the DUT’s width and length are obtained by scanning electron microscopy (SEM). The distance between the heater and thermometer is 21.7 µm. The membrane width is 1.04 mm. The film thickness measured by ellipsometry after step 1 in the fabrication process is approximately 320 nm. Using these dimensions, the value for \(\kappa\) is \(\approx 0.43 \text{ Wm}^{-1}\text{K}^{-1}\) at 200 K. The equivalent thermal circuit is schematically illustrated in Fig. 4.8. The DUT was designed so the sensor electrodes were positioned halfway between the heater and the suspended membrane edge. This allows for the approximation that \(R_{TH}\) of the four membrane segments \((R_{TH1–4})\) are equal.

The value of \(\kappa\) increases about 16% over the temperature range from 200 K to 400 K (Fig. 4.9). This trend is typical for amorphous materials and is in good agreement with previous studies of SiO\(_2\) thin films [18]. The trend can be explained using the simple kinetic theory:
\[ \kappa = \frac{1}{3} C \nu \Lambda \]  

where \( C \) is the volumetric heat capacity, \( \nu \) is the phonon group velocity, and \( \Lambda \) is the mean free path between phonon scattering events. In an amorphous material the \( \nu \) and \( \Lambda \) are nearly constant for the temperature range of our measurement. Therefore, the slight increase of \( C \) with temperature dominates the temperature dependence of the SiO\(_2\) thermal conductivity. The low \( \kappa \) of the suspended RF-sputtered SiO\(_2\) membrane as compared to thermally grown SiO\(_2\) is attributed to the higher porosity of the film and is in agreement with previous results for evaporated and sputtered SiO\(_2\) [19].

### 4.5 Conclusions and Application to CNT Networks

The fabrication and measurement of an electrical thermometry platform for thermal characterization of CNT thin films has been successfully demonstrated. Using sputtered SiO\(_2\), the stress in the film is reduced by a factor of 5 while maintaining surface roughness below 0.6 nm. Furthermore, the measurement setup and methods to extract the thermal conductivity of the suspended membrane have been demonstrated. A value of \( \kappa = 0.45 \text{ Wm}^{-1}\text{K}^{-1} \) at 300 K was obtained, in agreement with previous measurements of thin SiO\(_2\) films on bulk Si. Incorporating CNT films into this device can be accomplished by transfer printing CNTs to the substrate after step 1 in the fabrication process. Additionally, a lithographic step between steps 2 and 3 allows CNT films to be patterned in an O\(_2\) plasma between the heater and an edge sensor (Fig. 4.10 a,b). Etching is done in an RIE chamber at 100 W, 100 mTorr, 20 sccm of O\(_2\), for 45 seconds. The expected higher \( \kappa \) of the CNT film will lower the \( R_{\text{TH}} \) between the heater and edge sensor, \( R_{\text{TH}2} \) or \( R_{\text{TH}3} \) (Fig. 4.8). Therefore, the experimentally measured \( \kappa \) can be obtained as previously
shown, and the substrate effects can be subtracted by comparing measurement results for both sensors of the electrical thermometry platform.

In addition to thermal measurements of CNT random films and CNT aligned arrays, this platform may be used to measure the lateral $\kappa$ of graphene. Graphene is a 2-dimensional form of carbon with excellent electrical and thermal properties, which may help reduce power dissipation in future nanoelectronics. Its planar structure makes it an attractive material for integration into Si planar processing. With minor modifications this platform may also be used to measure electrical transport in CNT thin-film transistors (TFTs) (Fig. 4.10c). Because of their high mobility, as compared to poly-Si, CNT TFTs are an attractive device for use in applications such as displays and flexible electronics.
4.6 Tables and Figures

Table 4.1. Reported Thermal Conductivity Values for CNTs and CNT Networks

<table>
<thead>
<tr>
<th>Material</th>
<th>$\kappa$ (Wm$^{-1}$K$^{-1}$)</th>
<th>Refs.</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNT film</td>
<td>30-35</td>
<td>[10, 11]</td>
</tr>
<tr>
<td>Aligned CNT ropes</td>
<td>220</td>
<td>[20]</td>
</tr>
<tr>
<td>MWCNT* film</td>
<td>15–25</td>
<td>[21, 22]</td>
</tr>
<tr>
<td>MWCNT film (after correction)</td>
<td>200</td>
<td>[21]</td>
</tr>
<tr>
<td>MWCNT aligned sheets</td>
<td>50 (∥)</td>
<td>[23]</td>
</tr>
<tr>
<td></td>
<td>2.1 (⊥)</td>
<td></td>
</tr>
<tr>
<td>MWCNT rope</td>
<td>26</td>
<td>[23]</td>
</tr>
<tr>
<td>Individual MWCNT</td>
<td>550–3000</td>
<td>[24, 25]</td>
</tr>
<tr>
<td>Individual CNT</td>
<td>2000–10,000</td>
<td>[26, 27]</td>
</tr>
<tr>
<td></td>
<td>3500</td>
<td>[9]</td>
</tr>
<tr>
<td>Metal-coated vertical CNT array</td>
<td>8</td>
<td>[12]</td>
</tr>
</tbody>
</table>

*Multi-walled carbon nanotube (MWCNT)

Table 4.2. Film Stress Measurements for SiO$_2$ Films

<table>
<thead>
<tr>
<th>SiO$_2$ Film</th>
<th>$t_{ox}$ (nm)</th>
<th>Stress (MPa)</th>
<th>$R_q$(nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal (Dry)</td>
<td>280</td>
<td>-290</td>
<td>0.571</td>
</tr>
<tr>
<td>Sputtered 100 °C</td>
<td>320</td>
<td>11</td>
<td>0.691</td>
</tr>
<tr>
<td>Sputtered* 200 °C</td>
<td>320</td>
<td>-53</td>
<td>0.591</td>
</tr>
</tbody>
</table>

(*on 5nm Al$_2$O$_3$)
Figure 4.1: (a) SEM image of aligned CNT array grown on quartz, (b) SEM of random CNT network grown on amorphous SiO$_2$ (c) Optical image of fabricated test structure, with three heater-thermometer strips; CNT samples are patterned on SiO$_2$ membrane between the middle heater and an edge thermometer, later suspended with a back-etch.
Figure 4.2 (a–c): Schematic images of device fabrication process (d) schematic of final device.
Figure 4.3: (a) AFM image of sputtered SiO₂ surface, (b) AFM image of thermally grown SiO₂ surface, (c) height profile of sputtered SiO₂ compared to thermally grown SiO₂. Surface roughness is roughly equivalent.
Figure 4.4: Experimental setup and equipment for differential electrical thermometry of suspended SiO$_2$ and CNT thin films.

Figure 4.5: Temperature calibration of sensor and heater electrodes. Equation (4.4) results from a quadratic fit to the data, and is used to extract the sensor temperature as a function of heater power.
Figure 4.6: Electrical measurement of $R_{EL}$ as a function of heater power. The arrow indicates increasing ambient temperature from 200 to 400 K in steps of 20 K.

Figure 4.7: Extraction of $T_{SENSOR}$ as a function of heater power. The arrow indicates increased ambient temperature from 200 to 400 K in steps of 20 K. The slopes of the linear fits are equal to the $R_{TH}$ of the suspended membrane at the corresponding ambient temperature.
Figure 4.8: Schematic illustration of equivalent thermal circuit. Red arrows indicate direction of heat flow by conduction.

Figure 4.9: Comparison of $\kappa$ values for bulk thermal SiO$_2$ (red solid squares)[19], 1.5 µm magnetron sputtered SiO$_2$ (magenta right-facing triangles) [28], 2.18 µm reactive evaporated SiO$_2$ (down-facing black triangles)[28], 200 nm suspended thermal SiO$_2$ (open squares)[29], and 320 nm thermal SiO$_2$ (red x) and 270 nm evaporated SiO$_2$ (black x) on bulk Si [18]. The open blue circles are the values for this work.
Figure 4.10: (a) SEM and (b) Optical image of a device with a random film of CNTs patterned by O₂ plasma between the heater and an edge sensor. (c) Schematic illustration of a CNT TFT with a highly doped Si back-gate.
4.7 References


CHAPTER 5: CONCLUSION

In this study, the hysteretic behavior of the $I_{DS}$–$V_{GS}$ characteristics of CNTFETs at varying ambient conditions has been experimentally investigated through pulsed measurement techniques. It was found that hysteresis in air and under vacuum conditions can be reduced by increasing $t_{OFF}$ of the $V_{GS}$ pulse. Furthermore, the trap relaxation rate affecting hysteresis is found to be $\approx 100$ ms. It was shown hysteresis results in a factor-of-two disagreement on mobility extractions from the forward and backward DC $V_{GS}$ sweeps. It is also shown that long pulse intervals at high temperature and under vacuum result in the extraction of a more consistent, “true” mobility value for CNTFETs.

A systematic study of pulsed electrical breakdown of CNT thin films under varying ambient conditions is also presented. It is shown that this technique increases the device $I_{ON}/I_{OFF}$ ratio by three orders of magnitude, while only showing a reduction in $I_{ON}$ of $< 50\%$. The enhancement of the $I_{ON}/I_{OFF}$ ratio is comparable to results obtained by geometrically striping random CNT networks, which have been demonstrated as comparatively high-performance semiconductors for circuits on flexible substrates. However, work remains to be done to enhance the device saturation currents and extract the device mobility. If these device parameters are also comparable to results obtained by geometrically striping CNT networks, pulsed electrical stress of CNT thin films may enable advances in conformal consumer electronics, including reconfigurable medium-scale integrated circuits.

The fabrication and measurement of an electrical thermometry platform for thermal characterization of CNT thin films has been successfully demonstrated. Using
sputtered SiO₂, the stress in the film is reduced by a factor of 5 while maintaining surface roughness below 0.6 nm. Furthermore, the measurement setup and methods to extract the thermal conductivity of the suspended membrane have been demonstrated. A value of $\kappa = 0.45$ Wm⁻¹K⁻¹ at 300 K was obtained, in agreement with previous measurements of thin SiO₂ films on bulk Si. Incorporating CNT films into this device is also discussed.

In addition to electrical and thermal measurements of CNTFETs and CNT networks, the techniques and platform described herein may also find applications to graphene. Graphene is a 2-dimensional form of carbon with excellent electrical and thermal properties, which may help reduce power dissipation in future nanoelectronics. Its planar structure makes it an attractive material for integration into Si planar processing. Hysteretic behavior is common in the characteristic Dirac curves of graphene transistors, percolating networks of graphene nanoribbons (GNRs) may have metallic pathways due to edge states, and the lateral $\kappa$ of graphene measured by steady-state electrical thermometry has yet to be reported.
APPENDIX A: CNTFET MOBILITY EXTRACTION

%MATLAB Code:
qC = 1.602e-19;          % C
hbar = 6.582e-16;        % eV.s
G0 = 4*qC/(2*pi*hbar);   % G0 = 4*q^2/h, four nanotube channels
%
dname = '7-4';
tname = 'd=1.7 nm, L=2.6 um, Rc=100 kOhms';
d=1.7e-9;
L=2.6e-6;
RLowbias=100e3;    %From Id-VGS plot, VDS/ION
lambdaAC=280*d;
Ro=6.5e3*((L+lambdaAC)/lambdaAC); %Intrinsic CNT Resistance
Rc=RLowbias-Ro;

eps_ox = 2.2;          % Wunnicke "effective" result
eps_0 = 8.854e-12;     % F/m
tox = 70e-9;           % nm --> m
Cp = 2*pi*eps_ox*eps_0/acosh(tox/d);

chip='R4';
device = '7-4';

temp = '23C';
sweep = 'forward';

VDD = 50; %[-50 -20 -10 10 20 50];     % mV
% for iv = 1:length(VDD),
  Vds = VDD;
%
  Toff = [0 10000];       % ms [Array for multiple extractions]
  for it = 1:2,
    T = Toff(it);
    directory = strcat('Z:\David Estrada\Data\PulsedID-VG\',chip,'\',device,'\',temp,'\mobility\forward\');
    lpwd = pwd;
    cd(directory);
    fname =
    cat(2,'IDVG',dname,'_vd',num2str(Vds),'mV_',num2str(T),'ms.txt');
    %idvg = dimread(fname,'\t',[1 0 200 1]);%RANGE = [R1 C1 R2 C2]
where (R1,C1) is the upper-left corner of
%the data to be read and (R2,C2) is the lower-right corner

%Forward Sweep
idvg=load(fname);
id = idvg(:,2);
vgs = idvg(:,1);
smoothid = smooth(id(:,1),5); % use floor(dpoints/2) instead
of dpoints to take out reverse sweep
Gd = smoothid/(Vds*1e-3);       % convert mV --> V
Gd0 = Gd./(1-Gd*Rc);      % "intrinsic" Gd0 without Rc
ith = find(abs(Gd0/G0) < 0.0007);
%ith = find(abs(id) < 1e-8);
Vth = vg(min(ith)) % + vg(max(ith))/2;

igd = find((vg-Vth+4) > 0);
GG(it) = (Gd(min(igd)) + Gd(max(igd)))/2;

mobEF = 1e4*(L/Cp)*Gd0./(Vth-vg);
N1=(Cp/qC*(Vth-vg)/1e9);

%Reverse Sweep
directory2 = strcat('Z:\David Estrada\Data\PulsedID-VG\',chip,'\',device,'\',temp,'\mobility\backward\');

cd(directory2);

directory2 = strcat('Z:\David Estrada\Data\PulsedID-VG\',chip,'\',device,'\',temp,'\mobility\backward\');

fname2 = cat(2,'IDVG',dname,'_vd',num2str(Vds),'mV_',num2str(T),'ms.txt');
idvgb = dlmread(fname2,'	',[1 0 200 1]);
idvgb=load(fname2);
id2 = idvgb(:,2);
v2 = idvgb(:,1);
smoothid2 = smooth(id2(:,1),5);       % convert mV --> V

Gd2 = smoothid2/(Vds*1e-3);       % convert mV --> V
Gd02 = Gd2./(1-Gd2*Rc);      % "intrinsic" Gd0 without Rc

ith2 = find(abs(Gd02/G0) < 0.0007);

Vth2 = vg2(min(ith2)) % + vg(max(ith2))/2;

DeltaVth=Vth2-Vth

igd2 = find((vg2-Vth2+4) > 0);
GG2(it) = (Gd2(min(igd2)) + Gd2(max(igd2)))/2;

N2=(Cp/qC*(Vth2-vg2)/1e9);

%         %mobFE = 1e4*(L/Cp)*abs(diffe(vg,smooth(Gd0,7)));   % cm2/V.s
%         %mobFE = 1e4*(L/Cp)*abs(movingslope(Gd0,5,2)./gradient(vg));

figure(currentfig+10)
hold all;
plot(Vth-vg,abs(Gd0/G0),'d-',Vth2-vg2,abs(Gd02/G0),'d-');

xlabel('|V_T| (V)'); ylabel('G (4q^2/h)');
axis([0 4 0 0.1])

figure(currentfig+11)
hold all;
plot(N1(1:3:end),mobEF(1:3:end),'->');
plot(N2(1:3:end),mobEF2(1:3:end),'-<');

xlabel('N (nm^(-1))'); ylabel('Mobility (cm^2/V.s)');
axis([0 2 0 10e3]);
grid on;
end

cd(lpwd);
## APPENDIX B: ELECTRICAL THERMOMETRY PLATFORM FABRICATION PROCESS

<table>
<thead>
<tr>
<th>Process Step</th>
<th>Equipment/Chemical</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Prepare p+ Si wafer with etch stop layer and supporting membrane</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Piranha clean</td>
<td>5:1 H₂O₂ to H₂SO₄</td>
<td>15 min @ 120 °C</td>
</tr>
<tr>
<td>Deposit alumina</td>
<td>ALD MNTL</td>
<td>Grow 5 nm of Al₂O₃</td>
</tr>
</tbody>
</table>
| Sputter SiO₂                           | Lesker sputter system (MNTL) | ● 300 W  
● 5 mTorr  
● 200 ºC Substrate temp.  
● 5:1 (Ar:O₂)  
● Sputter 3 hr  
(≈3200 Å) |

**Random network devices**

| Evaporate catalyst                     | CHA evaporator             | Evaporate 2–10 Å Fe on 300 nm SiO₂ covered wafer                      |
| High density CNT growth                | Attomate CVD system        | Use highdensityswnt_ethylene.rcp  
● Decrease ethylene to adjust density |

**SEM sample to verify growth**

**Array devices MASK: CNT TRANSFER GRID**

| Transfer mask lithography              | MNTL spinner and flood exposure tools  
● S1813 Positive Resist  
● MF 319 Developer | Spin HMDS at 3000 RPM for 30 s  
Spin S1813 at 3000 RPM for 30 s  
Softbake at 110 ºC for 60 s  
Expose 150 mJ/cm² |
<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>Develop in MF</td>
<td>319 ~40 s</td>
</tr>
<tr>
<td>-</td>
<td>Hardbake at 110 °C</td>
<td>for 60 s</td>
</tr>
<tr>
<td>Oxide etch</td>
<td>Buffered oxide etch: 10:1 NH₄F:HF</td>
<td>30 s (etch rate of 120 nm/min)</td>
</tr>
<tr>
<td>Evaporate 100 nm Au on donor substrate</td>
<td>Cooke Ebeam evaporation system (MRL)</td>
<td>20 min (slow rate for first 10 nm, then 20.5 Å/s @ 10⁻⁶Torr for the next 90 nm)</td>
</tr>
<tr>
<td>Spin on PVA to donor substrate</td>
<td>MRL wafer spinners</td>
<td>25% wt, 1500 RPM 60 s</td>
</tr>
<tr>
<td>Softbake PVA</td>
<td>MRL hot plate</td>
<td>80 °C, 3 min</td>
</tr>
<tr>
<td>Transfer array with PDMS stamp</td>
<td>MRL clean room</td>
<td>5 min</td>
</tr>
<tr>
<td>Remove PVA residue</td>
<td>MRL clean room</td>
<td>DI drip, 1 min</td>
</tr>
<tr>
<td>Au droplet etch</td>
<td>MRL clean room</td>
<td>KI₂-based etchant</td>
</tr>
<tr>
<td>Step</td>
<td>Description</td>
<td>Equipment/Settings</td>
</tr>
<tr>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>Evaporate 100 nm Au on donor substrate</td>
<td>Cooke Ebeam evaporation system (MRL)</td>
</tr>
<tr>
<td></td>
<td>20 min (slow rate for first 10 nm, then 20.5 Å/s @ 10^-6 Torr for the next 90 nm)</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Spin on PI to donor substrate</td>
<td>MRL wafer spinners</td>
</tr>
<tr>
<td></td>
<td>25% wt, 3000 RPM 60 s Tape edges</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Transfer array with PDMS stamp</td>
<td>MRL clean room</td>
</tr>
<tr>
<td></td>
<td>5 min</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>Remove PVA residue</td>
<td>MRL clean room</td>
</tr>
<tr>
<td></td>
<td>DI drip, 1 min</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Au droplet etch</td>
<td>MRL clean room</td>
</tr>
<tr>
<td></td>
<td>3 min</td>
<td>KI₂-based etchant</td>
</tr>
<tr>
<td>6</td>
<td>SEM sample to check for quality of transfer</td>
<td></td>
</tr>
</tbody>
</table>

**Horizontal CNT array transfer method 2 (used in lieu of method 1)**

**MASK:**

<table>
<thead>
<tr>
<th>Electrode patterning/SiO₂ insulator</th>
<th>Electrode lithography</th>
<th>MNTL hotplate</th>
<th>150 °C for at least 5 min</th>
</tr>
</thead>
</table>

**SEM sample to check for quality of transfer**
<table>
<thead>
<tr>
<th>Step</th>
<th>Process</th>
<th>Equipment</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Spin on NR5-8000</td>
<td>MNTL spinner</td>
<td>• 3000 RPM for 40 s</td>
<td></td>
</tr>
<tr>
<td>Softbake</td>
<td>MNTL hot plate</td>
<td>• 150 °C for 60 s</td>
<td></td>
</tr>
<tr>
<td>Exposure</td>
<td>MNTL Quintel Aligner (24 s) MNMS (19.4 mJ for 30 s)</td>
<td>• 180 mJ dose</td>
<td></td>
</tr>
<tr>
<td>Post-exposure bake</td>
<td>MNTL hot plate</td>
<td>• 100 °C for 60 s</td>
<td></td>
</tr>
<tr>
<td>Develop</td>
<td>RD6</td>
<td>• ~120 s (by inspection)</td>
<td></td>
</tr>
<tr>
<td>Post-development bake</td>
<td>MNTL hot plate</td>
<td>• 60 °C for 120 s (if desired—check edge bead hardness)</td>
<td></td>
</tr>
</tbody>
</table>

For Thermal Test Structures

<table>
<thead>
<tr>
<th>Process</th>
<th>Equipment</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Evaporate SiO₂</td>
<td>MNTL Denton evaporator</td>
<td>8 × 10⁻⁷ Torr, 2 Å/s, 100 – 200 nm</td>
</tr>
<tr>
<td>Evaporate Ti/PD or Ti/Au electrodes</td>
<td>Cooke evaporator</td>
<td>8 × 10⁻⁷ Torr 1 nm/40 nm</td>
</tr>
<tr>
<td>Step</td>
<td>Process</td>
<td>Equipment</td>
</tr>
<tr>
<td>------</td>
<td>---------</td>
<td>-----------</td>
</tr>
<tr>
<td>Liftoff</td>
<td>Remover PG</td>
<td></td>
</tr>
<tr>
<td>Leakage current</td>
<td>Keithley 4200</td>
<td>Measure leakage between heater and thermometers</td>
</tr>
<tr>
<td>Bake out</td>
<td>MNTL hot plate</td>
<td></td>
</tr>
<tr>
<td>MASK 3 : Pads</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Spin on NR5-8000</td>
<td>MNTL Spinner</td>
<td></td>
</tr>
<tr>
<td>Soft Bake</td>
<td>MNTL hot plate</td>
<td></td>
</tr>
<tr>
<td>Exposure</td>
<td>MNTL Quintel Aligner (24 s) MNMS (19.4 mJ for 30 s)</td>
<td></td>
</tr>
<tr>
<td>Post-exposure bake</td>
<td>MNTL hot plate</td>
<td></td>
</tr>
<tr>
<td>Develop</td>
<td>RD6</td>
<td></td>
</tr>
<tr>
<td>Step</td>
<td>Equipment/Methodology</td>
<td>Conditions/Notes</td>
</tr>
<tr>
<td>-------------------------------------------</td>
<td>---------------------------------------------------------------------------------------</td>
<td>-------------------------------------------</td>
</tr>
<tr>
<td>Post-development bake</td>
<td>MNTL hot plate</td>
<td>• 60 °C for 120 s (if desired—check edge bead hardness)</td>
</tr>
<tr>
<td>Evaporate Pd pads</td>
<td>Cooke evaporator</td>
<td>260 nm</td>
</tr>
<tr>
<td>Liftoff</td>
<td>Shipley 1165</td>
<td>• 80 °C for ~40 min</td>
</tr>
<tr>
<td>MASK 3: Pattern CNTs</td>
<td>MNTL Spinner and Quintel Aligner AZ5214 AZ327 Developer</td>
<td>• Bakeout 115 °C for 2 min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Spin AZ 5214 at 3000 RPM for 30 s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Softbake at 110 °C for 60 s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Expose 110 mJ/cm² (15 s)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Develop ~40 s in 327 MIF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Post-bake 110 °C for 2 min</td>
</tr>
<tr>
<td>O₂ RIE</td>
<td>MNTL Plasma Therm RIE system</td>
<td>~45 s @ 20 sccm O₂, 100 mTorr, 100 W (22%)</td>
</tr>
<tr>
<td>Rinse</td>
<td>Acetone</td>
<td></td>
</tr>
<tr>
<td>MASK 4: Backside Preparation</td>
<td>MNTL Spinner and Quintel Aligner PMGI SF6 S1813 Positive Resist MF 319 Developer</td>
<td>• Bakeout 200 °C for at least 2 min</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Spin PMGI SF6 at 5000 rpm for 30 s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Post-bake 175</td>
</tr>
<tr>
<td>Step Description</td>
<td>Equipment Details</td>
<td>Temperature and Duration</td>
</tr>
<tr>
<td>------------------------------------------</td>
<td>----------------------------------------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>Backside PR Bake-out</td>
<td>MNTL hot plate</td>
<td>150 °C for at least 5 min</td>
</tr>
<tr>
<td>Spin on NR5-8000</td>
<td>MNTL Spinner</td>
<td>3000 rpm for 40 s</td>
</tr>
<tr>
<td>Softbake</td>
<td>MNTL hot plate</td>
<td>150 °C for 60 s</td>
</tr>
<tr>
<td>Exposure</td>
<td>MNTL Quintel Aligner MNMS (19.4 mJ for 25 s)</td>
<td>180 mJ dose (MNTL 41 s)</td>
</tr>
<tr>
<td>Post-exposure bake</td>
<td>MNTL hot plate</td>
<td>100 °C for 60 s</td>
</tr>
<tr>
<td>Develop</td>
<td>RD6</td>
<td>~120 s (by inspection)</td>
</tr>
<tr>
<td>Post-development bake</td>
<td>MNTL hot plate</td>
<td>60 °C for 120 s (if desired—check edge bead hardness)</td>
</tr>
<tr>
<td>Attach sample to carrier wafer</td>
<td>MNTL Spinner S1813</td>
<td>Coat carrier wafer with S1813, Spin 3000 rpm for 30 s</td>
</tr>
</tbody>
</table>
- Place sample (topside down) onto carrier wafer immediately following PR deposition
- Apply pressure for 1 min

<table>
<thead>
<tr>
<th>Bake</th>
<th>MNTL hot plate</th>
<th>90 °C for 2 min</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Backside etch</th>
<th>MNTL STS-ICP</th>
<th>Bosch-2 process etch—number of cycles to be determined by inspection (check after first 25, then every 50)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>- Use Jayclee2 recipe</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Etch 12 s</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Passivate 7 s</td>
</tr>
</tbody>
</table>