TRANSIENT PHASE CHANGE EFFECT IN PHASE CHANGE MEMORY DEVICES

BY

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DISSERTATION
Submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical and Computer Engineering in the Graduate College of the University of Illinois at Urbana-Champaign, 2010

Urbana, Illinois

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Abstract

Phase change random access memory (PCRAM) is a leading contender for next generation non-volatile memory. The phase change mechanism from high resistance amorphous phase to low resistance crystalline phase in nano-timescale is the most important characteristic of these materials. However, full understanding of the mechanism is still not achieved.

Two time parameters were identified from the transient waveform, namely the delay and current recovery times. The link between crystallization kinetics and the transient phase change effect was established by associating nucleation with delay time and growth with current recovery time. Real-time crystallization characterization was achieved.

Parasitic capacitance had strong implications on the programming performance of PCRAM. Larger parasitic capacitance results in a larger leakage current, and hence higher applied voltage for RESET operation needs to be applied. The larger parasitic capacitance also results in an increased quenching time due to a longer voltage fall time, which results in a partially crystallized amorphous state.

Continuing work is studying the effect of filament formation on phase change. Filament formation is linked to the actual operating performance of the PCRAM device. This link is important in understanding how phase change occurs electrically and whether filament formation has any effect on scaling of PCRAM devices.
Acknowledgments

I would like to thank A*star and Data Storage Institute (DSI) for their support of my PhD work. I would like to thank my advisers at DSI, Prof. Chong Tow Chong, Dr. Shi Luping and Dr. Zhao Rong, for their constant guidance and selfless contribution to this thesis. I would like to highlight discussions with Dr. Li Minghua and Mr. Lim Kian Guan, without which my understanding of this topic would be much less. I thank Prof. Ilesanmi Adesida, my adviser at UIUC, who despite his busy schedule makes time to discuss my progress toward my PhD. I would like to highlight much help from Miss Laurie Fisher, who I have inconvenienced many times because of my research work in Singapore. Lastly and most importantly, I would like to thank my family for being there when times are difficult, especially my wife for her support and my late mother for guiding me in spirit.
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Chapter 1

Introduction

1.1 Phase Change Memory Origins

Phase change materials have come a long way from the works of Ovshinsky to their applications in optical media and to current research in non-volatile memory devices [1]. Phase-change random access memory (PCRAM) was proposed by S.R. Ovshinsky, founder of Energy Conversion Devices Inc (ECD). The early devices had poor operating performances due to the high power consumption. The discovery of germanium-antimony-tellurium (GeSbTe) alloys was a breakthrough in PCRAM technology as phase change memory now needed less time and power to function. This resulted in the success of the rewritable optical disk and created renewed interest in phase change memory.

There are currently three major types of electronic memories. Static random access memory (SRAM) is the fastest and is typically used in microprocessor caches. It is expensive and less dense than the others. Dynamic random access memory (DRAM), though slower than SRAM, is cheaper and more dense. SRAM and DRAM both have the same disadvantage of being volatile, meaning that they will lose the data that they hold if power is switched off.
The non-volatile memory currently commercially available is Flash memory. Non-volatile means that the data would still be stored even if there is no power supplied to it. The non-volatile memory market is expected to grow much faster than the DRAM and SRAM market due to explosive growth in memory cards, handphones and memory sub-systems such as SoC (system-on-chip) and SiP (system-in-package). However, despite the high demand, there are still many problems with Flash memory. Flash memory is slow due to the erase sequences needed before writing data, resulting in writing time of at least one microsecond. Flash also begins to lose data after rewriting of around a million cycles. Furthermore, flash technology is hitting the physical limit of its scaling at about 45 nm, below which the oxide layer will break down resulting in tunneling. With so many fundamental limitations of flash memory, there is a search for the next generation non-volatile memory.

PCRAM is a leading contender for next generation non-volatile memory. It has many near ideal memory qualities such as non-volatility, fast switching speed, high endurance of more than $10^{13}$ read–write cycles, non-destructive read, direct overwriting and long data retention time of more than 10 years [2]. Its unique advantage over Flash and other next generation memory contenders is its scalability. The programming current of PCRAM decreases as the size of the cell is scaled down [3]. Hence, its theoretical performance actually improves as the dimensions are scaled down. Flash and other memories such as magnetic random access memory (MRAM), in contrast, have poorer performance. This is a major advantage for PCRAM as it can technically scale with lithography.

PCRAM is based on chalcogenide alloys, which are alloys containing selenium or tellurium. They generally contain one or more elements from Group VI of the periodic table. Phase change materials can change from the amorphous state to crystalline state in nano-timescale. A short,
high amplitude electric pulse such that the material reaches melting point and is rapidly quenched changes the material from crystalline phase to amorphous phase and is widely termed as RESET current; a longer, low amplitude electric pulse such that the material reaches only the crystallization point and is given time to crystallize, allowing phase change from amorphous to crystalline, is known as SET current.

1.2 Motivation

The phase change mechanism from high resistance amorphous phase to low resistance crystalline phase in nano-timescale is the most important characteristic of these materials. Yet full understanding of this mechanism has not been achieved. Recently, much research [4,5] has focused on the material analysis of the phase change material in an attempt to explain the high speed switching of these materials.

The motivation of this work is to study the phase change phenomenon from a transient study perspective. Looking into the kinetics of how phase change occurs, Ovshinsky found that there was a time gap between application of the pulse and current increase of the phase change material, which he attributed to nucleation and growth [6]. Despite the many years of research in phase change materials, understanding of the phase change mechanism is still not complete. In recent work by Kang et al. [7], work was done on the actual kinetics of the SET process and they related the voltage waveform to threshold switching, nucleation and growth. We believe a focus on the transient effect in the nanoseconds during phase change of the material can give insight into the actual mechanism of phase change.
1.3 Organization

This study is divided into six chapters. Chapter 1 gives a brief introduction to PCRAM and current research. It also outlines the problem involved. Chapter 2 shows the experimental setup and the device fabricated to investigate the problem. Chapter 3 shows the transient method that was used to study the phase change memory device. This method was then used to study scaling in these devices and also the physical model of phase change. Chapter 4 shows the effect of parasitic capacitance on the operating performance of phase change memory devices, adding another dimension to the transient phase change effect. Chapter 5 outlines the study of the filament size study in phase change memory devices and where future work will be done. Chapter 6 concludes the work and outlines future areas of study in transient analysis.
1.4 References


Chapter 2

Phase Change Memory Fundamentals

There is an intensive search for a next-generation nonvolatile memory due to the scaling limitations of flash memory. Phase change random access memory (PCRAM) is one such candidate with the most potential due to its many good memory characteristics. The reversible phase change between the high resistance amorphous state (RESET) and the low resistance crystalline state (SET) can be achieved by a current or voltage pulse at nanosecond timescale. For commercial viability, high density and high speed are crucial for PCRAM. Both can be achieved due to the high scalability of PCRAM. Phase change materials have two important characteristics, namely, threshold switching and phase change.
2.1 Phase Change Materials Characteristics

Phase change materials can change from the amorphous state to crystalline state in nanotimescale. The amorphous state means the atoms are arranged in a disorderly manner while in the crystalline phase the atoms are orderly. The disordered amorphous phase has many boundaries that absorb light and scatter electrons, resulting in high resistivity and low reflectivity, while the crystalline state has lower resistivity and higher reflectivity. These differences in resistivity and reflectivity have been applied in phase change memory and optical media respectively. A short, high amplitude electric pulse, such that the material reaches melting point and is rapidly quenched, changes the material from crystalline phase to amorphous phase and is widely termed as RESET current; a longer, low amplitude electric pulse such that the material reaches only the crystallization point and is given time to crystallize, allowing phase change from amorphous to crystalline, is known as SET current. The two currents are plotted in Figure 1. Due to the requirement of the RESET pulse, it is typically higher than the SET pulse and this sets a minimum current required for PCRAM operation.
There are two important characteristics of phase change materials: threshold switching and phase change. Threshold switching occurs when the programming voltage increases beyond the threshold voltage. Looking at the IV plot, it can be seen that in the amorphous state, current is very low at low voltage until a point which is called the threshold voltage is reached. The amorphous semiconductor now goes from a high resistive state to a conductive state, with a concurrent rapid increase in current after the voltage snapback. The material is now in the amorphous "ON" state, where the material is still amorphous, but in a pseudo-crystalline electric state. This mechanism was hypothesized to be related to impact ionization [1]. There is much debate about whether threshold switching is electrical or thermal in nature, and it was found that, at least in thin films, threshold switching is electrical [2].

The phase transformation kinetics can be illustrated on a time-temperature-transformation diagram as shown in Figure 2. This diagram shows how two contrasting factors, atom mobility and temperature dependency for reaction. At high temperatures near the melting point, the nucleation driving force is small but the atom mobility is large. This results in slow crystallization. Similarly, at low temperatures, the nucleation driving force is large but the atom mobility is small, which also results in slow crystallization. The highest crystallization rate is thus seen at an intermediate temperature termed the nose temperature, where both driving force and atom mobility are moderately high. Therefore, crystallization can be achieved most efficiently by heating the material to the nose temperature for some time so atoms have enough time to arrange themselves in an orderly manner. Reamorphization can only occur by heating the material to above melting point and quenching it faster than the material’s cooling time, which is typically the line that just touches the C shaped crystallization region as shown in the diagram.
The phase change mechanism from high resistance amorphous phase to low resistance crystalline phase in nano-timescale is the most important characteristic of these materials. Much research has focused on the material analysis of the phase change material in an attempt to explain the high speed switching of these materials as seen in Figure 3. In its stable state, crystalline Ge$_2$Sb$_2$Te$_5$ has two possible configurations: hexagonal and a metastable face centered cubic (FCC) lattice. When it is rapidly crystallized, however, it was found to have a distorted rock salt structure. It was later hypothesized from density functional theory (DFT) simulations that the
most stable amorphous state was the spinel structure, where Ge occupies tetrahedral positions and Sb and Te occupy octahedral positions, as the ground state energy was the lowest of all the possible configurations [3]. The small change in configuration from distorted rock salt to spinel suggests that nano-timescale phase change is possible. The most common phase change compound used is the GeSbTe group of compounds, which is shown in Figure 4. There is a pseudo-line where the most commonly used GeSbTe compounds are found. Moving down this pseudo-line, melting point and glass transition temperature increase, and crystallization time increases. Therefore, switching speed decreases while concurrently the stability of the crystalline state increases. This roadmap of phase change materials gives a whole range of phase change materials for which the requirements could be adjusted. For example, if higher stability or data retention is required, Ge rich phase change materials would be considered. Similarly, if high speed and low power are required, Sb rich phase change materials are considered.

Other than just working with this set of phase change materials, doping of these phase change materials was also considered. The idea behind doping is to introduce impurities in the material and thereby lower its melting point. This correspondingly results in lowering of the RESET pulse required for reamorphization. For example, programming current was lowered up to 40% for PCRAM with bismuth (Bi) doped GeSbTe compared to those with other GeSbTe compounds [4].
Phase change in these phase change materials was shown to be due to initial nucleation to form seed nuclei and then growth of these nuclei. Phase change materials can be characterized into two types, nucleation dominated and growth dominated [5]. If the nucleation rate is higher than its growth rate, this material is nucleation dominated and if vice versa, it is growth dominated. The mechanism by which crystallization occurs in optical media differs for the two types of phase change materials. For nucleation dominated materials, the nucleus will form in the center of the amorphous region and grow out. For growth dominated materials, the crystalline background will grow into the amorphous region as shown in Figure 5 [6].
Figure 5  The difference between nucleation and growth dominated phase change materials in optical media [7].

In optical media, the reflectivity changes during phase change were used to distinguish nucleation dominated materials from growth dominated materials. The nucleation dominated materials upon heating will have a longer incubation period before a short growth period while growth dominated materials will have a relatively short incubation period before a longer growth period. This is demonstrated in Figure 6.

Figure 6 Difference between nucleation and growth dominated phase change materials in reflectivity studies.
The electronic band diagram of crystalline and amorphous GeSbTe has been previously modeled as shown in Figure 7 [1]. In amorphous GeSbTe, the lone pair of electrons in Te results in the Urbach tail of the valence band. The donor-acceptor defect pairs are modeled as two levels of donor-like and acceptor-like traps close to the conduction and valence bands respectively. Also, the presence of structural vacancies results in acceptor-like traps that are present in the crystalline state.

The presence of these traps could be used to explain the Fermi level pinning effect seen in phase change materials [8]. This is illustrated in Figure 8. In the steady state equilibrium, donor acceptor defect pairs are equal in concentration. When the electric field is applied, the Fermi energy increases due to bias change or electron injection. This has the effect of neutralizing the ionized donors. This changes the level of the ionized donors, which would result in the ionizing of the neutral acceptors. This would then result in an increase in the density of ionized acceptors and the Fermi energy being pulled back to near its original level.
2.2 Previous Transient Study

S. R. Ovshinsky did the first work on transient study of phase change when he noticed a time difference between application of voltage and current increase as shown in Figure 9 [9]. The effect was associated with nucleation of the phase change material. The mechanism would be different for nucleation and growth dominated phase change materials. For the nucleation dominated mechanism, the crystalline nuclei would start to form upon application of the pulse. As more nuclei are formed over time, there would be a rapid growth phase which would join up
the individual nuclei to form the crystalline state. For growth dominated mechanism, seed nuclei would be formed and would grow bigger and bigger during the growth phase such that they join up and result in a crystalline phase.

Figure 10 Change in RC time delay as applied voltage is increased for SET operation for Ge₁Sb₂Te₄ device.

More recent research on the transient effect has tried to explain this phenomenon. It was found that the RC delay time decreased as the applied voltage was increased [10]. This is seen in Figure 10. It was hypothesized that the presence of this capacitance is due to the charged defects that are present in phase change materials. Under an external electric field, these defects would be lined up to contribute to the capacitance of the chalcogenide. Under increasing electric field, carrier generation is enhanced but the population of defects could be reduced faster by recombination processes, which explains the drop in RC time delay.
2.3 Device Scaling

Writing current is determined by the bottom electrode size because the heat generated is directly dependent on current density. Reduced contact size increases local current density and hence joule heating. A lower RESET current would then be needed to achieve the temperature required. Thus, the aim is to achieve the minimum amount of phase change material that can reliably undergo a phase transition. The smaller the programmable volume, the less power needed to heat up that volume and hence less programming current. This scaling capability is an important asset of the PCRAM as it allows the technology to be scaled for multiple generations. It can be seen from Figure 11 [11] that as the cell size is scaled down to the 50 nm range, the pulse width decreases to the pico-second range.
A possible problem during scaling is proximity disturbance when, as the size of the cells are reduced, there is a possibility that the heat from one cell could affect another in close proximity, due to the small size, and affect the reliability of the cell. This was shown to be not a problem [12] as there is no significant thermal influence at the 65 nm range and the reset current is scaled down almost linearly with the contact area. However, it was found that the smaller contact process is not reliable and demonstrated abnormal resistance distribution from $10^3 \, \Omega$ to $10^5 \, \Omega$ in 60% of the cells. Thus, reducing the bottom electrode size is effective only to a certain extent as it would affect the reliability of the phase change.

Work on scaling was done on thin film phase change materials and it was found that crystallization temperature increases while the thickness of $\text{Ge}_2\text{Sb}_2\text{Te}_5$ film decreases from 20 to 5 °C [13] as seen from Figure 12, while the melting point would decrease. Therefore, as the devices scaled down, the operation window of phase change would decrease as the difference between crystallization and melting point decreased.

![Figure 12 Crystallization temperature dependence of Ge$_2$Sb$_2$Te$_5$ film thickness at heating rate of 3°C/min](image)

Figure 12 Crystallization temperature dependence of Ge$_2$Sb$_2$Te$_5$ film thickness at heating rate of 3°C/min [10].


2.4 Device Fabrication and Setup

A simple device to test the phase change material was fabricated. The device structure is as shown in Figure 13. The phase change material used is Ge$_2$Sb$_2$Te$_5$, which is known for its thermal stability [14] and long lifetime [15]. There is a contact area of 1 μm from the TiW electrodes to the material. The dielectric layers are for better insulation to make the programming current in a suitable fixed testing range. The Ge$_2$Sb$_2$Te$_5$ was covered with 10 nm of TiW to reduce oxidation of the material. Photoresist used was PFI-26A and lithography was done using a Canon stepper system. The materials are sputtered using a Balzers cube sputtering system.

![Figure 13 Structure of phase change device fabricated.](image)

A testing circuit was set up as shown in Figure 14. A constant voltage is generated by the pulse generator and passed through the circuit. The current through the circuit is tracked by taping the current that passes through the resistor in series with the device. The voltage across the device is then calculated by subtracting the voltage from the pulse generator from the voltage across the series resistor. Passive probes are used as they have high resistances of 10 MΩ and hence more accurate measurement can be obtained compared to using an active probe.
Figure 14 Testing circuit for PCRAM device.
2.5 References


Chapter 3

Transient Analysis of PCRAM

The transient current waveform during a crystallization process revealed two important time parameters which were termed as delay time and current recovery time. A link between this transient phase change effect and its crystallization kinetics was established. The delay time was found to be the minimum pulse duration before an onset of resistance change. The current recovery time was the time the device takes to complete its transition from high resistance to low resistance. Real-time crystallization characterization was applied to demonstrate the differences between nucleation and growth dominated materials used in the devices. This method was then applied to study scaling effects in phase change devices and it was found that scaling not only lowers the programming current requirement, but also increases the phase change speed of the device. This suggests that high density and high speed phase change memory devices through scaling are achievable. This transient method would be an important analysis technique of novel phase change devices and materials.

Publications:
3.1 Development of Transient Analysis

Figure 15 Transient current and voltage waveforms during crystallization showing the two important time periods.

An interesting phenomenon was observed in the transient electric effect of the pulse passing through the phase change device during SET operation as shown in Figure 15. A RESET pulse with width of 40 ns and amplitude of 4 V and a SET pulse with width of 400 ns and amplitude 2 V were initially used for the device. The transient current increases initially with the application of the voltage pulse. After an initial surge in current, current starts decreasing exponentially with a concurrent increase in the voltage across the device. A certain time is reached when the current drops to a certain minimum, which is termed as delay time. Current then starts increasing very quickly until it settles at a certain plateau, which is termed as the current recovery time. There is a need to check if this waveform is actually due to the phase change material and not due to the testing circuit. The first test was to reduce the pulse width to check if the delay time drops. It was found that when the pulse is reduced, the delay time remains the same. This is shown in Figure 16 where the oscilloscope screen captures show that reducing the pulse to times longer than the delay time had no effect on the phase change process of the
device. This suggests that the delay time is related to the device and material characteristics rather than pulse length.

Figure 16 Oscilloscope data showing the decrease in pulse length having no effect on delay time.

The second test is the effect of read-write cycles on the delay time as shown in Figure 17. It can be seen that as the number of read-write cycles increases, the delay time drops. This has many implications. First it is clear that the drop in current is not due to the heating up of the material. If this is so, then it should not change with increased number of read-write cycles. Secondly, this is not a circuit phenomenon as it should be constant with increased read write cycles.
To determine whether this phenomenon was an artifact due to the test circuit, the same testing procedure was done using known resistors. Figure 18 shows the current waveform when a 10 kΩ resistor was connected. A square pulse was seen. This means that delay and current recovery times are specific to the device and not an artifact due to the test circuit.
The last test was to fabricate a test structure that is slightly different from the device under test to determine if it is due to the structure of the device. The test structure fabricated is shown in Figure 19. It can be seen that the structure is very similar and can be fabricated just by simple rotation of the masks to be used. Instead of the usual sequence, the phase change layer is first fabricated before the via is overlaid on top. The contact area remains at 1 μm diameter and it was found that there was no change to the transient effect observed. After all these tests, it could be said that this transient effect is a result of the phase change device and not because of the testing circuits and other effects.

It was also found that the delay time would increase when a lower voltage was applied. A plot of current waveforms at different voltages applied to the same device is shown in Figure 20. As seen from the current waveform using voltage of 1.6 V in Figure 21, the delay time is about 120
ns, which is longer than that of about 100 ns using 2 V in Figure 15. It can be seen that there is an exponential relationship between the delay time and the applied voltage.

Figure 20 Current waveforms at different applied voltages for a particular device.

Figure 21 Resistance changes and current waveforms of Ge2Sb2Te5 and AgInSbTe.

The current waveform was plotted with the steady state resistance plot in Figure 21. The significance of the delay and current recovery times can be seen from the steady state resistance plot. The plot was obtained by using pulses of different durations and measuring the resistance after the pulses with a low reading voltage of 0.2 V. From the figure, the initial drop in resistance
coincided with the delay time and the resistance only settled at a low value at the end of the current recovery time. Hence the delay time can be interpreted as the minimum SET pulse duration required for the device to begin phase change and it signifies the onset of resistance change. It is also easily measurable as reference is taken from the start of the pulse to the point when there is a sudden large increase in current. As seen from the figure, the current recovery time is the time the device takes to complete its transition from high resistance to low resistance, which represents the partial phase change period. Crystallization is only complete if the pulse duration is longer than the sum of the delay and current recovery time. If the pulse is longer than the delay time but shorter than the sum of the delay and current recovery time, the device is in a partial crystalline state. These two time parameters represent important periods of the phase change process and are easily identifiable.

Similar time parameters were also observed in reflectivity time measures during light induced phase change [1], namely the incubation and growth time. The incubation time refers to the time before reflectivity of the phase change material changes, while the growth time refers to the time period when reflectivity changes rapidly. Nucleation occurs during the incubation time where nuclei have to reach a critical size or density before growth takes place. During this time, there is little change in reflectivity. The reflection then increases rapidly, which is attributed to the growth of these nuclei until they coalesce [2]. Clearly, the measurement method using delay and current recovery time is very similar to the reflectivity time measures and relates to the nucleation and growth phases of crystallization correspondingly. The transient current waveform can therefore be explained by this nucleation and growth process that the chalcogenide goes through during phase change. During nucleation, the phase change material is still in the amorphous phase. Hence very little current flows through the phase change device. During the
growth period, the resistance changes rapidly such that the parasitic capacitor discharges, resulting in the initial current surge after the delay time. The current then remains stable when the material has completed phase change to the crystalline state. Hence, using the transient current waveform and the two time parameters, the link between the electrical characteristics and crystallization is established and the entire crystallization process can be characterized in real-time. Phase change materials are classified into two types, nucleation-dominated and growth-dominated [3]. If the nucleation rate is higher than its growth rate, this material is nucleation-dominated and if vice versa, it is growth-dominated. The above real-time transient measure with two time parameters can be applied to characterize crystallization in devices with two different types of phase change materials. AgInSbTe and Ge₂Sb₂Te₅ were studied here as they are the well-known growth-dominated and nucleation-dominated materials respectively. Figure 21 shows the transient measurement using the same SET pulse of 400 ns and amplitude of 1.6 V. AgInSbTe was found to have a much shorter delay time of around 50 ns compared to around 120 ns for Ge₂Sb₂Te₅ and a longer current recovery time of around 70 ns compared to around 50 ns for Ge₂Sb₂Te₅. These results indicate that Ge₂Sb₂Te₅ has a long nucleation period, followed by a relatively short growth period, while AgInSbTe tends to have a short nucleation and a relatively long growth period. This agrees with the observations from optical reflectivity measurements for these materials.

From Figure 21, it can also be seen that the steady-state resistance changes of the two materials just after delay time are very different. The partial crystalline states of AgInSbTe could hardly be seen in steady-state resistance measurements in contrast to those of Ge₂Sb₂Te₅. A possible reason could be the effect of explosive crystallization [4] in AgInSbTe. The heat of crystallization released by exothermic crystallization in these compounds would induce crystallization of the
surrounding amorphous regions. Hence the partial resistance states could not be observed in steady state.

Figure 22 (a) Delay time plot against voltage. (b) Current recovery plot against voltage.

A plot of the delay time and current recovery time against different applied voltages is shown in Figure 22 for both materials. It can be seen that delay time for Ge$_2$Sb$_2$Te$_5$ is larger than that for AgInSbTe while current recovery time for AgInSbTe is larger than Ge$_2$Sb$_2$Te$_5$. This corresponds to Ge$_2$Sb$_2$Te$_5$ and AgInSbTe being nucleation and growth dominated materials respectively. Delay time decreases as applied voltage increases for both materials. The delay time for AgInSbTe is less dependent on the applied voltage than that for Ge$_2$Sb$_2$Te$_5$. 
3.2 Parasitic Capacitance

The observed current is the sum of the current through the phase change material and the parasitic capacitance, which arises from the device, contacts and testing equipment. The effect of the parasitic capacitance could be removed using the following equation [5]:

\[ I_{PC} = \frac{V_{total} - V_{1k}}{R_{1k}} - C_{parasitic} \frac{dV_{1k}}{dt} \]

where \( I_{PC} \) is the current flowing through the phase change material. The first term is the observed current and the second term is the contribution from the parasitic capacitance. The parasitic capacitance was estimated from the waveform. The waveform during the delay time resembles the waveform of an RC circuit. Hence, using \( I = I_0 e^{-t/RC} \), \( C \) could be estimated from the waveform. The leakage current through the parasitic capacitance could now be eliminated. The current flowing through the phase change material was isolated as shown in Figure 23. It can be clearly seen that the current during the delay time is small at around 0.3 mA and there is a sudden large increase in current to a peak of around 1.2 mA after the delay time. This was attributed to the discharge of the parasitic capacitor due to the resistance change of the phase change device. The current then settles at around 0.7 mA. The delay and current recovery time remain the same after removal of the parasitic capacitance effect. This parasitic capacitance effect was found to strongly affect the programming performance of the devices. This is discussed in further detail in the next chapter.
Figure 23 Resistance changes and current waveforms of Ge2Sb2Te5 and AgInSbTe after removal of parasitic capacitance effect.

In summary, two time parameters, the delay and current recovery times, were measured from the transient waveform, which provided the link between crystallization kinetics and the transient phase change effect. Real-time crystallization characterization was achieved. This transient measure with two time parameters has been used to identify the crystallization differences between nucleation and growth dominated materials. This allows for quantitative assessment of material and device engineering effects on crystallization in phase change memory.
3.3 Transient Analysis of Scaling

Figure 24 Transient current waveforms of three devices with different via size.

This transient measurement method was used to investigate the scaling effect on device performance where the phase change device is scaled down and analyzed based on its transient electrical waveforms. A RESET pulse with width of 40 ns and amplitude of 4 V and a SET pulse with width of 400 ns and amplitude 1.6 V were initially used for the device. From Figure 24, it could be seen that as the device is scaled down from 1 to 0.7 μm, the delay time decreases from about 200 ns to 100 ns for the same applied SET voltage of 1.6 V. The average delay times of three devices were found and plotted in Figure 25. It can be seen that as the device is scaled from 1 to 0.7 μm, the delay time drops by about 50%. This indicates that for the range of via size of the device studied here, scaling not only reduces the programming current required but also the pulse duration required. Since the delay time is related to the nucleation time, a shorter delay time means that nucleation time for a smaller device is shorter for the same applied voltage. This coincides with previous observations in nano-phase-change cells of correlation between phase transition speed and device dimensions [6]. This suggests that the volume of phase change material that changes phase is smaller. Hence, scaling not only lowers current requirement, but also increases the phase change speed of the device. Also, using higher current for larger devices could achieve the same delay time as using lower current with smaller devices. For example, a
1 μm device has a delay time of about 100 ns with an applied voltage of 2 V, which is similar to a 0.7 μm device with an applied voltage of 1.6 V.

![Figure 25 Variation of delay time with voltage for phase change devices as the device is scaled down from 1 to 0.7 μm.](image)

The current recovery time reduces from 50 to 30 ns as the device is scaled down from 1 to 0.7 μm as shown in Figure 26. The current recovery time was previously found to be closely associated with growth. As the device scales down in size, the phase change volume that changes phase reduces. This correspondingly reduces the time it takes for the phase change device to coalesce.

![Figure 26 Variation of current recovery time with voltage for phase change devices as the device is scaled down from 1 to 0.7 μm.](image)

The reduced nucleation and coalescing time could also be strongly influenced by increased interface effects as the volume decreases. Diffusion-limited crystallization [7] is observed in
phase change materials, which are typically alloys. As crystal size gets smaller, surface to volume ratio increases. The interfaces and dangling bonds increase the surface energy of the atoms. This increased surface energy could reduce the Gibbs free energy difference required for formation of a critical cluster for nucleation. This means the number of atoms with free energy higher than the critical energy would be larger and the rate of nucleation would increase.

### 3.4 Studying the Phase Change Physical Model

![Graph](image)

**Figure 27 Comparison of delay time for phase change devices with 50 and 100 nm of GST for different voltages.**

The flexibility of the transient measurement method is again shown in the study of the phase change physical model. There are currently studies [8] suggesting that phase change in PCRAM devices occurs by filament formation, which focuses the electric field. This phenomenon was studied using the transient analysis using devices with 100 nm of GeSbTe (100 nm device), which is double the previous device GeSbTe thickness. The delay times of the 100 nm devices were plotted against those with 50 nm of GeSbTe in Figure 27. The crystallization temperature of GeSbTe is not expected to differ significantly for film thicknesses larger than 20 nm [9]. The 100 nm devices had marginal increases of 10 ns in delay time at higher voltage of 2 V. At lower voltages of 1.6 V, the delay time increased more significantly from about 200 ns to 300 ns. Nonetheless, the increase in delay time is not double despite the doubling of GeSbTe thickness.
This suggests that the mechanism does not proceed only through simple nucleation. There seems to be a minimum delay time for the device to form a minimum crystalline region. From the data, the formation of the filament seems to be strongly correlated to the applied voltage. A large voltage means the crystalline filament would be formed much more quickly through the amorphous material than when a smaller voltage was used. This supports the hypothesis of filament formation during phase change in PCRAM devices. This suggests that filament formation is an important area in the study of phase change device mechanisms.
3.5 References


Chapter 4
Parasitic Capacitance

Parasitic capacitance was found to have strong implications for the programming performance of PCRAM devices due to increased scaling and high frequency operation. Larger parasitic capacitance was associated with higher applied voltage for RESET operation due to a larger leakage current. The quenching time was also increased due to a longer voltage fall time, which results in a partially crystallized amorphous state. This has negative implications for overwrite cycle performance. However, it allows for lower SET voltage. Multilevel devices could be implemented by varying the parasitic capacitance to achieve different amorphous resistance.

4.1 Study of Transient Effect and Parasitic Capacitance

For commercial viability, high density and high speed [1] are crucial for PCRAM. Both can be achieved due to the high scalability of PCRAM. As devices scale down, the parasitic capacitance of the devices is expected to increase due to the reduced dimensions. Hence, parasitic capacitance is expected to have an increasing influence on programming performance in the future. Also, high speed switching of PCRAM requires high frequency programming pulse operation. Parasitic capacitance has been shown in transistors [2] and other electrical circuits [3] to limit their high frequency performance.

It was shown in recent research [4] that parasitic capacitance plays a part in PCRAM RESET operation as it results in a current overshoot during threshold switching which causes melting of the active material. This is shown in Figure 28. Hence, parasitic capacitance is expected to play a significant part in the programming performance of future devices. However, the relationship between parasitic capacitance and programming performance has not been studied in detail. There is thus no way to determine the beneficial or detrimental effects, if any, of parasitic capacitance on future devices. This chapter is dedicated to this study and the relationship of parasitic capacitance to other working parameters of phase change memory such as read-write cycles.
During amorphization, a high amplitude electrical pulse of short duration is used to heat the crystalline phase change material to above the melting point before it is rapidly quenched to the amorphous state [5, 6]. Quenching time is crucial during RESET operation as it could affect RESET resistance distribution, with increasing quenching time resulting in RESET fluctuation [7]. This quenching time is directly related to the fall time of the voltage across the PCRAM device when the pulse is turned off, which in turn is determined by the parasitic capacitance of the device. There is therefore a possible link between parasitic capacitance of the device and the RESET and SET performance.

The parasitic capacitance measured from the PCRAM devices has many origins, such as the contact pad and the electrical circuits in the testing setup. In the work done, 9 µm of SiO₂ was deposited on the thermal oxide using plasma enhanced chemical vapor deposition in order to reduce the parasitic capacitance due to the contact pad, which is the result of substrate coupling [8].
Figure 29 (a) Structure of high-cap PCRAM device fabricated. (b) Structure of low-cap PCRAM device fabricated.

Figure 29(a) and (b) show the schematic cross-sections of the high-cap and low-cap devices used, respectively. The high-cap device has a thinner oxide layer below the contact while the low-cap device has a thicker oxide layer. Using this setup, the transient voltage when the pulse is switched off is:

\[ V = V_0 e^{-\left(\frac{t}{RC_p}\right)} \]

The effective resistance, \( R \), is the result of the PCRAM resistance and the 1 k\( \Omega \) resistor in parallel. \( R \) therefore can be assumed to be 1 k\( \Omega \) since the amorphous resistance of the PCRAM device is much larger than 1 k\( \Omega \). \( C_p \) refers to the parasitic capacitance of the PCRAM device, which is in parallel to the device. It can be deduced that the fall time of the voltage pulse could be directly affected by the parasitic capacitance of the PCRAM device. An increase in parasitic capacitance corresponds to an increase in voltage fall time and in turn, a longer quenching time. This longer quenching time could have direct consequences for the crystallinity of the amorphous phase change material, due to its metastability, and thus could strongly affect programming performance of the device.
Figure 30 Low-cap device having the same voltage across PCRAM with less applied voltage compared to the high-cap device.

The parasitic capacitance can be estimated from the RC time constant of the current waveform when a low voltage pulse is used. The natural log of the waveform is taken and the gradient can give us the estimated parasitic capacitance. This parasitic capacitance includes not just the substrate coupling effect from the pads but also those of the testing circuit and structure. However, the difference between the parasitic capacitance of the high-cap and the low-cap device must be due to the reduction of the substrate coupling effect due to the thicker oxide layer. The estimated parasitic capacitance of the high-cap device and the low-cap device were found to be 140 pF and 50 pF respectively.

The RESET programming performance was first studied. An initial RESET pulse of 40 ns, 3 V was applied during amorphization to both devices. There is a constant read voltage of 0.2 V also applied to obtain the real-time resistance of the device. The transient voltage of both devices was tracked and shown in Figure 30. It can clearly be seen that the voltage across the low-cap device is much higher than that across the high-cap device even though the applied voltage is the same. This suggests that the higher parasitic capacitance had introduced a current leakage path across
the PCRAM device, which results in a smaller voltage drop. The impedance of the parasitic capacitance is known to be:

\[ Z = \frac{1}{j\omega C_p} \]

where \( C_p \) is the parasitic capacitance and \( \omega \) is the testing frequency. During high frequency testing of the PCRAM devices, \( \omega \) is large and the reactance becomes small. This is similar to shorting the PCRAM device with impedance, \( 1/j\omega C \). The impedance of the high parasitic capacitance is thus smaller than that of the low parasitic capacitance. There is therefore a larger leakage current for the high-cap device because of the smaller impedance, and hence the voltage across the PCRAM is smaller for the same applied voltage. To achieve the same joule heating across the PCRAM device such that the temperature is above the melting point, the high-cap device would require higher applied voltage to drive the same amount of current through the PCRAM so as to make up for the larger leakage current. Figure 30 shows the voltage of the low-cap device when a voltage pulse of 40 ns, 2 V was applied. The voltage waveform is very similar to that of the high-cap device when a voltage pulse of 40 ns, 3 V was applied. Hence, by reducing the parasitic capacitance, the applied RESET pulse voltage could be reduced even though the actual voltage drop across the PCRAM devices remains the same. The difference is that there is less leakage current, meaning there is a larger voltage drop across the PCRAM device.

The parasitic capacitance difference introduced a more subtle difference between the two transient voltages. The transient voltages of the two devices after the 40 ns pulse was switched off have differences in the quench times. The quench time of the high-cap device is about 100 ns while that of the low-cap device is about 40 ns. The quench time could be related to the different parasitic capacitance of the devices. At the end of the pulse, the parasitic capacitor would
discharge and the discharge current would flow through the PCRAM. The high-cap device with its higher parasitic capacitance would have more charge stored and the discharge time would be longer than the low-cap device. This longer discharge time is due to the larger RC constant of the circuit. The longer discharge would mean that $V_{\text{PCRAM}}$ of the high-cap device would decay much slower than that of the low-cap device, resulting in a longer quench time. The longer quench time could have a strong relation to the different final amorphous states of the two devices. This is because reamorphization requires fast crystallization such that the atoms could be locked in the amorphous phase. The RESET resistances of the two devices were found to be different. The low-cap device was found to have an RESET resistance of about 10 MΩ while that of the high-cap device has a RESET resistance of 3 MΩ. There is now a need to test this hypothesis of the relationship between quenching time and discharge time.

4.2 Pulse Manipulation

This hypothesis was tested using innovative pulse manipulation from the pulse generator. Two low-cap devices were used in this test. The applied pulse was manipulated such that the pulse decayed exponentially to simulate the larger parasitic capacitance of the high-cap device, as shown in Figure 31. The decay time was set to 100 ns, which is similar to that of the high-cap device. The low-cap device has an original resistance of 10 MΩ. Using the manipulated pulse, the RESET resistance was about 2 MΩ using this longer quench time. Hence, it can be seen that the quenching time has a large effect on the final amorphous resistance of the phase change device. There is now a need to establish the relationship between quenching time and amorphous resistance of the device. Once established, the link between parasitic capacitance and programming performance can then be built up.
4.3 Simulation
Simulation of the devices was done using ANSYS software to determine the effects of quenching time on the crystalline state of the phase change device. The ANSYS software allows for simulation of applied voltage to a certain phase change device structure to determine the achieved temperature. The material characteristics required include the thermal conductivity, electrical conductivity and density.

The same device structure was built up as shown in Figure 32 and the peak temperature after application of the RESET pulse was 620 °C for both devices. The low-cap device was quenched
in 40 ns and the high-cap device in 100 ns as in the case of the actual devices. It can be seen that the temperature after quenching time of 40 ns is about 170 °C for the low-cap device and 360 °C for the high-cap device as shown in Figure 33. Therefore, there is a difference in the cooling rate during quenching which was hypothesized previously. This difference in cooling rate is related to the crystallinity of the phase change material. The Johnson-Mehl-Avrami (JMA) equations [9-11] describe the crystallization heat generated and can be used to calculate the crystalline fraction of the devices.

\[
\text{Fraction} = 1 - e^{-(bt_c)^n} \\
\]
\[
b = b_o e^{\frac{-E}{RT}}
\]

where \( b \) and \( b_o \) are nucleation frequencies, \( n \) is the Avrami parameter, \( E \) is the activation energy of crystallization, \( R \) is the gas constant, \( T \) is the temperature and \( t_c \) is the time after the temperature goes below the nose temperature. Frequency \( b_o \) was taken as \( 2^{22} \), \( n \) is 2.8 and \( E_a \) is 2.25 eV [12].
Figure 33 Temperature profiles of (a) low-cap device after 40 ns of cooling and (b) high-cap device after 40 ns of cooling.

The crystalline fraction refers to the ratio of crystalline grains mixed in the amorphous state. Using a melting temperature of 600 °C and a nose temperature of 550 °C, the crystalline fraction
of the devices could be plotted as shown in Figure 34. Taking the amorphous state as 0 and the crystalline state as 1[13], this means that the high-cap device would result in a more crystallized amorphous state than the low-cap device. This could be due to the longer quenching time which allows the atoms more time to get into the crystalline configuration. Yet this quenching time is not long enough for the crystalline nuclei to grow into a complete crystalline region. This results in an amorphous region with many crystalline domains within, which explains the lower RESET resistance observed in the high-cap device.
Figure 34 Crystallization profiles of the (a) low-cap device and (b) high-cap device.

4.4 SET Operation

Since lower parasitic capacitance means a higher voltage could be maintained across the PCRAM device, a lower parasitic capacitance was expected to also reduce the applied SET
voltage for crystallization. On the contrary, the low-cap device required a higher applied SET voltage of 1.2 V compared to that of the high-cap device, which requires 1 V as shown in Figure 35. The peaks in the transient SET voltage curves in Figure 35 demonstrate which devices crystallized and the SET pulse amplitude at which it did [14]. This difference in SET dynamics is highly unlikely to be due to the discharge of the parasitic capacitor as the time is short as compared to the pulse length. There is a possibility that the thermal profiles of the two devices could be different due to the different SiO₂ thickness, resulting in different performance. The thermal profiles of the two devices were also simulated as shown in Figure 36. It was found that the temperature profiles of the two active regions were similar and not changed significantly by the additional SiO₂ layer.

Figure 35 SET current waveforms of the low-cap and high-cap device showing phase change at 1 V for the high-cap device and 1.2 V for the low-cap device.
Figure 36 Thermal profiles of (a) low-cap device and (b) high-cap device showing that the maximum phase change temperature is the same and there is no thermal effect for SiO₂ thicker than 1 µm.

In view of this, it can be concluded that the partially crystallized amorphous state of the high-cap device has a large effect on the SET voltage required. The low-cap device is crystallizing from a
fully amorphous state of about 10 MΩ compared to the high-cap device’s partially crystallized amorphous state of 3 MΩ. A low-cap device with a partially crystallized amorphous state was achieved using the exponentially decaying RESET pulse mentioned earlier. Using this device, a SET voltage of 1 V could be achieved.

The partially crystallized amorphous state has more crystalline domains formed within, which suggests that crystallization time for the low-cap device would be shorter than that for the high-cap device during the SET process. The partial crystallized amorphous state could have implications for data retention of the device, though this is still under debate. There were previous models [15], which suggested that imperfect RESET could result in early failure of devices due to percolation paths by the crystalline domains within. Though recent research put the cause of failure on spontaneous generation of crystalline nuclei and grain growth [16], the effect of a partially crystallized RESET state on data retention time is believed to be negative.

Parasitic capacitance of the PCRAM devices was found to strongly influence the phase change dynamics of the RESET and SET pulses. A higher parasitic capacitance increases the RESET voltage required for amorphization due to a larger leakage current at high frequency. The amorphous state, however, becomes partially crystallized due to the longer quench time. This lowers the crystallization voltage required but could potentially reduce the data retention time of the devices. Parasitic capacitance could also potentially be used in multi-level PCRAM applications to control the RESET resistance.
4.5 References


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Chapter 5

Physical Model Study

Actual device operation of PCRAM is very different from optical media operation. Previous research highlighted the possibility of filament formation that made the nano-second timescale phase change possible. This continuing work tries to link the filament formation to the actual operating performance of the PCRAM device. The study of the filament’s role in PCRAM operation was made possible through the use of a transparent conductive oxide as a top electrode. This link could be important in understanding the scaling limitation of PCRAM and establish the link between filament formation and operating performance of the PCRAM device.
5.1 Filament Formation in PCRAM

Filament formation was first observed in PCRAM [1], where etching methods were used to reveal the filaments within after phase change. This method is destructive and does not allow for concurrent study and operation of the device and filament. Previous models used the effect of filaments to model how phase change occurs in PCRAM devices as shown in Figure 37. One recent model [2] suggests that after nucleation has created a crystalline shunt, phase change occurs rapidly due to the lowered activation energy.

![Figure 37](image)

**Figure 37** Two possible models for PCRAM phase change through filament formation. The first is a nucleation model to form a shunt while the other is a current analysis model.

Hence, it can be seen that phase change and filament formation are closely related, and the study of the relationship between the two will have important implications on the actual mechanism for phase change in a PCRAM device. The understanding of filament formation in PCRAM would then be crucial in the understanding of PCRAM operation and physics. First, filament formation dynamics could have similarities with the initialization process in phase change material in optical media. This could have performance issues during the initial use of PCRAM. Secondly, filament formation and position could have implications for the reliability, lifetime and performance of PCRAM devices. Lastly, filament study could open new techniques of phase change operation and could allow for a new field of phase change technology which would allow for different methods of phase change to be integrated.
5.2 Integration of ITO in PCRAM

In order to directly observe the filament in PCRAM in-situ, there are a few requirements. The filament must be seen easily and observed properly. Also, the observation of the filament should be non-destructive so that one can observe the filament under different conditions. This is a very important point as this allows study of the filament under different conditions in PCRAM devices. In this work, the plan is to use transparent conductive oxide (TCO) as an electrode for PCRAM and attempt to observe the filament. The TCO used is tin doped indium oxide (ITO). ITO was chosen as it is the most common TCO used. ITO is also widely used in modern electronic technology such as solar cells, light emitting diodes, liquid crystal displays, etc. Hence, ITO technology is very well studied which allows for easier integration with phase change memory. In ITO, high transparency and high conductivity are attained by creating electron degeneracy in a wide bandgap. This is done by introducing appropriate dopants, in this case Sn. The dopants replace the In atoms, resulting in the Sn atoms existing as SnO or SnO₂. The high transmittance of 90-95% means that the probability of seeing the filament increases. Also, the resistivity range is 2-8 Ωcm, which makes it suitable for an electrode. The high conductivity is due to high carrier concentration rather than high Hall mobility. The direct bandgap of ITO is reported to be around 3.5 to 4eV, which explains the high optical transmittance of the material. The ITO films were sputtered by reactive r.f. sputtering in an Ar plasma. The sputtering rate used was 6.8 nm per second using 3kW.

Integration of ITO with phase change material is a novel technique and there has been no known previous work done. There is thus a need to work through the integration process. The device was fabricated with TiW with both electrodes replaced by ITO contacts of the same thickness of 200 nm. The resultant device was tested and found to have problems reamorphizing. This was
hypothesized to be due to the heat conductivity of ITO being much less than that of TiW, which means the heat quenching rate is much slower for the ITO device than for the TiW device. The simulation was done in ANSYS by first simulating the TiW device and later replacing both electrodes with ITO. This is shown in Figure 38 and Figure 39 respectively. It can be seen that when both electrodes were replaced with ITO, the maximum attainable temperature was much higher than 624 °C attained in the TiW devices. This is probably due to the low thermal conductivity of ITO resulting in very slow quenching and very slow heat loss resulting in high temperature. Hence, the device was designed such that only the top electrode was changed to ITO as shown in Figure 40 since it is the crucial electrode that needs to be transparent. This will reduce the slow heat loss problem and probably allow for faster quenching. Secondly, the active area is in close contact with the bottom electrode and so the quenching rate is fast enough for reamorphization.

Figure 38 TiW device simulated with RESET pulse of 40 ns, 3 V showing peak temperature of 624 °C.
Figure 39 ITO device with both top and bottom electrode replaced with ITO showing much higher temperature attained and very slow quenching, which explains why this ITO device cannot switch.

Figure 40 ITO device with only top electrode replaced with ITO showing lower attainable temperature and faster quenching on the TiW side.
The top ITO device performs well and allows for reamorphization to occur. The PCRAM device could now be actively switched between amorphous and crystalline phase. An IV sweep of the device was done as shown in Figure 41. It can be seen that threshold switching occurred at 2.7 V. The general shape of the ITO device is similar to that of the TiW device, but the current at the amorphous ON phase is higher than that of the TiW device.

![Figure 41 IV curve of the ITO device.](image)

However, the problem is that no filament could be seen with the use of an optical microscope. It was then hypothesized that the contrast between the crystalline and amorphous states could not been seen due to the refraction through different thicknesses of ITO. Experiments were done on different thicknesses of ITO on GeSbTe to determine which ITO thickness would give the highest possible contrast between the crystalline and amorphous phase. Samples were made using different ITO thickness on GeSbTe and one sample was heated to crystallize the GeSbTe. The reflectivity difference between the amorphous and crystalline phases was found to be highest at 50 nm. Hence, the top electrode thickness was reduced to 50 nm from 200 nm.
5.3 Observation of Filament

After a SET pulse was applied, the device was observed under the microscope to determine if there are any filaments. However, as the area is 1 µm, the filament cannot be clearly determined in the optical microscope due to the small size. Hence, a device with a larger contact area of 5 µm was fabricated. Using this larger area, a different spot was seen as shown in Figure 42.

The spots were not seen before the application of the SET pulse. After the SET pulse, the resistance of the device decreased from 1000 kΩ to about 50-70 kΩ. There is now a need to verify that this change is actually the filament that was formed. The device was reamorphized using a high amplitude pulse and it was found that the contrast was much smaller than the previous case. This is shown in Figure 43. One can compare the reamorphized spot on the right with the crystallized spot on the left. Another interesting point is that the reamorphized spot is not the same as the as deposited material in the background. It could be measured from the picture that the spot is about 0.3 µm in the 5 µm square via. Also, another observation is that the
spots are generally formed at or near the corners of the via. These results lead to planning for the next stage of experiments to test the hypothesis formed based on these results.

Figure 43 Photo taken using optical microscope at 1500X magnification showing the right reamorphized cell in contrast with the left crystallized cell and the difference in optical contrast of the two spots.

5.4 Hypothesis Testing

Based on the previous results, the following hypotheses were put forward.

1. Size of filament
   a. Size of filament is dependent on contact area of the via
   b. Size of filament is dependent on programming voltage of the via

2. Position of filament
   a. Position of filament is usually at the corners of the via
   b. Position of filament is independent of the corners of the via

To test the hypotheses formed, different masks were designed for layer 2 as shown in Figure 44 and Figure 45, which is the part which forms the via of the device. Different vias were designed to study the contact area.
Figure 44 Mask design for the via of the 8 bit cell with different square areas.

Figure 45 Mask designs for the vias of the 16 bit cell with different shapes.
For the 8 cell design, 4 different sizes of via from 1 to 4 µm were fabricated. This would allow testing of the size of the filament with respect to the different via sizes. For the 16 cell design, different shapes were used to determine the effect of corners on the position of the filament. The first shape is a 3 µm diameter circle. The second is a square of about 1 µm per side. The next two are rectangles with contact areas of 3 µm² and 4 µm², respectively. The fifth is an isosceles triangle with area of 2 µm². The sixth is an equilateral triangle with an equivalent area of a circle with diameter of 1 µm. The seventh is an equilateral triangle with an equivalent area of a circle with 2 µm diameter while the eighth is an equilateral triangle with an equivalent area of a circle with 3 µm diameter.

The experiment was first done on the 8 cell device. The typical RESET pulse used was 100 ns, 3.5 V, and the typical SET pulse used was 800 ns, 1.5 V. The programming currents required are longer and of higher amplitude compared to that of the TiW device. However, upon observation under the microscope, there was no filament observed. It is possible that the pulse applied could be too small to produce a filament that is observable under the optical microscope. Therefore, a large pulse of 10 V with duration of 5 s was applied to make a “large” filament. The large pulse produced a large spot that is seen easily on the microscope as seen in Figure 46. It was then thought that this is the filament and that now the sizes could be compared. The same reamorphization test was applied to the spot to check if it “disappears” upon reamorphization. It was found surprisingly, that the spot does not disappear even though the resistance increases. There are two possible explanations for this. One is that there was reamorphization but it does not cover the whole filament since the pulse used is a short pulse. There are some problems with this argument. Firstly, if the whole filament is not totally reamorphized, then the resistance should still be low, as current would flow through the lowest resistance path. Secondly, it could
be seen that the spots produced were slightly different from those produced earlier. It could be seen that the earlier spots had bright and faint outlines, but those that were produced now had dark outlines that were very clear. These two points suggest that the large pulses could have additional implications other than just making the filaments larger. The second conclusion is that the observed spot is not due to the phase change material and is due to other materials, most obviously ITO. This is the conclusion that seems more reasonable and experiments are designed to test this conclusion.

The most obvious solution is to use focused ion beam (FIB) to remove the specific section of interest and get a transmission electron microscope (TEM) image to determine what the specific cross-section is. However, efforts to get this image have been futile as the phase change material is very heat sensitive and during FIB the material would have been damaged significantly to see any crystalline filament that was possibly originally there. The next more complicated solution would be to etch the ITO to see exactly what is in the phase change material itself.

Figure 46 Filament formed after application of 5 s, 10 V pulse in 1 and 4 µm devices.
5.5 ITO Etching

According to the literature on ITO etching, the typical etchants used on ITO are hydrofluoric acid (HF) and concentrated hydrochloric acid (HCl). HF etching on ITO is reportedly unstable and uneven and it is more dangerous to use than HCl [3]. Hence, in this experiment, HCl will be used. The 34% mol HCl is diluted with a 1:1 ratio with water to get 17% mol HCl. During the etching test, it was found that the deposited ITO was etched very rapidly despite literature showing the rate to be in the 10 nm/min range [3]. Further research into the literature showed that HCl etched amorphous ITO so rapidly that it is indeterminate [4]. As such, the film was annealed at 250 °C for 1 h and it was found that the etching rate is 3.1 nm/min. This film was then sent to an x-ray diffraction (XRD) machine to verify if the ITO film is crystalline after annealing. It can be seen from Figure 47 that the peaks correspond to previously done experiments on crystalline ITO.

![Figure 47 XRD analysis of ITO film after annealing for 1 h at 250 °C showing the crystalline peaks of ITO.](image)

The top ITO was removed and it was found that the spot could still be seen on the microscope as seen in Figure 48. An atomic force microscope (AFM) scan was done and it was found that the
spot is a small dome of 0.3 μm diameter, about 50 nm high, and of unknown material. This is shown in Figure 49. A 3-D scan using the AFM showing the diameter of about 0.3 μm is shown in Figure 50. This sample was analyzed using energy-dispersive X-ray spectroscopy (EDX) and the result is shown in Figure 51. The dome was analyzed and compared to a spot in the via, not on the dome which is shown in Figure 52. It was found that the dome is ITO as the EDX data show indium and tin present in the dome but not on the other spot.

Figure 48 Device after etching amorphous ITO. It can be seen that the ITO layer is gone while the dome and the GeSbTe layer remain.
Figure 49 AFM scan showing the vertical height of the dome being about 65 nm.

Figure 50 3D scan showing the dome left after etching of the amorphous ITO.
Figure 51 EDX analysis done showing presence of indium and tin confirming the ITO dome.

Figure 52 EDX analysis of a spot in the via beside the dome showing no indium.
From the evidence seen, it could be concluded that the ITO could have crystallized during the phase change process generated by the pulse. The heat generated during phase change could have resulted in an ITO dome formed on top of the phase change crystalline filament. In fact, the sample was sent for further etching such that the crystalline dome was removed. It was found that a 0.3 \( \mu \text{m} \) diameter layer of about 50 nm was left from the AFM scan in Figure 53 and the GeSbTe layer was etched away by HCl. This 0.3 \( \mu \text{m} \) diameter layer was found to contain Ge as shown in Figure 54 which means it is the GeSbTe layer.

HCl was found previously to etch GeSbTe [5]. Etching of amorphous material is in general much faster than that of crystalline material. Therefore it is possible that HCl had etched the amorphous GeSbTe, leaving the crystalline shunt. This was verified when EDX analysis found traces of GeSbTe at that spot, further supporting the shunt theory.

Figure 53 AFM scan of the spot after further etching to remove the crystalline ITO dome showing the thickness to be about 50 nm and the size about 0.3 \( \mu \text{m} \).
Therefore, from the etching of ITO and GeSbTe, it was hypothesized that the crystalline ITO dome was an indirect method to determine the position and the size of the filament when using long pulses, and this allows analysis of the filament when previously it was not possible to do so due to the size of the filament.

### 5.6 Filament size

There is now a need to use different power to determine if there is a difference in the size of the filament produced. Pulses of 5 s with varying power of 4, 6, 8 and 10 V were applied and the sizes and positions of the spots were determined and compared. The images taken under the optical microscope were then compared to those taken before the pulses were applied.

The filament data is presented in Table 1. If the filament cannot be seen, then it is marked with “not seen.” If it is seen, the position will be marked in the diagram and the diameter shown. It was seen that the largest filaments in general were in the 2 and 3 μm vias when 10 V was used.
compared to 8 V. The filaments seen in the 4 μm device were smaller in diameter. Another point is that in most cases, the filaments would present at or near the corners or the edges. This has implications for the design of PCRAM devices. Also, the filaments seem to present themselves depending on the polarity of the device.

These results suggest that there are two factors that affect the size of the filament. The first is current density and the second is via size. For the 4 μm device, the current density is smaller than that of the 3 μm device as the voltage applied is the same. Therefore, the filament formed is smaller than that of the 3 μm device. However, the 1 μm device also seems to have filaments that are smaller than that of the 3 μm device, which suggests that area plays a part in determining the filament size.
Table 1 Size and position of filament formed with 5 s pulses of different amplitude.

<table>
<thead>
<tr>
<th>Square/V applied</th>
<th>4V</th>
<th>6V</th>
<th>8V</th>
<th>10V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1μm</td>
<td>Not seen</td>
<td>Not seen</td>
<td>Size: 0.3μm</td>
<td>Size: 0.3μm</td>
</tr>
<tr>
<td>2μm</td>
<td>Not seen</td>
<td>Not seen</td>
<td>Not seen</td>
<td>Size: 0.5μm</td>
</tr>
<tr>
<td>3μm</td>
<td>Not seen</td>
<td>Not seen</td>
<td>Size: 0.3μm</td>
<td>Size: 0.5μm</td>
</tr>
<tr>
<td>4μm</td>
<td>Not seen</td>
<td>Not seen</td>
<td>Size: 0.35μm</td>
<td>Size: 0.25μm</td>
</tr>
</tbody>
</table>

These results could have important implications. Firstly, the filament correlates with the contact area at this size range, which suggests that scaling would be possible as the filament would scale with the device size. Secondly, the current density depends on the applied voltage. The minimum required voltage would drop with scaling, which means that filament formation should not be a limiting factor in terms of scaling.

### 5.7 Filament Position

The filament positions for different shapes were checked and it was found that the positions in squares were near but not always at the corners. However, they were near the edges of the via. The same experiment was applied to the 16 bit device with the different shapes to determine the
position of the filaments in those shapes. It was found that the filaments in triangles tend to form at the corners while those of circles form at the edges. This is shown in Figure 55 and Figure 56.

Figure 55 Crystalline domes seen after etching of ITO electrodes in the triangle devices.
5.8 Discussion

The positions of the filaments tend to be on the edges and corners. There could be a few reasons for this. It is possible that the interfaces could result in bonding differences which weaken the thin film structure such that phase change preferentially occurs there. Also, the presence of these interfaces could change the electrical field effect on the phase change material. This effect could be enhanced such that crystallization occurs.

The position of the filaments also suggests that improvements could be made to the way PCRAM devices are fabricated. The formation of the filaments on the edge of the via is a disadvantage for current PCRAM devices. The phase change material on the edge could have slightly different characteristics, resulting in reliability issues in the device. Also, the formation of the filament on the edge means it is in contact with other materials on the edges. This, coupled with the rapid heating and cooling during operation, could mean that cross-diffusion of materials
could be an issue. Cross-diffusion could result in formation of compounds that could reduce device lifetime.

However, the discovery of the position of the filaments would also open up opportunities for better design of PCRAM devices to improve their performance. The presence of interfaces seems to catalyze the formation of the filaments. This means if we can increase the interface area or stress the phase change material, the formation of the filament could require less power and so performance of the devices would be better.
5.9 References


Chapter 6

Conclusion

Phase change memory is one of the most promising non-volatile memories. The phase change mechanism from high resistance amorphous phase to low resistance crystalline phase in nanosecondscale is the most important characteristic of these materials. Though phase change materials had previously been applied in optical media, full understanding of this mechanism has not been achieved as research was mainly based on applications of the phase change phenomenon. Research on the time-based kinetics of phase change has been surprisingly rare. In this thesis, the focus was placed on the transient effect in the nanoseconds during phase change of the material. A transient approach to understanding phase change was developed and the relationship of this effect to crystallization was established. It was found that two time periods, which were termed the delay time and current recovery time, were crucial in the phase change process. These two time periods were found to coincide with nucleation and growth of the phase change material. It was found that scaling of the devices also reduces the delay and current recovery time. This means that scaling not only reduces the programming current required, but also increases the speed of the device. This reduced nucleation and coalescing time was explained by the increased interface effects as volume decreases, which increased the free energy of the atoms and also the rate of nucleation.

The relationship between parasitic capacitance and phase change memory programming performance was studied due its strong effect on the transient effect. It was found that reducing
the parasitic capacitance reduced the leakage current, which correspondingly reduced the
programming current. More importantly, the RC time constant was reduced, resulting in the
reduction of the quenching time. This corresponds to the increase in amorphous resistance.
Hence after simulation, it was found that the amorphous state when there is large parasitic
capacitance is partially crystallized. This has implications for SET performance as the partially
crystallized state means the SET performance of the device with higher parasitic capacitance is
better. However, this would result in poorer memory lifetime and lower reliability.
Work was next done to study how phase change actually occurs by filament formation. To
observe the filament, the top electrode was replaced with indium oxide doped with tin (ITO),
which is a transparent oxide. This allows in-situ observation of the formation of the filament.
Integration of ITO with the phase change material was done and it was found that the filament
size was correlated to the current density and the area of the via. This has significant impact as it
will determine if filament size plays a significant part in scaling. The position of the filament is
not in the center of the contact area. This means one could hypothesize that the failure
mechanism of PCRAM could be due to this position being on the edge of the contact area, with
greater interdiffusion between surrounding layers, and this could result in failure. Hence, if we
were able to choose where the filament would form, then we could improve the overwrite cycles.
Due to the transparent electrodes, this means that use of a laser could be enough to mildly phase-
change the area where we want the filament to appear. Hence, if we put the filament in the
middle, the reliability and the read-write cycles should increase. Also, a new type of device
similar to that of heat assisted magnetic recording (HAMR) could be designed. A laser could be
used to assist the phase change of the material by priming the material with a low power laser
background.