CHARACTERIZATION OF THE PERFORMANCE VARIATION FOR
REGULAR STANDARD CELLS WITH PROCESS NON-IDEALITIES

BY

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THESIS
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ABSTRACT

In IC manufacturing, the performance of standard cells often varies due to process non-idealities. Some research work on 2-D cell characterization shows that the timing variations can be characterized by the timing model. However, as regular design rules become necessary in sub-45 nm node circuit design, 1-D design has shown its advantages and has drawn intensive research interest. The circuit performance of a 1-D standard cell can be more accurately predicted than that of a 2-D standard cell as it is insensitive to layout context. This thesis presents a characterization methodology to predict the delay and power performance of 1-D standard cells. We perform lithography simulation on the poly gate array generated by dense line printing technology, which constructs the poly gates of inverters, and do statistical analysis on the data simulated within the process window. After that, circuit simulation is performed on the printed cell to obtain its delay and power performance, and the delay and power distribution curves are generated, which accurately predict the circuit performance of standard cells. In the end, the benefits of our cell characterization method are analyzed from both design and manufacturing perspectives, which shows great advantages in accurate circuit analysis and improving yield.
I would like to express my gratitude to all the people that helped me in my research work. My sincerest thanks to my adviser, Professor Martin D. F. Wong, who helped me to come to my dream school and guided me to find a fantastic research area that I am interested in. His knowledge and wisdom often enlightened me when I felt confused, and he led me onto the way that I would like to go. I also want to thank the Chinese Scholarship Council. Without its financial support, I would not have been able to be here and focus on my research. Also thanks to Mr. Feng He, who helped me to win this scholarship. I am also thankful to all my colleagues who helped me in both my study and my life. Especially thanks to Hongbo Zhang, who always gives me detailed instructions whenever I have problems. Without his help, I would not have been able to get into this area quickly and find out my research interest. Thanks to Qiang Ma, who offers various help in my life. Thanks to Leslie Huang, who is so nice and always patiently shares her knowledge with me. Thanks to all my friends here in Champaign. I never feel lonely together with them. I also wish to convey utmost thanks to my family – my parents and my wife, Yang Luo, who always offer me the sincerest love and support. I am so lucky to find such a lovely and gentle wife here, who enables me to find the feeling of home while studying abroad by myself. Finally, thanks to Mr. Tom McGeary and Miss Janet “JP” Peters who patiently proofread my thesis. And thanks to the University of Illinois at Urbana-Champaign, where I learned a lot in the past two years. I will always be proud to be a student here.
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CHAPTER 1
INTRODUCTION

As VLSI technology scales down to sub-45 nm node, lithography has already become one of the most difficult challenges in the IC industry. New printing processes with finer resolution, such as extreme ultraviolet (EUV), imprint and maskless techniques, have been studied and expected for years, but due to the problems with reliability, defect control, etc., these technologies are still not ready for mass production. Thus 193 nm ArF is still the only applicable light source for 45 nm/32 nm mass production [1]. According to Equation 1.1, ArF-immersion lithography scanners with NA of 1.35 have reached the fundamental resolution limit of 40 nm half-pitch. Due to the limitation of current resolution enhancement technologies (RET), random 2-D circuit patterns are very difficult to print, and highly regular circuit patterns are preferred for the sub-45 nm node [2, 3, 4].

\[
\text{Resolution} = k_1 \times \frac{\lambda}{NA} \quad (1.1)
\]

A comparison between a conventional 2-D cell [5] and new 1-D cell [6] is provided in Fig. 1.1. 1-D design patterns can be in either the vertical or horizontal direction, with dummy insertion for better printing. Based on this comparison, we can find the advantages and disadvantages of 1-D design.

1.1 Advantages of 1-D Design

The first and most important advantage of 1-D design is that a 1-D cell with its regular patterns is very easy to print with dense line printing technology. In 1-D design, only one direction is allowed to layout the lines on each layer, and the line width and space are usually fixed, so the patterns on the mask are actually optical gratings. And consequently, only the dimension of line width is critical and needs to be accurately controlled. The Off-Axis Illumination
Figure 1.1: A comparison of AOI21 between a conventional 2-D design [5] and the corresponding 1-D design [6]. (a) shows an AOI21 cell in 2-D. (b) shows the same AOI21 cell in 1-D.

(OAI) technology is usually implemented to print 1-D gratings.

Fig. 1.2 shows the concept of OAI technology, where the solid lines represent the incident light and dash lines represent the diffraction light. The light that strikes the grating is diffracted in various directions. If the incident light is at a normal angle (along the axis of the optical system) (Fig. 1.2(a)), then the zero-th diffracted order continues to be along the optical system axis, while the other orders are diffracted sideways, with the amount of deviation increasing as the pitch of the grating is decreasing. For sufficiently small pitch, only the zero-th diffraction order manages to make it through the projection lens, with the other orders being lost. The result is that no pattern is created on the wafer, since the zero-th diffraction order only contains the average of the photomask pattern. However, by making the illumination off-axis (Fig. 1.2(b)), all the diffraction orders are tilted, which makes it more likely that the higher diffraction orders can make it through the projection
lens and help form the image of the mask onto the wafer [7].

![Diagram of dense line printing with off-axis illumination](image)

Figure 1.2: Dense line printing with off-axis illumination. (a) shows the projection without OAI technology. (b) shows the projection with OAI technology.

From Fig. 1.2 we can see, with OAI, the projection lens with same numerical aperture is able to collect twice the angle of diffraction light. In our simulation, a dipole light source in a perpendicular direction to the gratings is implemented to print the dense lines, as shown in Fig. 1.3. The parameter is optimized according to Equation 1.2, where \( \sigma \) is the distance from the center of the source to the center of one illumination spot, \( \lambda \) is the wave length.
of the illumination light, P is pitch size for the dense lines and NA is the numerical aperture of the projection lens. In the lithography process, \( \lambda \) and NA area are usually fixed, and the \( \sigma \) value should be adjusted according to the pitch size.

\[
\sigma = \frac{\lambda}{2 \times P \times NA}
\]  

(1.2)

Fig. 1.3: The dipole light source in OAI technology.

Fig. 1.4 shows the pre-OPC and post-OPC dense lines and the printed contours. In dense line printing technology, usually only the middle region of the poly gate array is used to lay out cells, which is marked as cell region in Fig. 1.4. From Fig. 1.4 we can see the printed contours are very regular and the Optical Proximity Correction (OPC) cost for dense line printing is low. Furthermore, by implementing Source Mask Optimization (SMO) technology, we can optimize the illumination source according to the regular patterns on the mask and improve the printing results even better, which in turn improves the yield.

The second advantage of 1-D design is that on-grid patterns permit a simplified set of design rules in the form of gridded design rules [8]. Design rules provide a solution that allows process and design development to occur concurrently rather than sequentially. In 2-D design, there are various complex patterns that should be taken into consideration when design rules are defined, because the printing images are sensitive to their context and 2-D design allows various types of patterns and context to exist. Unfortu-
nately, even with all this complexity, these rules cannot provide absolute assurance that all design-rule-clean layouts will yield or perform adequately. Some unanticipated structures or pattern combinations may cause serious hotspots while passing the design rule checking. On the other hand, some layout constructs that fail design rule checking might be adequately manufacturable. However, in 1-D design, since the environment is almost identical, the design rules are simplified and focused on the spaces. With the scaling down of pitch sizes, the influence between features becomes even more complex. The regular patterns and gridded design rules provide a simple and clear way that not only improves yield but also considers performance challenges.
Figure 1.5: Lithography simulation and hotspot detection. (a) and (b) show the simulated lithographic process window bands for 1-D design and 2-D design, respectively, and (c) shows the pinching and bridging hotspots occurring around 2-D constructs.

The regular design also reduce hotspots tremendously because single orientation layout completely eliminates all complex 2-D constructs that could lead to yield concerns. In [4], both the 2-D and 1-D layouts were simulated through the process-window. Fig. 1.5(a) and Fig. 1.5(b) show the simulated lithographic process window bands for the 1-D and 2-D layout, while Fig. 1.5(c) shows examples of typical layout sensitivities discovered in the 2-D layout. The hotspot count in Table 1.1 shows the improved patterning robustness of the regular design.
Table 1.1: Count of Lithography Hotspots in 2-D and 1-D Layout

<table>
<thead>
<tr>
<th>Lithography Hotspots</th>
<th>Poly Width</th>
<th>M1 Width</th>
<th>M1 Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-D</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>2-D</td>
<td>34</td>
<td>23</td>
<td>1634</td>
</tr>
</tbody>
</table>

Another advantage of dense line printing technology is its insensitivity to layout context. In 1-D design, the poly layer is generated by the combination of dense line mask and trim mask. Only the trim mask varies between different cells. The dense lines remain identical since pitch size is usually fixed for a certain design. As shown in Fig. 1.4, for any 1-D cell, the context of its poly gates is simply the optical grating structures.

The lithography simulation parameters for 30 nm gate length are shown in Table 1.2. Instead of the irregularity of printed contour introduced by layout context in 2-D cells [9], 1-D cells show much higher regularity in printed contour, which is insensitive to layout context. This property of 1-D cells makes them easier to characterize than 2-D cells. In 2-D design, all of the various context information which might affect the contour shape must be taken into consideration [9], while in 1-D design, there are only several systemic variation sources to be considered, such as defocus, exposure and pitch size.

Table 1.2: Lithography Optical Model for 30 nm Gate Length

<table>
<thead>
<tr>
<th>Wavelength</th>
<th>193 nm</th>
</tr>
</thead>
<tbody>
<tr>
<td>Numerical Aperture</td>
<td>1.35</td>
</tr>
<tr>
<td>Illumination</td>
<td>Dipole</td>
</tr>
<tr>
<td>Background</td>
<td>clear</td>
</tr>
<tr>
<td>Feature</td>
<td>dark</td>
</tr>
<tr>
<td>Aerial Image Intensity Threshold</td>
<td>0.3</td>
</tr>
</tbody>
</table>
1.2 Disadvantages of 1-D Design

Compared with 2-D design, 1-D design has some drawbacks as well. That is why 1-D design has not completely substituted for 2-D design in the current state of the art. The first drawback is that 1-D design is not as flexible as 2-D, especially for local connections. From the designer’s perspective, it is easier to lay out a circuit structure if two dimensions can be used in one layer. For example, in Fig. 1.1(a), since both horizontal and vertical directions are allowed in the Metal 1 layer, only two tracks are already enough to route the pins in the P-type active area. However, in the 1-D cell shown in Fig. 1.1(b), only the horizontal direction is allowed in the Metal 1 layer, and consequently, four tracks are needed to fully route the pins in the P-type active area. Secondly, a circuit designed in 1-D might use more layers than that in 2-D, which increases the cost of manufacturing. As shown in Fig. 1.1, to realize the same function, the 1-D cell in (b) uses two metal layers while the 2-D cell in (a) uses only one metal layer. Another disadvantage comes from the via layer in 1-D design. As mentioned above, more metal layers are needed in 1-D design, and for each layer only one direction is allowed. Consequently, the number of vias in 1-D design becomes bigger than that of 2-D design. Besides that, since the lines in 1-D are very dense, the distribution of the vias becomes denser as well, which increases the difficulty to fabricate the via layer.

1.3 The Future of 1-D Design

In spite of the drawbacks, 1-D regular circuit patterns still draw intensive research interest due to their great advantage in manufacturability. Taking a glimpse into Intel’s future lithography, we can see that Intel has already moved to 1-D design layouts at their 45 nm node. Figure 1.6 shows that 1-D gridded layout will be realized in a way where 193 nm lithography is implemented to print the unidirectional dense lines, and the trim mask is printed by more advanced lithography technology such as E-Beam or EUV. Therefore, this thesis is focused on the 1-D standard cell to characterize its circuit performance.
1.4 The Target of Our Methodology

For a certain design, the pitch size is usually fixed. With variations in exposure and defocus, the width of printed lines also varies within a certain range. Since the poly layer is generated by dense line printing technology, the line width variations turn out to be variations in gate length, which largely impacts the circuit performance. Thus, process non-idealities are crucial for the variations in circuit performance. Figure 1.7 shows the gate length variations observed at different exposure and defocus conditions. In the design phase, the model of lithography variations is provided by the manufacturers, and it is necessary for the designers to simulate the impact on the circuit’s performance by lithography variations before it is put into production. This is because after being printed on wafers, the gate length of cells might change due to process variations, which makes the circuit performance different from what the designer expected. With the scaling down of feature size, the process variations become more and more important for cell performance. Due to the impact from lithography variations such as exposure and defocus variations, the answer to a cell’s performance has changed from a fixed number to a distribution curve. As shown is Fig. 1.8, the delay of a certain cell is no longer a fixed value (5 ps); instead it can be any value within a region. The probability for each possible delay value can be found from the distribution curve, which is determined by the lithography variation distributions.
In this thesis, focusing on 1-D cells generated by dense line printing technology, we present a characterization methodology which predicts the distribution of their delay and power performance, considering the lithography non-idealities from defocus and exposure. In our methodology, we do lithography simulation on the 1-D layout of a standard inverter and extract the printed gate length at various process conditions, and then statistically analyze the simulated results to construct the gate length distribution model. After that, circuit simulation is performed on the extracted gate lengths to get the cell’s delay and power performance. Finally, its delay and power distribution models are obtained. With such models, the designers are able to predict the cell performance and use this information to guide the circuit design, and the manufactures can also adjust the lithography process parameters to improve the yield.

Figure 1.7: The PV band on poly gate for exposure and defocus variations.

Figure 1.8: The change in the answer to a cell’s performance.
The rest of the thesis is organized as follows. Chapter 2 gives an overview of our methodology. The detailed experiments and statistical analysis are described in Chapter 3. Chapter 4 shows the effect of pitch size on circuit performance. Chapter 5 illustrates the benefits of our characterization methodology. Finally, Chapter 6 concludes the thesis.
CHAPTER 2
CHARACTERIZATION METHODOLOGY

Characterizing the circuit performance of standard cells with lithography variations involves both lithography process simulation and circuit performance simulation. The four main steps to do this are shown in Fig. 2.1.

Firstly, the layout of a standard inverter is generated by 1-D dense line mask and trim mask. Figure 2.2(a) shows the original layout with both
dense line layer and trim layer. Figure 2.2(b) shows the real structure of the inverter after the trim layer has been applied to the poly layer. As shown in Fig. 2.2, the poly layer is generated by dense line printing, in which the line width is 30 nm, and the pitch size is set to be 130 nm. The patterns on the dense line mask are regular and identical for all cells. As a result, the gate length variation is insensitive to layout context. So for different cells fabricated by dense line printing technology, as long as the lithography conditions such as light source, defocus and exposure are the same, the gate length of the printed pattern will remain identical regardless of the structure and context of the cell. In 2-D cells, cell structure and layout context contribute a great deal to gate length and must be taken into consideration. This is the essential difference between the fabrication of 1-D and 2-D cells. Consequently, a simple cell structure such as an inverter is enough to illustrate the performance characterization methodology of the circuits fabricated by dense line printing technology. From the printing contour shown in Fig. 1.4, we can see that the printed patterns appear to be very regular except for some variations at the line ends, which are not used for cell layout. After the dense line patterns are printed on the wafer, a trim mask is applied to cut the dense lines into intervals. The patterns on the trim mask can be different depending on the cell structures. In Fig. 2.2(b), the poly interval and three M1 intervals intersecting with the active area construct a real inverter. There are also variations from the printing contours of the trim mask; however, those variations only affect the length of the polys, which is shown in Fig. 2.3(b), and thus have little effect on important circuit performance factors such as gate length or capacitance. Therefore, in this thesis we do not consider the variation from trim pattern and only consider the contribution of gate length variations to cell performance.

Secondly, lithography simulation is performed on the poly layer with different defocus and exposure conditions within the process window. Gate length variations are observed, as shown in Fig. 1.7. In this approach, the defocus variation region is from $-140 \text{ nm}$ to $140 \text{ nm}$ and the variation region for exposure is from $0.9$ to $1.1$. The variations on poly gate can be obtained from the lithography simulation result.

In the third step, the simulation results are plotted and fit in with a polynomial function. Based on the fitting equation, for any combinations of defocus and exposure conditions within the process window, the gate length can be
directly derived. Conversely, given a reasonable gate length, the correspond-
ing lithography conditions can also be derived from the model. As a result,
given the probability distributions of defocus and exposure, the distribution
model of gate length variation can be constructed, too.

In the final step, delay and power of the inverter are simulated by HSpice at
multiple gate lengths, which are sampled with equal space within the process
window. In Fig. 2.4, a 5-inverter oscillating ring is constructed to measure
the delay of the inverter. Figure 2.5 shows the circuit schematic to measure the power consumption of one inverter. The frequency of the input pulse voltage is set to be 250 MHz and the output capacitance is 5 fF. Since both delay and power change monotonously with the increase of gate length, the probability distribution of delay and power can be derived directly from the distribution of gate length.
3.1 Lithography Process Simulation

In the experimental part, we assume both defocus and exposure follow a normal distribution. The variation region for defocus is \([-140 \, \text{nm}, 140 \, \text{nm}]\), and the variation region for exposure dose is \([0.9, 1.1]\). Based on this assumption, the defocus condition is sampled from \(-140 \, \text{nm}\) to \(140 \, \text{nm}\) at \(5 \, \text{nm}\) step size and exposure dose is sampled from \(0.9\) to \(1.1\) with step size of \(0.01\), as shown in Fig. 3.1.

At each combination of defocus and exposure conditions, lithography simulation on the dense line mask is performed and the printed gate length is extracted. As shown in Fig. 1.7, the printed line width varies at different exposure and defocus conditions. The relationship between gate length and lithography variations is plotted in Fig. 3.2. Note that different combinations of defocus and exposure might produce the same printed gate length value. That’s the reason why only several gate length values are obtained from the various combinations of lithography variations. From Fig. 3.2 we can see that when exposure dose is fixed, gate length varies quadratically with the variation of defocus, and if defocus is fixed, the gate length varies linearly with the increase of exposure. Therefore, Equation 3.1 is used to fit in the data points.

\[
GateLength(F, E) = a_0 + a_1 F + a_2 E + a_3 FE + a_4 F^2 + a_5 F^2 E \quad (3.1)
\]
Figure 3.1: The sampling of lithography variations. (a) shows the sampling of defocus. (b) shows the sampling of exposure.
Figure 3.2: The relationship between printed gate length and lithography variations. (a) shows the relationship between gate length and defocus. (b) shows the relationship between gate length and exposure dose.

The cross validation methodology is applied to verify the correctness of the fitting equation, in which 90% of the simulated data points are randomly selected and fit in with Equation 3.1 to obtain the value of each coefficient, as shown in Table 3.1; then the remaining 10% of simulation results are substituted into the obtained equation to calculate the gate lengths. By comparing the calculated values with simulated values of the testing data, we can see the correctness of the fitting equation. This verification experiment is performed three times and the standard deviations of each experiment
are shown in Table 3.2. From the table we can see that the calculated gate lengths based on the fitting equation are quite close to the simulated results, with standard deviation less than 1 nm. This error exists because the gate length precision in the lithography simulation cannot be less than 1 nm; hence, the simulated data points are distributed discretely with step size equal to 1 nm, which can be observed from Fig. 3.2. In other words, if the difference between exposure doses or defocus levels is not big enough to cause at least 1 nm difference on the printed contour, that difference will not show up in the extracted gate length. In reality, the printed line widths on a wafer might have less than 1 nm difference for the different lithography conditions, which will turn out be continuous rather that discrete.

Table 3.1: Coefficients of the Fitting Equation for 130 nm Pitch

<table>
<thead>
<tr>
<th>Coefficients</th>
<th>( a_0 )</th>
<th>( a_1 )</th>
<th>( a_2 )</th>
<th>( a_3 )</th>
<th>( a_4 )</th>
<th>( a_5 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>value</td>
<td>75.75</td>
<td>-0.001348</td>
<td>-44.7</td>
<td>0.001438</td>
<td>8.839E-005</td>
<td>-0.0001941</td>
</tr>
</tbody>
</table>

Table 3.2: Error Analysis of the Fitting Equation

<table>
<thead>
<tr>
<th>Experiment</th>
<th>Standard Deviation (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.5687</td>
</tr>
<tr>
<td>2</td>
<td>0.5491</td>
</tr>
<tr>
<td>3</td>
<td>0.5320</td>
</tr>
</tbody>
</table>

The cross validation result shows that Equation 3.1 is able to predict the relationship between defocus, exposure and gate length accurately. In addition, since the dense line array of the poly layer remains identical among various cells, the same equation can be applied to calculate the printed gate length of every cell fabricated by dense line printing technology regardless of cell structure, and all the coefficients in the equation stay unchanged. The fitting surface is shown in Fig. 3.3.
3.2 Gate Length Distribution

For the simulated gate lengths, the minimum value $l_{\text{min}}$ and the maximum value $l_{\text{max}}$ can be found from the simulation result. And based on the fitting equation, for any value $l$ between $l_{\text{min}}$ and $l_{\text{max}}$, the corresponding lithography process condition (defocus $f$, dose $e$) can be derived by projecting the value $l$ onto the fitting surface. The projection introduces a continuous 2-D curve of defocus and dose. Without losing precision, we sample the curve with a very small step size and get a set of combinations of dose and defocus conditions $\{(f, e)\}$. Therefore, when defocus is set to $f$ and exposure dose is set to $e$, a combination that belongs to the set, then the printed gate length should be $l$. In order to obtain the gate length distribution, the distributions of both defocus and exposure should be provided. Here we assume the defocus and exposure follow normal distribution. For the defocus condition, the mean value is 0, and the 3-sigma value is set to be 140 nm. For exposure dose, the mean value is 1, and the 3-sigma value is set to be 0.1. As shown in Fig. 3.4, the probability of defocus $f$ $(P(f))$ or exposure $e$ $(P(e))$ is equal to the area
size under the distribution curve. The width of the area is exactly the step size. Since it is a normal distribution curve, the total area under the curve should be 1, which is equal to the probability summation of all sampling points.

![Defocus Probability Distribution](image1.png)
(a) The probability of defocus at level \( f \)

![Exposure Probability Distribution](image2.png)
(b) The probability of exposure at dose \( e \)

Figure 3.4: The probability that a sampling lithography condition occurs.

In addition, we assume defocus and exposure are two independent conditions. Thus, the probability that both defocus is at level \( f \) and exposure is at dose \( e \) can be obtained by the multiplication of \( P(f) \) and \( P(e) \). Therefore, for any gate length \( l \) between \( l_{\text{min}} \) and \( l_{\text{max}} \), the probability of its occurrence can be derived by Equation 3.2.

\[
P(l) = \sum_{\{(f,e)|\text{GateLength}(f,e)=l\}} P(f) \times P(e) \tag{3.2}
\]

In order to find the probability distribution of gate length variation, gate
lengths are first sampled with equal step size from $l_{\text{min}}$ to $l_{\text{max}}$. Then, based on our assumption, according to Equation 3.2, the probability of the occurrence of each sampled gate length can be calculated. Finally the distribution curve of gate length is constructed by those calculated probability results, which is shown in Fig. 3.5.

![Figure 3.5: The gate length distribution.](image)

Note that in reality, there is some correlation between defocus and exposure because of the complexity of the lithography system. So the probability of gate length should be corrected by Equation 3.3, where $P(e|f)$ is the probability that exposure is at dose $e$ after defocus is at level $f$. However, the correlation is not significant and very difficult to be characterized, so in this thesis, we only assume exposure and defocus are independent variables.

$$P(l) = \sum_{\{(f,e)|\text{GateLength}(f,e)=l\}} P(f) \times P(e|f) \quad (3.3)$$

### 3.3 Circuit Performance Simulation

After lithography simulation, the gate lengths are extracted at every process condition. Suppose the width of the active layer remains unchanged; then the equivalent channel $w/l$ ratio will be inversely proportional to the printed gate length. In the next approach, circuit performance simulation is performed
on each extracted gate length. By substituting different $w/l$ ratios for each transistor into the same circuit structures shown in Fig. 2.4 and Fig. 2.5, different delay and power responses are obtained. The relationships of delay vs. gate length and power vs. gate length are shown in Fig. 3.6. Figure 3.6(a) shows that the delay increases monotonously with the increase of gate length and (b) shows that power decreases monotonously with the increase of gate length. According to the properties of monotonic function, delay or power performance has a one-to-one correspondence to gate length. Hence, the probability distribution of both delay and power can be obtained directly from the gate length distribution, simply by substituting the gate length value with the corresponding circuit performance value. The distribution curves are shown in Fig 3.7.
Figure 3.6: Delay and power performance vs. gate length.
Figure 3.7: The delay and power distributions.
CHAPTER 4
THE EFFECT OF PITCH SIZE

In 1-D dense line printing technology, besides aspects of lithography process such as exposure and defocus, the pitch size also plays an important role in gate length variation. The pitch size is usually fixed before cell layout. And for different pitch sizes, the parameter of the light source should also be adjusted according to Formula 4.1, where $\lambda$ is the wavelength, $P$ is pitch size, $NA$ is the numerical aperture, and $\sigma$ is the inner sigma value. In our experiment, the inverter is laid out with three different pitch sizes 90 nm, 110 nm and 130 nm. And at each pitch size, the same simulation strategy as previously described is performed. For the 90 nm pitch size, 2 percent of the printed gate lengths are too small to be simulated by the HSpice model, and for 110 nm pitch size, 0.6 percent cannot be simulated. After getting rid of that small portion of data, the delay and power distributions are obtained at the three pitches as illustrated in Fig. 4.1.

$$\sigma = \frac{\lambda}{2P \ast NA}$$ (4.1)

From Fig. 4.1 we can see that the delay distribution curves still look like a normal distribution, but the mean and sigma values are slightly different for different pitch sizes, whereas the power distributions look quite identical, and the possible values are limited to a very narrow region. Therefore, we can declare that the power of a cell is not sensitive to the lithography variations from fabrication, and the delay follows a normal distribution, whose mean and sigma vary with pitch size.
Figure 4.1: The delay and power distributions at different pitches.
CHAPTER 5

BENEFITS OF OUR APPROACH

5.1 From the Designer’s Perspective

Because the poly layer which is printed by dense lines is insensitive to layout context, as long as the pitch size is fixed, the designer can perform the lithography simulation on the poly layer and obtain its gate length distribution for every cell. Based on that distribution, the performance of each cell can be accurately predicted. As is illustrated in Fig. 3.7 and Fig. 4.1, the delay distribution of the inverter appears like a normal distribution at different pitches. Their mean value and sigma value are slightly different for different pitch sizes. However, the power consumption remains almost identical and thus insensitive to photolithography variations. In that case, the designer should pay more attention to the circuit’s delay performance considering lithography variations. In the designing phase, the gate length distribution model is provided to the designer by the manufacturer. By performing circuit performance simulation at multiple gate lengths and substituting the simulated results into that model directly, the designer is able to accurately predict the cells’ performance and build the circuit structure accordingly to obtain optimal performance.

5.2 From the Manufacturer’s Perspective

From Fig. 3.5, we can see that the gate length varies between 24 nm and 36 nm, and the peak value is around 31 nm. So the printed gate length turns out to be a little wider because of the lithography process variations. Although when defocus is 0 nm and exposure dose is normalized to be 1, the printed gate length is 30 nm, which is exactly the gate length on the layout, for the
various other combinations of defocus and exposure conditions, the printed gate length is more likely to be around 31 nm. As mentioned in Section 3, we assume both defocus and exposure follow a normal distribution, and the probability that each gate length value occurs is calculated by Equation 3.2. It is possible that the gate length value with highest probability is not the value when both defocus and exposure are assigned the mean value in the normal distribution. In order to compensate for the offset caused by lithography process variations, a lithography process parameter such as exposure dose can be adjusted. For example, if the exposure dose is increased, the printed line width will decrease consequently because in our simulation, the background is set to be clear and patterns are set to be dark. As shown in Fig. 5.1, the mean value of normalized exposure dose is tuned up from 1 to 1.02, such that the mean value of the gate length is reduced from 31 nm to 30 nm, which is close to the expected gate length on the layout. Therefore, before putting a design into fabrication, the manufacturer can perform the lithography simulation first and adjust the parameters accordingly considering the process variations in real fabrication. In this way, the printed contours on the wafer are more likely to be identical to the patterns on the layout; thus the yield is improved.

Figure 5.1: The gate length distribution after exposure tune-up.
This thesis proposes three approaches to characterize 1-D standard cell circuit performance variations caused by process non-idealities. The first approach simulates the gate length variations at multiple points within the process window. The second approach does statistical analysis on the simulated data and fits them in with a polynomial function, upon which the gate length distribution model is built. In the third approach, two different circuit structures are constructed to measure the delay and power performance at different gate lengths, which finally gives out the circuit performance distributions. Based on the experimental results, our characterization methodology is able to accurately predict the circuit performance for 1-D cells, with which the designer is able to predict circuit performance and the manufacturer can adjust the process parameters to improve its yield.
REFERENCES


