CONTROL, ANALYSIS, AND DESIGN OF DISTRIBUTED INVERTER SYSTEMS

BY

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DISSERTATION

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ABSTRACT

As renewable energy sources and storage technologies become increasingly commonplace on the power grid, the number of power electronic inverters can be expected to grow. Since power delivery can be easily controlled with power electronic circuits, inverters offer a wealth of opportunities in the coordination of highly distributed ac power systems. This dissertation is focused on the development of inverter coordination methods such that system distortion is reduced and stability is maintained.

In particular, a method of switch interleaving is developed such that the distortion generated by a system of inverters is canceled. This method is applied to series connected H-bridge inverters which interface a distributed system of dc sources to an ac load. The resulting system can employ a very low switching frequency and small output filter while maintaining a low distortion ac output. A control system is developed which manages the cascaded H-bridge inverters during uniform and non-uniform conditions at the dc inputs. In addition, switch interleaving is applied to a system of parallel connected inverters. A closed-form expression is derived which describes the total current generated by a system of parallel interleaved converters. This result is presented with a level of generality such that it can be applied to both dc-dc and inverter systems.

A technique for coordinating parallel inverters in a microgrid is formulated such that they are able to synchronize their ac outputs. The resulting microgrid is modular and does not require communication between inverters. A theoretical framework is developed which leads to a sufficient condition for inverter synchronization. It is shown that the synchronization condition is independent of the number of parallel inverters and the load parameters. Throughout the thesis, experimental and simulation results are used to substantiate the analytical results and illustrate the merit of the proposed techniques.
To my wife, family, and friends.
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Chapter 1

INTRODUCTION

As the amount of distributed resources on the power grid grows, power electronic inverters will become increasingly ubiquitous. This follows from the fact that an inverter is needed to perform dc-ac power conversion whenever any dc energy resource is interfaced to the ac grid. Of particular importance to the modernizing energy infrastructure is the growing penetration of photovoltaics, batteries, fuel-cells, and other types of dc energy sources. Photovoltaics play a central role in the transition towards sustainable energy sources, and electric vehicles offer an unprecedented opportunity for the widespread grid-integration of energy storage. Since power delivery can be easily controlled with power electronic circuits, inverters offer a wealth of opportunities in the coordination of highly distributed ac power systems.

Microgrids are a natural extension of the distributed and renewable energy setting. A microgrid is a decentralized electrical power system composed of generation, storage, and loads that can operate independent of the bulk power system. As envisioned, the future infrastructure could be composed of a large number of interconnected microgrids which each contain energy resources and storage. Microgrids are poised to become a valuable technology in the distributed generation domain and are expected to provide several system-level advantages including: increasing renewable integration, reducing transmission and distribution losses, and ensuring a reliable power supply to loads in mission-critical applications.

This work is focused on the control, design, and analysis of distributed inverter systems for both grid-connected and microgrid systems. The central theme of this dissertation is the development of appropriate inverter coordination methods such that desired objectives are met. We introduce notions which depart from the conventional single-converter design paradigm in order to consider inverter systems as an integrated whole. In particular, methods of inverter switch interleaving are developed such that the distortion generated by a system of inverters is reduced. This
method is applied to both parallel and series connected inverters. Furthermore, technique for coordinating parallel inverters in a microgrid is developed such that they are able to synchronize their ac output without communication between inverters. A theoretical framework is developed which leads to a sufficient condition for inverter synchronization. Throughout much of the thesis, PV applications will be used to demonstrate the proposed techniques.

1.1 Trends in Distributed Power Electronic Systems

As the shift towards renewable energy sources is made, the power system will need to become increasingly decentralized. This follows from the fact that renewable energy sources, such as wind and solar, tend to be geographically diffuse. Within the renewable energy sector, the PV market has seen considerable growth in recent years and has been a large driver of advancements in power electronic technologies. In this section, an overview of recent advances in distributed power electronic architectures in grid-connected PV and microgrid systems is given.

1.1.1 Photovoltaic Power Conversion

![Diagram of PV power conversion architectures](image)

Figure 1.1: Diagram of PV power conversion architectures. The series string topology (a), a cascaded dc-dc optimizer system (b), and a microinverter system (c).

The centralized inverter topology, which is shown in Fig. 1.1(a), is the most con-
ventional type of dc-ac conversion system for PV. In this type of system, a collection of PV modules are connected in series until a sufficiently high voltage is attained. The central inverter performs maximum power point tracking (MPPT) on the PV string while simultaneously regulating the ac current at its output. In such a system, it is possible for a small section of mismatched PV cells to severely affect the power output of such a system. This effect can be caused by partial shading, degradation, manufacturing variation, and damage.

Generally speaking, a fundamental challenge associated with PV systems is the mismatch of $i-v$ characteristics among series connected PV cells. Traditionally, the undesired effects of mismatch are mitigated by placing bypass diodes across groups of PV cells. With this approach, a “weak” group of solar cells is circumvented if there is sufficient mismatch. However, it has been shown in [1, 2] that energy harvest can be strongly impacted during partial shading despite the use of bypass diodes. To overcome the drawback, interest in distributed power electronic architectures has grown.

The cascaded dc-dc optimizer system in Fig. 1.1(b) consists of $N$ series connected dc-dc converters [2]. Each converter performs MPPT on the set of PV cells at its input. The entire system is then interfaced to the grid through a centralized inverter. Several variations of this topology have been developed and an alternative approach called differential power processing is introduced in [3]. Although the dc-dc optimizer system maximizes power output during partial shading, the central inverter suffers from lower reliability due to the presence of low-cost electrolytic decoupling capacitors which are prone to drying. As a result, the central inverter typically needs to be replaced multiple times during the lifetime of the system.

Module-level inverters called microinverters have attracted significant interest in recent years [4–7]. This type of system, as illustrated in Fig. 1.1(c), is composed of several module-level inverters connected in parallel. As with the dc-dc optimizer system, module-level MPPT reduces the impact of mismatch on energy harvest and the presence of local electronics enables monitoring and diagnostics at the panel. Most importantly, because the central inverter is eliminated from the system, there is no single point of failure. Since inverters can be added and removed as necessary, system modularity is maximized. Some recent microinverter designs have eliminated the use of electrolytic capacitors entirely and transitioned to long-lifetime film capacitors. As a result, a highly reliable microinverter PV system can be achieved. Since microinverters typically have slightly lower power conversion efficiencies in compar-
ison to centralized inverters, they are most beneficial in installations where shading and mismatch are prevalent.

1.1.2 Microgrid Systems

![Figure 1.2: A microgrid composed of parallel inverters connected across a load.](image)

Given the growing penetration of storage and energy resources at the distribution level, research interest in microgrids has grown significantly. Consider the system in Fig. 1.2 which is composed of local loads and a heterogeneous set of dc energy sources which are interfaced by inverters. A microgrid such as this is able to separate from the grid-utility in the event of a black-out or abnormal grid conditions and provide uninterrupted power to its local loads. When the microgrid is operating independently of the grid, it is said to be islanded. In order for the system of inverters to provide energy within the islanded system, they must be able to maintain synchronization in the absence of the grid voltage or a generator. Furthermore, the inverter system must provide voltage and frequency regulation. In general, design objectives of microgrids are typically focused on minimizing communication [8, 9], maintaining stability [10–12], and ensuring inverters share the load in proportion to their ratings [13].
1.2 Scope of the Dissertation and Previous Work

This dissertation will be primarily focused on controlling and analyzing the multi-inverter systems shown in Fig. 1.3. In particular, the scope of investigation will be limited to:

- Coordinating the switching action of multiple inverters such that the distortion generated by the system is reduced
- Controlling a system of parallel inverters such that they are able to synchronize their ac outputs and form an islanded microgrid without communication

![Diagram of multi-inverter system architectures. System of cascaded inverters is given in (a) and a parallel inverter system is shown in (b).](image)

In this work, the first challenge is addressed by phase-shifting the pulse with modulation (PWM) carrier signal corresponding to each inverter such that they are interleaved. With this approach, emphasis is placed on reducing the distortion generated by the system rather than the individual inverter.

In particular, the system of cascaded inverters in Fig. 1.3(a) can be used to create a larger system called a multilevel inverter. By leveraging the distributed structure of the system and the benefits of interleaving, it is possible to synthesize a low distortion ac waveform while employing a very low switching frequency and small output filter. Furthermore, since each inverter is interfaced with an isolated dc energy source, this type of system can be readily applied towards PV. A portion of the presented work will be aimed towards developing a control system which manages non-uniform power generation among the dc energy sources.
Switch interleaving is also applied to the parallel system of inverters in Fig. 1.3(b). With the proposed technique, the distortion introduced by each inverter cancels once the currents combine at the ac load. Investigation will be particularly focused on developing an mathematical framework for analyzing ripple cancellation in parallel converter systems.

Investigation will also be focused on developing a method for controlling a system of parallel inverters such that they form a stable microgrid island. In particular, the objective will be to develop a control scheme that does not require communication between inverters (beyond the coupling inherently introduced by the electrical network). Investigation will be limited to microgrids formed by parallel inverters with identical ratings.

1.2.1 Literature Review

Multilevel Inverters:

Multilevel inverters can in general be categorized into three distinct circuit topologies: i) diode-clamped inverters, ii) flying-capacitor inverters, and iii) cascaded H-bridge inverters [14-16]. The first two types of circuits are generally used in three-phase systems in medium voltage (2.3 kV, 3.3 kV, 4.16 kV, or 6.9 kV) industrial applications and the cascaded H-bridge system is used in single-phase systems with isolated dc sources. Before describing the cascaded H-bridge topology and how it relates to the work presented here, a brief outline of the challenges associated with multilevel inverters will be given.

An equivalent circuit of a 5-level diode-clamped circuit is shown in Fig. 1.4. In a typical application, there is a single dc source which is connected across a stack of capacitors and the control objective is to balance the capacitor voltages while managing the ac output [17, 18]. If the midpoint of the capacitor stack (between \( C_2 \) and \( C_3 \) in Fig. 1.4) acts as a neutral point, then each phase can generate a voltage of 0 V, ±1\( V_{cap} \), ±2\( V_{cap} \), ..., ±\( \frac{N}{2} \)\( V_{cap} \), where \( N \) is even and it is assumed that each capacitor has an identical voltage equal to \( V_{cap} \). In general, \( N+1 \) voltage levels with respect to neutral are possible at each phase in the diode-clamped inverter. Because the number of switch configurations is large, a sophisticated control system is needed to manage capacitor charges while controlling the semiconductor devices.

In [19-23], a variety of control strategies have been developed which manage ca-
Figure 1.4: Equivalent circuit of a 5-level diode-clamped multilevel inverter, from [18]. The switches in the actual circuit are made up of interconnected diodes and power transistors.

Capacitor balancing in the diode-clamped multilevel inverter. In particular, a controller was developed in [18] which relies on a real-time assessment of the energy stored in each capacitor in conjunction with space vector PWM techniques to generate the switch states. Despite the use of such sophisticated techniques, it has been shown that the diode-clamped multilevel inverter has a limited operating regime where stability is maintained [18, 22]. Similar difficulties with flying capacitor multilevel inverters are outlined in [24–27].

In this dissertation, the primary focus will be distributed dc-ac power conversion in single-phase PV systems. However, the diode-clamped-inverter and flying capacitor topologies are generally used to deliver power from a single dc source to a three-phase ac load. Furthermore, as stated above, there are several complications associated with capacitor balancing in the diode-clamped and flying-capacitor multilevel topologies. Given that a PV system naturally provides a large number of isolated dc sources (groups of solar cells), the cascaded H-bridge inverter topology in Fig. 1.5 offers an attractive alternative.

One common method of controlling this type of system is referred to as carrier disposition. This variation of standard sine-triangle PWM is based on utilizing $N$
level-shifted and scaled carrier signals which correspond to the $N$ inverters [28–30]. One significant drawback of this method is that the power delivered by the cascaded inverters is difficult to control. In particular, inverters near the middle of the stack tend to deliver more power than the remaining inverters. Recent attempts at correcting this deficiency involve the use of variable offsets among carrier waveforms [30].

In this work, it is proposed that a system of cascaded PV inverters be controlled using $N$ pairs of interleaved carriers with 3-level PWM [31]. In existing literature, this is generally referred to as phase-shifted PWM [28, 32]. With this approach, each of the $N$ inverters utilizes a carrier signal which is phase-shifted by a unique multiple of $\frac{T}{N}$, where $T$ is the carrier period. With this type of implementation, the power delivered by each inverter can be easily controlled to accommodate non-uniform power generation among the PV at the inputs. Since the conditions at each dc input can be controlled [31], it is possible to perform MPPT on each set of PV cells despite mismatch.

Similar approaches to the proposed method have been given in [33–35]. In [33, 34], the power delivered by each inverter is adjusted by multiplying a reference signal for the modulation waveforms with a factor which depends on the measured power at each PV input. Unfortunately, experimental results are not given. Recently, a method was proposed in [35] where the control parameters are adjusted as the power

\begin{figure}[h]
\centering
\includegraphics[width=0.5\textwidth]{cascaded_hbridge_inverter_system.pdf}
\caption{Cascaded H-bridge inverter system.}
\end{figure}
generated by each set of PV cells changes. In general, previous work has been focused on small numbers of series-connected inverters. In this work, the aim is to formulate a technique which can be applied to an arbitrarily large number of inverters.

Parallel Interleaved Converters:

![Diagram of parallel interleaved converters controlled for ripple cancellation.]

Figure 1.6: Parallel interleaved inverters controlled for ripple cancellation.

Research on switch interleaving of parallel power converters is well established [36–40]. Interleaving in dc-dc converters began receiving significant attention in the 90's but seminal ideas for the interleaving concept can be traced back decades earlier [41]. As illustrated in Fig. 1.6, the general idea is to stagger the switch transitions of multiple parallel connected converters such that the current ripple introduced by each converter cancels when entering the load. In general, the amount of cancellation depends on the number of converters, the shape of the ripple, and the degree of uniformity among the individual converters. Previous attempts at deriving a closed-form expression for the net load ripple have had limited success. In [36], the net ripple amplitude was derived in terms of a finite series. Several methods have been introduced [37,42] to attain an estimate of the net current. However, these results do not lead to a closed-form expression and sometimes involve iterative techniques. Recently, floor and ceiling functions were used in an attempt to derive
the ripple amplitude [43]. However, the resulting estimation in [43] does not agree with established measurements.

Traditionally, switch interleaving has been applied in systems of parallel buck and boost converters. Depending on the application, interleaving can be used to minimize ripple either at the input or output of the system. In [44,45], multiple boost converters are placed in parallel at the input such that the ripple extracted from the single dc source is minimized. This method has been frequently used to minimize the ripple extracted from a PV module [46–48]. Countless other applications of ripple minimization in dc–dc systems exist. Previous work on interleaved parallel inverters has been rather limited. In [49–52] it was assumed that either all inverters share a common dc input source or that the number of interleaved inverters is small. In this work, it is proposed that the interleaving technique be applied to $N$ parallel inverters such that output distortion is minimized. A closed-form analytical result is derived which is generalized to arbitrary $N$.

Inverter-Based Microgrids:

As outlined in [8], existing microgrid control techniques can be broadly classified as being based on either master/slave, current sharing, or droop methods. One significant drawback of the master/slave and current sharing method is that they require a communication network which introduces a single point of failure in the system. Specifically, the master/slave method is based on selecting one “master” inverter to regulate the system voltage while the remaining “slave” inverters inject current into the system [53–56]. In such a system, one of the slave inverters must immediately assume the role of the master inverter if the original master inverter fails. This feature necessitates a communication network which can dynamically reassign inverter functionality. Alternatively, the current sharing method requires the total load current to be sensed. The load current is then divided by the number of inverters in the system and each inverter is then controlled to deliver its portion of the total current [57–60]. Because the master/slave and current sharing methods both require system-level control, they do not offer a genuinely distributed “plug and play” approach to microgrid design.

In recent years, droop control has emerged as the predominant microgrid inverter control technique which requires no explicit communication [61,62]. This method, as originally proposed in [63], is based on controlling an inverter such that the fre-
quency and output voltage are inversely proportional to the real and reactive power output, respectively [8, 64–66]. These relations, which are generally referred to as the $P$-$\omega$ and $Q$-$V$ droop equations, are similar to the physical behavior exhibited by a conventional synchronous generator in a power system. As a result, a system of droop controlled inverters mimics the behavior of a system of synchronous generators [66, 67]. Droop control has been applied to both three-phase and single-phase systems [68] and recent efforts are largely focused on improving sharing accuracy among inverters [69,70]. Several modifications to the original $P$-$\omega$ and $Q$-$V$ droop relations have been proposed in [71]. Recently, it has been shown that droop controlled inverters can be analyzed as coupled Kuramoto oscillators and that a sufficient condition for convergence and system stability can be attained [67, 72, 73].

In this work, an alternative control technique based on coupled oscillator theory is presented. Using a method called virtual oscillator control, each inverter will be controlled to behave as a nonlinear oscillator circuit. The proposed synchronization-based method differs from droop-control in several respects. In particular, the proposed control:

- Does not require computation of the real and reactive power output.
- Maintains system frequency regardless of load fluctuations.
- Does not require an explicit phase angle and voltage amplitude command for the inverter ac output.
- Can be guaranteed to synchronize over all initial conditions.

1.3 Organization

This work presents methods coordinating the behavior of distributed inverter systems to achieve system-level objectives. In particular, an emphasis is placed on methods for distortion cancellation and control of inverter based microgrids. Chapter 2 presents foundational concepts of inverters, PWM, PV, and control that will be utilized throughout the rest of the dissertation.

In Chapter 3, a method of controlling a system of cascaded inverters is proposed such that energy generated by multiple dc sources is delivered to an ac load. The proposed control is able to accommodate non-uniform power generation among a
system of PV elements at the inputs such that each PV source is operated at its maximum power point and system stability is maintained. Furthermore, a low-distortion output waveform can be generated while employing a very low switching frequency and small output filter. The proposed control is developed such that it can be applied to very large numbers of cascaded H-bridge inverters. Both simulation and experimental are presented.

An investigation of switch interleaving in parallel inverter systems is carried out in Chapter 4. The main contribution of this chapter is the formulation of a closed-form expression which can be used to assess ripple cancellation among $N$ parallel connected converters. The resulting expression is general and can be used to analyze both dc-dc systems and inverters. Combining the advantages of switch interleaving with the latest advances in PV cell technology, a three-phase microinverter design is also proposed.

Chapters 5 and 6 are both focused on developing a method for controlling $N$ parallel inverters such that they form a stable islanded microgrid. The proposed control scheme does not require communication between inverters beyond the coupling inherently introduced by the electrical network. In Chapter 5, we derive a sufficient condition for the synchronization of $N$ parallel oscillators coupled in a network with linear time-invariant (LTI) circuit elements (resistors, capacitors, inductors, and transformers). It is shown that the condition is independent of the number of oscillators and the load parameters. Theoretical results are applied in Chapter 6 where a design procedure and method for hardware implementation are developed. A method for adding inverters into an energized microgrid is also introduced. Both simulation and experimental case studies are presented to validate the analytical results and demonstrate the proposed application.
Chapter 2

BACKGROUND

Fundamental principles of inverters, PWM, control, and PV will be described in this chapter.

2.1 Inverters

Throughout the dissertation, it will be necessary to describe and analyze triangular waveforms. In light of this, a triangular waveform of amplitude one will be denoted with the function $f_{tri}(t - \phi, S, T)$, where $T$ is the period, and $\phi$ is the time-shift. The symmetry of the waveform is described by $S \in [0, 1]$ which is defined as

$$S = \frac{t_+}{T}, \quad (2.1)$$

where $t_+$ is the time interval during which the slope of $f_{tri}$ is positive. If $S = \frac{1}{2}$, the waveform is a symmetric triangle wave and if $S$ is 0 or 1, the waveform is a sawtooth. The function $f_{tri}$, which will be used to describe both current ripple and PWM carrier waveforms, is illustrated in Fig. 2.1.

![Figure 2.1: Triangular waveform.](image-url)
2.1.1 Half-Bridge Inverter: 2-Level PWM

The half-bridge converter is shown in Fig. 2.2. This elementary circuit will form the basis of the inverters considered in this thesis. The half-bridge converter is operated by generating on/off commands for each switch such that one and only one switch is closed in the switch leg at each instant in time. The most common PWM method for controlling such a circuit is called *sine-triangle PWM*.

![Figure 2.2: A half-bridge converter with sine-triangle PWM.](image)

This method relies on the presence of a high frequency *carrier* signal and a low-frequency control signal called a *modulation* signal. The carrier is a periodic waveform and is most commonly a triangular or sawtooth waveform that varies between ±1 during each period. The instantaneous magnitude of the slower moving modulation signal, denoted as \( m \), and the carrier waveform are then compared such that their intersections correspond to switch transitions. As illustrated in Fig. 2.2, this operation is carried out using a comparator which generates a binary high or low signal which controls the switching semiconductor devices. In this work, power transistors will be modeled as ideal controllable switches. As an example, a set of carrier and modulation signals are shown in Fig. 2.3 along with the resulting voltage output, \( v_o \). The output voltage waveform in Fig. 2.3 is said to provide two levels because it alternates between the two distinct voltages of \( \pm \frac{V_{dc}}{2} \).

Assuming the carrier frequency is much higher than the modulation frequency, the average inverter voltage over a small time interval is equal to \( m \frac{V_{dc}}{2} \) [74]. The average over a small moving time window is referred to as the *fast average* and will be denoted as \( \langle v_o \rangle \). The output voltage of a half-bridge inverter can be controlled to follow a commanded value, \( v^* \), by selecting the modulation signal, \( m \), to be equal to...
Figure 2.3: PWM control signals and half-bridge inverter output voltage.

\[ v^* \frac{2}{V_{dc}} \text{ such that} \]

\[ \langle v_o \rangle = m \frac{V_{dc}}{2} = v^* \frac{2}{V_{dc}} \frac{V_{dc}}{2} = v^*. \]  

(2.2)

Consequently, the half-bridge inverter acts as a controllable voltage source by means of manipulating the modulation signal, \( m \).

2.1.2 H-Bridge Inverter: 3-Level PWM

Consider the circuit in Fig. 2.4, which can be thought of as being composed of two parallel half-bridge voltage source inverters. This circuit is called an \textit{H-bridge inverter}. Three-level PWM relies on the presence of a modulation signal, \( m \), a

Figure 2.4: An H-bridge converter with 3-level sine-triangle PWM.
carrier waveform, and two comparators. As shown in Fig. 2.4, the original carrier waveform and an inverted version are each applied to a comparator. By comparing the instantaneous modulation and carrier magnitudes, the voltages in Fig. 2.5 result. Because the voltage output, \( v_o \), takes on values of \( \pm V_{dc} \) and zero, this method is said to provide 3 levels. As before, one and only one switch is closed in each leg at every instant in time. A zero output voltage is achieved when the bottom pair or top pair of switches (1,1’ or 2,2’) are closed. In such a state, the output terminals are short circuited through the closed switches. A non-zero voltage results when any two complementary switches (1,2’ or 2,1’) are closed.

A close inspection of Fig. 2.5 will reveal that the output voltage, \( v_o \), equals \( +V_{dc} \) when the instantaneous modulation signal is greater than both carrier waveforms. Similarly, the output voltage takes on a value of \( -V_{dc} \) when the modulation signal is less than the carriers and is otherwise zero. Assuming the modulation signal is sinusoidal, its peak amplitude is referred to as the modulation depth. The moving average of output voltage, \( \langle v_o \rangle \), is equal to \( mV_{dc} \). By selecting the modulation signal as \( \frac{v^*}{V_{dc}} \), it follows [74] that

\[
\langle v_o \rangle = mV_{dc} = \frac{v^*}{V_{dc}} V_{dc} = v^*. \tag{2.3}
\]

As with the half-bridge inverter, the output voltage of the H-bridge can be controlled to follow a desired average value, \( v^* \), by properly selecting the modulation signal.

As with the half-bridge inverter, the output voltage of the H-bridge can be controlled to follow a desired average value, \( v^* \), by properly selecting the modulation signal.
2.1.3 Three-Phase Inverter

The last type of inverter topology we consider is the three-phase hex-bridge inverter. As shown in Fig. 2.6, this type of inverter can also be controlled with sine-triangle PWM. This type of inverter is made up of three parallel connected half-bridge inverters. The three legs are typically controlled with a set of three-phase modulation signals, \( m_a \), \( m_b \), and \( m_c \), which are each shifted by \( 0 \), \( -\frac{2\pi}{3} \) rad, and \( +\frac{2\pi}{3} \) rad, respectively. One key advantage of the three-phase inverter is that the total power delivered at the output is constant under balanced conditions. This feature of the three-phase inverter will be utilized in Chapter 4.

Figure 2.6: An three-phase voltage source inverter with sine-triangle PWM.

2.2 Photovoltaics

The PV cell is the fundamental building block of a PV power system. Each PV cell converts incident solar radiation (insolation) into electrical current. A PV module is generally composed of several series-connected PV cells which are enclosed within a frame under glass. Higher power levels can be attained by connecting PV modules in various series and parallel combinations. In particular, a PV string is built from several series-connected PV modules, and an array is a collection of parallel strings.
To facilitate analysis of PV systems, it is useful to have a model which captures the electrical behavior of a collection of cells. The single-diode model, as shown in Fig. 2.7, can be used to model the electrical behavior of \( N \) series PV cells. In this model, \( I_{ph} \) is called the photocurrent, \( R_{sh} \) is the shunt resistance, and \( R_s \) is the series resistance. The photocurrent, \( I_{ph} \), is proportional to the insolation and the resistances account for various sources of loss such as contact resistance. The PV current, \( i_{pv} \), can be expressed \[75\] as

\[
i_{pv} = I_{ph} - I_s \left( e^{\frac{v_{pv} + i_{pv}R_s}{nNVT}} - 1 \right) - \frac{v_{pv} + i_{pv}R_s}{R_{sh}} ,
\]

where \( n \) is the ideality factor, \( I_s \) is the diode saturation current, and \( V_T \) is the diode junction thermal voltage which is given by

\[
V_T = \frac{kT}{q} .
\]

In (2.5), \( k \) is the Boltzmann’s constant \( (1.38065 \times 10^{-23} \text{ J/K}) \), \( T \) is the temperature in Kelvin, and \( q \) is the charge of an electron \( (1.602 \times 10^{-19} \text{ C}) \). Because \( R_{sh} \) and \( R_s \) typically have very large and small values, respectively, they are often omitted to yield the following simplified \[75\] relationship:

\[
i_{pv} = I_{ph} - I_s \left( e^{\frac{v_{pv}}{nNVT}} - 1 \right) ,
\]

A representative example of the \( i-v \) curve for a PV module is given in Fig. 2.8(a). As shown in Fig. 2.8(b), the module has a unique voltage which yields maximum power. This is called the maximum power point. Operation at the maximum power point can be sustained by controlling a power electronic circuit with a maximum power point tracking (MPPT) algorithm.
2.2.1 Maximum Power Point Tracking

In a PV system, the function of the MPPT is to control a power electronic circuit such that the power extracted from a group of PV elements is maximized. There are a variety of MPPT algorithms as summarized in [76]. However, most algorithms share several common features. As shown in Fig. 2.9, the measured PV current and voltage are processed to generate a command. Depending on the type of implementation, the command could correspond to a switching duty ratio, PV voltage, or PV current. In this dissertation, it will be assumed that the MPPT algorithm generates a PV voltage command, $v_{pv}^*$. As shown in Fig. 2.9, the error is calculated by taking the difference between the actual and commanded voltage. The error is then processed by a controller which regulates the power converter. Ideally, the control should drive the error signal to zero such that $v_{pv} \rightarrow v_{pv}^*$.

One of the most widely used MPPT algorithms is the perturb and observe algorithm. This method works by perturbing the command by a small amount in one direction (either increase or decrease) and observing the impact on the measured
power. If the power increases as a result of the perturbation, another step is taken in the same direction. Otherwise, the command is adjusted in the opposite direction. This particular algorithm is used throughout the dissertation for both simulation and experimental results.

2.3 Closed-Loop Inverter Control

In this section, a brief overview of linear control principles is given. At the end of the chapter, a grid-connected PV system with closed-loop control will serve as an illustrative example.

2.3.1 Linear Control Fundamentals

Consider the system in Fig. 2.10. The system consists of a controller and a physical system which is referred to as the plant. It will be assumed that the control and plant are both linear and time-invariant (LTI) such that they can both be represented by transfer functions, $H(s)$ and $G(s)$, respectively. The plant input signal, $u$, represents the control variable and the measured output, $y$, denotes the quantity which must be regulated. The error, $e$, is the difference between the command, $y^*$, and measured value of $y$. Since the system forms a loop, this is referred to as closed-loop control.

![System with closed-loop control](image)

**Figure 2.10: System with closed-loop control.**

The Laplace transformed variables $U(s)$, $E(s)$, $Y(s)$, and $Y^*(s)$ correspond to the time-domain variables $u$, $e$, $y$, and $y^*$, respectively. The output of the plant can be expressed as

$$Y(s) = G(s)U(s), \quad (2.7)$$
and the plant input is given by

\[
U(s) = H(s)E(s) = H(s)(Y^*(s) - Y(s)). \tag{2.8}
\]

Substituting (2.7) into (2.8) and solving for \(\frac{Y(s)}{Y^*(s)}\) gives

\[
\frac{Y(s)}{Y^*(s)} = \frac{G(s)H(s)}{1 + G(s)H(s)}. \tag{2.9}
\]

It follows that if \(|G(s)H(s)| \gg 1\), then \(\frac{Y(s)}{Y^*(s)} \approx 1\), which implies the output signal, \(y\), will track the command, \(y^*\). The quantity \(G(s)H(s)\) is referred to as the loop-gain. Using established design methods such as loop shaping [74, 77], the controller, \(H(s)\), is designed based on the properties of the loop-gain. Using such an approach, the system can be controlled to meet metrics associated with steady-state error, bandwidth, disturbance rejection, and stability.

Unless otherwise stated, each controller in this dissertation will take the particular form shown in Fig. 2.10. This type of controller is called a PI controller and its transfer function can be written as \(H(s) = \frac{k_i}{s} + k_p\), where \(k_i\) and \(k_p\) are referred to as the integral and proportional gains. Since \(\lim_{\omega \to 0} |H(j\omega)| = \infty\), the PI controller gives zero steady-state error as \(t \to \infty\) for a dc command and in the absence of disturbances.

### 2.3.2 PV Microinverter with Closed-Loop Control

In this section, a grid-connected PV microinverter will be studied to demonstrate closed-loop control in a PV application and outline several foundational concepts for the rest of the dissertation. Consider the two-stage microinverter shown in Fig. 2.11. This particular circuit consists of: i) an input stage which steps-up the voltage provided by the PV module and tracks the maximum power point, ii) a capacitive dc-link which decouples the input and output energy flow, iii) a dc-ac conversion stage, and iv) an output filter.

Conventional PV modules produce a relatively low voltage (20 V to 70 V) and the peak ac voltage in 120 V and 240 V single-phase ac systems reaches approximately 170 V and 340 V, respectively. In general, the dc-link voltage, \(v_{dc}\), must exceed the peak grid voltage for the H-bridge inverter to be operational [74]. Consequently,
the dc-link voltage often reaches and exceeds 400 V. Given the large output to input voltage ratio across the dc-dc converter, it is common to use an isolated dc-dc converter topology which contains a high-frequency step-up transformer [5]. In a conventional centralized inverter, the input-stage can be omitted since the PV string voltage is sufficiently high. Below, the operation of the controllers in Fig. 2.11 will be outlined.

We begin by considering the input stage. The MPPT generates an input voltage command, $v_{\text{pv}}^*$, and a PI controller regulates the dc-dc converter duty ratio, $d$, such that $v_{\text{pv}} \to v_{\text{pv}}^*$. In effect, the dc-dc converter is controlled to regulate its input voltage to extract maximum PV power. During steady-state insolation, the PV module generates constant power which is delivered to the dc-link [75].

The inverter stage is controlled to simultaneously regulate the dc-link voltage at its input and the ac current at the output. The measured dc-link voltage, $v_{\text{dc}}$, is compared to dc-link setpoint, $V_{dc}^*$, and the error is processed by a PI controller which generates the commanded ac current amplitude, $i_{pk}^*$. The phase-locked-loop (PLL) is designed to track the ac grid voltage angle. Expressing the grid voltage as $\sqrt{2}V \sin(\omega_o t)$, the PLL output equals $\sin(\omega_o t + \phi)$, where $\phi$ is the desired ac current phase shift. Assuming unity power factor operation is desired, then $\phi = 0$. The sinusoidal ac current command, $i^*$, is compared to the measured current, $i_o$, and the error is applied to a current controller which generates a sinusoidal modulation signal, $m$. Three-level PWM can then be used to generate the switching signals for
the H-bridge.

In this dissertation, the proportional-resonant (PR) current controller is used at several points [78]. The transfer function of the PR controller is

$$H_{PR}(s) = \frac{k_i s}{s^2 + \omega_o^2} + k_p.$$  \hspace{1cm} (2.10)

Because first term has infinite gain at the grid frequency, \(\omega_o\), it follows that the loop-gain for the ac output current control also has infinite gain at \(\omega_o\). Theoretically, the PR controller is able to follow a 60 Hz sinusoidal reference with zero steady-state error.

Writing the output current of a microinverter as \(i_o = \sqrt{2}I \sin(\omega_o t)\), the output power is

$$P_{\text{grid}}(t) = i_o(t) v_{\text{grid}}(t) = \left(\sqrt{2}I \sin(\omega_o t)\right)\left(\sqrt{2}V \sin(\omega_o t)\right)$$

$$= 2IV \sin^2(\omega_o t)$$

$$= P_o - P_o \cos(2\omega_o t), \hspace{1cm} (2.11)$$

where \(IV = P_o\). As (2.11) implies, the output power consists of a dc component and a fluctuating ac component which varies at twice the grid frequency. Neglecting power conversion losses and assuming constant dc power from the PV source, energy conservation can be used to show \(P_o = P_{\text{pv}}\) [75]. As shown in Fig. 2.12, the average value of \(P_{\text{grid}}\) is equal to the power generated by the PV.

Given that the input and output power can have a large difference as shown in Fig. 2.12, the converter must store and extract this difference in the dc-link capacitor. This is referred to as energy decoupling [79]. The bottom waveform in Fig. 2.12 shows that the voltage across the dc-link capacitor is regulated such that its average value equals \(V_{dc}\). When \(P_{\text{grid}} > P_{\text{pv}}\), power is extracted from the capacitor and its voltage decreases. When \(P_{\text{grid}} < P_{\text{pv}}\), excess PV energy is stored in the dc-link and its voltage increases. Denoting the dc-link peak-to-peak ripple magnitude as \(\Delta v\), it can be shown that the required dc-link capacitance can be approximated [75, 79] as

$$C = \frac{P_{\text{pv}}}{\omega_o V_{dc} \Delta v}, \hspace{1cm} (2.12)$$

in the limit of small ripple.

It is evident that the required capacitance is proportional to the rated PV power.
Figure 2.12: Dc-link energy storage dynamics.

and inversely proportional to the dc-component of the capacitor voltage and ripple. To improve reliability, recent designs use film decoupling capacitors instead of electrolytic capacitors which are prone to drying. However, the low energy-storage density of film capacitors can result in a bulky and expensive decoupling stage.

The output filter inductor is used to minimize distortion on the output waveform. The total distortion present in the output current will be quantified with total harmonic distortion (THD), which is defined \[80\] as

\[
\text{THD} = \sqrt{\sum_{j=2}^{\infty} \frac{I_j^2}{I_1^2}} \approx \frac{\text{unwanted components}}{\text{fundamental component}},
\]

(2.13)

where \(I_j\) is magnitude of the \(j^{th}\) harmonic of the current \(i_o\). There exist several international and regional standards which specify limits on the harmonics present

<table>
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<th>harmonic order</th>
<th>(h&lt;11)</th>
<th>(11 \leq h &lt; 17)</th>
<th>(17 \leq h &lt; 23)</th>
<th>(23 \leq h &lt; 35)</th>
<th>(35 \leq h)</th>
<th>THD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Percent %</td>
<td>4</td>
<td>2</td>
<td>1.5</td>
<td>0.6</td>
<td>0.3</td>
<td>5</td>
</tr>
</tbody>
</table>

Table 2.1: Maximum harmonic distortion of current as specified in IEEE 1547
in the current waveform of an inverter. In particular, IEEE 1547 Clause 4.3.1 states that the harmonic content must satisfy the limits in Table 2.1 and the THD must be kept below 5%. In forthcoming simulations, the primary aim will be to satisfy the 5% THD limit.
Chapter 3

INTERLEAVED AND CASCADED H-BRIDGES

In this chapter, a switch interleaving technique is developed and applied to single-phase multilevel inverters. Given a system with \( N \) isolated dc sources interfaced by H-bridge inverters, a multilevel inverter system will be created by connecting the H-bridge outputs in series. The primary contribution of this work is the development of a control system which can manage non-uniform energy generation among the dc inputs. By combining the switch interleaving technique with the proposed control, the system of inverters is controlled such that the \( N \) dc sources deliver power to an ac load. Furthermore, a low-distortion output waveform can be generated while employing a very low switching frequency and small output filter.

3.1 Interleaved and Cascaded H-bridge Inverters

Consider a system of \( N \) independent dc sources which are each interfaced by an H-bridge inverter. The multiple inverters are connected in series to create a larger multilevel inverter. With the proposed configuration, \( N \) isolated dc sources can deliver power to a single ac load. As shown in Fig. 3.1, the output voltage of the \( k^{th} \) H-bridge and the total voltage across the system will be denoted as \( v_k \) and \( v_o \), respectively. The dc voltage across the \( k^{th} \) dc-link is \( v_{ck} \).

Each H-bridge will utilize an interleaved carrier waveform that is shifted by a unique multiple of \( \Delta t \). Using notation from Chapter 2, the carrier of the \( k^{th} \) sub-inverter can be expressed as \( f_{11} (t - k\Delta t, S, T_{sw}) \), where \( S \) describes the symmetry of the carrier waveform. As defined in Section 2.1, \( S = 1/2 \) corresponds to a symmetric triangular carrier and if \( S \) is 1 or 0, the waveform is a sawtooth with positive or negative slope, respectively. If sawtooth carriers are used, then \( \Delta t = \frac{T_{sw}}{N} \). Alternatively, if symmetric triangular carriers are used, then \( \Delta t = \frac{T_{sw}}{2N} \). From here forward, the time time-shift will be denoted as \( \Delta t \) regardless of the carrier shape.
In existing literature, this approach is generally referred to as phase-shifted carrier PWM \([29, 32]\).

Assuming each dc-link voltage is equal such that \(v_{ck} = V_{dc}\) for \(k = 1, \ldots, N\), the output voltage can take on values of \(0\ V, \pm V_{dc}, \pm 2V_{dc}, \ldots, \pm NV_{dc}\). Because \(2N + 1\) distinct output voltages are possible, an ac output waveform with very low distortion can be created. In general, the distortion generated by the system decreases as the number of H-bridges increases. A detailed study of harmonics in multilevel inverters is given in \([32]\). Furthermore, as \(N\) grows larger, the switching frequency can be lowered such that losses are minimized and the size of the output filter can be decreased substantially. Next, the behavior of the cascaded H-bridge system will be compared when sawtooth and symmetric triangular carrier waveforms are used.

**Interleaved PWM with Sawtooth and Triangular Carriers**

To begin, it is assumed that an identical sinusoidal modulation signal, \(m\), with period \(T\) is applied to the comparators of each H-bridge and 3-level PWM is utilized.
To illustrate the proposed method, two example systems which are each composed of four series-connected H-bridges will be considered. Each respective system will use sawtooth and symmetric triangular carriers such that the carrier of $k^{th}$ H-bridge can be expressed as $f_{HT} \left(t - k \frac{T_{sw}}{4}, 1, T_{sw}\right)$ and $f_{HT} \left(t - k \frac{T_{sw}}{4 \times 2}, 0.5, T_{sw}\right)$, respectively. Furthermore, in each system, a very low switching frequency is used such that the sawtooth and triangular carrier periods are $\frac{T}{b}$ and $\frac{T}{f}$, respectively. In this example, the sawtooth carrier frequency was chosen to be twice the triangular carrier frequency.

![Figure 3.2](image-url)

Figure 3.2: Interleaved carrier PWM waveforms and corresponding system voltages. Sawtooth carriers are used in (a) and symmetric triangular carriers are used in (b).

The pair of interleaved carrier pairs and modulation signal are shown in the top four plots of Figs. 3.2(a) and (b) for the two example systems. The voltage across the system, $v_o$, is equal to

$$v_o = \sum_{k=1}^{N} v_k. \quad (3.1)$$

As shown on the bottom of Figs. 3.2(a) and 3.2(b), both systems produce identical
9-level voltage waveforms. Also, the time-shift interval, $\Delta t$, is equal for both systems. Observing the voltage across the system, it is apparent that the effective switching frequency of the aggregate is equal to $N$ times switching frequency of each H-bridge.

The results in this illustrative example hold for arbitrary $N$. Overall, the technique relies on the fact that each of the H-bridges is generating a unique 3-level voltage waveform which varies between $\pm V_{dc}$ and 0. It then follows that if $N$ unique waveforms are added, the resultant waveform has $2N + 1$ levels with a peak-peak voltage magnitude of $2NV_{dc}$. Next, a control method for a multilevel grid-connected PV system will be developed.

### 3.2 Control for Grid-Connected PV

This section presents a method for controlling a multilevel inverter which interfaces $N$ PV sources to the grid [31]. The proposed system, as depicted in Fig. 3.3, is capable of maintaining system performance despite non-uniformity among the PV sources. In [33], a similar approach for PV system design was proposed which did not utilize dc-dc converters at the inputs. This system topology is composed of $N$ circuits which have a dc-dc converter at the input, a dc-link capacitor, and an H-bridge at the output. Each of these circuits will be referred to as a sub-inverter. All sub-inverters are connected in series and then interfaced to the grid via an inductive output filter. Energy balance is managed by a single master controller and $N$ local sub-inverter controllers.

The $k^{th}$ sub-inverter contains a dc-link capacitor with voltage $v_{ck}$, and the output voltage across its respective H-bridge is $v_k$. Power generated by the $k^{th}$ PV source will be denoted as $p_k$. The system delivers an output current, $i_o$, to the grid-utility, which is modeled as an ac voltage source, $v_{grid}$. As shown in Fig. 3.3, it is assumed that the total filter inductance, $L$, is divided into two into two inductors with value $L/2$.

A master controller is used to manage energy flow between the aggregate system of sub-inverters and the grid-utility. In particular, the main functions of the master controller are to regulate the output current, $i_o$, and to manage the total voltage across the dc-link capacitors. The master controller generates a master modulation signal, $m_{sys}$, which is then fed to the $N$ individual sub-inverter controllers. Each local controller then scales $m_{sys}$ to create a unique modulation signal, $m_k$, such

29
that the local dc-link capacitor voltage is regulated. In addition, each PV source is interfaced to a dc-dc converter which performs MPPT. From inspection of Fig. 3.3, it is apparent that the MPPT controllers are decoupled from the rest of the control system.

With the proposed controller, the task of capacitor voltage balancing is decomposed into two separate problems. Namely, the master controller regulates the aggregate sum of the capacitor voltages and the local controllers manage their respective dc-link voltage.

3.2.1 Master Controller

The master controller, as illustrated in Fig. 3.4, has two purposes: i) regulate the sum of the dc-link voltages to a prescribed value, and ii) deliver a sinusoidal output current to the grid. The first objective can be recast in terms of energy balance. Since the dc-link capacitors are energy storage devices, their voltages can be maintained by ensuring that the energy generated by the PV (minus losses) is delivered to the grid. The current control stage can be designed using conventional current control
methods. Each of the two master control sections is described below.

For the system in Fig. 3.3, the $k^{th}$ sub-inverter has access to its respective dc-link and PV power measurements, $v_{ck}$ and $p_k$. It will be assumed that by either direct measurements or communication, the summed quantities, $\sum_{k=1}^{N} v_{ck}$ and $\sum_{k=1}^{N} p_k$, reach the master controller. Denote the total power conversion losses, RMS output current, and peak output current as $p_{loss}$, $I_{rms}$, and $i_{pk}$. Energy conservation can be used to write

$$\left( \sum_{k=1}^{N} p_k \right) - p_{loss} = V_{rms} I_{rms} = V_{rms} \frac{i_{pk}}{\sqrt{2}}. \quad (3.2)$$

Assuming losses are small so that $p_{loss} \approx 0$, then

$$\sqrt{2} \frac{1}{V_{rms}} \sum_{k=1}^{N} p_k \approx i_{pk}. \quad (3.3)$$

It then follows that the quantity, $i_{approx}$, in Fig. 3.4 is approximately equal to the required peak output current for energy balance. However, because losses are uncertain and nonzero, an adjustment term, $i_{adj}$, is necessary. This adjustment term is generated by comparing the aggregate dc-link voltage to a fixed setpoint, $V_{dcNet}^*$, and feeding the error to a PI controller. The aggregate dc voltage command value, $V_{dcNet}^*$, must be chosen sufficiently higher than the peak grid ac voltage. The sum of $i_{approx}$ and $i_{adj}$ then form the peak output current command $i_{pk}^*$.

The second stage of the master controller is designed to synchronize to the grid and regulate the output current. As shown in Fig. 3.3, the measured grid voltage is utilized by a phase-locked-loop (PLL) to generate a sinusoidal reference, $\sin (\omega t)$,
which is in phase with the grid voltage. Here it is assumed that operation at unity power factor is desired. The PLL is conventional, as outlined in [81], for the proposed application. A sinusoidal current reference is created by multiplying the peak current command with \( \sin(\omega t) \). Lastly, a conventional current controller can be used to generate the system level modulation signal, \( m_{sys} \), which then goes to the \( N \) local controllers. In forthcoming simulations, a proportional-resonant controller, as described in Chapter 2 and [78], will be used. Overall, the master controller can be designed using established techniques.

### 3.2.2 Local Control

As illustrated in Fig. 3.3, each sub-inverter is equipped with a MPPT controller at the input. The function of the MPPT algorithm is to generate an input voltage command which the dc-dc converter is then controlled to track. In this work, it will be assumed that any generic MPPT algorithm can be used. Because each MPPT operates independently and functions solely to track the PV maximum power point, it will not be shown in the block-diagram of the proposed local controller.

![Possible sub-inverter configurations](image)

**Figure 3.5: Possible sub-inverter configurations.**

Before detailing the operation of the local controllers, it will be instructive to examine Fig. 3.5, which summarizes three possible sub-inverter configurations.\(^1\) Because each sub-inverter output is connected in series, the grid-current, \( i_o \), is also the output current of each sub-inverter. Figures 3.5(a) and 3.5(b) illustrate switch configurations which correspond to non-zero power delivery. In this arrangement, the output current is extracted from the dc-link capacitor and it tends to discharge. Conversely, Fig. 3.5(c) illustrates one of two possible switch states which yield zero power output. During this state, the sub-inverter is bypassed from the perspective of the output terminals. Regardless of the output switch states, the PV source and

\(^1\)In general, there are a total of 8 possible sub-inverter configurations due to the 4 possible switch states and 2 possible directions of current flow.
its dc-dc converter continue to deliver power to the dc-link. Using conservation of energy, it is apparent that the dc-link voltage can be regulated by choosing how long the sub-inverter delivers power or is bypassed at the output. However, rather than explicitly command each sub-inverter to go into one of these possible configurations, it is more practical and simple to use 3-level PWM.

![PWM Local controllers](image)

**Figure 3.6:** $N$ local controllers.

The collection of $N$ local controllers are shown in Fig. 3.6. The primary purpose of each controller is to regulate the dc-link voltage of its respective sub-inverter. As shown, each dc-link voltage is compared to a fixed dc reference, $V_{dc}^*$. This voltage reference is related to the aggregate dc-link command by

$$V_{dc}^* = \frac{V_{dcNet}^*}{N}. \quad (3.4)$$

The output of the $k$th PI controller is then multiplied by the master modulation signal, $m_{sys}$, to create the local modulation signal $m_k$. Ultimately, the local modulation signals and interleaved carriers are used to generate PWM signals which control each H-bridge inverter. As the modulation signal, $m_k$, is decreased in amplitude, the output power of the $k$th sub-inverter decreases and the capacitor charges up. Alternatively, the $k$th capacitor is discharged more heavily as the modulation depth decreases.
of \( m_k \) increases.

### 3.2.3 Summary

In this section, a control system has been outlined which manages power delivery from \( N \) PV sources to the ac grid. The proposed system is comprised of a single master controller and \( N \) local controllers. The master controller regulates the aggregate dc-link voltage and the output current while each local controller manages the individual dc-link voltage of each respective sub-inverter. Each PV source is interfaced with a dc-dc converter which performs MPPT. The proposed system is able to accommodate non-uniform power generation among the PV inputs while regulating a low-distortion ac output. Next, the proposed system will be demonstrated with a set of simulation and experimental results.

### 3.3 Simulation Results

In this section, the grid-connected system of 30 series sub-inverters in Fig. 3.7 will be simulated. To demonstrate a highly distributed application, a system of 10 PV modules, each fitted with three sub-inverters, will be considered. As shown in Fig. 3.7, each sub-inverter interfaces an isolated group of solar cells which make up 1/3 of the module. Because these connection points are normally accessible from the module junction-box, the three sub-inverters could reside there in a practical implementation. In such a case, each converter could be used to substitute conventional bypass diodes.

In each simulation, each module is rated for 250 W. Consequently, each sub-inverter is rated to deliver 1/3 the rated module power. The series connected system of 30 sub-inverters will behave as a 61 level inverter (recall the number of levels equals \( 2N + 1 \) in general). As illustrated in Fig. 3.7, the total filter inductance of 150 \( \mu \)H is divided by \( 2N \) and distributed among the output terminals of each sub-inverter as small 2.5 \( \mu \)H inductors. Since each sub-inverter output is connected in series, the combined effect of the distributed inductors is identical to a single large inductor.

Each sub-inverter utilizes a 900 Hz sawtooth carrier which is phase shifted by a unique multiple of \( \frac{T_{sw}}{N} \), where \( T_{sw} = \frac{1}{900} \) s. Because of switch interleaving, the
effective switching frequency of the aggregate system is equal to $N \times 900$ Hz. In general, there is a trade-off between the switching frequency and size of the output filter. For instance, a higher switching frequency enables the use of a smaller filter but results in higher losses (unless resonant switching is used). The 60 Hz power system is a split-phase ac grid with a 220 V line-line RMS rating (peak rating is approximately 311 V). To ensure the aggregate dc-link is sufficiently higher than the 311 V peak grid voltage, the net dc-link voltage command will be chosen as $V_{dc,Net}^* = 400$ V. It then follows that the $N$ local dc-link voltage commands are equal to $V_{dc}^* = \frac{V_{dc,Net}^*}{N} \approx 13.3$ V.

Each dc-link capacitance is equal to 5 mF. Since the voltage rating of the capacitor is relatively small, the energy stored in each dc-link is modest. Given the current state of capacitor technology, a variety of options exist. First, the conventional electrolytic capacitor can be used. However, the low reliability of this device makes it unattractive. Recent developments include the metal organic polymer capacitor. This device offers high capacitance at low voltage ratings while exhibiting higher reliability than electrolytic capacitors. However it is costly.

Below, two simulations will be provided. First, an ideal case will be considered where all PV modules are producing their rated power of 250 W and each sub-inverter transfers an identical amount of energy. In the second case, system behavior will be
examined under non-uniform conditions with severe partial shading.

3.3.1 Uniform Conditions: No Partial Shading

In this simulation, each sub-inverter was interfaced to an isolated set of PV cells which generate one-third of the rated module power. Each of the 10 modules has a maximum power of 250 W so that the total dc power is 2.5 kW. Utilizing the controller
devolved in Section 3.2(a), the system injects an ac current into the grid-utility. As shown in Fig. 3.8(a), a low-distortion output current waveform with only 2.5% of THD is generated. The 61-level voltage waveform, $v_{o}$, in Fig. 3.8(a) corresponds to the sum of the H-bridge inverter output voltages. In Fig. 3.8(a), $p_o$ denotes the total ac power delivered to the grid and is equal to the product of the output current, $i_o$, and the grid voltage. It is apparent that the average value of $p_o$ corresponds to the total PV power of 2.5 kW minus losses.

To facilitate a better understanding of the circuit-level dynamics, the output current, output voltage, dc-link voltage, and power delivery of the 1st sub-inverter are shown in Fig. 3.8(b). Because the converter outputs are connected in series, the

Figure 3.8: System-level output waveforms in (a) with uniform PV power generation. Output current has 2.5% THD. Waveforms corresponding to sub-inverter #1 are shown in (b).
output current of the sub-inverter is equal to the grid current, $i_o$. The 3-level voltage output, $v_1$, is equal to $\pm 1$ or zero times the dc-link voltage, $v_c$. The output power of sub-inverter #1, $p_{o1}$, as shown on the bottom of Fig. 3.8(b), is the product of $i_o$ and $v_o$. By inspection, it can be seen that the capacitor tends to discharge when the power output is non-zero. Conversely, the capacitor charges up when the sub-inverter is bypassed such that $v_o = 0$. The efficacy of the local controller is evident in how $v_c$ closely follows the dc-link voltage command, $V_{dc}^* \approx 13.3$ V.

3.3.2 Non-Uniform Conditions: Partial Shading

System behavior with non-uniform power generation among the PV modules will now be simulated. In particular, a case will be considered in which one module (and the solar cells which connect to its three sub-inverters) is severely shaded. In addition, the power generated among the remaining nine modules will be allowed to deviate from the rated value. In the following simulations, the solar cells which interface each sub-inverter are shaded in such a way that they generate $1/3$ the power of its respective PV module. The power generated by the each of the 10 modules

![Figure 3.9: System-level output waveforms in (a) with non-uniform PV power generation. Output current has 7.5% THD. Waveforms corresponding to sub-inverter #1 are shown in (b).](image-url)
is summarized in Table 3.1 as a percentage of the 250 W module rating. A 900 Hz switching frequency is maintained at each H-bridge.

<table>
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<tr>
<th>Module #</th>
<th>1</th>
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<th>3</th>
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<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>10</th>
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<td>104</td>
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</tbody>
</table>

As shown in Fig. 3.9(a), the system successfully injects an ac current into the grid. However, the THD now exceeds 5%. This result implies that the output distortion increases in proportion to the disparity in power delivered among sub-inverters. A benefit of the proposed implementation is that each PV module is operated at its maximum power point despite non-uniformity among the PV module $i-v$ characteristics. In a conventional system with series PV modules, the shaded module would disproportionately degrade system power delivery or it would be bypassed entirely.

Because we are particularly interested in how the control handles partial shading, Fig. 3.9(b) shows the waveforms of sub-inverter #1 which is connected to cells with severe shading (cells produce 20% rated power). By inspection of the output voltage, $v_1$, it is apparent that the output voltage is zero over most of the 60 Hz cycle such that the sub-inverter is bypassed. Note how the power, $p_{o1}$, is delivered in short bursts to prevent capacitor discharging. The dc-link voltage, $v_{cl1}$, successfully tracks the 13.3 V voltage command.

### 3.3.3 Converter and PV Failure Modes

It is generally desirable to have a PV system which is reliable, exhibits low maintenance costs, and has a long lifetime. By leveraging the distributed structure of the proposed multilevel inverter, there are opportunities to enhance system robustness to certain types of failures. For instance, if a PV element at one of the dc inputs stops functioning, its corresponding sub-inverter could be controlled such that it is bypassed from the system. Furthermore, if the aggregate dc-link voltage is sufficiently higher than the peak ac grid voltage, multiple failures among the dc inputs could be tolerated. For instance, the simulated system above could tolerate a maximum of six PV input failures while still maintaining a sufficiently high dc-link for grid-connected operation. Failures of the dc-dc converter failures would be handled similarly.
The main challenge is to ensure that H-bridge failures do not impede the reliability of the entire system. Typically, a power MOSFET either fails as an open-circuit or short-circuit between the drain and source terminals. If an H-bridge MOSFET fails as a short-circuit, continuity among the series-connected sub-inverters is maintained and the faulty unit could simply be bypassed. Conversely, an open-circuit failure of a H-bridge MOSFET would affect the entire system. As a consequence, design and failure-mode analysis should be focused on minimizing the chance of open-circuit MOSFET failures in the H-bridges.

![Figure 3.10: Single H-bridge circuit shown in (a) and the system of 16 series H-bridges is given in (b).](image)

3.4 Experimental Results

This section offers a set of experimental results to confirm the proposed interleaved PWM method for multilevel inverters and the control system for multiple PV sources. The first set of experimental results corresponds to a system of 16 series-connected H-bridges which are controlled with interleaved PWM and a fixed sinusoidal modulation signal. The second set of experimental results will show a system of three sub-inverters which interface PV and utilize a closed-loop control system.
3.4.1 Cascaded H-bridges: Open-Loop Control

The experimental hardware consists of 16 series connected H-bridges as shown in Fig. 3.10. The input of each H-bridge is interfaced to an isolated dc-dc converter which provides a fixed 5 V dc voltage. The series connected H-bridges are connected across a RL load which consists of a 100 Ω resistor in series with a 300 μH inductor. Each H-bridge utilizes a pair of 180 Hz sawtooth carriers that are phase-shifted by a unique multiple of $\frac{1}{16\times180}$ and a common 60 Hz modulation signal was used. The modulation signal was created using an analog signal generator while the interleaved carriers, comparators, and gate logic signals were implemented on an Altera Cyclone II FPGA. Figure 3.11(a) shows the voltage across one three-level H-bridge inverter, the total voltage across the 16 series H-bridges, and the load current. Figure 3.11(b) contains the system modulation signal and the resulting PWM comparator outputs corresponding to one leg of each H-bridge.

3.4.2 PV System: Closed-Loop Control

The experimental hardware system consists of three PV modules which are each interfaced with a sub-inverter circuit as shown in Fig. 3.12. Each of the sub-inverters is composed of a boost converter at the input, a dc-link, an H-bridge, and an inductive output filter. All switching semiconductor devices are N-channel MOSFETs. The system of three cascaded sub-inverters delivers power to a single RL load. The circuit
Figure 3.12: Sub-inverter hardware shown in (a) and the experimental system with 3 PV modules is given in (b).

parameters of the sub-inverter, as labeled in Fig. 3.12, are summarized in Table 3.2.

<table>
<thead>
<tr>
<th></th>
<th>$C_{in}$</th>
<th>$L_{in}$</th>
<th>$C$</th>
<th>$L$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>68 $\mu$F $\times$ 4</td>
<td>100 $\mu$H</td>
<td>68 $\mu$F $\times$ 6</td>
<td>100 $\mu$H</td>
</tr>
</tbody>
</table>

Because the system is not grid connected, the control system developed in Section 3.2 can be simplified. In particular, the master controller can be removed entirely such that the master modulation signal, $m_{sys}$, is a fixed 60 Hz sinusoidal waveform of amplitude one. As shown in Fig. 3.13, the master modulation signal is applied to the three local sub-inverter controllers which regulate the dc-link voltages. Each dc-link voltage measurement is processed by a first-order low-pass filter with cutoff frequency $f_{lpf}$. The three resultant modulation signals and interleaved waveforms are used to generate the switching signals of each H-bridge. In each experiment, the interleaved carriers were sawtooth waveforms which were each phase-shifted by a unique multiple of $\frac{T_{swH}}{3}$, where $T_{swH} = \frac{1}{f_{swH}}$. The controllers in Fig. 3.13 were
implemented on a single Texas Instruments TMS320F28335 microcontroller.

Each of the three boost converter stages utilized the controller in Fig. 3.14. The $k^{th}$ PV current and voltage, denoted as $i_{pk}$ and $v_{pk}$, respectively, are multiplied to calculate the power entering the sub-inverter. Each power measurement is then processed by a perturb and observe MPPT algorithm which generates an input voltage command, $v_{pk}^*$. Subsequently, a PI controller generates a boost switching duty ratio such that the input voltage closely follows the MPPT voltage command. Lastly, the duty ratio is compared to a sawtooth carrier with frequency $f_{swB}$, where $f_{swB}$ corresponds to the boost converter switching frequency. The control parameters for both the boost and H-bridge controllers are given in Table 3.3. Parameters $k_{pB}$ and $k_{iB}$ denote the proportional and integral gains of the local H-bridge controllers in Fig. 3.13. Similarly, $k_{pB}$ and $k_{iB}$ correspond to the proportional and integral settings of the boost converter controllers as shown in Fig. 3.14. The MPPT perturbation time period is $T_{PO}$ and the voltage adjustment step size is 0.3 V.

Table 3.3: Control parameters

<table>
<thead>
<tr>
<th>$k_{pH}$</th>
<th>$k_{iH}$</th>
<th>$k_{pB}$</th>
<th>$k_{iB}$</th>
<th>$T_{PO}$</th>
<th>$f_{pf}$</th>
<th>$V_{dc}$</th>
<th>$f_{swB}$</th>
<th>$f_{swH}$</th>
<th>$\omega$</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.75x10^{-3}</td>
<td>0.1</td>
<td>20</td>
<td>1x10^{-7}</td>
<td>1 sec</td>
<td>5 Hz</td>
<td>60 V</td>
<td>50 kHz</td>
<td>10 kHz</td>
<td>$2\pi f_{tsw}$</td>
</tr>
</tbody>
</table>
In each experiment, the $i$–$v$ curve of each module was emulated with the parallel combination of a power supply and a dark PV module. Figure 3.15(a) shows the configuration of the PV emulation hardware. As illustrated, a dc power supply is connected in series with an inductor. The dc power supply can act as a current source by configuring it to operate in current limiting mode (this feature is available on most dc power supplies). During such operation, the power supply alters its voltage output such that the average output current does not exceed the set limit. In effect, the power supply and series inductor act as a constant current source as shown in Fig. 3.15(b). The resulting system is similar in structure to the single-diode model and behaves as an illuminated PV source, which will be denoted with the symbol in Fig. 3.15(c). Further details and discussion of this PV emulation method are given in [82]. Because the current limit, $I_{dc}$, is adjustable, different intensities of insolation can be easily emulated.

Below, experiments will be conducted for both uniform and non-uniform conditions among the PV inputs. In each experiment, Kenwood model P56-10D power supplies and BP model 7190S PV modules were used. The load consists of 62.5 Ω resistor in series with a 600 µH inductor. First, consider the case where all PV modules produce approximately the same power. Next, partial shading will be emulated such that the three PV sources produce different power.
3.4.2.1 Uniform Conditions

In the following experiments, each PV emulation circuit was configured such that the maximum power point was approximately 42.5 W. The sum of the voltages across the three H-bridges is illustrated in the 7-level waveform of Fig. 3.16. The individual H-bridge voltages and output current are shown in Fig. 3.17. As illustrated, each of the three H-bridges generates a 3-level voltage waveform. Furthermore, as shown in Fig. 3.17(b), the switch transitions are interleaved by one-third of the switching period. Because each of the sub-inverters is delivering approximately the same amount of power (within ±5%), the modulation depths of the H-bridges are also equal. This can be validated by observing by the voltage waveforms in Fig. 3.17(b).

As given in Table 3.3, the dc-link voltage command, \( V_{dc}^* \), was chosen as 60 V. Referring to the oscilloscope screenshot in Fig. 3.18, it is clear that each of the dc-link RMS voltages was successfully maintained at the desired voltage. Note that the dc-link voltage exhibits a 120 Hz ac component which is superimposed on the 60 V dc value. This is due to the 120 Hz ac power which exits the sub-inverter output.

The PV voltages at the input of the sub-inverters are shown in Figs. 3.19. As the results show, the input voltages closely track the PV maximum power voltage of 36.5 V. This verifies the functionality of the MPPT algorithm and the PI controller.
of the boost converters. As is evident in Fig. 3.19, there is a small 120 Hz ac component on the input waveforms. This is primarily due to the 120 Hz output power of the inverter propagating through to the sub-inverter inputs. In other words, the fluctuating output power manifests itself as a disturbance at the sub-inverter inputs.

3.4.2.2 Non-Uniform Conditions

In this experiment, the desire was to mimic a PV system with partial shading. This was accomplished by setting PV emulation sources #1, #2, and #3 to have maximum power points of approximately $14 \times 3\,\text{W}$, $14 \times 2\,\text{W}$, and $14\,\text{W}$, respectively. The net voltage across the three H-bridges is shown in Fig. 3.20. As confirmed in Fig. 3.21(b), the modulation depths of the three corresponding H-bridges are proportional.
to PV power. In other words, the output voltage of H-bridge #3 is zero for a greater proportion of the ac period because it delivers less power to the output.

After comparing Figs. 3.17 and 3.21, it can be observed that the current output waveform has more distortion as compared to the measurements under uniform conditions. It should be noted that the current ripple in this case would still be smaller in comparison to a system with no interleaving because of the increase in the effective switching frequency. Specifically, the effective output switching frequency of this system is $3 \times 10\, \text{kHz}$, whereas the effective switching frequency of a system with no interleaving would be $10\, \text{kHz}$. As a consequence, the interleaved system would still provide a lower ripple in comparison to a traditional system non-uniform conditions.

The dc-link voltages are shown in Fig. 3.22. As indicated by the RMS measurements on the oscilloscope screenshot, the three dc-link voltages closely follow the 60 V command. This result confirms the effectiveness of the local controllers in Fig. 3.13 despite non-uniform conditions.

For this test, the three PV voltages are shown in Fig. 3.23. As the measurements illustrate, the MPPT and boost converter controllers were able to regulate the input voltage such that they closely followed the PV maximum power points. As in Fig. 3.19, there is a 120 Hz ac component on input waveforms due to fluctuating ac output power.
Figure 3.20: Measured 7-level voltage across 3 H-bridges during non-uniform PV conditions.

3.5 Conclusion

In this chapter, a control technique based on interleaved carrier 3-level PWM was put forward. It was shown that capacitor voltage balancing in the system of cascaded H-bridges is achievable under uniform and non-uniform conditions at the PV inputs and the proposed method can be applied to very large numbers of inverters. Simulation and experimental results were presented to validate the proposed method. In the next chapter, switch interleaving will be used to coordinate a system of parallel inverters.
Figure 3.21: Output current and output voltages across each sub-inverter H-bridge.

Figure 3.22: Measured dc-link voltages.

Figure 3.23: Measured PV voltages.
Chapter 4

PARALLEL INTERLEAVED INVERTERS

An investigation of switch interleaving in parallel connected inverters is conducted in this chapter. The main contribution of this chapter is the formulation of a closed-form expression which can be used to analyze the output current of parallel interleaved converters. This result is presented with a level of generality such that it can be applied to both dc-dc and inverter systems. Experimental results are used to validate the analytical model. Furthermore, a cost-effective design for a three-phase microinverter is proposed. This design is based on the benefits of interleaving and unique properties of emerging PV cell technologies.

4.1 Single Inverter

Consider a single grid-connected inverter, as illustrated in Fig. 4.1, with modulation signal, \( m \), and symmetric triangular carrier \( f_{\text{tri}}(t - \phi, \frac{1}{2}, T_{\text{sw}}) \), where \( f_{\text{sw}} = \frac{1}{T_{\text{sw}}} \) is the switching frequency. In such a system, the controller is designed to regulate the output current such that it follows a sinusoidal reference. As the experimental result in Fig. 4.1 shows, the measured output current consists of a desired fundamental sinusoidal component and an undesired high-frequency ripple component which resembles a triangular waveform on small time scales.

In light of this observation, the output current will be expressed as

\[
\begin{align*}
i_o &= \sqrt{2}I_o \sin(\omega t + \phi) + i_r \\
&= \sqrt{2}I_o \sin(\omega t + \phi) + I_r f_{\text{tri}} \left( t, \frac{1}{2} (1 + m), T_{\text{sw}} \right),
\end{align*}
\]  

(4.1)

where \( i_r \) encapsulates the ripple component, and in the second line the ripple was approximated as being a triangular waveform with amplitude \( I_r \). As expressed in (4.1), the symmetry of the triangular ripple is dependent on the modulation signal.
For the half-bridge inverter, the switch duty ratio, $d \in [0, 1]$, is equal to the symmetry parameter of the triangular ripple as defined in (2.1). It can be shown that the duty ratio and modulation signal are related by

$$d = \frac{1}{2} (1 + m).$$

(4.2)

In addition, as is evident in Fig. 4.1, the amplitude of the ripple, $I_r$, is also time-varying. Typically, the magnitude of the unwanted current ripple is reduced by using a larger filter inductance, a more complex filter structure, and/or increasing the switching frequency. However, these approaches have drawbacks since a larger filter adds costs and a higher switching frequency increases switching power loss.

### 4.2 System of Parallel Interleaved Inverters

Next, consider the system of $N$ parallel inverters in Fig. 4.2 connected across a load. To preserve generality, it will be assumed that the load can represent anything that absorbs the power delivered by the inverters. For instance, the load could be the grid, a passive load, or a mechanical load. Assuming all inverters produce an output current with an identical fundamental frequency and phase shift such they can be
written in the form of (4.1), the net load current is equal to

$$i_{\text{load}} = \sum_{k=1}^{N} i_{ok}$$

$$= \sum_{k=1}^{N} \left( \sqrt{2}I_k \sin (\omega t + \varphi) + i_{rk} \right)$$

$$= \sqrt{2} \sin (\omega t + \varphi) \sum_{k=1}^{N} I_k + \sum_{k=1}^{N} i_{rk}. \quad (4.3)$$

Further, if we assume that the fundamental component of each waveform is equal such that $I = I_1 = \ldots = I_N$, and all inverters are controlled with identical modulation signals $m = m_1 = \ldots = m_N$, then we obtain

$$i_{\text{load}} = N \sqrt{2}I \sin (\omega t + \varphi) + \sum_{k=1}^{N} i_{rk}. \quad (4.4)$$

In this work, it is proposed that the $k^{th}$ inverter utilizes a triangular carrier waveform equal to $f_{\text{tri}} \left( t - k \frac{T_{sw}}{N} \right)$, such that each carrier is phase-shifted by a unique multiple of $\frac{T_{sw}}{N}$. When applied to $N$ parallel inverters, the net current can be written
as

\[
  i_{\text{load}} = N\sqrt{2}I \sin(\omega t + \varphi) + \sum_{k=1}^{N} i_{r_k}
  \]

\[
  = N\sqrt{2}I \sin(\omega t + \varphi) + I_r \sum_{k=1}^{N} f_{tri} \left( t - k\frac{T_{sw}}{N}, \frac{1}{2} (1 + m), T_{sw} \right). \quad (4.5)
\]

This result follows from the fact that interleaved carriers imply interleaved ripple [44]. With this method, the triangular ripple components undergo cancellation once the currents sum together as \(i_{\text{load}}\), and the desired fundamental components constructively reinforce once summed. As a result, filtering components can be kept small while retaining a low distortion output. It will be shown that the degree of distortion cancellation grows with \(N\) and is dependent on the instantaneous value of the modulation signals. As shown in (4.5), the degree of ripple cancellation can be quantified by analyzing the superposition of \(N\) interleaved triangular waveforms. In the next section, a closed-form expression for \(\sum_{k=1}^{N} f_{tri} (t - k\frac{T_{sw}}{N}, S, T_{sw})\) will be given. Equipped with this analytical result, we will quantify the net ripple generated by a system of \(N\) parallel inverters controlled with identical modulation signals.

### 4.3 Superposition of \(N\) Interleaved Triangular Waveforms

This section provides a closed-form expression for the summation of \(N\) interleaved triangular waveforms. Because the derivation is lengthy, details are in Appendix A.1. A summary of results is provided below.

#### 4.3.1 Summary of Analytical Results

Given \(N\) interleaved triangular waveforms with amplitude one, symmetry \(d\), and period \(T\), it is possible to express the superposition of these waveforms as the product of a net amplitude and another triangular waveform with amplitude one. Specifically,

\[
  \sum_{k=1}^{N} f_{\text{tri}} \left( t - k\frac{T}{N}, d, T \right) = A f_{\text{tri}} \left( t - q\phi \frac{T}{2N}, \text{mod} (Nd, 1), \frac{T}{N} \right), \quad (4.6)
\]
where
\[
A = \frac{\mod (Nd, 1) (1 - \mod (Nd, 1))}{Nd (1 - d)}, \quad (4.7)
\]
\[
d' = \mod (Nd, 1), \quad (4.8)
\]
and
\[
q_\phi = \begin{cases} 
0 & \text{for } \mod (Nd, 2) \leq 1 \\
1 & \text{for } \mod (Nd, 2) > 1 
\end{cases}. \quad (4.9)
\]

The amplitude of the \(n^{th}\) harmonic of the net waveform is given by
\[
h_n = \begin{cases} 
N \frac{\sin(q_n d)}{n \pi d (1 - d)} & \text{for } n = N, 2N, 3N \ldots \\
0 & \text{otherwise}
\end{cases}. \quad (4.10)
\]

This shows that all harmonics except those that are multiples of \(N\) are canceled. Furthermore, if \(Nd\) is an integer, then all harmonics are equal to zero such that the net waveform is zero for all \(t\). This follows from the fact that \(\sin (X\pi) = 0\) when \(X\) is an integer.

The family of curves in Fig. 4.3 show the amplitude of the net waveform, \(A\), for various values of \(N\) as \(d\) is varied between 0 and 1. These were calculated analytically using (4.7). As is evident from Fig. 4.3, the amplitude of the net waveform tends to get smaller when \(N\) increases. Furthermore, there are always \(N - 1\) unique values of \(d\) between 0 and 1 which give perfect cancellation such that \(A = 0\).

Figure 4.3: The amplitude, \(A\), of the resultant waveform after interleaving for various values of \(N\) as a function of \(d\).

If these insights are applied to interleaved inverters, the following conclusions can be made:
a. The degree of ripple cancellation increases as the number of inverters grows.

b. The number of switch duty ratios which result in perfect cancellation increases with the number of inverters.

As a result, systems with larger numbers of interleaving inverters will produce less distortion. The analytical results in this section are general and can also be used to study systems of interleaved dc-dc converters.

4.3.1.1 Illustrative Example

An example case is considered when $N = 5$ and $d = \frac{1}{7}$. The individual waveforms and summed waveforms are shown in Fig. 4.4. Using (4.7), the magnitude of the resultant waveform after superposition is $A = \frac{1}{7}$. Applying (4.8) yields

$$d' = \text{mod} \left( 5 \times 7, 1 \right) \approx 0.71$$

$$T' = \frac{T}{7}$$

and

$$\phi' = 0$$

because $\text{mod} \left( 5 \times 7, 2 \right) < 1$ so that $q_\phi = 0$ in (4.9).

Figure 4.4: (Top) Interleaved triangular waveforms. (Bottom) Resultant waveform after superposition.
The harmonics of the resultant waveform after superposition are shown in Fig. 4.5. These were calculated using (4.10). As illustrated, the only harmonics that remain are those which are multiples of $N = 5$ and not a multiple of $\frac{1}{d} = 7$. For instance, although $n = 35$ is a multiple of $N = 5$, it is canceled because 35 is also a multiple of $\frac{1}{d} = 7$.

![Figure 4.5: Harmonics after interleaved waveform superposition. Scale is normalized to unity.](image)

4.4 Experiment: Interleaved Grid-Connected Inverters

4.4.1 Description

Consider the system of three parallel interleaved single-phase half-bridge inverters in Fig. 4.6. The $k^{th}$ inverter utilizes a symmetric triangular carrier waveform equal to $f_{\text{tri}} \left( t - k \frac{T_{\text{sw}}}{3}, \frac{1}{2}, T_{\text{sw}} \right)$, where $f_{\text{sw}} = 10$ kHz and $T_{\text{sw}} = \frac{1}{f_{\text{sw}}}$, and each inverter is equipped with a 6 mH inductive output filter. A bipolar dc supply with a rail-rail voltage 225 V is connected to each inverter input. The 60 Hz grid was interfaced through a step-down transformer such that its measured RMS voltage was 65 V. Each inverter was controlled to inject a sinusoidal current into the grid with unity power factor. This was accomplished by controlling each inverter with an independent proportional-resonant current controller. The three controllers and PWM interleaving were implement on a single TMS320F28335 microcontroller.

The measured output currents are shown in Fig. 4.7. As the grid current waveform illustrates, the ripple which was originally present at the three inverter outputs...
Figure 4.6: Diagram of experimental system which consists of three parallel grid-connected inverters.

is significantly reduced after superposition. Furthermore, the fundamental 60Hz components constructively reinforce. Next, the analytical results of the previous section will be validated by deriving the net ripple component and comparing the analytical result to the measurements in Fig. 4.7.

4.4.2 Approximation of Ripple and Comparison of Analytical and Measured Results

A suitable design will have $L/R$ time constants much larger than $T_{sw}$. This supports approximation of the ripple as a piecewise linear triangular waveform [80]. When the top switch in each inverter is closed, the voltage across the inductor, $v_L$, can be estimated as

$$v_L = \frac{V_{dc}}{2} - |v_{grid}| \approx L \frac{\Delta i}{\Delta t} = L \frac{2I_s}{dT_{sw}}, \quad (4.14)$$
where $v_{\text{grid}}$ is the grid voltage, $\Delta i$ denotes the peak-peak ripple amplitude, and $\Delta t$ is the length of the time interval when the top switch is closed. Since $\Delta i$ corresponds to the peak-peak amplitude, it follows that $\Delta i$ is simply related to the peak amplitude by $\Delta i = 2I_r$. Drawing from the definition of the duty ratio, time-interval $\Delta t = dT_{\text{sw}}$. Rearranging, (4.14) the peak amplitude of the ripple is

$$I_r = \frac{1}{2} T_{\text{sw}} d \frac{|v_L|}{L} = \frac{1}{2} T_{\text{sw}} \left( \frac{1}{2} (1 + m) \right) \frac{1}{L} \left( \frac{V_{\text{dc}}}{2} - |v_{\text{grid}}| \right), \quad (4.15)$$

where the grid voltage can be expressed as $v_{\text{grid}} = \sqrt{2} V \sin (\omega t)$.

Using (4.5), the net current entering the grid can be written as

$$i_{\text{grid}} = t_{o1} + t_{o2} + t_{o3}$$

$$= N\sqrt{2} I \sin (\omega t) + I_r \sum_{k=1}^{3} f_{\text{tri}} \left( t - k \frac{T_{\text{sw}}}{3}, d, T_{\text{sw}} \right) \quad (4.16)$$

$$= 3\sqrt{2} I \sin (\omega t) + I_r \sum_{k=1}^{3} f_{\text{tri}} \left( t - k \frac{T_{\text{sw}}}{3}, \frac{1}{2} (1 + m), T_{\text{sw}} \right), \quad (4.17)$$

where the first term is based on the fact that all three inverters were controlled to inject an identical fundamental component with RMS value $I$. The second line results after substituting $d = \frac{1}{2} (1 + m)$ and assuming each controller produces an
identical modulation signal, i.e., \( m = m_1 = m_2 = m_3 \). Before the analytical result for the superposition of \( N \) triangular waveforms is applied, we will need to estimate the control modulation signal, \( m \).

Each inverter was controlled to inject real and reactive power, \( P = 34.1 \text{ W} \) and \( Q = 0 \text{ VAR} \), respectively. The modulation signal is \( m = M \sin(\omega t + \phi_m) \), and each inverter and the grid can be modeled as shown in Fig. 4.8. As illustrated in Fig. 4.8, the inverter is modeled as a voltage source with magnitude \( \frac{MV_{dc}}{2\sqrt{2}} \), and angle \( \phi_m \), while the grid is modeled as a voltage source with a zero angle. The equations for \( P \) and \( Q \) of such a system [66] are

\[
\begin{align*}
P &= \frac{MV_{dc}V}{2\sqrt{2}L} \sin(\phi_m), \\
Q &= \frac{MV_{dc}V}{2\sqrt{2}} \cos(\phi_m) - \frac{V^2}{\omega L}.
\end{align*}
\]

Solving (4.18) iteratively for \( M \) and \( \phi_m \) yields: \( M = 0.817 \) and \( \phi_m = 18.2 \times 10^{-3} \text{ rad} \).

After substituting (4.15) into (4.17), applying the results in Section 4.3.1, and inserting numerical values, we attain a closed-form time-domain expression for the grid current. The analytically derived result and measured current are compared in Fig. 4.9. To facilitate a better inspection of the ripple, Fig. 4.9 corresponds to the region in Fig. 4.7 enclosed by the box. The results in Fig. 4.9 show the validity of the analytical model and demonstrate the proposed method for distortion reduction.

### 4.5 PV Systems

In this section, the interleaving method is applied towards the development of a single-stage microinverter topology for emerging PV cell technologies. First, a conventional microinverter design will be characterized. Next, the proposed design which
Figure 4.9: Up-close comparison of analytically estimated and measured net grid current.

offers several advantages will be described. Lastly, simulation results of a system of interleaved microinverters will be given.

4.5.1 Applications for High-Voltage PV Modules

4.5.2 Conventional Microinverter

Figure 4.10 shows a typical microinverter topology which interfaces a single conventional module to the power grid. Recall that this circuit was characterized in Section 2.3.2. As illustrated, this type of circuit consists of: i) an input stage which steps up the voltage provided by the module, ii) capacitive dc-link which decouples the input and output energy flow, and iii) a dc-ac conversion stage, and iv) an output filter. This is generally described as being a two-stage converter because of the presence of a dc-dc converter at the input and a dc-ac stage at the output.

The presence of a voltage boosting stage and the need for decoupling capacitors both add costs to the single-phase microinverter. Furthermore, since the conventional microinverter is generally designed to meet IEEE 1547 distortion in isolation, the output filter tends to be large. Next, a simplified design for a three-phase microin-
verter which leverages the benefits of interleaving and emerging PV cell technologies will be proposed.

4.5.3 Three-Phase Microinverter

Recently, there have been several advancements in the development of PV modules which are built from very large numbers of cells [83]. For instance, one team of researchers at Sandia labs is developing a type of PV module made up of several thousand solar cells with integrated optics [84–87]. Utilizing the micro-transfer printing technique described in [88, 89], a company called Semprius is marketing a concentrating PV module made up of a large collection of small solar cells. Along similar lines, researchers in Japan are developing PV modules which contain large arrays of small spherical solar cells [90].

Because the voltage across a PV module is directly proportional to the number of series PV cells, it is possible to develop a PV module which delivers power at a high voltage and low current. Here, it is assumed that the module can be designed such its voltage at the maximum power point meets or exceeds 400 V. With this type of module, a voltage boosting stage at the input would be unnecessary and the module could be connected directly across the dc-link.

![Figure 4.11: Proposed three-phase PV inverter.](image.png)

Furthermore, if the inverter interfaces to a three-phase system, the size and cost of the decoupling capacitor could be reduced substantially. This follows from the fact that the total power flowing across a balanced three-phase system is constant. Writing the three-phase output currents of a inverter as $i_a = \sqrt{2}I \sin(\omega t)$, $i_b = \sqrt{2}I \sin(\omega t - \frac{2\pi}{3})$, and $i_c = \sqrt{2}I \sin(\omega t + \frac{2\pi}{3})$, and denoting the grid voltages as $v_a$, $v_b$, and $v_c$. 

60
v_b, and v_c, the power output is

\[
p(t) = i_a(t)v_a(t) + i_b(t)v_b(t) + i_c(t)v_c(t)
= 2IV\left(\sin^2(\omega t) + \sin^2\left(\omega t - \frac{2\pi}{3}\right) + \sin^2\left(\omega t + \frac{2\pi}{3}\right)\right)
= 3IV.
\]

(4.19)

As is evident in (4.19), the power delivered by the three-phase inverter is constant under balanced conditions. As a consequence, the decoupling capacitor does not need to store bulk energy and a much smaller capacitance can be used. In this case, the decoupling capacitor is needed merely to accommodate phase imbalances and switching transients.

Given that a system of microinverters is generally composed of a very large number of parallel inverters, the interleaving method described in this chapter can be utilized to realize the design in Fig. 4.11. In comparison to the conventional microinverter, it is possible utilize a single-stage topology with a reduced dc-link capacitance and a small output filter size. It is likely that the resulting design can be made physically smaller and at a lower cost. Also, given that the number of power conversion stages is reduced, efficiency can be increased in comparison to the conventional design.

4.5.4 PV System Simulation

In this section, a system of grid-connected three-phase microinverters is simulated. Each inverter uses the simplified design in Fig. 4.11 with high-voltage PV. The system of inverters is interfaced to a 60 Hz three-phase system with a line-line voltage rating of 208 V. Each PV module is rated to deliver 400 W with a maximum power point voltage and current of 400 V and 1 A, respectively.

First consider the case of one inverter. In order to satisfy the 5% THD requirement at rated conditions, a relatively high switching frequency and large filter inductor are required. Fig. 4.12 shows the output current of the single inverter when a switching frequency of 50 kHz was used in conjunction with an 8 mH output inductor. Next, we will demonstrate the benefits of interleaving in a multi-inverter system.

Now consider a system of 5 parallel interleaved inverters. Each inverter utilizes an independent current controller to regulate its respective output, and each carrier waveform is phase-shifted by a unique multiple of \( \frac{T_{sw}}{5} \). Because interleaving is used, the switching frequency and output filter inductance are reduced to 25 kHz and 1 mH,
Figure 4.12: Simulation: Phase a output current of a single inverter with a large filter inductor. Current waveform has 4.5% THD.

Figure 4.13: Simulation: Resultant phase a grid current from five parallel interleaved inverters with reduced filter size. Ideal uniform conditions were used in (a) such that THD is approximately 3.3%. Non-uniform conditions were simulated in (b) where the resultant THD is approximately 4.3%.
Figure 4.14: Simulation: Output currents of each of the five interleaved inverters with reduced filter size and under non-uniform conditions.
Table 4.1: Parameters of simulation with non-uniform conditions

<table>
<thead>
<tr>
<th>PV #</th>
<th>Power [W]</th>
<th>Voltage [V]</th>
<th>Output Current THD [%]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>361</td>
<td>394.7</td>
<td>78</td>
</tr>
<tr>
<td>2</td>
<td>364</td>
<td>392.5</td>
<td>76</td>
</tr>
<tr>
<td>3</td>
<td>334</td>
<td>392.7</td>
<td>83</td>
</tr>
<tr>
<td>4</td>
<td>322</td>
<td>405.2</td>
<td>90</td>
</tr>
<tr>
<td>5</td>
<td>266</td>
<td>403.1</td>
<td>109</td>
</tr>
</tbody>
</table>

respectively. In comparison to the single inverter, the switching frequency is reduced by half and the filter inductance was reduced by a factor of eight.

Figure 4.13(a) shows the net grid current generated by the system of inverters during ideal uniform conditions. In this case, each PV module was operating at rated conditions and each inverter delivered 400 W. In this scenario, each controller converges to an identical modulation signal. The analytical result presented in this chapter could be used to approximate the waveform in Fig. 4.13(a). It is interesting to note that the points with zero ripple in Fig. 4.14(a) correspond to the instants when \( Nd \) is an integer.

Next, examine a more realistic scenario where each module is generating a different amount of power at a slightly different voltage. Specifically, it was assumed that the PV modules for inverters 1–5 have the conditions specified in Table 4.1. Despite the differences between each PV module, the grid current, as illustrated in Fig. 4.13(b), satisfies the 5% THD specification. Furthermore, a comparison of the waveforms in Fig. 4.13 reveals that the grid current waveform for the systems with uniform and non-uniform conditions are relatively similar. This result implies that the proposed interleaving method is relatively robust against deviations in PV characteristics. The output currents of the individual inverters are shown in Fig. 4.14 and their corresponding THD is summarized in Table 4.1.

4.6 Conclusion

A method for coordinating the switching action of \( N \) parallel inverters was developed. Using conventional sine-triangle PWM with interleaved carriers, it is possible for a system of parallel inverters to generate a low-distortion output current while simultaneously reducing the switching frequency and output filter size. As shown
in Appendix A.1, Fourier series was used to derive a closed-form expression for the superposition of $N$ interleaved triangular waveforms. This expression was then used to model the aggregate current generated by an experimental system of three interleaved inverters. Simulation results were presented for a PV system. The next chapter will be focused on the coordination of parallel inverters in a microgrid using nonlinear control.
Chapter 5

SYNCHRONIZATION OF NONLINEAR OSCILLATORS COUPLED THROUGH AN LTI NETWORK

Synchronization of distributed oscillator systems is relevant to several research areas, including neural processes, coherency in plasma physics, communications, and electric power systems [91–97]. In this chapter, a sufficient condition for the global asymptotic synchronization of a class of identical nonlinear oscillators coupled through an electrical network with LTI elements (resistors, capacitors, inductors, and transformers) is presented. As a particular case, symmetric networks composed of oscillators connected to a common node through identical branch impedances are examined. Here, it will be shown that the synchronization condition is independent of: i) the load impedance, and ii) the number of oscillators in the network. These results will then be used to formulate a control paradigm for the coordination of parallel inverters serving a passive electrical load in a microgrid.

Relevant to this work is a body of literature that has examined synchronization conditions for diffusively coupled oscillators using passivity theory [98–101]. Passivity-based analysis was applied in [102], where it was first proposed that inverters could be controlled to act as nonlinear oscillators in a power system. As developed in [99, 100], passivity-based approaches require the formulation of a storage function which is proportional to the oscillator state-variable differences. It then follows that a sufficient condition for synchronization can be attained by showing the conditions under which the time-derivative of the storage function was strictly negative. However, one shortcoming of this approach is that it is difficult to formulate an appropriate storage function when the coupling network contains energy storage elements such as capacitors and inductors. Because power networks are generally comprised of LTI circuit elements (resistors, capacitors, inductors, and transformers), passivity-based synchronization analysis is difficult to apply in this setting.

Alternatively, the notion of $\mathcal{L}_2$ input-output stability was used in [103–105] to analyze synchronization in cyclic feedback systems coupled through an LTI network.
Given the differential equations of the original system, a transformation is performed such that an equivalent system based on signal differences is formulated. If the resulting differential system is input-output stable, it can be shown that all signal differences decay to zero and oscillator synchronization results. One significant advantage of this technique is that the analyst does not need to formulate a storage function. Using established $\mathcal{L}_2$ input-output stability methods, a sufficient condition for synchronization can be attained. The results in this chapter derive from $\mathcal{L}_2$ methods because they facilitate analysis of LTI power networks.

The results in this chapter are primarily focused on the theory and analysis of coupled oscillator systems. To summarize, the contributions of this chapter are as follows:

a. A sufficient global asymptotic synchronization condition is derived for a class of identical nonlinear oscillators coupled through an LTI network.

b. For the particular network topology where the oscillators are connected to a common node through identical branch impedances, it is shown that the synchronization condition is independent of the number of oscillators and the load impedance.

c. From an application perspective, these results are applied to the coordination of inverters in a single-phase microgrid to achieve a control and design paradigm that is robust (independent of load) and modular (independent of number of inverters).

In general, results will be presented with a level of generality such that they can be applied to a variety of problems. Later in this thesis, theoretical results derived in this chapter will be applied towards the practical design and implementation of a microgrid with $N$ parallel inverters.

5.1 Preliminaries

For the $N$-tuple $(u_1, \ldots, u_N)$, denote $u = [u_1, \ldots, u_N]^T$ to be the corresponding column vector, where $^T$ indicates transposition. The $N$-dimensional column vectors of all ones and all zeros are denoted by $\mathbf{1}$ and $\mathbf{0}$, respectively. $N \times N$ matrices will be denoted by $U$ and they will be diagonalized as $U = QAQ^{-1}$, where $\Lambda$ denotes the
diagonal matrix of eigenvalues and the column vectors of $Q$ are the corresponding eigenvectors.

The Laplace transform of the continuous-time function $f(t)$ is denoted by $f(s)$, where $s = \rho + j\omega$ is a complex number, and $j = \sqrt{-1}$. Transfer functions are denoted by lower-case $z(s)$, and transfer matrices are denoted by upper-case $Z(s)$. Unless stated otherwise, $Z(s) = z(s)I_N$, where $I_N$ is the $N \times N$ identity matrix.

The Euclidean norm of a real or complex vector, $u$, is denoted by $\|u\|_2$ and is defined as

$$\|u\|_2 = \sqrt{u^* u}, \quad (5.1)$$

where $^*$ indicates the conjugate transpose. If $u$ is real, then $u^* = u^T$. For some continuous-time function $u(t)$, $u : [0, \infty) \rightarrow \mathbb{R}^N$, the $L_2$ norm of $u$ is defined as

$$\|u\|_{L_2} = \sqrt{\int_0^\infty u(t)^T u(t) \, dt}, \quad (5.2)$$

and the space of piecewise-continuous and square-integrable functions where $\|u\|_{L_2} < \infty$ is denoted by $L_2 [106]$. If $u \in L_2$, then $u$ is said to be bounded. A causal system, $H$, with input $u$ and output $y$, is said to be finite-gain $L_2$ stable if there exist finite, non-negative constants, $\gamma$ and $\eta$, such that

$$\|y\|_{L_2} = \|H(u)\|_{L_2} \leq \gamma \|u\|_{L_2} + \eta, \quad \forall u \in L_2. \quad (5.3)$$

The smallest value of $\gamma$ for which there exists a $\eta$ such that (5.3) is satisfied is called the $L_2$ gain of the system. The $L_2$ gain of $H$, denoted as $\gamma(H)$, provides a measure of the largest amplification applied to the input signal, $u$, as it propagates through the system $H$. Intuitively, (5.3) can be understood as stating that norm of the output, $H(u)$, will not be larger than the linearly scaled norm of the input $u$. Hence, the system is described as being input-output stable when the $L_2$ gain of $H$ is finite.

If $H$ is linear and can be represented by the matrix of transfer functions $H(s)$ such that $H(s) \in \mathbb{C}^{N \times N}$, it can be shown that the $L_2$ gain of $H$ is equal to its $H$-infinity norm, denoted by $\|H\|_\infty$, and defined as

$$\gamma(H) = \|H\|_\infty = \sup_{\omega \in \mathbb{R}} \frac{\|H(j\omega) u(j\omega)\|_2}{\|u(j\omega)\|_2}, \quad (5.4)$$

where $\|u(j\omega)\|_2 = 1$, provided that all poles of of $H(s)$ have strictly negative real
Because (5.4) is the ratio of the output to input norms, it is clear that \( \gamma(H) \) gives a measure of the largest amplification of the vector \( u \) when it is multiplied by the matrix \( H(s) \). Stated alternatively, \( \gamma(H) \) is the largest singular value of the matrix \( H(s) \). Note that if \( H(s) \) is a single-input single-output transfer function such that \( H(s) \in \mathbb{C} \), then \( \gamma(H) = \|H\|_\infty = \sup_{\omega \in \Re} \|H(j\omega)\|_2 \).

A classical result that will be useful in showing synchronization is Barbalat’s lemma [104, 105]. Consider the continuous function \( \phi : [0, \infty) \to \Re \). Barbalat’s lemma [107] states that if \( \lim_{t \to \infty} \int_0^t \phi(\tau) \, d\tau < \infty \), then

\[
\lim_{t \to \infty} \phi(t) = 0. \tag{5.5}
\]

Later, this property will be used to show that all signal differences decay to zero when the system meets the sufficient condition for synchronization.

The electrical networks under study have underlying graphs that are undirected and connected. The corresponding Laplacian matrix, denoted by \( \Gamma \in \Re^{N \times N} \), has the following properties (see [104, 108, 109] for proofs and additional discussion):

a. \( \text{rank}(\Gamma) = N - 1 \).

b. The eigenvalues of \( \Gamma \) (ordered in ascending order by magnitude) are denoted by \( \lambda_1 < \lambda_2 < \cdots < \lambda_N \), where \( \lambda_1 = 0 \).

c. \( \Gamma \) is symmetric with row and column sums equal to zero such that \( \Gamma 1 = \Gamma^T 1 = 0 \).

d. The eigenvector \( q_1 \) (corresponding to \( \lambda_1 = 0 \)) is given by \( q_1 = \frac{1}{\sqrt{N}} 1 \).

e. The Laplacian can be diagonalized as \( \Gamma = QAQ^T \), where it follows that \( Q^{-1} = Q^T \) because \( \Gamma = \Gamma^T \).

A useful construct that will be employed to compare individual oscillator outputs with the average of all \( N \) oscillator outputs is the projector matrix, \( \Pi \), defined [99, 100, 104] as

\[
\Pi = I_N - \frac{1}{N} 11^T. \tag{5.6}
\]

For some vector \( u \in \Re^N \), denote \( \tilde{u} = \Pi u \), and refer to \( \tilde{u} \) as the corresponding differential vector (in previous work, see, e.g., [99,100,103–105], the quantity \( \tilde{u} \) is referred to as an incremental quantity). A causal system, \( H \), with input \( u \) and output
\( y \), is said to be differentially finite-gain \( \mathcal{L}_2 \) stable if there exist finite, non-negative constants, \( \bar{\gamma} \) and \( \bar{\eta} \), such that
\[
\|\tilde{y}\|_{\mathcal{L}_2} \leq \bar{\gamma} \|\tilde{u}\|_{\mathcal{L}_2} + \bar{\eta}, \quad \forall \tilde{u} \in \mathcal{L}_2,
\]
(5.7)
where \( \tilde{y} = \Pi y \). The smallest value of \( \bar{\gamma} \) for which there exists a \( \bar{\eta} \) such that (5.7) is satisfied, is called the differential \( \mathcal{L}_2 \) gain of the system and is denoted as \( \bar{\gamma}(H) \).
The differential \( \mathcal{L}_2 \) gain provides a measure of the amplification of signal differences as they propagate through a system.

5.2 Conditions for Global Asymptotic Synchronization

In this section, a system-level description of the coupled nonlinear oscillators is provided. Next, the projector matrix is used to derive a corresponding system based on signal differences. Finally, equipped with the differential system description, the main result of this chapter will be presented: a sufficient condition for global asymptotic synchronization of the coupled oscillators.

5.2.1 System Description

Consider the class of electrical oscillators that can be described by the circuit diagram depicted in Fig. 5.1. The oscillator has: i) a linear subsystem comprised of passive circuit elements with impedance \( z_{\text{osc}}(s) \), and ii) a nonlinear voltage-dependent current source, \( g(\nu) \). The source \( g(\nu) \) is required to be continuous and differentiable, and additionally requires
\[
\sigma \triangleq \sup_{\nu \in \mathbb{R}} \left| \frac{d}{d\nu} g(\nu) \right| < \infty.
\]
(5.8)
In other words, the slope of \( g(\nu) \) with respect to the oscillator voltage must be
Consider a system in which $N$ such oscillators are coupled through a passive electrical LTI network, and the coupling is captured through

$$i(s) = Y(s)v(s),$$

(5.9)

where $i(s) = [i_1(s), \ldots, i_N(s)]^T$ is the vector of oscillator output currents, $v(s) = [v_1(s), \ldots, v_N(s)]^T$ is the vector of oscillator terminal voltages, and $Y(s)$ is the network admittance matrix of the general form

$$Y(s) = \alpha(s)I_N + \beta(s)\Gamma,$$

(5.10)

where $\alpha(s), \beta(s) \in \mathbb{C}$, and $\Gamma$ is the network Laplacian with the properties described in Section 5.1. Later, it will be shown that the admittance matrix of the microgrid network under consideration does have the form shown in (5.10). Conceptually, the admittance, $\alpha(s)$, in the first term can be understood as the local load observed from the output of each oscillator while the second term, $\beta(s)\Gamma$, accounts for the interaction between units. As the system synchronizes, the interaction between
oscillators decays to zero and the effective output impedance observed from the each oscillator is equal to \(\alpha(s)^{-1}\).

Figure 5.2 depicts the network of oscillators described above. From Fig. 5.2, it is apparent that the terminal voltage of the \(j\)th oscillator, \(v_j(s)\), can be expressed as

\[
v_j(s) = z_{osc}(s)(i_{src}(s) - i_j(s)), \quad \forall j = 1, \ldots, N.
\]  

(5.11)

Writing all terminal voltages in matrix form yields

\[
v(s) = Z_{osc}(s)i_{src}(s) - Z_{osc}(s)Y(s)v(s),
\]

(5.12)

where \(Z_{osc}(s) = z_{osc}(s)I_N \in \mathbb{C}^{N \times N}\), \(i_{src}(s) = [i_{src1}(s), \ldots, i_{srcN}(s)]^T\), and in the second line of (5.12), \(i(s) = Y(s)v(s)\) from (5.9) has been substituted. \(v(s)\) can be isolated from (5.12) as follows:

\[
v(s) = (I_N + Z_{osc}(s)Y(s))^{-1}Z_{osc}(s)i_{src}(s)
\]

\[
= F(Z_{osc}(s), Y(s))i_{src}(s),
\]

(5.13)

where \(F : \mathbb{C}^{N \times N} \times \mathbb{C}^{N \times N} \rightarrow \mathbb{C}^{N \times N}\) is called the linear fractional transformation [110]. In general, for some \(A, B\) of appropriate dimension and domain, the linear fractional transformation is defined as

\[
F(A, B) := (I_N + AB)^{-1}A.
\]

(5.14)

Using (5.13), the system of coupled oscillators admits the compact block-diagram representation in Fig. (5.3), where the linear and nonlinear portions of the system are clearly compartmentalized by \(F(Z_{osc}(s), Y(s))\) and \(g(v) = [g(v_1), \ldots, g(v_N)]^T\), respectively.

Figure 5.3: Block-diagram representation of coupled oscillator system. \(g(v)\) is a vector which captures the input-output relation of all the nonlinear circuit elements in the oscillators.
5.2.2 Corresponding Differential System

The primary objective is to show global asymptotic synchronization in the network introduced above. Specifically, oscillator synchronization is defined as

$$\lim_{t \to \infty} v_j(t) - v_k(t) = 0 \forall j, k = 1, \ldots, N.$$  \hspace{1cm} (5.15)

For ease of analysis, it will be useful to transform to a coordinate system based on signal differences. Subsequently, such a system will be referred to as the corresponding differential system. Towards this end, note that the projector matrix defined in (5.6) has the following property:

$$\tilde{v}(t)^T \tilde{v}(t) = (\Pi v(t))^T (\Pi v(t)) = \frac{1}{2N} \sum_{j=1}^{N} \sum_{k=1}^{N} (v_j(t) - v_k(t))^2.$$  \hspace{1cm} (5.16)

Therefore, it is evident that the synchronization condition in (5.15) is equivalent to requiring $\tilde{v}(t) = \Pi v(t) \to 0$ as $t \to \infty$.

The corresponding differential system will now be derived. First, the differential terminal-voltage vector, $\tilde{v}(s)$, can be expressed as

$$\tilde{v}(s) = \Pi v(s) = \Pi (Z_{\text{osc}}(s) (i_{\text{src}}(s) - i(s)))$$
$$= Z_{\text{osc}}(s) (\Pi i_{\text{src}}(s) - \Pi Y(s) v(s))$$
$$= Z_{\text{osc}}(s) \left( \tilde{i}_{\text{src}}(s) - Y(s) \tilde{v}(s) \right),$$  \hspace{1cm} (5.17)

where in the first line, $v(s)$ from (5.12) has been substituted, and in the second line, the relation $i(s) = Y(s) v(s)$ from (5.9) was used and the fact that $\Pi Z_{\text{osc}}(s) = \Pi z_{\text{osc}}(s) I_N = z_{\text{osc}}(s) I_N \Pi = Z_{\text{osc}}(s) \Pi$. Finally, the last line follows from the fact that the projector and admittance matrices commute, i.e., $\Pi Y(s) = Y(s) \Pi$. To prove this, for the class of admittance matrices given by (5.10), note that

$$\Pi Y(s) = \Pi (\alpha(s) I_N + \beta(s) \Gamma)$$
$$= \alpha(s) I_N \Pi + \beta(s) \Pi \Gamma$$
$$= \alpha(s) I_N \Pi + \beta(s) \left( I_N - \frac{1}{N} 11^T \right) \Gamma$$
$$= \alpha(s) I_N \Pi + \beta(s) \left( \Gamma I_N - \frac{1}{N} \Gamma 11^T \right)$$
$$= (\alpha(s) I_N + \beta(s) \Gamma) \Pi = Y(s) \Pi,$$  \hspace{1cm} (5.18)
where the fact that the row and column sums of $\Gamma$ are zero was used, which implies $11^T \Gamma = 00^T = 11^T$. $\tilde{v}(s)$ in (5.17) can now be isolated as follows:

$$\tilde{v}(s) = (I_N + Z_{osc}(s)Y(s))^{-1} Z_{osc}(s)\tilde{i}_{src}(s)$$

$$= \mathcal{F}(Z_{osc}(s), Y(s))\tilde{i}_{src}(s). \quad (5.19)$$

Notice the similarity between (5.19) and (5.13). In particular, note that the linear fractional transformation also maps $\tilde{i}_{src}(s)$ to $\tilde{v}(s)$.

Finally, define a map $\tilde{g}$ that captures the impact of $g(v)$ in the corresponding differential system as follows:

$$\tilde{g} : \tilde{v} \rightarrow -\tilde{i}_{src}. \quad (5.20)$$

A complete description of the equivalent differential system has now been attained. In particular, this system admits the block diagram representation in Fig. 5.4, where, as in Fig. 5.3, the linear and nonlinear subsystems are clearly compartmentalized using $\mathcal{F}(\cdot, \cdot)$ and $\tilde{g}$, respectively.

![Figure 5.4: Block-diagram representation of the equivalent differential system.](image)

5.2.3 Sufficient Conditions for Global Asymptotic Synchronization

We now derive sufficient conditions that ensure global asymptotic synchronization in the sense of (5.15) for the system of oscillators described above. Before the main theorem is stated, a lemma is first presented which gives an upper bound on the differential $L_2$ gain of the nonlinearity $g(\cdot)$.

**Lemma 1.** The differential $L_2$ gain of $g$ is finite and upper bounded by $\sigma$ such that

$$\tilde{\gamma}(g) \leq \sigma = \sup_{\nu \in \mathbb{R}} \left| \frac{d}{d\nu} g(\nu) \right| < \infty. \quad (5.21)$$

**Proof:** By definition of $\sigma$, for any pair of terminal voltages $v_j$ and $v_k$, and the corresponding source currents $\tilde{i}_{srcj}$ and $\tilde{i}_{srck}$, where $j, k \in \{1, \ldots, N\}$, the mean-
value theorem [107] can be applied to give

\[ \sigma \geq \frac{|i_{\text{src},j}(t) - i_{\text{src},k}(t)|}{|v_j(t) - v_k(t)|} \]

\[ \implies \sigma^2 (v_j(t) - v_k(t))^2 \geq (i_{\text{src},j}(t) - i_{\text{src},k}(t))^2. \]  

(5.22)

Summing over all indices, \( j, k \in \{1, \ldots, N\} \) in (5.22) yields

\[ \sigma^2 \sum_{j=1}^{N} \sum_{k=1}^{N} (v_j(t) - v_k(t))^2 \geq \sum_{j=1}^{N} \sum_{k=1}^{N} (i_{\text{src},j}(t) - i_{\text{src},k}(t))^2, \]  

(5.23)

which can be rearranged and simplified as follows

\[ \sigma \geq \sqrt{\frac{\sum_{j=1}^{N} \sum_{k=1}^{N} (i_{\text{src},j}(t) - i_{\text{src},k}(t))^2}{\sum_{j=1}^{N} \sum_{k=1}^{N} (v_j(t) - v_k(t))^2}}. \]  

(5.24)

Since (5.24) holds for any set of terminal voltages, this implies

\[ \sigma \geq \sup_{v \in \mathbb{R}^N} \sqrt{\frac{1}{2N} \sum_{j=1}^{N} \sum_{k=1}^{N} (i_{\text{src},j}(t) - i_{\text{src},k}(t))^2}{\frac{1}{2N} \sum_{j=1}^{N} \sum_{k=1}^{N} (v_j(t) - v_k(t))^2}}, \]  

(5.25)

which can be rewritten compactly using the projector-matrix notation in (5.16) as

\[ \sigma \geq \sup_{v \in \mathbb{R}^N} \sqrt{\frac{i_{\text{src}}(t)^T \tilde{i}_{\text{src}}(t)}{\tilde{v}(t)^T \tilde{v}(t)}}. \]  

(5.26)

By definition of the differential \( L_2 \) gain,

\[ \tilde{\gamma}(g) = \sup_{v \in \mathbb{R}^N} \frac{\|\tilde{i}_{\text{src}}\|_{L_2}}{\|v\|_{L_2}} \]

\[ \quad = \sup_{v \in \mathbb{R}^N} \sqrt{\int_0^\infty i_{\text{src}}(t)^T i_{\text{src}}(t) \, dt} \int_0^\infty \tilde{v}(t)^T \tilde{v}(t) \, dt}. \]  

(5.27)
Applying (5.26) in the definition above,

\[
\tilde{\gamma}(g) \leq \sup_{v \in \mathbb{R}^N} \sqrt{\frac{\sigma^2 \int_{0}^{\infty} \tilde{v}(t)^T \tilde{v}(t) \, dt}{\int_{0}^{\infty} \tilde{v}(t)^T \tilde{v}(t) \, dt}} = \sigma < \infty, \tag{5.28}
\]

which completes the proof. \[\square\]

We are now ready to state and prove the main result of this chapter: a sufficient condition for global asymptotic synchronization in the network of oscillators described in Section 5.2.1.

**Theorem 1.** The network of \(N\) oscillators coupled through (5.9) with the admittance matrix in (5.10), synchronizes in the sense of (5.15), if

\[
\|F(\zeta(s), \beta(s) \lambda_2)\|_\infty \sigma < 1, \tag{5.29}
\]

where \(\lambda_2\) is the smallest positive eigenvalue of \(\Gamma\), and

\[
\zeta(s) := \frac{z_{osc}(s)}{1 + \alpha(s) z_{osc}(s)}. \tag{5.30}
\]

**Proof:** Consider the block-diagram of the differential system in Fig. 5.4. Denote the differential \(\mathcal{L}_2\) gain of the linear fractional transformation by \(\tilde{\gamma}(F(Z_{osc}(s), Y(s)))\). The finite-gain differential \(\mathcal{L}_2\) stability of \(F(Z_{osc}(s), Y(s))\) gives

\[
\|\tilde{v}\|_{\mathcal{L}_2} \leq \tilde{\gamma}(F(Z_{osc}(s), Y(s))) \left\|\tilde{v}_{src}\right\|_{\mathcal{L}_2} + \tilde{\eta}, \tag{5.31}
\]

for some non-negative \(\tilde{\eta}\). Applying (5.21) from Lemma 1, it follows that

\[
\left\|\tilde{v}_{src}\right\|_{\mathcal{L}_2} \leq \sigma \|\tilde{v}\|_{\mathcal{L}_2}. \tag{5.32}
\]

Combining (5.31) and (5.32) yields

\[
\|\tilde{v}\|_{\mathcal{L}_2} \leq \tilde{\gamma}(F(Z_{osc}(s), Y(s))) \sigma \|\tilde{v}\|_{\mathcal{L}_2} + \tilde{\eta}. \tag{5.33}
\]

It will be required that

\[
\tilde{\gamma}(F(Z_{osc}(s), Y(s))) \cdot \sigma < 1. \tag{5.34}
\]
Isolating $\|\tilde{v}\|_{L_2}$ leads to

$$
\|\tilde{v}\|_{L_2} \leq \frac{\eta}{1 - \bar{\gamma}(F(Z_{osc}(s), Y(s))) \sigma}, \quad (5.35)
$$

which implies that $\tilde{v} \in L_2$. It follows from Barbalat’s lemma [103–105, 107] that

$$
\lim_{t \to \infty} \tilde{v}(t) = 0 \implies \lim_{t \to \infty} v_j(t) - v_k(t) = 0 \quad \forall j, k = 1, \ldots, N. \quad (5.36)
$$

That is, if the system of oscillators satisfies the condition in (5.34), global asymptotic synchronization can be guaranteed.

The result in (5.29) will now be derived by showing $\bar{\gamma}(F(Z_{osc}(s), Y(s)))$ equals $\|F(\zeta(s), \beta(s) \lambda_2)\|_\infty$. From the definition of the linear fractional transformation in (5.14), and the general form of the admittance matrix in (5.10), note that

$$
F(Z_{osc}(s), Y(s)) = (I_N + Z_{osc}(s)Y(s))^{-1} Z_{osc}(s)
$$

$$
= (I_N + Z_{osc}(s)(\alpha(s)I_N + \beta(s)\Gamma))^{-1} Z_{osc}(s)
$$

$$
= ((1 + \alpha(s)z_{osc}(s)) I_N + z_{osc}(s)\beta(s)\Gamma)^{-1} Z_{osc}(s)
$$

$$
= \left(I_N + \frac{z_{osc}(s)}{1 + \alpha(s)z_{osc}(s)} \beta(s)\Gamma\right)^{-1} \frac{z_{osc}(s)I_N}{1 + \alpha(s)z_{osc}(s)}
$$

$$
= F(\zeta(s)I_N, \beta(s)\Gamma). \quad (5.37)
$$

Because $F(\zeta(s)I_N, \beta(s)\Gamma)$ is a linear system, it follows that the differential $L_2$ gain of $F(Z_{osc}(s), Y(s))$ can be calculated using the $H$-infinity norm. Now, by definition of the $H$-infinity norm and differential $L_2$ gain, it follows that

$$
\|F(\zeta(s)I_N, \beta(s)\Gamma)\|_\infty
$$

$$
= \sup_{\omega \in \mathbb{R}} \frac{\|\tilde{v}(j\omega)\|_2}{\|\tilde{i}_{src}(j\omega)\|_2}
$$

$$
= \sup_{\omega \in \mathbb{R}} \frac{\left\|\left(I_N + \zeta(j\omega)\beta(j\omega)\Gamma\right)^{-1} \zeta(j\omega)\tilde{i}_{src}(j\omega)\right\|_2}{\left\|\tilde{i}_{src}(j\omega)\right\|_2}
$$

$$
= \sup_{\omega \in \mathbb{R}} \frac{\left\|Q(I_N + \zeta(j\omega)\beta(j\omega)\Lambda)^{-1} \zeta(j\omega)Q^T\tilde{i}_{src}(j\omega)\right\|_2}{\left\|Q^T\tilde{i}_{src}(j\omega)\right\|_2}, \quad (5.38)
$$

where $\Gamma$ was diagonalized as $\Gamma = Q\Lambda Q^T$ in the second line above. Two key observa-
tions will now be made to simplify (5.38):

i) The first column of $Q$ is given by $q_1 = \frac{1}{\sqrt{N}}1$. Furthermore, $1^T \Pi = 1^T (I_N - \frac{1}{N}11^T) = 1^T - \frac{1}{N} (1^T 1) 1^T = 0^T$. Therefore, the vector $Q^T i_{\text{src}}(s) = Q^T \Pi i_{\text{src}}(s)$ is given by

$$Q^T i_{\text{src}}(s) = Q^T \Pi i_{\text{src}}(s) = [0, D(s)]^T,$$

where $D(s) \in \mathbb{C}^{N-1 \times 1}$ is made up of the non-zero elements of the vector $Q^T \Pi i_{\text{src}}(s)$.

ii) Denote the diagonal matrix with diagonal entries comprised of the non-zero eigenvalues of $\Gamma$ by $\Lambda_{N-1}$, i.e., $\Lambda_{N-1} = \text{diag}\{\lambda_2, \ldots, \lambda_N\} \in \mathbb{R}^{N-1 \times N-1}$.

Using the two observations highlighted above, (5.38) can now be simplified as

$$\|F(\zeta(s)I_N, \beta(s)\Gamma)\|_\infty = \sup_{\omega \in \mathbb{R}} \left| \left( I_{N-1} + \zeta(j\omega)\beta(j\omega)\Lambda_{N-1} \right)^{-1} \zeta(j\omega)D(j\omega) \right|_2 = \sup_{j=2, \ldots, N} \left( \sup_{\omega \in \mathbb{R}} \left( \frac{D^*(j\omega) (1 + \zeta(j\omega)\beta(j\omega)\lambda_j)^{-1} \zeta(j\omega)D(j\omega)}{D^*(j\omega)D(j\omega)} \right)^{\frac{1}{2}} \right) \sup_{\omega \in \mathbb{R}} \|F(\zeta(s), \beta(s)\lambda_j)\|_\infty = \|F(\zeta(s), \beta(s)\lambda_2)\|_\infty,$$

where the last equality follows from the fact that $\|F(\zeta(s), \beta(s)\lambda)\|_\infty$ is a decreasing function of $\lambda$ [104]. From (5.34) and (5.40), it is apparent that (5.29) is a sufficient condition for global asymptotic synchronization. \(\square\)

Intuitively, the proof for Theorem 1 can be thought of as being based on the closed-loop block-diagram of the differential system in Fig. 6.5. Recall that the $L_2$ gain provides a measure of the largest amplification imparted by a system as a signal propagates through it. Thus, if the product of the differential $L_2$ gains, $\bar{\gamma}(F(Z_{\text{osc}}(s), Y(s)))$ and $\bar{\gamma}(g)$, is less than 1, it follows that the differential vectors, $\tilde{v}$ and $\tilde{i}_{\text{src}}$, both decay to zero and oscillator synchronization results. It can equivalently be stated that because the differential system in Fig. 6.5 is stable, the differential vectors tend towards zero.
5.3 System of Deadzone Oscillators

In this section, the oscillator model which will form the basis of the inverter control will be described and the coupling network of a microgrid with $N$ parallel inverters will be characterized. It will be shown that when Theorem 1 is applied to the system of interest, the synchronization criterion is independent of the number of oscillators and load parameters.

Before describing the oscillator, Liénard’s theorem is stated below. This theorem will be used to establish the existence of a stable and unique limit cycle in the particular oscillator under study.

**Theorem 2.** (Liénard’s Theorem [94]) Consider the system

$$\ddot{v} + r(v)\dot{v} + m(v) = 0, \quad (5.41)$$

where $v : [0, \infty) \to \mathbb{R}$ and $r(v), m(v) : \mathbb{R} \to \mathbb{R}$ are differentiable with respect to $v$. The functions, $r(v)$ and $m(v)$, are even and odd, respectively. In addition, define

$$R(v) := \int_0^v r(\tau) \, d\tau. \quad (5.42)$$

The system in (5.41) has a unique and stable limit cycle if: i) $m(v) > 0 \forall v > 0$, ii) $R(v)$ has one positive zero for some $v = p$, iii) $R(v) < 0$ when $0 < v < p$, and iv) $R(v)$ monotonically increases for $v > p$ and $\lim_{v \to \infty} R(v) = \infty$.

5.3.1 Oscillator Description

In this work, the *dead-zone oscillator* shown in Fig. 5.5 is used, in which the linear subsystem is composed of a parallel $RLC$ circuit with impedance

$$z_{osc}(s) = R \| sL \| (sC)^{-1}, \quad (5.43)$$

and the nonlinear current source is given by

$$g(v) = f(v) - \sigma v, \quad (5.44)$$

where $f(\cdot)$ is a continuous, differentiable dead-zone function with slope $2\sigma$, and $f(v) \equiv 0$ for $v \in (-\varphi, +\varphi)$, as illustrated in Fig. 5.6(a). The function $g(v)$, which
is plotted in Fig 5.6(b), resembles a piecewise linear function. As illustrated in Fig 5.6(b), the nonlinear current source, \( g(v) \), acts as a power source for \( v < 2\varphi \) and as a dissipative element when \( v > 2\varphi \).  

![Figure 5.5: A single nonlinear oscillator.](image)

Using Kirchhoff’s voltage and current laws, the terminal voltage of the dead-zone oscillator can be derived as

\[
LC \frac{d^2 v}{dt^2} + L \left( \frac{df(v)}{dv} + \frac{1}{R} - \sigma \right) \frac{dv}{dt} + v = 0. \tag{5.45}
\]

(5.45) can be rewritten by expressing the derivatives of \( v \) with respect to \( \tau = t/\sqrt{LC} \) to get

\[
\ddot{v} + \sqrt{\frac{L}{C}} \left( \frac{df(v)}{dv} + \frac{1}{R} - \sigma \right) \dot{v} + v = 0, \tag{5.46}
\]

\[\text{1} \text{The proposed dead-zone oscillator is very similar to the well-known Van der Pol oscillator which utilizes a cubic nonlinearity instead of a deadzone nonlinearity as used here [99].}\]
which is of the form in (5.41), with

\[
\begin{align*}
m(v) &= v \\
r(v) &= \sqrt{\frac{L}{C}} \left( \frac{df(v)}{dv} + \frac{1}{R} - \sigma \right).
\end{align*}
\] (5.47)

For the case \( \sigma > 1/R \), it is easy to see that \( m(v) \), \( r(v) \), and \( R(v) \) satisfy the conditions in Liénard’s theorem, implying that the dead-zone oscillator has a stable and unique limit cycle. The steady-state limit cycles of the dead-zone oscillator are plotted for different values of \( \epsilon = \sqrt{\frac{L}{C}} (\sigma - \frac{1}{R}) \) in Fig. 5.7(a). For comparison, the limit cycles of the well-known Van der Pol oscillator for the same set of parameters is shown in Fig. 5.7(b). When \( \epsilon \ll 1 \), it can be shown that the steady-state oscillation will have a frequency approximately equal to \( \frac{1}{\sqrt{LC}} \). Furthermore, it is evident that for small values of \( \epsilon \), the phase-plot resembles a unit circle, and as a result, the voltage oscillation approximates an ideal sinusoid in the time-domain.

![Figure 5.7: Phase-plot of steady-state limit-cycles in the (a) dead-zone and (b) Van der Pol oscillators for varying \( \epsilon \).](image)

Intuitively, the oscillation results from a periodic energy exchange between the passive RLC circuit and nonlinear element, \( g(v) \), at the RLC resonant frequency, \( \omega_0 = \frac{1}{\sqrt{LC}} \). The piecewise nonlinearity in Fig. 5.6(b) acts as a dissipative circuit element when the \( i-v \) curve lies in quadrants I and III and as a power source when in quadrants II and IV. As a result, the nonlinear current source injects power into the system for small values of \( v \), and dissipates power for large values of \( v \). The overall
tendency is for small oscillations to grow while large oscillations are damped such that a unique steady-state oscillation of some intermediate amplitude is reached.

Example

In the following example, the objective will be to design a 60 Hz deadzone oscillator. The parameters $R$, $L$ and $\varphi$ were selected as 10 $\Omega$, 500 $\mu$H, and 0.4695 V, respectively. The resonant frequency, denoted as $\omega_o = 2\pi 60$ rad/s, was maintained by choosing $C = \frac{1}{\omega^2_o L}$. Figure 5.8 shows the steady-state oscillation when $\sigma$ is chosen as approximately 0.63 $\Omega^{-1}$, 5.4 $\Omega^{-1}$, and 16 $\Omega^{-1}$ such that the resulting value of $\epsilon$ is 0.1, 1, and 3, respectively. It can be seen that as $\sigma$ increases, the distortion in the waveform increases. Furthermore, the desired frequency is attained for small values of $\epsilon$.

![Figure 5.8: Deadzone oscillator limit-cycle for various values of $\epsilon$ as $\sigma$ is changed. The amplitude of the oscillation has been normalized to facilitate comparison.](image)

5.3.2 Network Description

Microgrids are regularly made up of $N$ parallel inverters connected across a load [8, 66], and this motivates investigation of the network topologies in Figs. 5.9 and 5.10. Each oscillator is connected to a common node through a branch impedance, $z_{\text{net}}(s)$, which may contain any combination of linear circuit elements. The voltage at the common node to which all the network impedances are connected is denoted by
Consider the case when no load is connected to the common node. The results from Section 5.2.2 can be used to derive a sufficient condition for oscillator synchronization. The synchronization condition will be shown to be independent of the number of oscillators. In the forthcoming section, the case where the oscillators deliver power to a load (connected at the common node) will be analyzed, and it will be demonstrated that the synchronization condition is identical to the case with no load. This is a remarkable result, because it implies the system can be designed independent of the load parameters and knowledge of number of inverters.

5.3.2.1 System of Oscillators Connected to No Load

Consider first the no load case. From Fig. 5.9, the $j^{th}$ oscillator output current is given by

$$i_j (s) = \frac{1}{z_{net} (s)} (v_j (s) - v_{load} (s)).$$  \hspace{1cm} (5.48)

Since the output currents must sum to zero,

$$0 = \sum_{k=1}^{N} i_k (s) = \frac{1}{z_{net} (s)} \left( \sum_{k=1}^{N} v_k (s) \right) - N v_{load} (s).$$  \hspace{1cm} (5.49)
Rearranging terms,
\[ v_{\text{load}}(s) = \frac{1}{N} \sum_{k=1}^{N} v_k(s). \]  
(5.50)

Substituting (5.50) in (5.48) leads to
\[ i_j(s) = \frac{1}{z_{\text{net}}(s)} \left( v_j(s) - \frac{1}{N} \sum_{k=1}^{N} v_k(s) \right). \]  
(5.51)

Writing all output currents in matrix form gives
\[ i(s) = \frac{1}{z_{\text{net}}(s)} \left( I_N - \frac{1}{N} \mathbf{1} \mathbf{1}^T \right) v(s) = \frac{1}{N z_{\text{net}}(s)} \Gamma v(s), \]  
(5.52)
where
\[ \Gamma = N I_N - \mathbf{1} \mathbf{1}^T = \begin{bmatrix} N & -1 & \cdots & -1 \\ -1 & N & \cdots & -1 \\ \vdots & \vdots & \ddots & \vdots \\ -1 & -1 & \cdots & N - 1 \end{bmatrix}, \]  
(5.53)
for this particular network. The smallest non-zero eigenvalue, \( \lambda_2 \), of this Laplacian is equal to \( N \). Comparing (5.52) with (5.9), it is clear that
\[ Y(s) = \frac{1}{N z_{\text{net}}(s)} \Gamma. \]  
(5.54)

Furthermore, by referring to (5.10) and (5.30), it follows that for the no-load case
\[ \begin{cases} \\ \alpha(s) = 0 \\ \beta(s) = (N z_{\text{net}}(s))^{-1} \\ \zeta(s) = z_{\text{osc}}(s) \end{cases}. \]  
(5.55)

Applying \( \zeta(s), \beta(s), \) and \( \lambda_2 \) for this network in the linear fractional transformation of Theorem 1 leads to
\[ \mathcal{F}(\zeta(s), \beta(s)\lambda_2) = \left( 1 + \zeta(s)\beta(s)\lambda_2 \right)^{-1} \zeta(s) \]  
\[ = \frac{z_{\text{osc}}(s)}{1 + z_{\text{osc}}(s) (N z_{\text{net}}(s))^{-1} N} \]  
\[ = \frac{z_{\text{osc}}(s) z_{\text{net}}(s)}{z_{\text{net}}(s) + z_{\text{osc}}(s)}. \]  
(5.56)
It is interesting to note that \( F(\zeta(s), \beta(s) \lambda_2) \) equals the impedance of the parallel combination of \( z_{\text{osc}}(s) \) and \( z_{\text{net}}(s) \). Applying (5.29) of Theorem 1 gives the following synchronization condition:

\[
\sup_{\omega \in \mathbb{R}} \left( \frac{z_{\text{net}}(j\omega) z_{\text{osc}}(j\omega)}{z_{\text{net}}(j\omega) + z_{\text{osc}}(j\omega)} \right)^2 \sigma < 1. \tag{5.57}
\]

Note that the condition for synchronization is independent of \( N \) and depends only on the impedance of the oscillator linear subsystem, \( z_{\text{osc}}(s) \), and the branch impedance, \( z_{\text{net}}(s) \).

5.3.2.2 System of Oscillators Connected to a Passive Linear Load

Consider now a linear load case. In Fig. 5.10, the load can be made up of any arbitrary combination of passive LTI circuit elements. The \( j \)th oscillator output current is given by (5.48), and further,

\[
v_{\text{load}}(s) = z_{\text{load}}(s) \sum_{k=1}^{N} i_k(s). \tag{5.58}
\]
Substituting (5.58) in (5.48) yields

\[ i_j(s) = \frac{1}{z_{\text{net}}(s)} \left( v_j(s) - z_{\text{load}}(s) \sum_{k=1}^{N} i_k(s) \right), \quad (5.59) \]

from which \( v_j(s) \) can be isolated to get

\[ v_j(s) = z_{\text{net}}(s)i_j(s) + z_{\text{load}}(s) \sum_{k=1}^{N} i_k(s). \quad (5.60) \]

Collecting all terminal voltages in matrix form yields

\[ v(s) = \left( z_{\text{net}}(s) I_N + z_{\text{load}}(s) 11^T \right) i(s). \quad (5.61) \]

Comparing (5.61) with (5.9) indicates

\[ Y^{-1}(s) = z_{\text{net}}(s) I_N + z_{\text{load}}(s) 11^T. \quad (5.62) \]

To invert (5.62), begin by diagonalizing \( 11^T = QAQ^T \), where \( \Lambda = \text{diag}(0, \ldots, 0, N) \in \mathbb{R}^{N \times N} \), to get

\[
Y^{-1}(s) = z_{\text{net}}(s) I_N + z_{\text{load}}(s) Q\Lambda Q^T \\
= z_{\text{net}}(s)Q \left( I_N + \frac{z_{\text{load}}(s)}{z_{\text{net}}(s)} \Lambda \right) Q^T. \quad (5.63)
\]

It will be useful to define

\[ z_{\text{eq}}(s) \triangleq z_{\text{net}}(s) + Nz_{\text{load}}(s). \quad (5.64) \]
Inverting the expression in (5.63) yields

\[
Y(s) = \frac{1}{z_{\text{net}}(s)} \frac{1}{z_{\text{eq}}(s)} Q \left( I_N - \frac{z_{\text{load}}(s)}{z_{\text{eq}}(s)} A \right) Q^T
\]

\[
= \frac{1}{z_{\text{net}}(s)z_{\text{eq}}(s)} Q \left( z_{\text{eq}}(s) I_N - z_{\text{load}}(s) A \right) Q^T
\]

\[
= \frac{1}{z_{\text{net}}(s)z_{\text{eq}}(s)} \left( (z_{\text{net}}(s) + Nz_{\text{load}}(s)) I_N - z_{\text{load}}(s) 11^T \right)
\]

\[
= \frac{1}{z_{\text{net}}(s)z_{\text{eq}}(s)} \left( z_{\text{net}}(s) I_N + z_{\text{load}}(s) (NI_N - 11^T) \right)
\]

\[
= \frac{1}{z_{\text{net}}(s)z_{\text{eq}}(s)} \left( z_{\text{eq}}(s) z_{\text{load}}(s) \Gamma \right),
\]  \hspace{1cm} (5.65)

where in the third line above, the definition of \(z_{\text{eq}}(s)\) from (5.64) was used, and in the last line, the \(\Gamma\) defined in (5.53) was utilized. Comparing (5.65) with (5.10), and using (5.30), it is evident that for the linear-load case:

\[
\begin{align*}
\alpha(s) &= z_{\text{eq}}^{-1}(s) \\
\beta(s) &= z_{\text{load}}(s) z_{\text{net}}(s) z_{\text{eq}}^{-1}(s) \\
\zeta(s) &= z_{\text{osc}}(s) z_{\text{eq}}(s) (z_{\text{osc}}(s) + z_{\text{eq}}(s))^{-1}
\end{align*}
\]  \hspace{1cm} (5.66)

As the system synchronizes and the interaction between oscillators decays to zero, the effective impedance observed from the output of the oscillator is equal to \(z_{\text{eq}}(s) = z_{\text{net}}(s) + N z_{\text{load}}(s)\). In other words, the effective load seen by each oscillator during synchronized system conditions is equal to \(z_{\text{eq}}(s)\).

For the \(\zeta(s)\) and \(\beta(s)\) in (5.66), it follows that

\[
\mathcal{F}(\zeta(s), \beta(s) \lambda_2) = (1 + \zeta(s) \beta(s) \lambda_2)^{-1} \zeta(s)
\]

\[
= \frac{z_{\text{osc}} z_{\text{eq}} (z_{\text{osc}} + z_{\text{eq}})^{-1}}{1 + z_{\text{osc}} z_{\text{eq}} (z_{\text{osc}} + z_{\text{eq}}) z_{\text{load}} z_{\text{net}} z_{\text{eq}}^{-1} N}
\]

\[
= \frac{z_{\text{osc}} (z_{\text{osc}} + z_{\text{eq}}) + z_{\text{osc}} z_{\text{eq}} z_{\text{load}} z_{\text{net}} z_{\text{eq}}^{-1} N}{z_{\text{osc}}}
\]

\[
= \frac{1 + z_{\text{osc}} z_{\text{eq}}^{-1} (1 + z_{\text{load}} z_{\text{net}}^{-1} N)}{z_{\text{osc}}}
\]

\[
= \frac{z_{\text{osc}}}{1 + z_{\text{osc}} z_{\text{eq}}^{-1} (z_{\text{eq}} z_{\text{net}}^{-1})} = \frac{z_{\text{osc}}(s) z_{\text{net}}(s)}{z_{\text{net}}(s) + z_{\text{osc}}(s)}.
\]  \hspace{1cm} (5.67)
Applying (5.29), the synchronization condition

$$\sup_{\omega \in \mathbb{R}} \left\| \frac{z_{\text{net}}(j\omega) z_{\text{osc}}(j\omega)}{z_{\text{net}}(j\omega) + z_{\text{osc}}(j\omega)} \right\|_2 < 1$$

(5.68)

follows, which is the same condition as the no-load case in (5.57). Notice that the synchronization condition is independent of the number of oscillators and the load impedance.

5.4 Case Studies

In this section, simulation results are presented to validate the synchronization condition. In particular, it will be demonstrated that a system of inverters controlled as deadzone oscillators satisfying (5.29) will synchronize in a passive electrical network and deliver power to a load.

In all the case studies, a network with the topology in Fig. 5.10 will be considered. The network branch impedance is given by $z_{\text{net}}(s) = sL_{\text{net}} + R_{\text{net}}$, where $L_{\text{net}}$ and $R_{\text{net}}$ correspond to the combined line and inverter-output-filter inductance and resistance, respectively (the inverter output-filter inductance is used to reduce harmonics in the inverter output current that arises due to switching [80]). Finally, it is assumed that the load is resistive such that $z_{\text{load}}(s) = R_{\text{load}}$.

Table 5.1: System parameters used in the case studies.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Case Study I, II</th>
</tr>
</thead>
<tbody>
<tr>
<td>$N$</td>
<td>100</td>
</tr>
<tr>
<td>$R$</td>
<td>8.66 Ω</td>
</tr>
<tr>
<td>$L$</td>
<td>433.2 µH</td>
</tr>
<tr>
<td>$C$</td>
<td>16.2 mF</td>
</tr>
<tr>
<td>$\sigma$</td>
<td>1.15 S</td>
</tr>
<tr>
<td>$\varphi$</td>
<td>146.1 V</td>
</tr>
<tr>
<td>$\epsilon$</td>
<td>0.170</td>
</tr>
<tr>
<td>$R_{\text{net}}$</td>
<td>0.1 Ω, 0.02 Ω</td>
</tr>
<tr>
<td>$L_{\text{net}}$</td>
<td>500 µH</td>
</tr>
<tr>
<td>$R_{\text{load}}$</td>
<td>91.96 mΩ</td>
</tr>
</tbody>
</table>

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For this system, the linear fractional transformation is given by

$$
F(z_{osc}(s), z_{net}^{-1}(s)) = \frac{z_{osc}(s)z_{net}(s)}{z_{net}(s) + z_{osc}(s)}
$$

$$
= \frac{1}{s} \frac{1}{s^2 + \frac{1}{RC} s + \frac{1}{LC} + \frac{s}{C} (L_{net} s + R_{net})^{-1}}
$$

$$
= \frac{(L_{net} s + R_{net}) s}{L_{net} C s^3 + (\frac{L_{net}}{R} + R_{net} C) s^2 + (\frac{L_{net}}{L} + \frac{R_{net}}{R} + 1) s + \frac{R_{net}}{L}}. \tag{5.69}
$$

The design objective is to select $R$, $L$, $C$, $\sigma$, and $\varphi$ for a given $z_{net}(s)$, such that the load voltage and system frequency meets performance specifications. Further, to guarantee synchronization, the system design should satisfy the synchronization condition $\|F(z_{osc}(j\omega), z_{net}^{-1}(j\omega))\|_\infty \sigma < 1$. The next chapter outlines a parameter selection technique which guarantees the inverters oscillate at the desired frequency and that in steady-state $v_{load}$ stays within $\pm5\%$ of the rated voltage across the entire load range (no-load to maximum rated load).

![Figure 5.11: Inverter output currents, voltages, and voltage synchronization error in the case when $\|F(z_{osc}(j\omega), z_{net}^{-1}(j\omega))\|_\infty \sigma < 1$.](image)

In case studies I and II, a power system consisting of 100 parallel inverters which are each rated for 10 kW was simulated. The RMS voltage and frequency ratings of the system are 220 V and 60 Hz, respectively, and the maximum load power is 1 MW. The system parameters used in each case study are summarized in Table 5.1.
5.4.1 Case Study I (Simulation)

Figure 5.12: Evolution of state-variables during startup in the presence of a load. Waveforms for 10 (out of 100 simulated) are shown for clarity.

Substituting the corresponding values in Table 5.1 into (5.69), it can be shown that \( \| F(z_{\text{osc}}(j\omega), z_{\text{net}}^{-1}(j\omega)) \|_\infty \sigma = 0.77 < 1 \). Therefore, synchronization of the oscillator system is guaranteed. At \( t = 0 \), all currents are zero and the oscillator capacitor voltages are chosen to be uniformly distributed between ±10 V. Initially, the system contains no load. After successful synchronization, the load is abruptly added at \( t = 300 \) ms. As shown in Fig. 5.11, the voltage stays within ±5\% of the rated value during steady-state conditions.

A second simulation was prepared to demonstrate synchronization in the presence of the load. In other words, the load is connected at \( t = 0 \) s. Given identical initial conditions as used above, Fig. 5.12 shows the trajectories of the state-variables (only 10 out of 100 waveforms are shown for clarity). The inductor current within the oscillator RLC circuit is denoted as \( i_L \). As shown in Fig. 5.12, the state-variables reach a stable limit-cycle.

5.4.2 Case Study II (Simulation)

All parameters, except \( R_{\text{net}} \), and initial conditions in case study I were re-used. The value of \( R_{\text{net}} \) was reduced such that \( \| F(z_{\text{osc}}(j\omega), z_{\text{net}}^{-1}(j\omega)) \|_\infty \sigma = 2.78 \not< 1 \), and synchronization is not guaranteed. At \( t = 0 \), the load is connected to the system. As illustrated in Fig. 5.13, the inverters do not reach synchrony.
5.5 Conclusion

In this chapter, it was proposed that inverters in a microgrid be controlled to act as nonlinear oscillators. The resulting microgrid is modular and does not require communication between inverters. A general theorem was developed which gives a synchronization condition for $N$ nonlinear oscillators coupled through an LTI electrical network. It was shown that when this theorem is applied to $N$ oscillators connected in parallel across a load, the synchronization condition is independent of $N$ and the load parameters. Simulation results were used to substantiate the analytical framework and illustrate the merit of the proposed application. In the next chapter, practical design and implementation techniques will be outlined in addition to extensive experimental results.
Chapter 6

VIRTUAL OSCILLATOR CONTROL OF
SINGLE-PHASE INVERTERS IN A MICROGRID

This chapter introduces a method for coordinating parallel inverters such that each inverter is digitally controlled to mimic the nonlinear oscillator introduced in Section 5.3.1. This method will be called virtual oscillator control. A practical method is outlined for the control design and implementation of a microgrid with \( N \) parallel inverters controlled as deadzone oscillators. In the previous chapter, it was shown that the system synchronization condition depends only on the oscillator parameters and output filter impedance of a single inverter. Here, this result is applied by putting forward a design procedure based on the parameters of one inverter. A method for adding inverters into an energized microgrid is also introduced and experimental results are presented.

6.1 Approach

Consider the system of parallel single-phase voltage source inverters in a microgrid, as shown in Fig. 6.1(a). The objective is to control this system of inverters such that

a. Communication between inverter controllers is unnecessary.

b. The load is shared equally between inverters.

c. All ac outputs synchronize and oscillate at desired frequency.

d. Inverter synchronization is guaranteed for any number of parallel inverters.

e. Load voltage is maintained within desired limits.

In this work, it is proposed that the inverters in Fig. 6.1(a) be controlled to mimic the system of parallel deadzone oscillators in Fig. 6.1(b) such that the objectives,
Figure 6.1: The system of inverters in (a) will be controlled to emulate the system of oscillators in (b).

as outlined above, are satisfied. Next, a practical method of controlling inverters by digital means such that they act as deadzone oscillators is described.

6.1.1 Control Implementation

To control a single-phase inverter such that it mimics a deadzone oscillator, it is proposed that the differential equations of the oscillator be programmed on the digital controller of the inverter. Because the deadzone oscillator does not physically exist, it is described as being “virtual.” A representative implementation of the proposed control on a single-phase H-bridge inverter is given in Fig. 6.2. As depicted, the measured output current of the inverter is scaled by $\kappa_i$ and extracted from the virtual oscillator. The oscillator voltage is then multiplied by $\kappa_v$ and used to generate a modulation signal, $m$. Lastly, the inverter switching signals are generated by applying a PWM technique, i.e., sine-triangle PWM or some other established technique.

With the proposed method, the inverter will emulate the dynamics of the nonlinear oscillator such that the inverter output voltage, $v$, follows the scaled oscillator voltage, $\kappa_v v_{osc}$. Furthermore, the current extracted from the virtual oscillator is
equal to the scaled output current, $\kappa_i i$. Later the scaling parameters, $\kappa_v$ and $\kappa_i$, will be used to aid the design process.

6.2 System Analysis

In this section, the dynamic system equations of an inverter system with the proposed control implementation are derived. Effort will be focused on the parallel topology with a load connected at the common node. Because the analysis in this section closely mirrors that of Section 5.2.1, several references to the previous chapter will be made to avoid repetition. One key difference of the analysis presented here is that there is a distinction between a virtual system of oscillators, which reside within the digital controllers, and a system of inverters coupled through a physical electrical network. After the system equations are derived, Theorem 1 of the previous chapter will be used to attain a synchronization condition.

6.2.1 System Description

As outlined in Section 6.1.1, each inverter is digitally controlled to mimic the dynamics of a deadzone oscillator. A system of $N$ parallel connected inverters with virtual oscillator control can be modeled using the diagram in Fig. 6.3. The system on
Figure 6.3: \(N\) parallel connected inverters and associated virtual oscillator controllers coupled through a microgrid network.

The left represents the \(N\) virtual oscillators which reside within the microcontroller associated for each inverter. The right-hand side of the diagram is a representation of the \(N\) inverters and the microgrid network. The \(j\)th inverter is modeled as the controlled voltage source \(v_j\), and \(v = [v_1(s), \ldots, v_N(s)]^T\) is the vector of inverter voltages.

Using Fig. 6.3, the inverter voltages and currents are related by

\[ i(s) = Y(s)v(s), \]  

(6.1)

where \(i(s) = [i_1(s), \ldots, i_N(s)]^T\) is the vector of inverter output currents and \(Y(s)\) is the network admittance transfer matrix. As shown in the previous chapter, the admittance matrix for the network in Fig. 6.3 can be written as

\[ Y(s) = \frac{1}{z_{\text{net}}(s)z_{\text{eq}}(s)} \left( z_{\text{net}}(s)I_N + z_{\text{load}}(s)\Gamma \right). \]  

(6.2)

Recall that \(z_{\text{eq}}(s)\) is defined as

\[ z_{\text{eq}}(s) \triangleq z_{\text{net}}(s) + Nz_{\text{load}}(s), \]  

(6.3)

and the Laplacian, \(\Gamma\), for this particular network is given by (5.53).
From Fig. 6.3, it follows that the voltage of the \( j \)th virtual oscillator, \( v_{\text{osc}}(s) \), can be expressed as

\[
v_{\text{osc}}(s) = z_{\text{osc}}(s) (i_{\text{src}}(s) - i_{\text{osc}}(s)), \quad \forall j = 1, \ldots, N, \tag{6.4}
\]

where \( i_{\text{osc}}(s) \) is the output current the \( j \)th virtual oscillator. The output voltages and currents of the \( j \)th oscillator and inverter are related by

\[
v_{\text{osc}}(s)\kappa_v = v_j(s), \tag{6.5}
\]

and

\[
i_{\text{osc}}(s) = i_j(s)\kappa_i, \tag{6.6}
\]

where \( \kappa_v, \kappa_i \in \mathbb{R} \) are the voltage and current scaling gains, respectively, described in Section 6.1.1. From (6.5) and (6.6), it is apparent that the inverter voltage equals the scaled oscillator voltage and the oscillator output current is nothing more than the scaled inverter output current. It will be useful to define

\[
\kappa \triangleq \kappa_i\kappa_v \tag{6.7}
\]

Writing all \( N \) oscillator voltages in matrix form gives

\[
v_{\text{osc}}(s) = Z_{\text{osc}}(s) (i_{\text{src}}(s) - i_{\text{osc}}(s))
= Z_{\text{osc}}(s) (i_{\text{src}}(s) - \kappa i(s))
= Z_{\text{osc}}(s) i_{\text{src}}(s) - \kappa Z_{\text{osc}}(s) Y(s) v_{\text{osc}}(s). \tag{6.8}
\]

In the second line, (6.6) is substituted for \( i_{\text{osc}}(s) \), and in the last line \( i(s) = Y(s) v(s) = \kappa v Y(s) v_{\text{osc}}(s) \) comes from the substitution of (6.5) into \( v(s) \). Solving for \( v_{\text{osc}}(s) \) in (6.8) yields

\[
v_{\text{osc}}(s) = (I_N + \kappa Z_{\text{osc}}(s) Y(s))^{-1} Z_{\text{osc}}(s) i_{\text{src}}(s)
= F(Z_{\text{osc}}(s), \kappa Y(s)) i_{\text{src}}(s), \tag{6.9}
\]

where \( F(Z_{\text{osc}}(s), \kappa Y(s)) \) is the linear fractional transformation as defined in (5.14). Using (6.9), the system of coupled virtual oscillators can be represented compactly as the block-diagram in Fig. (6.4) where the linear and nonlinear portions of the system are clearly compartmentalized by \( F(Z_{\text{osc}}(s), \kappa Y(s)) \) and \( g(v) = [g(v_1), \ldots, g(v_N)]^T \).
respectively. Note that this diagram is very similar to that of Fig. 5.3.

![Block-diagram representation of coupled oscillator system](image)

Figure 6.4: Block-diagram representation of coupled oscillator system. Linear and nonlinear portions of the system are contained in $F(Z_{osc}(s), \kappa Y(s))$ and $g(v) = [g(v_1), \ldots, g(v_N)]^T$, respectively

### 6.2.2 Corresponding Differential System

The desire is to analyze global asymptotic synchronization in the network of virtual oscillators described above. Synchronization can be described by the condition

$$\lim_{t \to \infty} v_{oscj}(t) - v_{osck}(t) = 0 \forall j, k = 1, \ldots, N.$$  \hspace{1cm} (6.10)

Because the inverter voltages equal the scaled oscillator voltages within the controllers, it follows that virtual oscillator synchronization implies inverter voltage synchronization. Applying the projector matrix to the vector of oscillator voltages gives

$$\tilde{v}_{osc}(t)^T \tilde{v}_{osc}(t) = (\Pi v_{osc}(t))^T (\Pi v_{osc}(t))$$

$$= \frac{1}{2N} \sum_{j=1}^{N} \sum_{k=1}^{N} (v_{oscj}(t) - v_{osck}(t))^2.$$  \hspace{1cm} (6.11)

Recall that the projector matrix, $\Pi$, is defined in (5.6). It is apparent that oscillator voltage synchronization results when $\tilde{v}_{osc}(t) = \Pi v_{osc}(t) \to 0$ as $t \to \infty$.

Following along the same lines of the previous chapter, it can be shown that

$$\tilde{v}_{osc}(s) = (I_N + \kappa Z_{osc}(s)Y(s))^{-1} Z_{osc}(s) \tilde{i}_{src}(s)$$

$$= F(Z_{osc}(s), \kappa Y(s)) \tilde{i}_{src}(s).$$  \hspace{1cm} (6.12)

The map $\tilde{g} : \mathbb{R}^N \to \mathbb{R}^N$ captures the impact of $g(v)$ in the corresponding differential
Figure 6.5: Block-diagram representation of the corresponding differential system.

system and is defined as follows:

\[ \tilde{g} : \tilde{v}_{\text{osc}} \rightarrow -\tilde{i}_{\text{src}}. \]  

(6.13)

(6.12) and (6.13) form a complete description of the dynamics in the corresponding differential system. Furthermore, these results permit the block-diagram representation in Fig. 6.5, where, as in Fig. 6.4, the linear and nonlinear subsystems are compartmentalized using \( F(\cdot, \cdot) \) and \( \tilde{g} \), respectively.

6.2.3 Sufficient Condition for Global Asymptotic Synchronization

In this section, a sufficient synchronization condition for the parallel inverter system in Fig. 6.3 is given.

**Corollary 1.** The network of \( N \) parallel inverters in Fig. 6.3 synchronizes in the sense of (6.10), if

\[
\max_{\omega \in \mathbb{R}} \left\| \frac{\kappa^{-1} z_{\text{net}}(j\omega) z_{\text{osc}}(j\omega)}{\kappa^{-1} z_{\text{net}}(j\omega) + z_{\text{osc}}(j\omega)} \right\|_2 < 1.
\]  

(6.14)

The proof for Corollary 1 is included in the appendix. Notice that the synchronization condition in (6.14) is nearly identical to the condition given in (5.68). The only difference is that the impedance, \( z_{\text{net}} \), is scaled by \( \kappa^{-1} \). As before, the synchronization condition is independent of the number of inverters and the load parameters. A method for control design will now be outlined.

6.3 Control Design

In this section, a set of guidelines for parameter selection is presented. In addition, a technique which facilitates the addition of inverters in an energized system is developed.
6.3.1 Parameter Selection

Because the synchronization condition is independent of \( N \) and the load parameters, the task of system design is reduced to that of one inverter and its associated control. It will be assumed that the design of the inverter hardware is complete and that the design task is exclusively focused on control. In particular, the analyst is provided with an inverter which has a given filter impedance, \( z_{\text{net}} \), and power rating, \( P_{\text{max}} \). Furthermore, a system frequency rating, \( \omega_o \), is given. It will be assumed that the peak load voltage is allowed to deviate between upper and lower limits, \( v_{\text{max}} \) and \( v_{\text{min}} \), respectively. From here forward, \( v_{\text{pk}} \) denotes the peak value of \( v_{\text{load}} \) in steady-state conditions. The control design problem can be stated as given below.

**Design Problem Statement.** Select the virtual oscillator parameters \( R, L, C, \sigma, \varphi, \kappa_v \), and \( \kappa_i \) such that

\[
\begin{align*}
\frac{1}{\sqrt{LC}} &= \omega_o \\
\sigma &> \frac{1}{R} \\
v_{\text{pk}} &= v_{\text{max}} \text{ under no-load conditions} \\
v_{\text{pk}} &= v_{\text{min}} \text{ under maximum rated load conditions, } P_{\text{max}} \\
\epsilon &= \sqrt{\frac{L}{R} (\sigma - \frac{1}{R})} \text{ is minimized} \\
\sup_{\omega \in \mathbb{R}} \left\| \frac{\kappa - 1}{z_{\text{net}}(j\omega)z_{\text{osc}}(j\omega)} \right\|_2 \sigma < 1
\end{align*}
\]

(6.15)

Stated another way, the objectives are to ensure:

a. The inverters oscillate at \( \omega_o \).

b. Voltage limits are respected such that \( v_{\text{min}} \leq v_{\text{pk}} \leq v_{\text{max}} \) across the entire load range (no-load to maximum rated load).

c. The distortion on the sinusoidal output is minimized.

d. The synchronization condition is satisfied.

Given the nonlinear nature of the system and lack of analytical tools for the proposed deadzone oscillator, the iterative design process in Fig. 6.6 is proposed. In steps 3 and 4, the analyst must simulate the model in Fig. 6.7 until steady-state conditions are reached. In step 2, the parameters \( R \) and \( C \) are selected such that the individual inverter has a stable oscillation at the rated system frequency. The constraint \( \sigma > \frac{1}{R} \) ensures that a stable oscillation exists (see Lienard’s theorem in the previous chapter
for justification), and the relation \( \omega_0 = \frac{1}{\sqrt{LC}} \) guarantees that the circuit oscillates at the rated frequency, \( \omega_0 \). Steps 3 and 4, which require a time-domain simulation of the model in Fig. 6.7, are motivated by the observation that the amplitude of \( v_{\text{load}} \) decreases as the real power consumed in the load increases. Consequently, the maximum and minimum load voltages correspond to the no load and full-rated load cases, respectively. It follows that once steps 3 and 4 are complete, then \( v_{\min} \leq v_{pk} \leq v_{\max} \) will be satisfied across the entire rated load range. Lastly, if the synchronization condition is satisfied, a system of \( N \) inverters with identical design parameters is guaranteed to synchronize.

Figure 6.6: Design process for computation of \( R, L, C, \sigma, \varphi, \kappa_v, \) and \( \kappa_i \).
Figure 6.7: Circuit model used in control parameter selection. Design parameters are highlighted in red.

If the synchronization condition in step 5 fails, the analyst must return to step 2 and adjust the RLC parameters by decreasing $L$ and/or $R$. This guideline is based on the empirical observation that the values of $L$ and $R$ tend to have the largest influence on the value of \[ \max_{\omega \in \mathbb{R}} \left\| \kappa^{-1} z_{\text{net}}(\omega) z_{\text{osc}}(\omega) \right\|_2 \]. Future work will be focused on analyzing the dependence of the linear fractional transformation norm on the control parameters so that a more precise design procedure can be attained. Optimization techniques will also be explored. An illustrative example will be given to illustrate the dependence of the synchronization condition on the oscillator parameters.

### 6.3.2 Inverter Addition and Pre-Synchronization

This section addresses the challenge of adding inverters to an energized system. As previously shown, the condition for global asymptotic synchronization is independent of $N$ and the load parameters. This implies that as the number of inverters changes, the system is guaranteed to synchronize. In other words, so long as the synchronization condition is satisfied, inverters can be added and removed as needed and the system is guaranteed to synchronize in the steady-state. Despite this favorable property, it is possible that system transients can be undesirably large when inverters are added. In order to facilitate the seamless addition of inverter units and avoid hardware damage due to large transients, the concept of \textit{pre-synchronization} is introduced.
Assume that for $t < t_o$, there are $N$ inverters operating in a microgrid with a load. At $t = t_o$, the desire is to add an additional inverter (or multiple inverters) to the system. Assume that the additional inverter is capable of measuring the common node voltage, $v_{\text{load}}$, prior to being added. As shown in Fig. 6.8, for $t < t_o$ the virtual oscillator of the inverter to be added will be augmented with a pre-synchronization circuit which consists of: i) a scaled filter impedance, $\kappa^{-1} z_{\text{net}}$, ii) a virtual load, $z_{\text{virt}}$, and iii) a voltage source which follows $v_{\text{load}}$ and is interfaced through a series resistor, $R_{\text{link}}$. Before the additional inverter is connected to the system, it is assumed that the $N$ operational inverters are synchronized and in steady-state. The purpose of the pre-synchronization circuit is to bring the state-variables of the additional inverter controller as close as possible to synchronization with the operational inverter controllers before being added to the system.

It is proposed that the pre-synchronization control in Fig. 6.8 be allowed to reach steady-state before the inverter is added to the system at $t = t_o$. The design of the pre-synchronization circuit was based on some key observations. During steady-state conditions: i) if the virtual load is chosen such that $z_{\text{virt}} \approx \kappa^{-1} N z_{\text{load}}$, then the virtual oscillator state variables in the additional unit closely match that of the operational inverter controllers, and ii) $v_{\text{virt}} \approx \kappa v_{\text{load}}$, where $v_{\text{virt}}$ is the voltage across the virtual load and $v_{\text{load}}$ is load voltage in the energized system. During these conditions, inverters can be added with minimal system transients. When the inverter is added at $t = t_o$, the pre-synchronization circuit is removed and the
original virtual oscillator control remains.

6.4 Experimental Results

In this section, a hardware validation of the proposed control technique is demonstrated. Furthermore, the synchronization condition is applied to a practical system. In each experiment, a system with the topology illustrated in Fig. 6.9 is considered. The three single-phase H-bridge inverters and accompanying control, as shown in Fig. 6.10, are configured to deliver power to a load. Each inverter is interfaced to a common node through identical branch impedances, \( z_{\text{net}}(s) = sL_f + R_f \). The filter inductance is denoted as \( L_f \) and the combined resistance of the inductor windings, connectors, and conductors is lumped into \( R_f \). Each inverter is rated to deliver approximately 50 W and has a 100 V dc source at the input. The controllers were implemented on a Texas Instruments TMS320F28335 microcontroller and each inverter utilized an independent control loop.

Figure 6.9: Diagram of experimental system.

For the system structure in Fig. 6.9, the linear fractional transformation is given
Figure 6.10: Hardware setup of three parallel inverters with control.

Table 6.1: Control and hardware parameters used in experiments

<table>
<thead>
<tr>
<th>System parameters</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>$\omega_0 = 2\pi 60 \text{ rad/s}$</td>
<td>$\sigma = 1 \text{ S}$</td>
</tr>
<tr>
<td>$v_{\text{rated}} = 60\sqrt{2} \text{ V}$</td>
<td>$R = 10 \Omega$</td>
</tr>
<tr>
<td>$v_{\text{max}} = 1.05v_{\text{rated}}$</td>
<td>$L = 500 \mu\text{H}$</td>
</tr>
<tr>
<td>$v_{\text{min}} = 0.95v_{\text{rated}}$</td>
<td>$C = \frac{1}{L\omega^2} \approx 14.07 \text{ mF}$</td>
</tr>
<tr>
<td>$\kappa_v = 60\sqrt{2}$</td>
<td>$\varphi = 0.4695 \text{ V}$</td>
</tr>
<tr>
<td>$\kappa_i = 0.1125$</td>
<td>$\epsilon = 0.170$</td>
</tr>
<tr>
<td>$z_{\text{virt}} = 2\kappa^{-1}57.5 \Omega$</td>
<td>$R_f = 1 \Omega$</td>
</tr>
<tr>
<td>$R_{\text{link}} = \kappa^{-1}100 \Omega$</td>
<td>$L_f = 6 \text{ mH}$</td>
</tr>
</tbody>
</table>

by

$$F(z_{\text{osc}}(s), \kappa z_{\text{net}}^{-1}(s)) = \frac{\kappa^{-1}z_{\text{net}}(j\omega)z_{\text{osc}}(j\omega)}{\kappa^{-1}z_{\text{net}}(j\omega) + z_{\text{osc}}(j\omega)}$$

$$= \frac{1}{s^2 + \frac{1}{RC}s + \frac{1}{LC} + \frac{s}{C}\kappa(L_is + R_f)^{-1}}$$

$$= \frac{(L_{\text{net}}s + R_{\text{net}})s}{L_{\text{net}}Cs^3 + (\frac{L_{\text{net}}}{R} + R_{\text{net}}C)s^2 + (\frac{L_{\text{net}}}{R} + R_{\text{net}} + \kappa)s + \frac{R_{\text{net}}}{L}}. \quad (6.16)$$

In each experimental case study, the peak voltage and frequency ratings of the system are $60\sqrt{2} \text{ V}$ and $60 \text{ Hz}$, respectively. Using the design procedure in Section 6.3.1, the parameters in Table 6.1 were selected such that the load voltage stayed within $\pm 5\%$ of the rated value across the load range (no-load to maximum rated load).
Substituting the corresponding values in Table 6.1 into (6.16), it can be shown that 
\[ \|F(z_{osc}(j\omega), \kappa z_{net}^{-1}(j\omega))\|_{\infty} \sigma = 0.93 < 1. \]
Therefore, synchronization of the inverter system is guaranteed. In the forthcoming experiments, the inverter system will be connected to a variety of loads. Although the synchronization condition has been proven for systems with passive linear loads, stable operation with nonlinear and mechanical loads will also be demonstrated. System startup and load transients will be considered in addition to inverter removal and addition dynamics. In each oscilloscope screenshot, the top three waveforms will correspond to the measured inverter currents and the bottom waveform is the load voltage.

6.4.1 Resistive load

Startup

To mimic non-ideal startup conditions, the virtual oscillator voltages were initialized such that \( \kappa_v v_{osc} (0) = v (0) = [5 \text{ V}, 4 \text{ V}, 3 \text{ V}]^T \) for each of the respective inverter controllers. Figure 6.11 shows the system currents and load voltages during start-up in the presence of a 50 Ω load.

![Figure 6.11: Measured inverter output currents and load voltage during system startup with a resistive load.](image)

Load Transients

In this experiment, \( R_{load} \) undergoes step changes between 500 Ω and 71.4 Ω. As shown in Figs. 6.12(a) and 6.12(b), the inverters increase and decrease their output
currents almost instantaneously as the load power changes. Furthermore, the load voltage amplitude remains nearly constant during transients.

Figure 6.12: Resistive load transients. Inverter output currents and load voltage during load step-up (a) and load step-down(b).

Inverter Removal and Addition

Now, consider the case when the number of inverters in the microgrid undergoes a change. System dynamics during inverter removal and addition are shown in Figs. 6.13(a) and 6.13(b), respectively. In both transients, $R_{\text{load}} = 66 \, \Omega$. During inverter removal, the remaining units quickly compensate by increasing their output currents. The pre-synchronization technique, with parameters as summarized in Table 6.1, was implemented before adding inverter #3 back into the system. As demonstrated in Fig. 6.13(b), system transients are relatively small during unit addition. Furthermore, the load voltage waveform is largely unaffected during both inverter removal and addition transients.

6.4.2 RLC load

Startup

In this section, the RLC load in Fig. 6.14(a) was used. Here, system start-up is demonstrated when the switch in the RLC load is closed. As before, the virtual oscil-
Figure 6.13: Inverter output currents and load voltage when an inverter is removed (a) and added (b) in the presence of a resistive load.

Figure 6.14: (a) Linear RLC load, and (b) nonlinear diode bridge rectifier load used in experiments.

![RLC Load Circuit](image1)

![Diode Bridge Rectifier Load Circuit](image2)

Load Transients

Now, consider transients in the RLC load where the switch in Fig. 6.14(a) is opened and closed. The system dynamics in Figs. 6.16(a) and 6.16(b) correspond to the opening and closing of the switch which interfaces the RL branch of the load, respectively.
Figure 6.15: Measured inverter output currents and load voltage during system startup with an RLC load.

Figure 6.16: RLC load transient. Inverter output currents and load voltage when RL load branch is added (a) and removed (b).

6.4.3 Nonlinear Diode Rectifier Load

In this section, the system is configured to deliver power to the nonlinear load in Fig. 6.14(b). Although the synchronization condition has not yet been proven to be valid in the presence a nonlinear load, experimental evidence is presented which shows that the proposed control is compatible with such loads.

Startup

The inverter controllers were initialized with non-uniform initial conditions as in the previous two experiments. As demonstrated in Fig. 6.17, the system of inverters
successfully synchronizes and delivers power to the load.

Figure 6.17: Measured inverter output currents and load voltage in the presence of a diode bridge rectifier load.

Inverter Removal and Addition

In this experiment, the number of parallel inverters connected to the nonlinear load will undergo changes. As illustrated in Fig. 6.18(a), the remaining inverters maintain synchronization and deliver power to the load when one inverter is removed. The pre-synchronization circuit parameters in Table 6.1 have been used such that $z_{\text{virt}} = 2\kappa^{-1} 57.5 \Omega$ and $R_{\text{link}} = \kappa^{-1} 100 \Omega$. The inverter addition transient in Fig. 6.18(b) is relatively small. It is worth noting that seamless unit addition results despite the fact that the actual load is nonlinear and the pre-synchronization virtual load is purely resistive. This implies that performance during unit addition is not particularly sensitive to the accuracy of the following approximation: choose $z_{\text{virt}} \approx \kappa^{-1} N z_{\text{load}}$.

6.4.4 Single-Phase Induction Machine Load

In the following experiments, the inverter system is delivering power to a pair of parallel-connected single-phase fans. Each mechanical load is rated for 120 V ac operation and the power ratings of each fan were 80 W and 260 W. Because an induction machine contains a back electromotive force voltage, the fan is not a passive LTI load. Consequently, the synchronization condition does not apply. However, it will be shown that the proposed inverter control still retains the desired performance.
Figure 6.18: Inverter output currents and load voltage when connected to a diode bridge rectifier load and an inverter is removed (a) and added (b).

Startup

Figure 6.19: Measured inverter output currents and load voltage in the presence of a two parallel fan loads.

Reusing previously stated initial conditions, the startup performance of the inverter system can be seen in Fig. 6.19. Results indicate that the inverters successfully synchronize and deliver power to the mechanical load.

Load Transients

In this experiment, the power consumed by the mechanical load is abruptly increased and decreased. Figures 6.20(a) and 6.20(b) illustrate system dynamics during a step-up and step-down in load power, respectively.
Figure 6.20: Mechanical load transients. Inverter output currents and load voltage during load step-up (a) and load step-down (b).

Figure 6.21: Single-phase constant power load.

6.4.5 Simulation of a Constant Power Load

In this section, a simulation is conducted of a system of inverters which are configured to deliver power to a constant power load. An average value simulation of the inverter system of the previous section is utilized. All control parameters and initial conditions are reused for consistency. As shown in Fig. 6.21, the load consists of a diode bridge rectifier and a 35 W constant power load on the dc side. The system of three inverters was allowed to synchronize and then the load was abruptly activated at approximately 0.16 s. As illustrated in Fig. 6.22, the system of inverters successfully delivers power to the load and maintains synchronization. The dc load power is denoted as $p_{cpl}$ in Fig. 6.22.
6.5 Conclusion

In this chapter, a practical method for the implementation of virtual oscillator control was developed. After giving the synchronization condition for a hardware system of parallel inverters, a design procedure was outlined. Furthermore, a method for seamlessly adding inverters into an energized microgrid was developed. Experimental results were used to demonstrate the merit of the proposed techniques. In particular, results demonstrated rapid system response to transients and synchronization despite non-ideal initial conditions. Seamless addition of inverters into the energized system was achieved with the proposed pre-synchronization method. Although the synchronization condition has been proven valid for linear loads only, hardware results indicate that the proposed control performs as desired with a variety of load types. Future work will be focused on developing control for systems of inverters with non-identical power ratings.
Chapter 7

CONCLUDING REMARKS AND FUTURE WORK

This dissertation presented methods for control, design, and analysis of distributed inverter systems in both grid-connected and microgrid applications. The central theme of this dissertation was the development of appropriate inverter coordination methods such that desired objectives are met. In particular, methods which departed from the conventional single-converter design approach were proposed such that inverter systems were considered as an integrated whole.

Several challenges arise when large numbers of power electronic devices are integrated into power systems. In particular, the amount of distortion present on the ac grid tends to increase due to the presence of switching harmonics. To address this challenge, it was proposed that the switch transitions of multiple inverters be staggered. This method was first applied to a multilevel inverter composed of cascaded H-bridge inverters which interfaced a set of distributed PV sources to an ac load. The switch interleaving method enabled the use of a very low switching frequency and a reduced filter inductance while maintaining a low-distortion ac output. A control system was developed which managed non-uniform conditions among the PV inputs.

Subsequently, switch interleaving was used to coordinate a system of parallel inverters. A closed-form expression for the ripple generated by a system of parallel converters was derived. The result was presented with a level of generality such that it could be applied to both dc-dc and inverter systems. Experimental results were used to validate the analytical results. Furthermore, a simple three-phase microinverter design for PV was proposed which utilized the benefits of interleaving.

Lastly, a method for coordinating a system of parallel inverters in a microgrid without communication was analyzed and developed. It was proposed that parallel inverters in a microgrid be controlled to act as nonlinear oscillators. The resulting microgrid is modular and does not require communication between inverters.
A theorem was developed which gives a synchronization condition for \( N \) nonlinear oscillators coupled through a symmetric LTI network. It was shown that the synchronization condition is independent of \( N \) and the load parameters. In addition, a practical method for hardware implementation was given along with a set of design guidelines. Simulation and experimental results were used to substantiate the analytical framework and illustrate the merit of the proposed application.

7.1 Future Work

Several areas within this work can be improved or extended with further investigation. For instance, virtual oscillator control has only been analyzed and demonstrated for islanded microgrids. Further effort is needed to extend this inverter control technique towards grid-connected applications. Within this context, there exists a body of literature within the systems biology community which examines the behavior of oscillators connected to a stiff voltage source. It is likely that insights in driven oscillator systems could be used to extend the proposed control to grid-connected systems. If this succeeds, a “complete” microgrid control method would be attained which allows the system to work in both grid-connected and islanded modes.

In the chapters focused on switch interleaving, it was assumed that the carrier waveforms were appropriately phase shifted to begin with or that a centralized controller was used. However, in a distributed implementation, it would be necessary to have a communication link(s) or an alternative control technique which yields interleaved carrier waveforms. An interesting approach would be to apply theory of coupled oscillator systems in the development of an automated self-interleaving method. For instance, each parallel inverter could use information attained from its terminal measurements to adjust its carrier phase shift. In such a system, the distortion measured at the output would serve as the coupling mechanism between the PWM carrier generators. Such an approach would eliminate the need for a communication network and would be novel within the power electronics area.

Alternatively, a more conventional communication system could be used to manage carrier interleaving for both the series and parallel inverter systems. Instead of designing a dedicated system which maintains proper interleaving, it may be possible to use an existing communication network in an inverter installation. Given that
microinverters on the market today typically include a communication system for monitoring and diagnostics, this method is especially attractive.

With regard to the multilevel inverter system, a dedicated investigation into electromagnetic emissions is needed. In a typical PV installation, the frame of each module is connected to ground. Given that there is a parasitic capacitance between each PV cell and the grounded module frame, it is possible for current to be injected into the ground node during switching transients. This type of noise injection must be sufficiently reduced in any PV installation to ensure compliance with IEEE standards. This is of particular concern in a non-isolated multilevel system because each group of PV cells will be subjected to rapid changes in voltage with respect to ground. To overcome this potential challenge, the extent of noise injection will need to be characterized and noise mitigation techniques may need to be used. A similar investigation will also be needed to assess electromagnetic radiation at higher frequency ranges.
Appendix A

DERIVATION, PROOF, AND PROTOTYPES

A.1 Derivation of Results in Section 4.3

In this section, a closed-form expression is given for the superposition of \( N \) interleaved triangular waveforms. The result can be used to apply ripple cancellation in systems of interleaved and parallel-connected power converters.

Triangular Waveform with Zero Phase-Shift

We will begin by analyzing the triangular waveform in Fig. 2.1 which is described by the function \( f_{\text{tri}}(t - \phi, d, T) \), where \( \phi \) is the phase-shift and \( T \) is the period. The symmetry of the waveform will be quantified using \( d \).

The Fourier series of a generic time-domain waveform can be represented in several forms. Most commonly, the Fourier series of a function, \( f(t) \), with period \( T \) is represented as

\[
f(t) = a_0 + \sum_{n=1}^{\infty} \left[ a_n \cos \left( \frac{2\pi}{T} t \right) + b_n \sin \left( \frac{2\pi}{T} t \right) \right]
\]  

(A.1)

where \( a_0 \) is the average value of \( f(t) \) over one period. Furthermore, the \( a_n \) and \( b_n \) coefficients can be expressed as

\[
a_n = \frac{2}{T} \int_{-T/2}^{+T/2} f(t) \cos \left( \frac{2\pi}{T} t \right) \, dt
\]  

(A.2)

\[
b_n = \frac{2}{T} \int_{-T/2}^{+T/2} f(t) \sin \left( \frac{2\pi}{T} t \right) \, dt.
\]  

(A.3)

For a triangular waveform with zero phase shift, \( a_n = 0 \) \( \forall n \) because \( f_{\text{tri}}(t, d, T) \) is
an odd function with a zero average value. The series reduces to

\[ f_{\text{tri}}(t, d, T) = \sum_{n=1}^{\infty} b_n \sin \left( \frac{2\pi}{T} t \right). \quad (A.4) \]

\( f_{\text{tri}}(t, d, T) \) can be represented as a piecewise function over the time interval \( t \in [0, T] \).

\[ f_{\text{tri}}(t, d, T) = \begin{cases} 
\frac{2}{T} t & \text{for } 0 \leq t \leq \frac{dT}{2} \\
1 - \frac{2}{(1-d)T} \left( t - \frac{dT}{2} \right) & \text{for } \frac{dT}{2} \leq t \leq T \left( 1 - \frac{d}{2} \right) \\
\frac{2}{T} (t - T) & \text{for } T \left( 1 - \frac{d}{2} \right) \leq t \leq T 
\end{cases} \quad (A.5) \]

Using (A.5) in (A.3), the \( b_n \) coefficients in (A.4) can be expressed as

\[ b_n = \frac{2}{T} \int_0^{\frac{dT}{2}} \sin \left( \frac{2\pi}{T} t \right) dt + \frac{2}{T} \int_{\frac{dT}{2}}^{T \left( 1 - \frac{d}{2} \right)} \left( 1 - \frac{2}{(1-d)T} \left( t - \frac{dT}{2} \right) \right) \sin \left( \frac{2\pi}{T} t \right) dt \]

\[ = \frac{4}{T} \left[ \int_{-\frac{dT}{2}}^{\frac{dT}{2}} \frac{d}{dT} t \sin \left( \frac{2\pi}{T} t \right) dt + \int_{\frac{dT}{2}}^{T \left( 1 - \frac{d}{2} \right)} \frac{d}{dT} \left( 1 - \frac{2}{(1-d)T} \left( t - \frac{dT}{2} \right) \right) \sin \left( \frac{2\pi}{T} t \right) dt \right]. \quad (A.6) \]

Evaluating and simplifying yields

\[ b_n = \frac{-2 (-1)^n}{n^2 \pi^2 d (1 - d)} \sin (n\pi d). \quad (A.7) \]

Substituting (A.7) into (A.4), the Fourier series of \( f_{\text{tri}}(t, d, T) \) can be expressed as

\[ f_{\text{tri}}(t, d, T) = \sum_{n=1}^{\infty} \frac{-2 (-1)^n \sin (n\pi d)}{n^2 \pi^2 d (1 - d)} \sin \left( \frac{2\pi}{T} t \right). \quad (A.8) \]

Next, the Fourier series of a triangular waveform with a non-zero phase-shift is formulated.

Triangular Waveform with Non-Zero Phase Shift

If (A.1) is used to analyze \( f_{\text{tri}}(t - \phi, d, T) \), it will be necessary to recalculate the \( a_n \) and \( b_n \) coefficients as \( \phi \) is varied. For the case where an arbitrary phase-shift is introduced, it was found that the following form of the Fourier series was most convenient:

\[ f(t) = c_0 + \sum_{n=1}^{\infty} c_n \sin \left( \frac{2\pi}{T} t - \theta_n \right). \quad (A.9) \]
In (A.9), \( c_n = \sqrt{a_n^2 + b_n^2} \) for \( n > 0 \) and \( c_0 \) is the average value of \( f(t) \) over one cycle. Since the duty ratio and period of \( f_{\text{tri}} (t, d, T) \) and \( f_{\text{tri}} (t, d, T) \) are identical, it is only necessary to consider a time-shift. The \( \theta_n \) terms in (A.9) account for the time shift by setting \( \theta_n = \frac{n2\pi\phi}{T} \). Because the average value of \( f_{\text{tri}} \) equals zero, \( c_0 = 0 \) and the series for \( f_{\text{tri}} (t - \phi, d, T) \) reduces to
\[
f_{\text{tri}} (t - \phi, d, T) = \sum_{n=1}^{\infty} c_n \sin \left( n \frac{2\pi}{T} (t - \phi) \right).
\] (A.10)

Recalling that \( a_n = 0 \) for \( f_{\text{tri}} (t, d, T) \), it can be concluded that \( c_n = b_n \) so that
\[
f_{\text{tri}} (t - \phi, d, T) = \sum_{n=1}^{\infty} \frac{-2 (-1)^n \sin (n\pi d)}{n^2\pi^2 (1 - d) \sin \left( n \frac{2\pi}{T} (t - \phi) \right)} \sin \left( n \frac{2\pi}{T} (t - \phi) \right). \] (A.11)

From here forward, a triangular function with symmetry \( d \), phase-shift \( \phi \), and period \( T \) will be represented with (A.11). Furthermore \( c_n \) will be defined as
\[
c_n := \frac{-2 (-1)^n \sin (n\pi d)}{n^2\pi^2 (1 - d) \sin (n\pi d)} \sin (n\pi d). \] (A.12)

It should be noted that \( c_n = 0 \) when \( n \) is an integer multiple of \( \frac{1}{d} \).

Superposition of \( N \) Interleaved Triangular Waveforms

In a system with ideal interleaving, it will be assumed that each waveform has an identical symmetry parameter and period. The \( k^{\text{th}} \) waveform will be denoted as \( f_{\text{tri}} (kT/N, d, T) \). As indicated in (A.13) below, it will be assumed that the superposition of \( N \) interleaved triangular waveforms can be expressed as the product of a \textit{net amplitude} and a \textit{net triangular component} which are denoted as \( A \) and \( f_{\text{tri}} (t - \phi', d', T') \), respectively.

\[
\sum_{k=1}^{N} f_{\text{tri}} (kT/N, d, T) = Af_{\text{tri}} (t - \phi', d', T'). \] (A.13)

In (A.13), \( \phi' \), \( d' \), and \( T' \) are the effective phase-shift, symmetry, and period of the net triangular component. The remainder of this section will be devoted to analyzing the harmonics of \( \sum_{k=1}^{N} f_{\text{tri}} (kT/N, d, T) \) and deriving closed-form expressions for \( A \) and \( f_{\text{tri}} (t - \phi', d', T') \).
Using (A.11) in (A.13), the superposition of $N$ interleaved waveforms can be expressed as

$$\sum_{k=1}^{N} f_{\text{tri}}(t - k \frac{T}{N}, d, T)$$

$$= \sum_{n=1}^{\infty} \frac{-2 (-1)^{n} \sin (n \pi d)}{n^2 \pi^2 d (1 - d)} \sin \left( n \frac{2\pi}{T} \left( t - \frac{T}{N} \right) \right)$$

$$+ \sum_{n=1}^{\infty} \frac{-2 (-1)^{n} \sin (n \pi d)}{n^2 \pi^2 d (1 - d)} \sin \left( n \frac{2\pi}{T} \left( t - \frac{2T}{N} \right) \right)$$

$$\vdots$$

$$+ \sum_{n=1}^{\infty} \frac{-2 (-1)^{n} \sin (n \pi d)}{n^2 \pi^2 d (1 - d)} \sin \left( n \frac{2\pi}{T} \left( t - \frac{NT}{N} \right) \right)$$

(A.14)

Factoring out $c_n$ and collecting terms gives

$$\sum_{k=1}^{N} f_{\text{tri}}(t - k \frac{T}{N}, d, T) = \sum_{n=1}^{\infty} c_n \sum_{k=1}^{N} \sin \left( n \frac{2\pi}{T} \left( t - k \frac{T}{N} \right) \right)$$

(A.16)

It can be shown that

$$\sum_{k=1}^{N} \sin \left( n \frac{2\pi}{T} \left( t - k \frac{T}{N} \right) \right) = \begin{cases} N \sin \left( n \frac{2\pi t}{T} \right) & \text{for } n = N, 2N, 3N \ldots \\ 0 & \text{otherwise} \end{cases}$$

(A.17)

This follows from the fact that when $N$ sinusoids are uniformly phase-shifted across $2\pi$, they sum to zero. Harmonic analysis will be facilitated if (A.16) is rewritten as

$$\sum_{k=1}^{N} f_{\text{tri}}(t - k \frac{T}{N}, d, T) = \sum_{n=1}^{\infty} h_n \sin \left( n \frac{2\pi}{T} t \right)$$

(A.18)

where $h_n$ is amplitude of the $n^{th}$ harmonic of the net waveform. Using the property summarized in (A.17) and recalling that $c_n = 0$ when $n = \frac{1}{d}, \frac{2}{d}, \frac{3}{d}, \ldots$, the $n^{th}$ harmonic can be expressed as
Using (A.19) in (A.18), the net waveform can be expressed as a series. This result analytically confirms that all harmonics are canceled except those that are integer multiples of $N$ and not an integer multiple of $1/d$. Furthermore, if $Nd$ is an integer, all harmonics are canceled (i.e. $h_n = 0 \forall n$) and the net waveform is zero.

### A.1.1 Derivation of Net Amplitude $A$

Building on the results of the harmonic analysis, $A$ will now be derived. It is well known that the peak amplitude of a triangular waveform can be expressed as

$$A = \sqrt{3}A_{\text{rms}}, \quad (A.20)$$

where $A_{\text{rms}}$ is the root mean square (RMS) of the triangular waveform. The RMS value of any waveform can be expressed in terms of the harmonics:

$$A_{\text{rms}} = \sqrt{h_0^2 + \frac{3}{2} \sum_{n=1}^{\infty} h_n^2}. \quad (A.21)$$

Since the dc-component of the triangular waveform is zero, $h_0 = 0$ and (A.20) can be written as

$$A = \sqrt{\frac{3}{2} \sum_{n=1}^{\infty} h_n^2}. \quad (A.22)$$
Substituting (A.19) into (A.22) yields

\[
A = \sqrt{\frac{3}{2} \sum_{n=N,2N,3N...}^{\infty} \left( \frac{N^2 - 2(-1)^n \sin(n\pi d)}{n^2\pi^2d(1-d)} \right)^2} 
\]

\[
= \sqrt{\frac{3}{2} \cdot \frac{2N}{\pi^2d(1-d)}} \sum_{n=1}^{\infty} \frac{\sin^2(Nn\pi d)}{(Nn)^4} 
\]

\[
= \frac{\sqrt{6}}{N\pi^2d(1-d)} \sum_{n=1}^{\infty} \frac{1 - \cos(2Nn\pi d)}{n^4} 
\]

\[
= \frac{\sqrt{6}}{N\pi^2d(1-d)} \sum_{n=1}^{\infty} \frac{1}{2} \left( \frac{\pi \mod(2\pi Nd,2\pi)}{12} - \frac{\pi \mod(2\pi Nd,2\pi)}{12} + \frac{\pi \mod(2\pi Nd,2\pi)}{12} \right) . 
\]

(A.23)

where in the second and third lines we factor and multiply all constants, and in the last line the identity \( \sin^2(x) = \frac{1}{2} (1 - \cos(x)) \) was used.

It will be useful to employ the modulo operation, denoted as \( \mod(x,b) \), which gives the remainder after the number \( x \) is divided by \( b \). It follows that \( b \) acts as an upper limit such that the result of the modulo operation wraps to zero when \( x \) equals or exceeds any multiple of \( b \). In particular, \( \mod(x,2\pi) \) always yields a number between zero and \( 2\pi \). Using

\[
\sum_{n=1}^{\infty} \frac{\cos(nx)}{n^4} = \frac{\pi^4}{90} - \frac{x^2}{12}x^2 + \frac{x^3}{12}x^3 - \frac{1}{45}x^4 , \quad 0 \leq x \leq 2\pi , 
\]

(A.24)

and

\[
\sum_{n=1}^{\infty} \frac{1}{n^4} = \frac{\pi^4}{90} , 
\]

(A.25)

which were attained from [111], the summation in (A.23) can be rewritten as

\[
\sum_{n=1}^{\infty} \frac{1}{2} \frac{1 - \cos(2Nn\pi d)}{n^4} 
\]

\[
= \frac{1}{2} \left( \frac{\pi \mod(2\pi Nd,2\pi)}{12} - \frac{\pi \mod(2\pi Nd,2\pi)}{12} + \frac{\pi \mod(2\pi Nd,2\pi)}{12} \right) . 
\]

(A.26)

where in the second line, the modulo function was utilized to ensure that the in-
equality in (A.24) was upheld. It is straightforward to show
\[ \text{mod} \left( a, 2\pi \right) = 2\pi \text{mod} \left( \frac{a}{2\pi}, 1 \right) \]

\[ \implies \text{mod}^m \left( a, 2\pi \right) = (2\pi)^m \text{mod}^m \left( \frac{a}{2\pi}, 1 \right). \tag{A.27} \]

It then follows that
\[
\sum_{n=1}^{\infty} \frac{1}{n^4} \frac{1 - \cos (2Nn\pi d)}{n^4} = \frac{\pi^4}{12} \left( \frac{(2\pi)^2 \text{mod}^2 (Nd, 1)}{12} - \frac{\pi (2\pi)^3 \text{mod}^3 (Nd, 1)}{12} + \frac{(2\pi)^4 \text{mod}^4 (Nd, 1)}{48} \right)
\]

\[ = \frac{\pi^4}{6} \left( \text{mod}^2 (Nd, 1) - 2\text{mod}^3 (Nd, 1) + \text{mod}^4 (Nd, 1) \right) \]

\[ = \frac{\pi^4}{6} \text{mod}^2 (Nd, 1) \left( 1 - 2\text{mod} (Nd, 1) + \text{mod}^2 (Nd, 1) \right) \]

\[ = \frac{\pi^4}{6} \text{mod}^2 (Nd, 1) (1 - \text{mod} (Nd, 1))^2 \tag{A.28} \]

Substituting (A.28) into (A.23) gives the following result for \( A \):
\[
A = \sqrt{\frac{6}{N\pi^2 d(1-d)}} \sqrt{\frac{\pi^4}{6} \text{mod}^2 (Nd, 1) (1 - \text{mod} (Nd, 1))^2} 
\]

\[ = \frac{\text{mod} (Nd, 1) (1 - \text{mod} (Nd, 1))}{Nd (1-d)}. \tag{A.29} \]

Now that a closed-form expression for \( A \) is attained, the net triangular component will now be derived.

**Derivation of Net Triangular Component \( f_{\text{tri}} (t - \phi', d', T') \)**

Using (A.11), we can write the Fourier series of a net triangular waveform as
\[
f_{\text{tri}} (t - \phi', d', T') = \sum_{n=1}^{\infty} \frac{-2 (-1)^n \sin (n\pi d')}{n^2 \pi^2 d' (1 - d')} \sin \left( \frac{n \pi}{T'} (t - \phi') \right). \tag{A.30} \]
Rearranging (A.13), and solving for the net triangular component gives

\[ f_{\text{tri}}(t - \phi', d', T') = \frac{\sum_{k=1}^{N} f_{\text{tri}k}\left(t - k\frac{T}{N}, d, T\right)}{A}. \]  \hspace{1cm} (A.31)

In order to determine the precise values of \( \phi', d', \) and \( T' \), the right-hand side of (A.31) will be rewritten in the form shown in (A.30).

First, the series in the numerator of (A.31) will be rewritten. Substituting (A.19) into (A.18), \( \sum_{k=1}^{N} f_{\text{tri}k}\left(t - k\frac{T}{N}, d, T\right) \) becomes

\[ \sum_{k=1}^{N} f_{\text{tri}k}\left(t - k\frac{T}{N}, d, T\right) = \sum_{n=N, 2N, 3N...}^{\infty} Nc_n \sin\left(\frac{2\pi}{T}t\right) \]  \hspace{1cm} (A.32)

\[ = \sum_{n=N, 2N, 3N...}^{\infty} N\frac{-2 (-1)^n \sin(n\pi d)}{n^2\pi^2d(1 - d)} \sin\left(\frac{2\pi}{T}t\right) \]

\[ = \sum_{n=1}^{\infty} \frac{N}{n} \frac{-2 (-1)^n \sin(n\pi d)}{n^2\pi^2d(1 - d)} \sin\left(\frac{2\pi}{T}t\right) \]

\[ = \sum_{n=1}^{\infty} \frac{1}{N} \frac{-2 (-1)^n \sin(n\pi d)}{n^2\pi^2d(1 - d)} \sin\left(\frac{2\pi}{T}t\right) \]  \hspace{1cm} (A.33)

Dividing this result by \( A \) gives

\[ \frac{\sum_{k=1}^{N} f_{\text{tri}k}\left(t - k\frac{T}{N}, d, T\right)}{A} = \frac{Nd (1 - d)}{\text{mod} (Nd, 1) (1 - \text{mod} (Nd, 1))} \sum_{n=1}^{\infty} \frac{-2 (-1)^n \sin(n\pi d)}{n^2\pi^2d(1 - d)} \sin\left(\frac{2\pi}{T}t\right) \]

\[ = \sum_{n=1}^{\infty} \frac{-2 (-1)^n \sin(n\pi d)}{n^2\pi^2 \text{mod} (Nd, 1) (1 - \text{mod} (Nd, 1))} \sin\left(\frac{2\pi}{T}t\right). \]  \hspace{1cm} (A.34)

Now, the \( \sin(n\pi d) \) factor in the numerator will be rewritten to obtain the desired form in (A.30). Since the \( \sin \) function is periodic over \( 2\pi \), this implies

\[ \sin(n\pi d) = \sin(\text{mod} (Nn\pi d, 2\pi)) = \sin(n\pi \text{mod} (Nd, 2)) = \eta^n \sin(n\pi \text{mod} (Nd, 1)), \]  \hspace{1cm} (A.35)
where
\[
\eta = \begin{cases} 
+1 & \text{for } \text{mod } (Nd, 2) \leq 1 \\
-1 & \text{for } \text{mod } (Nd, 2) > 1 \end{cases} . \tag{A.36}
\]

Inserting (A.35) into (A.34) yields
\[
\sum_{k=1}^{N} f_{\text{tri}} (t - k \frac{T}{N}, d, T) = \sum_{n=1}^{\infty} -2 (-1)^n \sin (n \pi \text{mod } (Nd, 1)) \eta^n \sin \left( Nn \frac{2\pi}{T} t \right) . \tag{A.37}
\]

Noting that \(\eta^n\) equals \(\pm 1\) and that \(\sin (x - n\pi) = (-1)^n \sin (x)\), it is evident that \(\eta^n \sin (x)\) can be expressed alternatively as
\[
\eta^n \sin (x) = \sin \left( x - n \left( \frac{1 - \eta}{2} \right) \pi \right) , \tag{A.38}
\]

where
\[
\frac{1 - \eta}{2} = \begin{cases} 
0 & \text{for } \text{mod } (Nd, 2) \leq 1 \\
1 & \text{for } \text{mod } (Nd, 2) > 1 \end{cases} . \tag{A.39}
\]

Applying this property to (A.37):
\[
\sum_{k=1}^{N} f_{\text{tri}} (t - k \frac{T}{N}, d, T) = \sum_{n=1}^{\infty} -2 (-1)^n \sin (n \pi \text{mod } (Nd, 1)) \left( \frac{1 - \eta}{2} \right) \frac{2\pi}{T} \left( t - n \left( \frac{1 - \eta}{2} \right) \pi \right)
\]
\[
= \sum_{n=1}^{\infty} -2 (-1)^n \sin (n \pi \text{mod } (Nd, 1)) \sin \left( Nn \frac{2\pi}{T} t - n \left( \frac{1 - \eta}{2} \right) \pi \right)
\]
\[
= \sum_{n=1}^{\infty} -2 (-1)^n \sin (n \pi \text{mod } (Nd, 1)) \sin \left( Nn \frac{2\pi}{T} \left( t - \left( \frac{1 - \eta}{2} \right) \frac{T}{2N} \right) \right)
\]
\[
= \sum_{n=1}^{\infty} -2 (-1)^n \sin (n \pi \text{mod } (Nd, 1)) \sin \left( n \frac{2\pi}{T/N} \left( t - q_\phi \frac{T}{2N} \right) \right)
\]
\[
= f_{\text{tri}} \left( t - q_\phi \frac{T}{2N}, \text{mod } (Nd, 1), \frac{T}{N} \right) \tag{A.40}
\]

where
\[
q_\phi = \left( \frac{1 - \eta}{2} \right) = \begin{cases} 
0 & \text{for } \text{mod } (Nd, 2) \leq 1 \\
1 & \text{for } \text{mod } (Nd, 2) > 1 \end{cases} . \tag{A.41}
\]

Comparing (A.30), (A.31), and (A.40), it can be concluded that the desired form
was attained and that

\[ f_{\text{tri}} \left( t - \phi', d', T' \right) = f_{\text{tri}} \left( t - q_\phi \frac{T}{2N} \mod (Nd, 1), \frac{T}{N} \right). \]  \hspace{1cm} (A.42)

Therefore, the effective phase-shift, duty ratio, and period of the net triangular waveform are:

\[
\begin{aligned}
\phi' &= q_\phi \frac{T}{2N} \\
d' &= \mod (Nd, 1) \\
T' &= \frac{T}{N}
\end{aligned}
\]  \hspace{1cm} (A.43)

This confirms the well-known observation that the frequency of the net waveform is equal to \( N \) times the frequency of the constituent interleaved waveforms.
A.2 Proof for Corollary 1

Consider the block-diagram of the differential system in Fig. 5.4. Denote the differential $L_2$ gain of the linear fractional transformation by $\tilde{\gamma}(\mathcal{F}(Z_{osc}(s), \kappa Y(s)))$ so that

$$\|\tilde{v}\|_{L_2} \leq \tilde{\gamma}(\mathcal{F}(Z_{osc}(s), \kappa Y(s))) \|\tilde{i}_{src}\|_{L_2} + \eta, \quad (A.44)$$

for some non-negative $\eta$. Applying the result (5.21) in Lemma 1 gives

$$\|\tilde{i}_{src}\|_{L_2} \leq \sigma \|\tilde{v}\|_{L_2}. \quad (A.45)$$

Combining (A.44) and (A.45), leads to

$$\|\tilde{v}\|_{L_2} \leq \tilde{\gamma}(\mathcal{F}(Z_{osc}(s), \kappa Y(s))) \sigma \|\tilde{v}\|_{L_2} + \eta. \quad (A.46)$$

Let us assume that

$$\tilde{\gamma}(\mathcal{F}(Z_{osc}(s), \kappa Y(s))) \cdot \sigma < 1. \quad (A.47)$$

Isolating $\|\tilde{v}\|_{L_2}$,

$$\|\tilde{v}\|_{L_2} \leq \frac{\eta}{1 - \tilde{\gamma}(\mathcal{F}(Z_{osc}(s), \kappa Y(s))) \sigma}, \quad (A.48)$$

which implies that $\tilde{v} \in L_2$. It follows from Barbalat’s lemma [103-105, 107] that

$$\lim_{t \to \infty} \tilde{v}(t) = 0 \implies \lim_{t \to \infty} v_j(t) - v_k(t) = 0 \forall j, k = 1, \ldots, N. \quad (A.49)$$

That is, if the system of oscillators satisfies the condition in (A.47), we can guarantee global asymptotic synchronization.

We will now derive the result in (5.29) by showing the differential $L_2$ gain of $\mathcal{F}(Z_{osc}(s), \kappa Y(s))$ is equal to $\|\mathcal{F}(\zeta(s), \kappa \beta(s) \lambda_2)\|_{\infty}$. From the definition of the linear fractional transformation in (5.14), and the general form of the admittance
matrix in (5.10), note that

\[
\mathcal{F}(Z_{\text{osc}}(s), \kappa Y(s)) = (I_N + \kappa Z_{\text{osc}}(s)Y(s))^{-1} Z_{\text{osc}}(s)
\]

\[
= (I_N + \kappa Z_{\text{osc}}(s)(\alpha(s)I_N + \beta(s)\Gamma))^{-1} Z_{\text{osc}}(s)
\]

\[
= ((1 + \kappa \alpha(s)z_{\text{osc}}(s))I_N + \kappa z_{\text{osc}}(s)\beta(s)\Gamma)^{-1} Z_{\text{osc}}(s)
\]

\[
= \left( I_N + \frac{z_{\text{osc}}(s)}{1 + \kappa \alpha(s)z_{\text{osc}}(s)}\kappa\beta(s)\Gamma \right)^{-1} \frac{z_{\text{osc}}(s)I_N}{1 + \kappa \alpha(s)z_{\text{osc}}(s)}
\]

\[
= \mathcal{F}(\zeta(s)I_N, \kappa\beta(s)\Gamma).
\] (A.50)

Because \( \mathcal{F}(\zeta(s)I_N, \kappa\beta(s)\Gamma) \) is a linear system, it follows that

\[
\tilde{\gamma}(\mathcal{F}(Z_{\text{osc}}(s), \kappa Y(s))) = \| \mathcal{F}(\zeta(s)I_N, \kappa\beta(s)\Gamma) \|_{\infty}.
\]

Now, by definition of the \( \mathcal{H} \)-infinity norm, it follows that

\[
\| \mathcal{F}(\zeta(s)I_N, \kappa\beta(s)\Gamma) \|_{\infty} = \sup_{\omega \in \mathbb{R}} \left\| \tilde{i}_{\text{src}}(\omega) \right\|_{2}.
\]

where we have diagonalized \( \Gamma = Q\Lambda Q^T \) in the second line above. We two key observations will be made to simplify (A.51):

i) The first column of \( Q \) is given by

\[
q_1 = \frac{1}{\sqrt{N}} \mathbf{1}.
\]

Furthermore, \( \mathbf{1}^T \Pi = \mathbf{1}^T (I_N - \frac{1}{N} \mathbf{1}\mathbf{1}^T) = \mathbf{1}^T - \frac{1}{N} (\mathbf{1}^T \mathbf{1}) \mathbf{1}^T = \mathbf{0}^T \). Therefore, the vector \( Q^T \tilde{i}_{\text{src}}(s) = Q^T \Pi \tilde{i}_{\text{src}}(s) \) is given by

\[
Q^T \tilde{i}_{\text{src}}(s) = Q^T \Pi \tilde{i}_{\text{src}}(s) = [0, D(s)]^T,
\] (A.52)

where \( D(s) \in \mathbb{C}^{N-1 \times 1} \) is comprised of the non-zero elements of \( Q^T \Pi \tilde{i}_{\text{src}}(s) \).

ii) Denote the diagonal matrix with diagonal entries comprised of the non-zero eigenvalues of \( \Gamma \) by \( \Lambda_{N-1} \), i.e., \( \Lambda_{N-1} = \text{diag}\{\lambda_2, \ldots, \lambda_N\} \in \mathbb{R}^{N-1 \times N-1} \).

Using the two observations highlighted above, (A.51) can now be simplified as
\[ \| F(\zeta(s)I_N, \kappa\beta(s)\Gamma)\|_{\infty} \]
\[ = \sup_{\omega \in \mathbb{R}} \left\| \left( I_{N-1} + \zeta(j\omega)\kappa\beta(j\omega)\Lambda_{N-1} \right)^{-1} \zeta(j\omega)D(j\omega) \right\|_2 \]
\[ = \sup_{j=2, \ldots, N} \left( \sup_{\omega \in \mathbb{R}} \left( \frac{D^*(j\omega)\left(1 + \zeta(j\omega)\kappa\beta(j\omega)\lambda_j \right)^{-2} \zeta^2(j\omega)D(j\omega)}{D^*(j\omega)D(j\omega)} \right)^{\frac{1}{2}} \right) \]
\[ = \sup_{j=2, \ldots, N} \left( \sup_{\omega \in \mathbb{R}} \left( 1 + \zeta(j\omega)\kappa\beta(j\omega)\lambda_j \right)^{-1} \zeta(j\omega) \right) \]
\[ = \sup_{j=2, \ldots, N} \| F(\zeta(s), \kappa\beta(s)\lambda_j)\|_{\infty} = \| F(\zeta(s), \kappa\beta(s)\lambda_2)\|_{\infty}, \quad (A.53) \]

where the last equality follows from the fact that \( \| F(\zeta(s), \kappa\beta(s)\lambda)\|_{\infty} \) is a decreasing function of \( \lambda \) \([104]\). From (A.47) and (A.53), it is apparent that (5.29) is a sufficient condition for global asymptotic synchronization.
A.3 Hardware Prototypes

A.3.1 Sub-inverter for Multilevel Inverter System

Figure A.1: Sub-inverter schematic. Top-view of board layout.
Figure A.2: Sub-inverter schematic. Power-stage and gate-drivers.
Figure A.4: Sub-inverter schematic. Protection and user-disable logic.
Figure A.5: Sub-inverter schematic. Sensing circuitry.
A.3.2 Three-Phase Inverter

Figure A.6: Three-phase inverter schematic. Top-view of board layout.
Figure A.3: Sub-inverter schematic. Sensing and auxiliary power supplies.
Figure A.7: Three-phase inverter schematic. Phase b power stage.
Figure A.8: Three-phase inverter schematic. Sensing and auxiliary power supplies.
Figure A.9: Three-phase inverter schematic. Protection and user disable logic.
Figure A.10: Three-phase inverter schematic. Dc-link and input sensing.
Figure A.11: Three-phase inverter schematic. Phase b power stage.
Figure A.12: Three-phase inverter schematic. Phase c power stage.
REFERENCES


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