PLANAR GAAS NANOWIRE ARRAYS FOR NANOELECTRONICS:
CONTROLLED GROWTH, DOPING, CHARACTERIZATION, AND DEVICES

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ABSTRACT

The Vapor-Liquid-Solid (VLS) mechanism is a bottom-up approach to produce one-dimensional semiconductor structures, or nanowires. VLS nanowires are formed via a chemical or physical deposition process, where a metallic nanoparticle (seed) facilitates the growth. Nanowire growth diameter is strongly correlated to seed size, therefore top-down patterning can control site location and diameter of nanowire growth. Nanowires are sought after for their potential use as a manageable way produce small dimensioned semiconductor features without the need of expensive lithographic techniques.

VLS nanowires commonly grow out-of-plane with respect to their growth substrate, resulting in difficulty with integrating VLS nanowires into existing device processing which is intended for planar geometries. Nanowires are typically removed from the substrate, which requires painstaking and uneconomical methods to pattern and align the nanowires. Planar nanowires are a potential solution to this issue; they grow in-plane on the substrate surface, epitaxially attached along its entire axis. Planar nanowires, as is, can be integrated into any preexisting planar semiconductor process, combining the advantages of nanowires with increased manufacturability.

In this dissertation, planar GaAs nanowires are grown using metal organic chemical vapor deposition (MOCVD) with Au nanoparticles as the liquid metal seed. Growth occurs across multiple substrates to elucidate the mechanism behind planar nanowire growth direction. Knowledge gained by observing planar nanowire growth is used to precisely control nanowire growth direction. Subsequently the doping of planar nanowires is explored and unique phenomena related to the p-type doping of planar nanowires are investigated and discussed.

The advantages of using planar nanowires are demonstrated through the controlled growth and doping of planar nanowires, and ultimately fabrication of electronic devices using
conventional planar process techniques without the need for vertical nanowire processes or nanowire transferring. Devices are characterized and results are presented with discussion. The next steps for the future of planar nanowires are presented with initial results highlighting future applications and issues that must be solved.

Chapter 1 is an introduction to the history of Vapor-Liquid-Solid nanowires, and as well as a brief overview of the accomplishments of the field and highlighting unsolved issues.

Chapter 2 introduces the planar nanowire and discusses the motivation behind researching planar nanowires as a potential solution to the fundamental problems with vertical VLS nanowires.

Chapter 3 gives a short background into VLS nanowire growth and properties, introduction to MOCVD growth and reactor design, and material properties of GaAs, the semiconductor material of interest in this dissertation.

Chapter 4 presents the experimental details of planar GaAs nanowire growth on various substrates and the concept of projection theory to determined planar nanowire growth direction, as well as intrinsic growth phenomena.

Chapter 5 delves into the doping of planar nanowires, both n-type and p-type. The morphological changes and perturbations to planar nanowire that are caused by p-type dopants are discussed.

Chapter 6 demonstrates electrical devices such as MESFETS, inverting amplifiers and p-n diodes fabricated using planar GaAs nanowires as the active structure. Devices performance and metrics are discussed in this chapter.

Chapter 7 outlines several future directions for planar nanowires and presents initial results in a variety of areas such as potential devices, modeling opportunities and fundamental issues that need to be solved.
To my mother, father, and sister
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# TABLE OF CONTENTS

## CHAPTER 1 - INTRODUCTION ................................................................. 1

## CHAPTER 2 - MOTIVATION ...................................................................... 3
  2.1 Planar Nanowire Integration with Planar Processing .................................. 3
  2.2 Investigation of Novel Nanowire Growth Method ......................................... 4
  2.3 Planar Nanowire Growth Quality ............................................................... 4
  2.4 Figures ...................................................................................................... 7

## CHAPTER 3 - BACKGROUND INFORMATION ..................................... 10
  3.1 VLS Nanowires ...................................................................................... 10
  3.2 MOCVD Growth .................................................................................... 11
  3.3 Properties of GaAs ................................................................................ 12
  3.4 Figures .................................................................................................... 13

## CHAPTER 4 - GROWTH OF PLANAR GaAs NANOWIRES' ................ 16
  4.1 Experimental Details of Planar GaAs Nanowires ...................................... 16
  4.2 Planar Nanowire Growth Rate Model .................................................... 17
  4.3 GaAs (100) Growth .............................................................................. 20
  4.4 GaAs (110) Growth .............................................................................. 20
  4.5 Projection Theory .................................................................................. 22
  4.6 GaAs Off-Cut Growth ............................................................................ 23
  4.7 Patterning of Planar GaAs (110) Nanowires .......................................... 25
  4.8 Interaction between Planar Nanowire and Obstacles .............................. 27
  4.9 Figures and Tables ............................................................................... 29

## CHAPTER 5 - DOPING OF PLANAR NANOWIRES ........................... 44
  5.1 N-Type Doping of Planar GaAs Nanowires ........................................... 44
  5.2 P-Type Doping of Planar GaAs Nanowires ........................................... 45
  5.3 Figures ................................................................................................... 54

## CHAPTER 6 - GaAs PLANAR NANOWIRE BASED ELECTRONIC DEVICES' ... 69
  6.1 GaAs Planar Nanowire MESFETs ....................................................... 69
  6.2 Planar Multi-Nanowire Array Devices .................................................. 73
  6.3 Planar Nanowire p-n Junction ............................................................... 74
  6.4 Figures ................................................................................................... 78

## CHAPTER 7 - FUTURE DIRECTIONS FOR PLANAR NANOWIRES .... 93
  7.1 Annealing Intolerability ........................................................................ 93
  7.2 Interaction between Planar Nanowires and Thin Films .......................... 94
  7.3 Lateral Heterojunctions, Hetero Epitaxy and New Material Systems .... 96
  7.4 Planar Nanowire Modeling .................................................................. 97
  7.5 Multi-Junction Light Scatterer ............................................................... 98
  7.6 Figures .................................................................................................. 100

## CHAPTER 8 - SUMMARY ................................................................. 111

## REFERENCES ......................................................................................... 113
CHAPTER 1 - INTRODUCTION

It began in 1959 when Feynman gave his famous lecture, “There’s Plenty of Room at the Bottom”[1], encouraging scientists to explore nanotechnology for new discoveries. The synthesis of nanotechnology building blocks, such as dots, tubes, wires, membranes have been envisioned as a potential solution to many classic problems and scaling issues for future devices. A few years later, in 1964 Ellis and Wagner introduced the Vapor-Liquid-Solid mechanism to grow “silicon nanowiskers,” one-dimensional structures using small metallic nanoparticles to facilitate crystal growth without the use of lithography. Since then the field of nanowires has exploded, with the number of nanowire based publications increasing monotonically since 1990. Alternatively to the VLS mechanism, nanowires have been created by laser ablation [2], dry etching [3], SAE [4], liquid solution [5] and other techniques, however, the VLS process is arguably the most prominent method to create semiconductor nanowires. VLS nanowires have been demonstrated in almost every semiconductor material system [6-10] and been functionally utilized in a wide range of optical, mechanical and electrical devices: transistors [11], lasers [12], LEDs [13], solar cells [14], gas detectors [15], bio-sensors [16], electromechanical resonators [17] and so on. Throughout the last decade, much progress has been made with understanding and controlling the VLS growth mechanism. Researchers have been able to reduce crystal plane defects [18], model thermodynamic and kinetic processes [19, 20], map out parameter spaces for material systems [21], and create defect free heterostructures between many different material systems [22-24]. Many theoretical phenomena have been demonstrated in nanowires such as ballistic transport [25], twinning superlattices[26] and wurtzite formation in zinc-blende stable crystals [27]. Ultimately, nanowires have potential to be incorporated into commercial and industrial products, already with some success with the Si nanowire anode for lithium ion batteries [28]. However, there
are issues that need to be improved such as high yield growth and assembly [29], doping control [30] and metallic seed migration [31]. Nevertheless, semiconductor nanowires are still an attractive platform, progressing with momentum and with still room to grow.
CHAPTER 2 - MOTIVATION

2.1 Planar Nanowire Integration with Planar Processing

Semiconductor nanowires grown by the VLS typically exhibit a set of characteristic features when grown under standard growth conditions. VLS nanowires display one-dimensional crystal growth with well-defined crystal facets, and grow along low energy crystal directions, which tends to be the \(<111>\) crystal direction (\(<111>B\) for III-V materials). While the crystal orientation of the substrate determines the relative position of the nanowire to the surface, the majority of these potential growth directions are non-planar, i.e. growing away from the substrate at a specific angles [32]. The non-planarity of nanowires results in their difficulty to be integrated into the well-refined and robust planar CMOS processing techniques that are used to fabricate almost all electrical and optical devices. The two most popular solutions to this problem are to develop a geometry specific vertical process(es) [33] (Figure 2.1) or forcibly remove nanowires from their host substrate and place them horizontally on a chosen substrate (Figure 2.2). The first method results in an increased expense of fabrication from new tool and process development. Contact placement and thin film deposition are not trivial for vertical NANOWIREs because of shadowing. For vertically stacked contacts a filling matrix is necessary; usually consisting of a polymer or spin-on-glass (SoG) [34] to provide a planar surface for the contact to reside on. There are further issues of integrating back-end processes such as creating interconnects for vertical structures. The second method requires the nanowires to be placed onto a host substrate and aligned for both their absolute position and orientation. Many processes have been developed [35-37] to combat this issue but they are expensive, cumbersome or ineffectual.
2.2 Investigation of Novel Nanowire Growth Method

The VLS mechanism is a complex growth phenomenon mediated by a liquid metal seed and vapor phase precursors. Even though the VLS growth mode was discovered in the 1960s, progress is continuously being made to understand, model and control VLS growth. Extensive work has been done to map out potential growth parameters and their effect on nanowire growth for a wide variety of material systems [38-40]. While planar nanowire growth itself is a modification of VLS growth, it opens up brand-new opportunities to study and explore the effects of growth parameters combined with the unique planar nanowire geometry. Fundamentally, vertical nanowires growth in a different kinetic growth regime than planar nanowires which can have noticeable effect on nanowire growth rate, dopant incorporation, tapering, etc. Finally, the intimate proximity of the metallic seed particle with the surface of the GaAs substrate, along its entire length, allows surface properties of the substrate to have a strong influence on the nanowires growth. The differences between vertical and planar nanowire growth allow us to gain further insight about VLS growth in general, as well as specific knowledge about aspects of planar nanowire growth.

2.3 Planar Nanowire Growth Quality

While VLS nanowires tend to have good morphology and crystallinity they are often plagued by random planar defects such as twin plane and stacking faults. VLS nanowires usually come in one of two crystal structures, wurtzite (WZ) (more common structure) or zinc-blende (ZB). WZ nanowires follow an ABAB repeating crystal stacking structure with ZB having an ABCABC stacking structure along the <111> crystal direction. A stacking fault is when a forming crystal layer is out of sequence, i.e. ABBA and a twin plane is when a repeating crystal structure reverses its stacking sequence around a specific crystal plane, i.e. ABCBA. Non-ordered stacking faults and twin planes have been shown to cause electrical transport degradation and unwanted optical transitions in affected materials.
Another feature of vertical nanowires is a narrowing of their diameter as a function of nanowire length, also known as tapering [41]. Tapering is a result of precursor’s diffusion during the nanowire growth process. Precursors that impinge directly onto the nanoparticle and diffuse along the surface of the substrate/nanowire to the growth front contribute to nanowire growth. As the nanowire length increases, it becomes increasingly more difficult for precursors to diffuse to the growth front, relying solely on direct impingement and the nanowire growth rate decreases rapidly. As the diffusing precursors cannot contribute to VLS growth, they deposit on the sidewalls of the nanowire resulting in a tapered geometry. The varying diameter along the length of the nanowire can have detrimental effects for device performance by unexpectedly altering the nanowires doping concentration, optical properties, quantum effects and electrical resistance. There has been a strong research effort to combat these problems and there has been some success in reducing defect formation in nanowires by controlling basic growth parameters [42-44] and other techniques, but it still tends to be an inherent problem for vertical nanowires.

Our research group reported on a repeatable and controllable technique to produce nanowires that grow along the surface of the growth substrate (Figure 2.3) [45]. Planar nanowires offer many benefits when compared to their vertical counterparts. Planar nanowires are epitaxially attached to their growth substrate along the length of their axis with well-defined crystal facets and full registry with the substrate, a trapezoidal cross section, with a height and width on the same order of magnitude as the nanoparticle catalyst chosen. Combining their epitaxial nature with the VLS growth process, they grow in well-defined crystal directions. Their low profile allows them to be fully compatible with any pre-existing planar process, potentially able to be inserted into any traditional process flow without any retooling. Additionally, their low profile allows for further non-VLS, vapor phase epitaxy (VPE) growth to occur at the surface. Planar nanowires also benefit from having naturally low defect planar defect densities.
Compared to vertical nanowires, they only come in the ZB crystal phase. ZB nanowires have much lower stacking fault densities than WZ nanowires. Random twin plane formation usually occurs within vertical ZB nanowires; however planar nanowires are nearly twin free [45]. Lastly, planar nanowires do not suffer from tapering when grown at reasonable lengths (several microns). Since the growth front occurs at the surface of the substrate, precursors that diffuse along the substrate always contribute to VLS growth, regardless of nanowire length, resulting in a fast but constant growth rate with low tapering. Combining these qualities, innately planar process friendly and exceptional material quality, together leave planar nanowires as an excellent candidate for nanowire based devices.
2.4 Figures

Figure 2.1 A potential fabrication scheme for a two terminal vertical nanowire device. A bottom contact is first deposited followed by a filling matrix material to provide a stable surface for the secondary, top contact.
Figure 2.2 A diagram depicting the growth, removal and transfer of vertical nanowires. (1) Vertical VLS nanowires are grown from Au nanoparticles. Post growth they are forcibly removed (2) from their original host substrate, usually by sonication in a solution or mechanical scraping. Finally, (3) nanowires are transferred via solution or dry printing to their destination substrate. Without intervention, nanowires are randomly arranged on the surface.
Planar <110> GaAs Nanowires

(100) GaAs
Semi-Insulating Substrate

Figure 2.3 Illustration of bi-directional planar nanowire growth on a GaAs (100) SI substrate.

Planar nanowires grow epitaxially attached to the surface along specific crystal directions with full registry to the substrate.
CHAPTER 3 - BACKGROUND INFORMATION

3.1 VLS Nanowires

The VLS growth mechanism is a technique used to fabricate one-dimensional, high aspect ratio semiconductor nanostructures [46]. The VLS process (as illustrated in Figure 3.1) starts with a metallic nanoparticle (typically Au) which is used as a seed to facilitate nanowire growth. For basic VLS growth, the seed is deposited on the surface of a semiconductor substrate and heated to a temperature beyond the eutectic point of the metal-semiconductor system to form a liquid binary-alloy. At this point, vapor phase precursor is introduced to the seed and the incorporation of material supersaturates the seed. Once the seed is supersaturated, semiconductor material crystallizes underneath the seed and forms solid material roughly the same diameter as the seed itself. As the process continues, the seed is propelled along the growth front of the nanowire, leaving behind a one-dimensional nanowire. The VLS growth process is considered a layer by layer process: each layer starts with a crystal nucleus forming along the edge of the nanowire at a triple phase boundary (Vapor, Liquid, and Solid) as shown in Figure 3.2. This nucleus propagates across the width of the nanowire, thus forming a new layer, repeating this process until nanowire growth is terminated. VLS growth offers unique growth advantages over standard thin film growth because of the seed facilitating growth.

Semiconductor junctions in VLS nanowires have been investigated and demonstrated in both their radial [47] and axial [48] varieties as shown in Figure 3.3. Radial junctions are usually achieved by growing a complete nanowire (core) under a VLS growth regime, then switching the growth conditions to favor thin film growth thus creating junctions radially from the core. The nanowire is then coated with heterogeneous (doping type or heterojunction) material along its entire axis (shell). Core-shell geometry is difficult to achieve in traditional thin film growth and highly improbable to create monolithically. It has benefits such as complete
interfacial passivation, increased strain accommodation, and reduced electrical transport length. Axial junctions occur when heterogeneous segments are created along the length of the nanowire. Ideally, axial junctions are controlled by the VLS process, incorporated through the metallic nanoparticle, and properly distributed spatially, although this is not trivial to achieve [49-51]. Immiscibility between the metallic seed and precursor can prevent VLS mediated incorporation into the nanowire. This leads to either precursors being incorporated through vapor-solid growth, VS, or not at all leading to a varied distribution radially [52] or axially [53] along the nanowire. Enhanced metallic seed affinity for precursors leads to non-constant incorporation rates and can create a gradual profile along the length of the nanowire. Additionally, the reservoir effect [51] can affect the abruptness of junctions between axially defined segments. As material is precipitated out of the metallic seed and incorporated into the nanowire, a fractionally alloy between the two exist within the seed. When precursors are switched in vapor phase, pre-existing material will precipitate out of the seed as new material is collected. As this process occurs, a graded junction is created with a length that is proportional to the metallic seed diameter. The reservoir effect can be reduced by precise control over the growth conditions to purge out existing material before the junction is created. Minimizing the reservoir effect is key to creating abrupt axial junctions.

3.2 MOCVD Growth

Metal organic chemical vapor deposition, or MOCVD, is a thin film growth technique which utilizes metalorganic gas phase precursors, and often combined with gas phase hydrides, which are mixed then flown into a reaction chamber then chemically react to form thin films on the surface of a substrate, usually epitaxially. MOCVD reactors are typically designed with separate lines for each precursor which are then flown into a mixing manifold before it enters the growth chamber. Metalorganics are usually in liquid form, and a bubbler is used with a high purity carrier gas, i.e. purified H₂ with a palladium cell, to flow through the liquid and the vapor
from the liquid is used as the gaseous source. The reactor is temperature controlled, typically in the range of 400-800 °C although some materials such as GaN require higher temperatures, usually by a remotely heated susceptor with IR or RF radiation (in a cold wall reactor setup). The susceptor resides in a heat resistant, non-reactive chamber usually made from quartz or stainless steel. Samples are placed on the susceptor with constant rotation to promote uniform deposition as the precursors flown over the samples pyrolyze and chemically react over the heated substrate. Unused precursor and byproducts are flown out the exhaust and treated before released into the atmosphere. When compared to other III-V growth methods, such as liquid phase epitaxy (LPE) and molecular beam epitaxy (MBE), MOCVD provides a good compromise between material quality, growth speed and parallel processing for production needs. The MOCVD reactors specifically used in this dissertation are the vertical flow Thomas Swan Atmospheric MOCVD reactor and the horizontal flow Aixtron 200/4 MOCVD reactor [54].

3.3 Properties of GaAs

GaAs is a compound semiconductor consisting of Ga (group III) and As (group V) atoms. GaAs typically forms in zincblende but can form wurtzite, especially in small diameter nanowires. GaAs has a direct band gap of approximately 1.42 eV in the Γ-valley, with bulk high electron mobility of 8500 cm²/V·s. GaAs has a spherical surface in k-space, indicating that carriers experience isotropic effective mass, unlike Si or Ge which has ellipsoidal surfaces in k space. GaAs forms non-stoichiometric oxides which are not of good quality or of much use in electronics. The lattice constant of GaAs is 5.65 Å with close proximity to AlAs in lattice spacing. The low lattice mismatch allows thick layers of AlₓGa₁₋ₓAs to be deposited on GaAs without forming misfit dislocations, combined with the capability to deposit thin layers of InₓGa₁₋ₓAs allows GaAs to form many useful heterostructures. The direct band gap and high
electron mobility of GaAs has lead it to being used in many electrical and optical devices such as HEMTs, diode (quantum well) lasers, solar cells, optical sensors, etc.

3.4 Figures

Figure 3.1 Illustration depicting VLS growth for a vertical nanowire on a (111) crystal substrate. Gas phase precursors enter the metallic seed and precipitate out, thus forming a nanowire.
Figure 3.2 Illustration depicting nucleation at the triple phase boundary (vapor, liquid, solid). Once the nucleus, or step, forms it then propagates across the liquid-solid interface forming a new layer of crystal.
Figure 3.3 Illustration depicting the difference between axial and radial (core-shell) heterostructures. The lettering A and B represent heterogeneous material through either majority carrier type (n or p) or elemental composition.
CHAPTER 4 – GROWTH OF PLANAR GaAs NANOWIRES†

4.1 Experimental Details of Planar GaAs Nanowires

Planar GaAs nanowires were grown on GaAs substrates using metalorganic chemical vapor epitaxy (MOCVD). The substrates chosen to study planar nanowire growth are on-axis (100), (110), and 10° off-cut (100) GaAs substrates. Preparation for nanowire growth begins by dispersing colloidal Au nanoparticles on the surface of the substrates. Au nanoparticles, with diameters ranging from 20 to 250 nm, are typically dispersed in an aqueous solution which is evaporated at 115 °C on a hotplate, leaving behind a random distribution of Au nanoparticles on the surface of the substrates. Arsine (AsH₃) was used as the group V precursor and trimethylgallium (TMGa) was used as the group III precursor. The reactor pressure during growth is near atmospheric, between 950-1013 mbar and is crucial to maintain planar yield [45]. Samples were heated to 625 °C under AsH₃ overpressure to desorb native oxides on the substrate surface and promote alloying between the Au nanoparticles and GaAs substrates. Samples are then cooled to temperatures ranging between 460-480 °C to begin nanowire growth and promote nanowire planarity. Typical AsH₃ and TMGa flows range from 2.23 x 10⁻⁴ to 8.93 x 10⁻³ and 1.99 x 10⁻⁵ to 1.17 x 10⁻⁴ mol/min, respectively, with V/III ratios ranging between 19-447. The growth rates of GaAs planar nanowires are directly proportional to the absolute molar flow of TMGa. After growth, samples were cooled under arsine overpressure. Visual inspection for planar nanowires after growth was performed with a Hitachi S-4800 field emission scanning electron microscope to examine the physical characteristics of nanowires for this chapter and subsequent chapters.

†Some of the content in this chapter was adapted from Dowdy, R. S., D. A. Walko, et al. (2013). "Relationship between planar GaAs nanowire growth direction and substrate orientation." Nanotechnology 24(3): 035304.
4.2 Planar Nanowire Growth Rate Model

The epitaxial nature of planar nanowires put them into a unique growth regime that is different from out-of-plane nanowires. Various mass transport models of vertical nanowires have been put forth and extensively covered, however they generally model the axial growth rate similarly [55-57]. Essentially, there are three contributions to the growth rate of vertical nanowires: (1) precursor diffusion along the substrate to the metallic nanoparticle, (2) impingement of precursor onto the sidewall of the nanowire then diffusion to the metallic nanoparticle and (3) finally direct impingement of precursor onto the nanoparticle. There are three regimes of vertical nanowire growth: (1) initially precursor adatoms on the surface are able to diffuse within a surface diffusion length, $\lambda_S$, to the metallic nanoparticle, (2) once the nanowire grows sufficient length, $L \leq \lambda_S$, the contribution of surface adatoms decreases; the diffusion of adatoms from the surface up the nanowire sidewall and precursors impinging on the sidewall then diffusing to the tip dominate the growth rate, and (3) finally, once the nanowire grows longer than adatom precursor diffusion length, $L > \lambda_S$, precursors impinging on the nanowire sidewall then subsequently diffusing to the seed and direct impingement of precursors onto the seed dictate the nanowire growth rate. This causes the nanowire to grow quickly, then the growth rate slows dramatically and finally become constant once the nanowire is sufficiently long.

In contrast, the metallic particles for planar nanowires growth are always within a diffusion length of adatoms on the surface. Figure 4.1 highlights the contributions to planar nanowire growth. Compared to vertical nanowire growth, adatom diffusion along the substrate and nanowire can essentially be lumped together as we assume the effect of the growing nanowire body on adatom concentration and diffusion length is negligible. Under this assumption we can derive an equation for the growth rate of planar nanowires that is a
modification of vertical nanowire transport theory under the unique boundary conditions of the planar nanowire. Starting with the diffusion equation for the surface adatom concentration, \( n \):

\[
\frac{dn}{dt} = D \nabla^2 n - \frac{n}{\tau} + J
\]  

(4.1)

where \( D \) is the diffusion coefficient of Ga adatoms on the surface, \( \nabla \) is the 2D Laplace operator, \( \tau \) is the average lifetime of a Ga adatom before adsorption/desorption and \( J \) is the direct flux from the vapor phase. Assuming rotational symmetry of Ga adatom concentration on the surface, we can convert the 2D Laplace operator from Cartesian to cylindrical coordinates. In addition, we can simplify the equation by introducing the diffusion length, \( \lambda \), where \( \lambda = \sqrt{D \tau} \). The steady-state equation, \( \frac{dn}{dt} = 0 \), can be written as follows:

\[
0 = \lambda^2 \left( \frac{1}{r} \frac{d}{dr} n(r) + \frac{d^2}{dr^2} n(r) \right) - n(r) + J \tau
\]  

(4.2)

the general solution to the differential equation 4.2 is the modified Bessel function of the first, \( I_n \) and the second, \( K_n \), kind:

\[
n(r) = c_1 I_0 \left( \frac{r}{\lambda} \right) + c_2 K_0 \left( \frac{r}{\lambda} \right) + J \tau
\]  

(4.3)

Equation 4.3 can be solved by using the following boundary conditions:

\[
n(R_{NP}) = 0
\]  

(4.4)

where \( R_{NP} \) is the radius of the Au nanoparticle. The adatom concentration is vanishing as it is assumed that all precursors that reach the seed will contribute to growth [58]. The second boundary condition is:

\[
\frac{d}{dr} n(r) \bigg|_{r=R_{cap}} = 0
\]  

(4.5)

where \( R_{cap} \) is the radius of the capture zone of adatoms of the Au nanoparticle. \( R_{cap} \) is essentially the radius of influence the seed has of depleting adatoms from the surface. \( R_{cap} \) is a valid boundary condition for a single nanowire or when nanowires are sufficiently spaced apart;
if other nanowires have overlapping capture zones, the boundary condition will not be equal to 0. Using the boundary conditions and solving for the coefficients $C_1$ and $C_2$, we find the Ga adatom concentration along the surface is equal to:

$$n(r) = \frac{f r_{1}(Q_{r_{1}}^{R_{NP}} - Q_{r_{0}}^{R_{NP}}) + K_{r_{1}}^{R_{NP}}(Q_{r_{0}}^{R_{NP}} - Q_{r_{0}}^{R_{NP}}))}{I_{1}(Q_{r_{1}}^{R_{NP}} - Q_{r_{0}}^{R_{NP}}) + K_{1}^{R_{NP}}(Q_{r_{0}}^{R_{NP}} - Q_{r_{0}}^{R_{NP}})}$$

(4.6)

plugging the surface adatom concentration into Ficks first law of diffusion, we derive a Ga adatom diffusion current, $j_{diff}$:

$$j_{diff} = -D 2 \pi R_{NP} \frac{d}{dr} n(r) |_{r=R_{NP}}$$

(4.7)

Finally, we can determine the impingement flux [59], $J_{imp}$ of Ga precursor from the vapor phase directly onto the Au nanoparticle:

$$J_{imp} = \frac{1}{\sqrt{2\pi mk_B T}} \left( P - P_{\infty} e^{\left(\frac{2\sigma_{lv}}{R_{NP} k_B T}\right)} \right)$$

(4.8)

where $P$ is the partial pressure of Ga in the vapour phase, $P_{\infty}$ is the Ga pressure within the Au droplet, $\sigma_{lv}$ is the surface energy density of the vapour-liquid interface, $\Omega_i$ is the volume per mole of Ga in the liquid phase, $m$ is the molar mass of the Ga atom, $k_B$ is the Boltzmann constant and $T$ is temperature. The left side of the equation corresponds to the adsorption rate into the Au and the right side accounts for the Gibbs-Thomson effect [57, 60], which accounts for the reduction of supersaturation of nanowire particles of decreasing size, which ultimately decreases the growth rate. The growth rate of planar GaAs nanowires can be written as:

$$\pi R_{NP}^2 J_{imp} + j_{diff} = \frac{\pi R_{NP}^2 \frac{dL}{dt}}{\Omega_s}$$

(4.9)

where $\Omega_s$ is the volume per mole of Ga in the solid phase. By examining Equations 4.7, 4.8 and 4.9 we can determine that planar nanowire growth rate is constant; assuming steady flow rate of precursors, the growth rate depends only upon constant values, while the most tunable values are Au nanoparticle size, diffusion length (dependent on pressure, V/III ratio, and molar
flow) and surface adatom concentration which depends upon precursor molar flow rate and temperature. The constant growth rate, the axial length of the nanowire as a function of growth time, of planar GaAs nanowires has been experimentally demonstrated previously [45].

4.3 GaAs (100) Growth

The most commonly reported out-of-plane and in-plane nanowires grown by the VLS mechanism, for non (111) substrates, are summarized in Figure 4.2. On GaAs (100) substrates, out-of-plane VLS nanowire growth favors nanowires propagating in the <111>B crystal direction (35.3° from the surface) [61], as illustrated in Figure 4.2a. These GaAs <111> nanowires exhibit bi-directional growth resulting from the two available <111>B crystal directions available on the surface of (100), specifically, [1 1 -1] and [1 -1 1]. Planar nanowires on (100) substrates exhibit the same bi-directionality, growing in either the [0 1 -1] or [0 -1 1] crystal directions [61], as illustrated in Figure 4.2b. The cross-sectional profiles of planar <110> nanowires on (100) substrates have been identified as trapezoidal with a top <100> facet and two side <111>A facets that are 54.7° off from the surface [62] (Figure 4.2c). Note that the facets are only readily apparent under SEM on nanowires that are approximately larger than 150 nm in diameter; nanowires with a diameter that is less 150 nm tend to have a more circular cross-section with unresolved facets [45]. Planar nanowires grown on GaAs (100) have an optimal temperature of 460 °C, but still form 440-480 °C [45]. At lower growth temperatures, planar yield diminishes while at higher temperatures planar yield is improved but parasitic vapor phase epitaxy (VPE) growth is enhanced.

4.4 GaAs (110) Growth

In contrast to (100) substrates, on a (110) substrate there is only one available <111>B direction (Figure 4.2d). Under growth conditions that favor out-of-plane growth, the nanowires grow along the single <111>B direction at a 54.7° angle off the surface of the substrate (Figure
4.2d). With planar growth conditions, planar nanowires unanimously grow in the [00-1] direction [63], as illustrated in Figure 4.2e. The realization of unidirectional planar nanowire growth has significant implications since it is now possible to make completely aligned arrays of epitaxial planar nanowires. The cross-sectional profile of the unidirectional planar nanowires is trapezoidal, consisting of a top <110> facet and two <100> facets that are 45° off from the surface (Figure 4.2f).

To further identify the crystal orientations of these planar nanowires on (110) substrates, X-ray microdiffraction scans were performed. X-ray microdiffraction experiments were performed at Beamline 7ID of the Advanced Photon Source at Argonne National Laboratory. Kirkpatrick-Baez mirrors focused the 10-keV x-rays to a 30 µm diameter spot at the center of rotation of a six-circle goniometer. However, grazing incidence geometry was used for some measurements to enhance surface sensitivity, which extended the x-ray footprint across the surface of the sample. The resulting x-ray diffraction data reflects an ensemble average of many nanowires. Once a sample was mounted on the goniometer, the orientation of the surface normal was determined by the usual technique of specularly reflecting a laser beam off the surface, and adjusting the chi and phi angles of the Eulerian cradle until the reflected beam does not move upon rotation about the theta axis [64]. With knowledge of these positions of chi and phi, the direction of the surface normal is then calculated once the crystallographic orientation is determined. The measured substrate normal of the (110) is [0.9988, 1, 0.0048], which is 0.1976° from the [110] direction. Since these nanowires grow in complete registry with the substrate, their Bragg peaks overlap those of the substrates; instead, we focus our analysis on rods of diffuse scattering [65] from the well-defined facets of the nanowires. The directions of truncation rods have been used to identify the orientation of vicinal facets [66], nanofacets [67], and edges of isolated nanowires [68]. The series of scans in Figure 4.3a are collected at various out-of-plane momentum transfers, next to the GaAs (111)
Bragg peak and perpendicular to the growth axis of the nanowires. In Figure 4.3b we map the positions of the peaks found in each scan. The central peaks are due to the crystal truncation rod running parallel to the surface normal. This rod, appearing at constant in-plane momentum transfer, is due to scattering from the flat substrate and the top surface of the nanowires. The side peaks' in-plane positions vary with out-of-plane momentum transfer, and linear fits show they make an angle of $45.0 \pm 0.9^\circ$ to normal, i.e., these peaks reflect scattering from the side facets of the planar nanowires. Within our resolution, the two facet rods intercept at the (111) Bragg peak, indicative of unstrained nanowires. In contrast, scans along the nanowire axis have no additional features; the nanowires have no facets or other features which contribute to scattering in this direction. Shown in Figure 4.3c is an in-plane scan in the [00L] direction at $H = 2.03$ and $K = -1.97$, i.e., near the $(2,-2,0)$. Similar scans near the GaAs (200) Bragg peaks show the same features. The X-ray microdiffraction results thus confirm the nanowire top and side facet orientations.

Planar $<100>$ GaAs nanowires have an optimum growth temperature of 480 °C; below this temperature planar yield is greatly affected and at around 520 °C and above this unidirectionality is no longer present. $<100>$ planar wires have a naturally higher yield than $<110>$ nanowires at a given growth temperature and pressure. This is most likely due to the difference of angle between the growth plane, (111)B, and the substrate. The contact angle between the grown interface and the Au seed is an important factor for determining nucleation energies during growth [69]. As highlighted in Figure 4.2a-b, the steeper growth plane angle of 54.7° for $<100>$ planar nanowires vs. 35.3° for $<110>$ nanowires likely accounts for the different in planar yield between the two substrates.

### 4.5 Projection Theory

After examining the growth of planar nanowires on GaAs (100) and (110) substrates as seen in Figure 4.4, we hypothesize that the planar nanowire growth direction is simply the
vector projection of the $<111>B$ growth directions along the surface of the substrate for growth on (100) and (110) substrates under optimized growth conditions [45]; this point is illustrated in Figure 4.5. Taking the vector projection of $<111>B$ crystal directions on the surface of (100) and (110) substrates does yield their respective planar growth directions: [0,-1,1] and [0,1,-1] on the (100) substrates and [0,0,-1] on the (110) substrates. Assuming this hypothesis is true, for an arbitrary substrate, such as a vicinal substrate offcut to a specific angle, the planar growth direction can be projected by taking available $<111>B$ crystal directions on the surface and projecting them onto the substrate.

4.6 GaAs Off-Cut Growth

To test this model, nanowires were grown on a GaAs (100) substrate that is off-cut by 10° toward [0,-1,0]. The off-cut angle was defined by the manufacturer (AXT, Inc) by tilting a GaAs (100) crystal ingot 10° toward the [0-10] direction. A growth temperature of 460 °C and pressure of 1013 mbar were used. As can be seen from the SEM micrograph in Figure 4.6a, two propagating directions (red and blue colored) are observed. In contrast to growth on on-axis (100) substrates, the two directions are no longer parallel (or antiparallel), but rather with an intercepting angle of 165° (or ∼15°) as measured from top-view SEM images. Interestingly, when utilizing small Au colloids (20 nm), off-cut nanowires have a reduced planar yield and a majority of nanowires remain planar for a short distance then become non-planar as shown in Figure 4.7.

X-ray microdiffraction was used to determine the orientations of the two sets of nanowires with respect to the substrate. These nanowires, unlike those grown on GaAs (100) or (110), are misoriented with respect to the substrate crystal lattice, so their orientations can be directly determined by finding their Bragg peaks. The orientation of the surface normal was found to be [.9846, -.1747, 0], with better than 0.05° accuracy, by comparing the optically specular surface with the crystal orientation of the substrate. Figure 4.8a shows the [220] Bragg
peaks of both sets of nanowires, offset by several degrees on opposite sides of the much stronger substrate Bragg peak. In Figure 4.8b we place this azimuthal scan in its reciprocal-space context. The growth directions of the nanowires, assumed to be perpendicular to the surface normal, were then found to be [.1298, .7315, -.6694] and [-.0962, -.5425, .8345], corresponding to an intercepting angle between the two groups of nanowires of 165.45°, as summarized in Table 4.1.

To test the validity of nanowire projection theory and we have performed simple vector analysis to verify our theory and compare it to our x-ray diffraction experiments. To determine the theoretical substrate orientation of the off-cut wafer, we have to rotate the (100) wafer surface by 10° toward the off-cut direction. We can define the surface as a plane with a vector normal to it as [1 0 0]. Since the wafer off-cut direction is [0 -1 0], we can simulate the rotation easily by rotating the [1 0 0] surface normal clockwise about the Z-axis. The matrix operation can be represented as:

$$
\mathbf{V}_{\text{off-cut}} = \begin{bmatrix}
1 \\
0 \\
0
\end{bmatrix} * \begin{bmatrix}
\cos 10° & -\sin 10° & 0 \\
\sin 10° & \cos 10° & 0 \\
0 & 0 & 1
\end{bmatrix}
$$

$$
(4.1)
$$

$\mathbf{V}_{\text{off-cut}}$ is vector that is normal to the off-cut surface, which is equivalent to the surface of the substrate. To calculate the vector projections of the available <111> crystal directions on the surface, we can solve this by taking the vector orthogonal to the vector projection of <111> onto the surface normal. The vector that is orthogonal to the substrate normal must lie along the surface of the substrate. This is also known as the vector rejection. This can be calculated as follows:

$$
\mathbf{V}_{\text{proj}} = \mathbf{V}_{<111>B} - (\mathbf{V}_{<111>B} \cdot \mathbf{V}_{\text{off-cut}})\mathbf{V}_{\text{off-cut}}
$$

$$
(4.2)
$$

The projections are then normalized and compared with the normalized vectors that were found empirically by X-Ray diffraction. These comparisons appear in Table 4.1. For the angle measurements, the angles compared are between vectors using a simple operation:
The growth directions are also shown in Figure 4.8b. Also listed in Table 4.1 are values of crystal orientations, [.1314, .7455, -.6545] and [-.1094, -.6204, .7766] (thus 169.85° angle between the two nanowire orientations), obtained from the aforementioned vector projection theory and analysis. Good agreement between the calculated projection theory directions and the experimentally derived values are found. Substrate surface morphology such as atomic terraces on off-cut substrates [70, 71], one of the factors the projection model did not consider, could affect the planar nanowire growth direction. However, it is not clear what caused the slight discrepancy between the calculated and measured growth directions at this point. The presence of several peaks for the [11-1] nanowires on the high-angle side of Figure 4.8a indicates these nanowires may grow in a small range of orientations, apparently determined by local surface morphology rather than by registry with the substrate lattice. Our results indicate that utilizing vector projection and analyzing available surface growth directions, planar nanowires could theoretically be produced in any orientation, limited only by the substrate orientation itself.

4.7 Patterning of Planar GaAs (110) Nanowires

VLS planar GaAs NANOWIREs were grown using 250 nm colloidal gold (Au) nanoparticles as seeds and growth was carried out specifically in a horizontal flow Aixtron MOCVD reactor under atmospheric pressure. Epi-ready semi-insulating GaAs substrates (110) were used for growth. JEOL JBX-6000FS and Raith e-Line electron beam lithography systems were used to pattern the GaAs substrates using PMMA resist, followed by the evaporation of approximately 20-50 nm of Au thin film using an electron beam evaporator then liftoff. Initial processes for the removal of residual PMMA included an exposure to a 10 minute, 300W O₂ plasma and then soaked in three different solvent baths consisting of
acetone, methanol, and isopropanol for 10 minutes each leaving behind an array of Au nanoparticles and a clean surface as shown in Figure 4.9. An improved process has been developed with improved consistency between growths. Instead of using conventional solvents, a commercial n-methylpyrrolidone (NMP) based stripper was used. Remover PG is specifically designed to remove PMMA and is GaAs safe. Traditionally, PMMA residue is non-trivial to remove from GaAs because most conventional organic etches (i.e. $\text{H}_2\text{SO}_4$:$\text{H}_2\text{O}_2$) also aggressively attack GaAs. Remover PG is heated to 80 °C in a beaker before samples are added. Samples soak in heated PG remover for approximately 20 minutes, then sonicated while still warm for an additional 5 minutes. This cycle is repeated three times, using a fresh beaker for each subsequent cycle to prevent PMMA residue from settling on the substrate in additional cycles. After the cycles of Remover PG, the samples are sonicated traditional solvents (acetone, methanol, and isopropanol) for another 10 minutes each. After each solvent cleaning process is complete, beakers are cleaned with a self-heated piranha solution, 3:1 $\text{H}_2\text{SO}_4$:$\text{H}_2\text{O}_2$, for 10 minutes. This step is critical to make quality and clean patterns repeatable as PMMA residue tends to stick to used glassware and redeposit on the surface of samples intended to be cleaned. Organic residue left from PMMA resist films negatively impact planar nanowire growth by reducing planar yield and perturbing planar nanowire morphology as shown in Figure 4.10. Lastly, the samples are placed in an oxide etch solution of 1:1 HCL:$\text{H}_2\text{O}$. The final step is also crucial to the cleanliness of the surface; the etch undercuts and lifts-off any residual PMMA left behind by the solvent clean. Although the oxide etch produces a very clean sample, it lowers the energy barrier for new nanowire growth directions to occur as shown in Figure 4.11, however this only has a minor impact on yield.

The successful demonstration of high quality, unidirectional planar nanowire growth by using (110) substrates makes it possible to realize completely ordered nanowires arrays for array based high performance nanoelectronics. The ordering will be determined by the site
control of the Au nanoparticles by lithographical patterning. One of the challenges of patterning is the introduction of organic contamination from the resist chemicals. Nanowires are known to be sensitive to contaminants during growth as the metallic nanoparticles can absorb precursors and impurities alike depending on their solid solubility. Impurities can dope the wire as well as cause abnormal growth to occur [26]. Planar nanowires are extremely sensitive to impurities as they cannot only infiltrate the nanoparticle but contaminate the substrate surface that the epitaxial relationship of the entire nanowire bottom facet is built upon, preventing planar nanowire growth. Depending on the substrate treatment, we have observed nanowires grown initially in the planar fashion but taking off from the surface to grow in out-of-plane mode soon after. Shown in Figure 4.12 is an array of planar GaAs nanowires on a (110) substrate successfully grown from Au seed nanoparticles patterned using electron beam lithography. It is evident that all the nanowires unanimously propagated along the same direction, [00-1].

4.8 Interaction between Planar Nanowires and Obstacles

The unique geometry of planar nanowires allows them to interact with their substrate along the entire length of its axis instead of just during initial nucleation as with out-of-plane. Additionally, their growth trajectory puts them in the path of any in-plane structures residing on the surface. This allow for a unique opportunity to study the interaction between planar nanowires and obstacles which impede its growth. Figure 4.13 illustrates the result of the process to create vertical micropillars on a GaAs (100) substrate. Photolithography was used to create 5x5 µm² resist protected regions and the exposed substrate was etched for 5 minutes using a 1:8:80 solution of H₂SO₄:H₂O₂:H₂O with a nominal etch rate of ~8 nm/s. The etch left behind ~2 µm tall pillars with a slightly sloped profile due to some anisotropy of the etching process. 250 nm Au colloid was then dispersed on the sample and nanowires were grown for 100 s with a growth rate of 30 nm/s for a nominal length of 3 µm. Figure 4.14 highlights some
of the interaction between $<110>$ planar nanowires and obstacles in its path. Figure 4.14a shows a planar nanowire that grew on the etched surface and encountered the sloped edge of a micropillar. The nanowire climbs up the sloped edge, hits a vertical segment while remaining planar. When the nanowire encounters the abrupt $90^\circ$ interface between the top and side of the pillar, the nanowire ceases to be planar and takes off in a non-planar trajectory. In contrast, Figure 4.14b, shows a nanowire that was able to overcome the abrupt interface by meeting the edge with a shallower intercepting angle while remaining planar. The directional difference between the two wires is due to different exposed crystal facets along the side of the pillar after etching. It is remarkable that the planar nanowire can maintain its planarity on a differently oriented surface along the length of its axis. These results give us insight into alternative methods to control nanowire growth directions in addition to substrate choice and surface treatment.
4.9 Figures and Tables

Figure 4.1 Illustration highlighting the routes growth precursors can take to influence the growth rate of planar nanowire growth.

1. Direct Impingement 4. Desorption from nanowire
2. Diffusion along nanowire 5. Desorption from substrate
3. Diffusion along substrate 6. Thin film deposition
Figure 4.2 Illustrative comparison of crystal orientations between Au-catalyzed GaAs nanowires grown on GaAs (100) and (110) substrates. (a,d) available (111)B off-plane nanowire directions with their respective nanowire-to-substrate angles as labeled; (b,e) available growth directions for planar nanowires on their substrates with the wafer flats identified, and (c,f) the cross-section geometry of planar nanowires with crystal facets labeled, and SEM images as insets. The scale bar for both insets is 200 nm.
Figure 4.3 X-ray diffraction scans to determine the orientation of GaAs nanowires grown on a GaAs (110) substrate. The Miller indices are referenced to the substrate crystal lattice.

a) In-plane scans near the (111) Bragg peak, with a large angle of incidence. Scans are in the [H,H,0] direction, i.e., transverse to the nanowires, at various out-of-plane momentum transfer values (indexed as H+K in the legend). Scans are normalized and offset, to be able to display them on the same axes. b) Map in the L = 1 plane of reciprocal space of the peak positions (symbols) and linear best-fits (dashed lines). The central peaks (at H-K = 0) are from the truncation rod of the flat substrate surface, while the rotated rods (± 45°) arise from the two angled sides of the trapezoidal nanorods. c) In-plane scan in the [00L] direction, i.e., along the nanowire growth direction. Scan performed near the (2,-2,0) Bragg peak at H = 2.03 and K = -1.97, with an angle of incidence of 0.2° for enhanced...
Figure 4.4 SEM images of (a) <110> GaAs planar nanowires on GaAs (100) substrates and (b) <100> GaAs planar nanowires on GaAs (110) substrates. Inset highlights the trapezoidal cross section for each type of nanowire.
Figure 4.5 Illustration highlighting the planar projection of $<111>B$ growth directions on to GaAs (100). There are two available $<111>B$ growth directions available on the surface of GaAs (100) and their projections coincide with planar GaAs nanowire growth directions.
Figure 4.6 a) 75° tilted SEM image (false-color) of planar GaAs nanowires grown on a GaAs (100) substrate offcut by 10° toward [0-10]), showing two groups of nonparallel planar nanowires. b) A diagram illustrating the projections of the <111>B directions onto the substrate, which correspond to the growth directions of the planar nanowires observed in (a). The red-colored planar nanowire is along the projection of [1-11]B crystal direction and the blue-colored nanowire is along the projection of [11-1]B crystal direction, as verified by X-ray microdiffraction.
Figure 4.7 SEM image of small colloid (20 nm) nanowires growing on a GaAs (100) substrate offcut by 10° toward [0-10]. In contrast to large colloid nanowires, after a short distance nanowires cease to remain planar and start growing in <111>B growth directions out of plane.
Figure 4.8 a) Azimuthal scans around the (220) Bragg peak of a sample with GaAs nanowires grown on a GaAs (100) substrate offcut by 10° toward [0-10]. For these scans, the angle of incidence with respect to the surface plane was 2° in order to enhance surface sensitivity. The small peaks on either side of the substrate’s central peak are the Bragg peaks of nanowires with growth orientations as labeled. High-resolution scans of these side peaks (not shown) were used to identify the nanowires’ exact crystal orientations with respect to the substrate crystal orientation, as described in the text. b) Reciprocal-space schematic of the azimuthal scan in a). Major axes of the substrate’s reciprocal lattice are shown in blue. The surface normal, $n$, is shown as a dashed red line, and the light green plane represents the offcut surface. The 220 Bragg peak is shown as a large circle; the arc cutting through it shows the direction of the azimuthal scan. The locations of the small peaks found in a) are shown as diamonds; the resulting growth directions of the respective nanowires are shown as lines on the surface plane.
Table 4.1 Comparison between calculated and experimental nanowire growth directions for a GaAs (100) vicinal substrate 10° off-cut toward [0-10].

<table>
<thead>
<tr>
<th></th>
<th>Calculated Direction</th>
<th>X-Ray Diffraction</th>
<th>SEM Visual Inspection</th>
<th>Angle Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Normal</td>
<td>[.9848, -.1736, 0]</td>
<td>[.9846, -.1747, 0]</td>
<td>-</td>
<td>0.06°</td>
</tr>
<tr>
<td>[1,1,-1] Projected Nanowire</td>
<td>[.1314, .7455, -.6545]</td>
<td>[.1298, .7315, -.6694]</td>
<td>-</td>
<td>1.17°</td>
</tr>
<tr>
<td>[1,-1,1] Projected Nanowire</td>
<td>[-.1094, -.6204, .7766]</td>
<td>[-.0962, -.5425, .8345]</td>
<td>-</td>
<td>5.62°</td>
</tr>
<tr>
<td>Angle Between Planar Nanowires</td>
<td>169.85°</td>
<td>165.45°</td>
<td>164.5°</td>
<td>-</td>
</tr>
</tbody>
</table>
Figure 4.9 Electron beam lithography patterned array of Au nanoparticles used for planar nanowire VLS growth. 20 nm of Au was evaporated into opened pours in a PMMA resist layer. Extensive cleaning was performed to leave the surface free of PMMA residue.
Figure 4.10 (a) SEM micrograph of the result of a planar nanowire growth on aGaAs (110) substrate where PMMA residue was not fully removed. Nanowires grow with poor morphology, inconsistent growth direction and with non-planarity resulting from organic contamination. (b) In addition to the poorly formed wires, unwanted nanowhiskers form along the surface of the substrate.
Figure 4.11 SEM micrograph of EBL patterned array of planar GaAs nanowires on GaAs (110) after an HCL oxide etch was performed. The surface is very clean, however, a small percentage of nanowires do not grow unidirectional but in a comparable energy direction caused by the etch.
Figure 4.12  a) Illustration of site-controlled uni-directional planar nanowire array growth, with Au particles defined lithographically and growth taken place on a (110) substrate along [00-1] direction. b) Tilted (75°) SEM micrograph of a completely ordered array of [00-1] GaAs nanowires grown from E-Beam patterned Au nanoparticles on a (110) GaAs substrate. The Au nanoparticle size is approximately 175 nm in diameter and the nanowires are approximately 1.2 µm long.
Figure 4.13 Illustrated schematic of etched GaAs micropillars used to create planar nanowire growth obstacles. 5 x 5 µm² pads of photoresist were lithographically placed before a wet chemical etch was used to define the pillars. Pillars are approximately 2 µm
Figure 4.14 SEM images of planar $<110>$ GaAs nanowires that encounter a GaAs micropillar during the growth. (a) A planar nanowire is able to grow up the side of a micropillar, however when reaching the top surface and sidewall junction becomes non-planar. (b) Utilizing a shallower intercepting angle by growing on a different sidewall, a
5.1 N-Type Doping of Planar GaAs Nanowires

The successful N type doping of planar GaAs nanowires is critical for GaAs based electronic devices. Historically, the majority of GaAs electronic devices have been unipolar N-Type from the comparatively large electron mobility and properties of the AlGaAs/GaAs heterojunction conduction band profile [72]. Utilizing silane, SiH₄, and disilane, Si₂H₆, as n-type precursors, planar nanowires have been doped N-type. Si, technically, is an amphoteric dopant impurity which can either behave as an acceptor or donor depending on growth conditions. Incorporation of Si into planar nanowires appears to behave similarly to their vertical analogs [73]. Si has been confirmed to be an N-type dopant, under planar nanowire growth conditions, by transistor turn-on behavior (transistor details are outlined in Chapter 6).

The majority of Si is incorporated through the Au seed into the core of the nanowire with minor incorporation into thin film growth that occurs along the surface of the substrate and sidewalls of the nanowire. The incorporation rate, under constant Si flow, appears steady along the length of the nanowire. Figure 5.1 shows the resistance of a Si doped <100> planar GaAs nanowire under constant gas phase Si/Ga ratio of 1.84 x 10⁻² with a total Si₂H₆ molar flow of 1.34 x 10⁻⁶ mol/min throughout its entire growth. AuNiGe alloyed ohmic contacts are placed with 1 µm spacing along the length of a <100> planar GaAs nanowire. The resistance shows no trend and minimal variation along the length of the nanowire indicating no accumulation of dopants along the axial direction or a radial thin VPE film. Si incorporation into the parasitic thin VPE layer appears to be minimal. For thin VPE layers, ~30 nm or less, the parasitic VPE is mostly depleted with minimal conduction occurring through the film. Figure 5.2 shows a two terminal I-V measurement comparing a Si doped planar <100> GaAs nanowire with the background leakage of the parasitic VPE layer on substrate surface. There is a ~10³ order of magnitude difference in conductivity, indicating the majority of the conduction takes place...
within the nanowire. For especially long nanowire growths and/or high Si flows during growth, “hot spots” (regions of high Si doping) can occur and can cause substantial leakage. Hot spots are rare for nanowire grown for reasonable lengths (< 20 µm) on GaAs (100) substrates and virtually non-existent on GaAs (110) substrates. In addition, there appears to be no morphology or growth direction changes to the nanowire under Si flow.

5.2 P-Type Doping of Planar GaAs Nanowires

Zinc (Zn) and carbon (C) are both important p-type dopants in III-V semiconductors. Zinc is one of the most commonly used p-type dopants for GaAs, readily available in its metalorganic precursors (DEZn or DMZn). It is non-amphoteric, unlike silicon and carbon. It does not have the etch-back issues of carbon tetrachloride or tetrabromide [74]. Several groups have done extensive work on studying and controlling dopants in vertical <111> nanowires, [73, 75-78] including through Zn implantation, [76] zinc diffusion [79] and in situ incorporation of zinc [77]. The dopant incorporation can take place either through the seed by VLS growth mode or onto the sidewall surface by unassisted vapor phase epitaxy (VPE) mode [75, 78]. Although for Ge and many other VLS nanowires, it appears that most dopants reside in the thin epitaxial layers that form on the nanowire sidewall contributed from non-VLS growth, [75] it has been confirmed that Zn incorporates through the Au seed in vertical GaAs VLS nanowires [77]. To gauge the effect of Zn precursors on planar <110> GaAs nanowires, a two segment growth experiment was performed. The total growth time, 140 s, is split evenly between two phases of the nanowire growth. During the first segment, a constant growth temperature of 460 °C and TMGa flow rate of 10 sccm (2.488 x 10^{-5} mol/min) is used to facilitate planar nanowire growth using a 250 nm Au seed. Halfway through the growth, Zn precursors are turned on and flown at a constant Zn/Ga gas phase ratios ranging between 5.9 x 10^{-4} to 1.2 x 10^{-1}. Figure 5.3 highlights the results of the two-step growth. In Figure 5.3(b), for Zn/Ga gas phase ratios of 5.9 x 10^{-2} and above, the effect of Zn during the course of planar
nanowire is evident. At these gas phase ratios, nanowires do not remain planar when Zn is switched on, with virtually no delay between introduction to Zn in the reactor and the observed effect on nanowire morphology. The wires cease to remain planar, and seemingly twist around arbitrary out-of-plane directions; any registration with the substrate is lost. In addition, the trademark well-defined crystal facets are no longer present, and the nanowires exhibit fluctuating diameters along its axial dimension. Nevertheless, lowering the Zn/Ga ratio to $5.9 \times 10^{-3}$ exhibits a unique perturbation of the nanowire morphology. Typically, $<110>$ planar GaAs nanowire have a trapezoidal cross-section with smooth top and side facets. The presence of low levels of Zn cause a change of the nanowire faceting to alter to a more triangular cross-section before peaking then reverting back to the trapezoidal cross-section at regular intervals. To determine the cause of the perturbation, cross-sectional transmission electron microscopy (TEM) was performed to examine the crystal structure of the nanowires. Through bright field transmission electron microscopy (TEM) imaging (Figure 5.4a), we have determined that the corrugated morphology along the length of the nanowire corresponds to periodic twinning in the axial direction. The twin planes are aligned with the $<111>B$ crystal planes while the nanowire propagates along the $<110>$ direction. The selected area electron diffraction pattern along $[110]$ zone axis of the nanowire (Figure 5.4c) shows the existence of a twin boundary, while the split spots are likely from the small angle grain boundary in the nanowire. This implies that the VLS growth of $<110>$ planar nanowires occurs at the $<111>B$/Au interface, and the impurity atoms perturb the nucleation, as is the case for out-of-plane $<111>$ nanowires [80].

The periodic notching along the surface corresponds to an internal twinning super lattice (TSL) along the axis of the nanowire. TSLs in nanowires have been projected to introduce minibands [81], direct carrier generation-recombination transitions [82], and increased sidewall phonon scattering [83].
Interestingly, the morphology of the Zn-doped nanowires further changes as growth proceeds without changing the Zn precursor flows at all. For example, at Zn/Ga of $5.9 \times 10^{-3}$ (halfway in-between the levels in Figure 5.3a and 5.3b), nanowires propagate in plane initially then grows out of plane after ~1.8 $\mu$m in length as shown in Figure 5.5b. Also at this concentration, we notice solid precipitates on the surface of some of the Au colloids after growth as seen in Figure 5.5a. Since this happens at a higher Zn/Ga ratio, it is possible these deposits are Zn rich. Combining this observation with the Zn concentration effect on nanowire morphology shown in Figure 5.3, it suggests that the Zn incorporation in the nanowires increases with growth time and beyond a threshold, the nanowires start to grow out of plane. Note that when Zn doping is at a lower level (e.g. $5.9 \times 10^{-4}$ Zn/Ga), the nanowires remain planar for the same growth time (same length), indicating that the threshold for out-of-plane growth mode is dependent upon a critical Zn concentration instead of being simply dependent upon growth duration. Clearly there is an accumulation effect in the amount of Zn incorporated, even though the gas phase Zn flow is constant during the entire growth process. This phenomenon indicates that Zn does incorporate through the Au seeds in planar GaAs nanowire VLS growth, otherwise accumulation in the axial direction cannot happen. This conclusion is in agreement with a previous report [77] on <111> vertical nanowires where under constant Zn precursor flow, Zn doping (characterized by electrical measurement) increases along the axis of the nanowire (i.e. with growth time). This is because if Zn is incorporated through thin film growth, the doping would be expected to be higher at the base of the wire due to tapering from VPE.

The effect of C-doping using CBr$_4$ as the precursor for planar nanowire growth is also studied. Figure 5.6 shows the effect of CBr$_4$ on planar nanowire growth as a function of doping concentration, for C/Ga ratios (gas phase molar flows of CBr$_4$ relative to TMGa) of $1.6 \times 10^{-3}$, $2.4 \times 10^{-3}$ and $3.2 \times 10^{-3}$. Note that CBr$_4$ was turned on at the same time as TMGa for all
experiments in Figure 5.6 (one-step doping experiment) and the growth rate does not seem to be affected by the presence of CBr4. Similar to Zn doping, periodic corrugation occurs in the presence of CBr4. However, in contrast to Zn doping, the onset of the periodic corrugation has a significant delay, presumably because of the extremely low solubility of C in Au [84]. Under the conditions we investigated, structural perturbation can be observed by SEM only when the nanowire length exceeds ~5 - 7 µm depending on the doping level. The higher the CBr4 flow, the shorter the latency period is and the longer the TSL segment will be for a fixed total nanowire growth time or length. As can be seen in Figure 5.6, for the same total nanowire length, 1.6 x 10^{-3} C/Ga produced ~9 corrugations (Figure 5.6b), while a longer TSL segment with ~13 periods of corrugations is produced with 2.4 x 10^{-3} of C/Ga (Figure 5.6d), indicating an accumulation effect of carbon within the Au colloid during nanowire growth. When the doping level exceeds 3.2 x 10^{-3} (Figure 5.6e and 5.6f), controlled nanowire growth ceases after the latency period and the nanowires crawl along the surface without defined orientation or facets. This is in sharp contrast to Zn-doping, where the highest doping level nanowires stop propagating in plane and grow in seemingly amorphous state but out of plane.

For both types of p-type dopants (Zn and C), we have found that the corrugation period, the distance between adjacent ridges, has a strong correlation with the nanowire size which is a direct function of the Au seed particle size. An atomic force microscopy (AFM) scan (Figure 5.7) shows the similarities of facets between Zn and C induced twinning in planar GaAs nanowires. Plotted in Figure 5.8a and 5.8b are the relationship between the corrugation period and nanoparticle size for TSL formations in DEZn and CBr4 doped planar GaAs nanowires, respectively. Good linear fits with a slope of .91 for DEZn and .76 for CBr4 doped nanowires are observed between corrugation period and nanoparticle size over several nanowire sizes. This suggests that the twinning period is almost linearly dependent on the seed particle size for the range of II/III ratios used for our experiments. This is similar to the nanowire particle size
dependence in the Zn induced TSL system for vertical wires [26, 85]. Note that for C-doped GaAs planar nanowires, the TSLs are spaced tighter than Zn-doped for the same Au seed particle size.

In addition to perturbing the nanowire growth using dopant impurities from the gas phase, we have also performed experiments where Zn or C impurities originate from either the substrates or Au seed particles. Shown in Figure 5.9 is an array of Au-assisted VLS GaAs planar nanowires grown on a highly Zn-doped (> 5 x 10^{19} \text{cm}^{-3}) GaAs (100) wafer. Corrugated faceting can be clearly seen in these nanowires after a short latency period. Undoped and low level (1 x 10^{18} \text{cm}^{-3}) Zn-doped GaAs wafers loaded in the same growth run did not produce the characteristic corrugated morphology, presumably because the minimum Zn concentration threshold for twinning was not reached for the growth period (100 s) examined.

To introduce C-doping impurities from a non-gaseous source, we have used Au catalyst from Au thin film that is contaminated with C during evaporation by using a graphite crucible. Interestingly, the incubation time that was mentioned before in the case of the carbon-doped planar nanowire growth using CBr4 can be eliminated by introducing carbon contamination in the Au catalyst before the growth. Figure 5.10a shows a nanowire grown from a Au dot formed from Au thin film patterned by lithography and deposited by electron-beam evaporation. Periodic corrugation (notches) can be clearly seen on the nanowire facet. In contrast, a control experiment using Au dots that are carbon free show no notches (Figure 5.10b). The ratio between the notch period and Au particle size is also found to be close to .7 in this case (Figure 5.10c), just as those in Figure 5.8b.Interestingly, the latency period described before when doing with CBr4 from the gas phase is not observed here, since C is already premixed with Au before growth and not limited by equilibrium solubility.
TSL formation can be modulated by switching the flow of dopant impurity precursors on and off, creating periodically corrugated and non-corrugated segments along the axis of the nanowire. Shown in Figure 5.11b are two different size GaAs nanowires with Zn-doping modulated three times with a 50% duty cycle between a set flow and no flow at all. First, it can be clearly seen that the corrugation period increases with the wire size, as shown in Figure 5.8. Second, the less than abrupt termination of corrugation at the beginning of each off-segment, especially for the smaller wire, is probably a result of accumulated Zn within the Au nanoparticle that continues to precipitate into the nanowire after the source is off. This further proves that Zn dopants are incorporated and accumulate through Au seeds. TSL formation is modulated with C as seen in Figure 5.12, however, a substantial incubation time is needed to induce twinning before modulation can be performed.

The perturbation of VLS nanowire growth due to the introduction of impurities during growth presents an interesting opportunity to study the effects of dopants to the traditional binary phase VLS system. While it is known that Zn precursors cause TSL formation in most VLS nanowires systems, the upper range of the precursor effect has not been fully investigated. Besides the well reported kinking [86], Regolin et al. report briefly on the effect of DEZn at high II/III concentrations in vertical nanowires [48]. They noticed a fragmenting of the Au nanoparticle and many smaller nanowires with poor morphology shooting off from the fragmentation point. In our experiments, we noticed a growth of material on the surface on the Au nanoparticle during the nanowire growth. In VLS growth theory, nucleation occurs at a triple phase boundary (vapor, liquid, solid) and surface energy dictating the growth direction. With high Zn/Ga ratios, it appears this growth mode breaks downs and growth occurs at every VL interface resulting in radial growth from the nanoparticle as seem in Figure 5.13a. This modified version of VLS growth could potentially be used to create non-nanowire structures. This is evident in Figure 5.13b where the modified VLS is used to make uniform pyramidal
structures, with well-defined crystalline facets, along the surface of the substrate. The use of impurities to modify VLS growth has potential to create a whole new paradigm of nanostructures.

Two terminal electrical measurements were performed on a set of 10 \( \mu \)m long Zn-doped GaAs nanowires to verify their electrical activity. Zn doped planar VLS nanowires can be particularly challenging to test electrically when the wire is long, because of the interference of a parasitic thin VPE film deposited over the entire surface along with the VLS nanowire axial growth. The low growth temperature and higher pressure required for planar VLS nanowire growth favor the incorporation of Zn in the VPE film, as a result the parasitic thin film is typically heavily doped instead of depleted, under the growth condition specified in this dissertation. Note that the parasitic VPE thin film does not seem to present a problem for Si-doped planar GaAs nanowires \([63, 85]\) and can also be significantly reduced (to as little as 1/1000 of the axial VLS growth rate) under optimized conditions. Figure 5.14 shows the process of removing the thin VPE layer by wet chemical etching, revealing the planar VLS nanowire core underneath and taking two terminal electrical measurements step by step until the Zn-doped nanowire is \( \approx 10^6 \) times more conductive than the substrate at 3 V bias of a representative Zn-doped nanowire with Zn/Ga ratio of \( 4.14 \times 10^{-3} \). The resistivity of a planar nanowire can be estimated using the simple resistivity model, assuming minimal space charge depletion and ignoring contact resistance while approximating the cross-sectional area of the wire as a trapezoid \([45]\):

\[
R = \rho \frac{L}{A} = \rho x \frac{L}{\frac{1}{2}(a+b)h}
\]  

(5.1)

where \( R \) is resistance, \( \rho \) is resistivity, \( A \) is the nanowire cross-section area, \( L \) (7 \( \mu \)m) is the length of the nanowire, \( a \) (92 nm) and \( b \) (231 nm) are the widths of the nanowire top and bottom facets, and \( h \) (98 nm) is the nanowire height, as determined by planar GaAs nanowire geometry.
The nanowire resistivity (lower limit since depletion width is ignored) is then calculated to be on the order of $10^{-3}\ \Omega\cdot\text{cm}$, which corresponds to a Zn doping concentration of $\sim 7 \times 10^{19} \text{cm}^{-3}$ based on the empirical curves for VPE films in literature [88]. On the other hand, for all attempted electrical testing of C doped GaAs nanowires, no electrical activity was measurable, indicating a doping level lower than $\sim 1 \times 10^{17} \text{cm}^{-3}$ considering the nanowire size and depletion width. Note that there was no detectable highly doped VPE parasitic thin film under our C-doping condition which is in contrast to what has been previously reported [89]. Phase diagrams for the C/Au system indicate a low solubility of C in Au, possibly implying that VPE could dominate under different growth conditions [84]. Furthermore, Zn doping can be modulated with n-type Si doping, forming lateral p-n junctions monolithically in situ. Shown in Figure 5.15 is an n-p-n junction doped with Si-Zn-Si sequentially as the GaAs nanowire growth proceeds laterally. The Si/Ga ratio for the Si segment is $1.84 \times 10^{-2}$ and the Zn/Ga ratio for the Zn segment is $4.14 \times 10^{-3}$. Signature periodic corrugation appears in the Zn-doped segment as expected. Importantly smooth morphology returns after switched back to Si-doped segment.

TSL formation in vertical nanowires has been reported in several binary III-V systems such as InAs [90], GaP [91] and InP nanowires [26], induced by adjusting temperature, impurity doping, or V/III ratio [43] during nanowire growth. Polytypic growth, switching between crystal structures (typically wurtzite and zinc blende), has been also reported in conjunction with TSL formation. TSLs in planar nanowires share the same basic properties with their vertically oriented counterparts: twin planes coinciding with (111) crystal planes and responsive to growth and doping conditions. However, there are pronounced differences arising from the inherent geometry of planar nanowires. Planar GaAs nanowires on GaAs (100) share the same $<111>B$ growth interface with vertical nanowires except the planar nanowire propagation direction is not orthogonal with the growth plane. The growth plane, consequently the twin plane, forms a $35.3^\circ$ intersection with the $<110>$ crystal direction which is the planar
nanowire propagation direction on GaAs (100) substrates. The non-orthogonality of growth and propagation directions, and epitaxial attachment to the surface leads to a cross-section and outward surface faceting that are different from those for vertical <111>B III-V nanowires [32]. Algra et al. proposed a model that relates the periodic twinning to the minimization of Au seed surface area and liquid-solid interface energy during nanowire growth [26]. While the twinning is highly periodic in planar nanowires, it appears the separation between non-twinned and twinned segments are uneven (the twinned segment is significantly shorter) based on TEM examination. Adapting Algra’s model to planar nanowires suggests the uneven segments are a result of the twinned segments becoming energetically unfavorable at a shorter segment length than the untwinned segments. The difference is likely because of the unique planar nanowire geometry and epitaxial nature of the planar nanowires. Likewise, polytypism in planar GaAs nanowires has not been observed, probably a result of their epitaxial relationship along the nanowire axis with the zinc-blende crystalline substrate.
5.3 Figures

Figure 5.1 Two terminal measurements of a Si doped planar $<100>$ GaAs nanowire taken at multiple lengths along an individual wire. Similar resistance levels and no obvious trend suggest that dopants are not accumulated along the length of the nanowire.
Figure 5.2 Two terminal measure of a Si doped planar <100> GaAs nanowires comparing the conductivity of the nanowire vs. the background substrate leakage. The 3 order magnitude difference between the conductivity of the nanowire and substrate confirms that transport occurs in the nanowire and not through the substrate or parasitic films.
Figure 5.3 <110> GaAs planar nanowires grown on GaAs (100) substrates utilizing a two-step growth scheme with half the nanowire growth (70 s) under undoped growth conditions and the second half of the nanowire grown in the presence of Zn dopants. The dashed line represents the halfway point when the Zn precursor is turned on. At low Zn/Ga gas phase molar ratio of $5.9 \times 10^{-4}$ (a), periodic corrugation appears along the axis of the planar nanowire. Further increasing II/III gas phase ratios to $5.9 \times 10^{-2}$ (b) alters the nanowire growth with no defined crystalline direction or morphology. The scale bars are 500 nm.
Figure 5.4 (a) High magnification SEM image of a Zn-doped planar GaAs nanowire showing periodic corrugation on the nanowire top and side facets. The scale bar is 500 nm. (b) A bright-field TEM image shows twin boundaries in the nanowire, indicated by the red arrows. The growth direction of the nanowire is along <110>, while the twin boundary is in (111) plane. The scale bar is 20 nm. (c) Selected-area electron diffraction pattern along [110] zone axis of the nanowire shows the existence of the twin boundary.
Figure 5.5 (a) Solid precipitants on face of Au colloid, indicating additional nucleation at the VL interface. (b) Nanowires that started planar but then changed growth direction after a critical distance during Zn influenced planar GaAs nanowire growth.
Figure 5.6 SEM images of planar GaAs nanowires grown at three C doping levels: $1.6 \times 10^{-3}$ for (a and b), $2.4 \times 10^{-3}$ for (c and d), and $1.6 \times 10^{-3}$ (e and f), in CBr$_4$/TMGa gas phase molar ratio. CBr$_4$ is kept on at a constant level from the beginning of their growth. Two images are shown for each doping level with different magnification and angle, and the scale bar is 500 nm for all images. At low doping level (a,b), the nanowires exhibit a long latency period before exhibiting TSL formation. As the doping increases (c,d), the latency period shortens and TSL emerges earlier given identical growth times. When the doping level exceeds $3.2 \times 10^{-3}$ (e,f), controlled nanowire growth ceases after the latency and the nanowires “crawl” along the surface with a concave surface.
Figure 5.7 AFM images of the periodic faceting occurring with TSL formation on (a) Zn and (b) C influenced planar GaAs growth on GaAs (100) substrates.
Figure 5.8 Relationship between corrugation period and Au nanoparticle size for (a) Zn-doped and (b) C-doped planar GaAs nanowires. Linear fits with slopes of .91 for DEZn and .76 for CBr4 doped nanowires are found size over a wide range of Au seed sizes for several doping levels.
Figure 5.9 Periodic corrugations in planar GaAs nanowires grown on a heavily Zn-doped ($> 5 \times 10^{19}$ cm$^{-3}$) GaAs epilayer.
Figure 5.10 (a) A planar GaAs nanowire grown with Carbon contaminated Au catalyst. The notches were induced with no apparent latency. The Au dots are fabricated through electron-beam lithography and electron-beam evaporation. The Carbon contamination is created in evaporation by using graphite crucible. (b) A planar GaAs nanowire grown with Au colloid which is supposed to be contamination free. No notches are observed. (c) plot of notch period versus Au diameter. The Au dots are contaminated by carbon and produced as mentioned above.
Figure 5.11 (a) Schematic showing the precursor flow pattern during the growth of planar nanowire growths with modulated Zn-doping. TMGa and AsH3 flows are kept constant throughout nanowire growth while DEZn is modulated at a 50% duty cycle every 30 s. (b) SEM image showing two planar nanowires with Zn-doping switched on and off as indicated. See text for details. The scale bar is 1 µm.
Figure 5.12 Modulation of CBr$_4$ induced twinning in a planar GaAs <100> nanowire. After the incubation period CBr$_4$ was turned on and off to produce regions with normal GaAs <100> morphology and regions of periodic twinning.
Figure 5.13 (a) At high Zn/Ga ratios, one-dimensional VLS nanowire growth breaks down and rapid nucleation on the gold surface occurs, encasing the Au colloid in crystalline GaAs. (b) At very high Zn/Ga ratios, well faceted nanostructures grow from the Au colloid in all directions indicating a breakdown of one-dimensional growth
Figure 5.14 Two terminal IV characteristics of intentionally Zn doped planar GaAs nanowires grown on GaAs(100) substrates with a Zn/Ga ratio of $4.14 \times 10^{-3}$, comparing the conductivity between the nanowire and substrate surface as a function of etching time: (a) as grown before etching, (b) 2s, (c) 4s, and (d) 6s.
Figure 5.15 Doping modulation along planar GaAs nanowire between Si and Zn, allowing the formation of n-type and n-type segments laterally in situ. The Si/Ga ratio for the Si segment is $1.84 \times 10^{-2}$ and the Zn/Ga ratio for the Zn segment is $4.14 \times 10^{-3}$. Signature periodic corrugation appears in the Zn-doped segment and smooth morphology returns after switched back to Si-doped segment. The scale bars are 2 µm.
CHAPTER 6 – GaAs PLANAR NANOWIRE BASED ELECTRONIC DEVICES†

6.1 GaAs Planar Nanowire MESFETs

Metal Semiconductor Field Effect Transistors (MESFETs) have long been a robust, reliable and easily fabricated transistor design. MESFETs utilize a Schottky contact, a potential barrier formed by mismatch between the metallic work function and the combined electron affinity and Fermi level of the semiconductor, to create a rectifying junction to control the concentration of carriers in the channel. A quality metal-semiconductor interface is easy to achieve when compared to metal oxide semiconductor (MOS)FETs, where interface traps can easily deplete the channel and make accumulation or inversion of charge difficult. MOSFETs on GaAs are notoriously challenging to design because of Fermi level pinning [92], unpassivated surface states trap carriers and push the Fermi level toward the mid gap, on GaAs (100) surfaces; combined with minimal available passivation techniques, MOSFETs on GaAs require a great deal of optimization. MESFETs are attractive devices for initial electronic material characterization of planar GaAs nanowires.

Figure 6.1 illustrates the process to fabricate GaAs planar nanowire MESFETs. Fabrication of planar nanowire MESFETs begins with MOCVD growth. Either GaAs (100) or GaAs (110) substrates are suitable for planar nanowire growth. (110) substrates offer unidirectional growth and less leakage than (100) substrates because of slower growth rates of parasitic VPE, however, subsequent regrowth is challenging on (110) [93] and, currently, p-type.

†Some of the content in this chapter was adapted from Dowdy, R., D. A. Walko, et al. (2012). 'Realization of unidirectional planar GaAs nanowires on GaAs (110) substrates.' IEEE Electron Device Letters 33(4): 522-524.
doping precursors cause non-planarity in <100> planar nanowires. Au colloid, typically between 100-250 nm, suspended in an aqueous solution is dispersed by evaporation on a 115 °C hotplate. Samples are annealed at 625 °C for GaAs (100) and 650 °C for GaAs (110) substrates under a $8.93 \times 10^{-3}$ mol/min (200 sccm) AsH$_3$ overpressure and remains constant throughout the growth. Growth takes place at 460 °C for GaAs (100) and 480 °C for GaAs (110). The higher temperatures used for GaAs (110) substrates promote increased planar yield without the drawback of a thick parasitic VPE layer. TMGa is used as the group III precursor to initiate the nanowire growth and Si$_2$H$_6$ is used to dope the nanowires n-type. Flow rates of TMGa and Si$_2$H$_6$ are variable and selected to create a specific doping concentration with the absolute flow of Ga determining the nanowire growth rate and the ratio of TMGa/ Si$_2$H$_6$ dictating the doping concentration; although the growth rate of the nanowire influences the dopant incorporation as well. Nanowires are grown to a sufficient length, depending on subsequent processing parameters, in order to bridge source and drain contacts. For randomly placed contacts, nanowires are grown in excess length to increase the probability that a given nanowire will make contact with source and drain pads. After growth, samples are sonicated in methanol for 2 minutes to remove any non-planar nanowires. Repeated patterns of 20 x 20 µm$^2$ pads are lithographically opened in a AZ5214 photoresist layer to define the source and drain regions. Source to drain distance can vary between 3, 5, or 7 µm with actual lengths depending on accuracy of the lithographic process. Before metallization, opened regions are exposed to a 300 W O$_2$ plasma for 1 minute to remove any residual photoresist in the opening. To remove any oxide generated by the plasma, samples are dipped in a solution of 1:1 HCl:H$_2$O for 15 s before they are placed in the evaporator. A metallic thin film stack of 20 nm/50 nm/30 nm/50 nm of Ge/Au/Ni/Au is evaporated to create the ohmic contacts for the source and drain regions. Lift-off occurs in a sonicated bath of acetone for ~ 5 minutes and subsequently rinsed in methanol and isopropyl alcohol. The metal stacked is annealed for 15 s at 400 °C in a N$_2$
ambient annealing chamber to alloy the contacts to reduce contact resistance. After annealing
the gate region is opened up with a 20 x 20 µm$^2$ square region with a long thin fin that extends
$\sim$25 µm to make contact with the actual nanowire; gate lengths are selected from 1 or 2 µm
depending on the intended process. The lithographic process is repeated prior to evaporation.
A metal stack of 10 nm/140 nm of Ti/Au is evaporated, without annealing, to create the
Schottky barrier for the gate contact. A SEM image of completed fabrication of a planar GaAs
nanowire MESFET is shown in Figure 6.2.

Previously, device results have been reported for MESFETs [94] using planar GaAs
$<110>$ nanowires on semi-insulating-GaAs (100) substrates as the channel. In this dissertation
we demonstrate MESFETs utilizing $<100>$ planar nanowires on a GaAs (110) substrate to
prove their viability as a FET device channel and compare them to fabricated GaAs $<110>$
nanowires. Figures 6.3 and 6.4 show the DC characteristics of a depletion mode MESFET with
an n-type Si doped $<100>$ planar nanowire as the channel with a gate length, $L_g$ of $\sim$ 2 µm. The
family of $I_{ds}$-$V_{gs}$ curves exhibits a linear region, onset of pinch-off, and saturation as shown in
Figure 6.3, indicating well defined channel modulation behavior. The transfer characteristics
($I_{ds}$-$V_{gs}$) in Figure 6.4 is shown for $V_{ds}$ values in the range of 0.25 to 1.5V, with the semilog plot
of the same type shown in the inset. The $I_{on/off}$ ratio of the device is $\sim$ 1246. Further increases
of $I_{on/off}$ are expected with improved device isolation and reduction of parasitic deposition on
the substrate. The subthreshold slope (SS) is 182mV/dec and the threshold voltage is -1.135 V
taken at $V_{ds}$ of 100 mV. The maximum drive current, $I_{ds-max}$ at $V_{gs}$ of 0 V is 78.1 µA/µm; the
transconductance, $g_m$, is shown in Figure 6.5 with maximum $g_m$ at 36.5 µS or 103.69 mS/mm,
where the base width of the nanowire (base, top and height dimensions are 378 nm, 135 nm,
and 122 nm) is used for dimension normalization. Dozens of devices were tested and
nanowires of similar base widths showed comparable device performance.
To gauge the relative performance of GaAs <100> planar nanowire MESFETs, planar nanowire MESFETs using <110> nanowires were fabricated for comparison. Growth conditions and fabrication process steps were identical between the different substrates to minimize variation due to processing differences. Figures 6.6 and 6.7 show the DC characteristics of a selected device from multiple devices on GaAs (100) samples with Lg of ~ 2 µm. The SS of this device is approximately 224 mV/dec with an I_on/off ratio of the device of 1442. The threshold voltage of -1.654 V was taken at Vds of 100 mV. The dimensions of the selected nanowire are 503 nm base width, 220 nm height and 190 nm top width. The maximum drive current Ids-max is 61.63 µA/µm taken at Vgs of 0 V. In Figure 6.8 gm is plotted and found to have a maximum of 21.3 µS or 42.34 mS/mm. The DC characteristics of the <100> nanowire MESFET on (110) substrates demonstrated previously are comparable to the control devices grown on (100) substrates. This confirms that <100> planar nanowires grown on (110) substrates are just as viable as <110> nanowires on (100) substrates for MESFET devices, yet with better manufacturability for array based channels as a result of unidirectional growth.

In addition to testing device performance, device data was used to perform a simulation to calculate the doping concentration and mobility of a <100> planar nanowire MESFET. The simulation utilizes the finite element method (FEM), because of the unique trapezoidal geometry of the nanowire, to solve Poissons equation at the onset of pinch-off to find the concentration of ionized donors, Nd. The value of Nd is then utilized to calculate the electron mobility, µn, in the channel. More in-depth details of the simulation can be found elsewhere [94]. Utilizing the same nanowire selected for the <100> MESFET, before gate deposition, two terminal measurements were taken (results are shown in Figure 5.1 of Chapter 5) to calculate the resistance per unit length of the nanowire, which was found to be approximately 3.77 kΩ/µm. Next, the Schottky barrier height is extracted from the Igs-Vds curve (illustrations of the
Schottky barrier band diagram and the Igs-Vds curve are shown in Figure 6.9) and found to be approximately 460 mV. Using extracted parameters from the DC measurements of the MESFET, a simulated ionized donor concentration of $3.45 \times 10^{17} \text{ cm}^{-3}$ was determined. Taking the simulated donor concentration, a simulated Ids-Vds plot was generated and then a value $\mu_n$ was used as a fitting parameter to match the simulated curves to real measured data of the device. Figure 6.10 shows the comparison of the simulated family of curves to the measured curves, when $\mu_n$ is set to $4563 \text{ cm}^2/\text{V}\cdot\text{s}$. Good agreement is found between simulated and measured IV-curves. The value of $\mu_n$ reveals that <100> nanowires do indeed have bulk-like mobility which is indicative of their excellent material quality.

6.2 Planar Multi-Nanowire Array Devices

As-grown planar multi-nanowire array devices and circuits are the ultimate testament of their unique geometry and epitaxial nature; additionally it is also a demonstration of the planar nanowires compatibility with conventional CMOS process techniques. The process to fabricate multi-nanowire based MESFET circuits requires the combination of MESFET processing procedures with the electron beam lithography patterning outlined in Chapter 4. The main difference for multi-nanowire devices is that contact regions were defined using electron beam lithography with a PMMA resist instead of using contact photolithography. To maximize yield, unique patterns are generated with EBL instead of relying on arbitrary contact placement. Additionally Au nanowire seeds were intentionally placed lithographically, not randomly dispersed as with aforementioned MESFETs reported. All multinanowire devices/circuits mentioned in this section use identical growth conditions mentioned in Section 6.1 for <100> planar nanowires on GaAs (110) substrates.

Figure 6.11a shows the circuit diagram of a class A inverting amplifier in the common-source configuration representing an actual fabricated circuit using two n-type planar GaAs <100> nanowires. Instead of a typical pull-up resistor connecting $V_{DD}$ to the drain of the input
drive transistor, \( Q_2 \), a depletion load transistor, \( Q_1 \), is utilized. Since the gate of \( Q_1 \) is connected to its source, \( V_{gs,Q1} \) is 0 V, the transistor is active at all times. Depletion load allows us to have a proper resistance value to drop the output, \( V_{out} \), low when \( Q_2 \) enters the triode regime. Using a depletion load transistor allows us to simply use a MESFET without having to create a specific valued resistor, which can be challenging since nanowire dimensions and doping corporation depend on the size of the Au seed which is sensitive to process variations. Figure 6.11b is a SEM micrograph of the fabricated amplifier with terminals labeled.

Figure 6.12 shows the output curve of \( V_{in} - V_{out} \) of the multi-nanowire amplifier. The amplifier shows excellent peak gain of \( \sim 117 \text{ V/V} \), which is nearly an order of magnitude higher than traditional MESFET inverting amplifiers [95]. This is a result of a high output resistance, \( r_o \), of our nanowire MESFETS which is directly related to the channel length modulation factor, \( \lambda \), which is \( \sim 0.029 \text{ V}^{-1} \), which is roughly an order of magnitude lower than typical MESFET values [95]. The low value \( \lambda \) implies that the drain has a lower impact on increasing the channel length with increasing \( V_{ds} \) as a result of the geometry of planar nanowires. This circuit design can be modified into a logic inverter with the inclusion of additional diodes (Schottky diodes are suitable and can be doped unipolar n-type for easy fabrication) to ensure the output and input have similar ranges to allow the logic to cascade to different logic gates. While the amplifier is a simple circuit, it demonstrates the potential use of multiple nanowires in a circuit, as-grown with the use of conventional CMOS processing.

6.3 Planar Nanowire p-n Junction

Lateral junctions have been a growth challenge that has been difficult to demonstrate experimentally. The ability to create monolithic junctions laterally would allow for extra degrees of freedom for growth structures and device design without dramatically increasing the cost. Monolithically grown lateral p-n junctions are virtually impossible to make with traditional thin
film growth techniques. Non-monolithic advanced growth and fabrication techniques such as selective area epitaxy and ion implantation combined with etching techniques could be used to create lateral p-n junctions but with much difficulty and increased processing steps. Imprecise junctions and processing damage diminish device performance and reduced quality of subsequent regrowth. Planar nanowires offer a unique and interesting opportunity to create lateral p-n junctions utilizing the VLS mechanism to control doping incorporation along the axis of the nanowire.

Monolithic lateral p-n junctions in planar GaAs (100) planar nanowires are realized utilizing a simple approach. Au nanoparticles (250 nm) are distributed across the surface of a GaAs (100) substrate by evaporating an aqueous Au colloidal solution at 115 °C. Annealing takes place at 625 °C for 10 min under constant AsH₃ flow of 3.71 x 10⁻⁵ mol/min (83 sccm) mol/min; the temperature is lowered to 460 °C where growth commences. TMGa and Si₂H₆ are turned on simultaneously to begin the growth of the n-type segment. Constant flow rates of 1.86 x 10⁻⁴ mol/min (10 sccm) of TMGa and 3.57 x 10⁻⁶ mol/min (400 sccm) Si₂H₆ are introduced continuously for 90 s at a Si/Ga gas phase ratio of 3.12 x 10⁻² and V/III ratio of 31.6. After completion of the N-Type segment, Si₂H₆ is switched off and DMZn is switched on while the TMGa flow rate is kept constant to begin the p-type segment. DMZn is flown at a low rate of 4.85 x 10⁻⁷ mol/min (0.1 sccm) with a Zn/Ga gas phase ratio of 4.14 x 10⁻³ to now dope the nanowire p-type without introducing any unwanted morphological changes. The p-type segment was grown for 90 s as well, leading to an approximate length of ~14 µm with a growth rate of ~75 nm/s. After growth, samples are sonicated in methanol for 2 minutes to remove any non-planar nanowires. Prior to metallization, the samples are subjected to a slight etch in a solution of 1:8:80 H₂SO₄:H₂O₂:H₂O for 4 s to remove the thin highly doped parasitic VPE layer. Patterns of 20 x 20 µm² pads are lithographically opened in an AZ5214 photoresist layer and the opening is cleaned using a 1 minute 300 W O₂ plasma. A 15 s dip into 1:1 HCL:H₂O
is used to remove any oxide generated by the plasma. Ohmic n-type metals are evaporated first because of a subsequent annealing step. A thin film metal stack consisting of 20 nm/50 nm/30 nm/50 nm of Ge/Au/Ni/Au is deposited then lifted off in an agitated acetone bath for 5 minutes. A 15 s anneal at 400 °C is used to alloy the metal film to reduce contact resistance.

After annealing, the lithography process is repeated and an identical pattern is created for p-type ohmic contacts. A metal stack consisting of 10 nm/140 nm of Ti/Au is evaporated, and lifted-off in acetone without subsequent annealing. Figure 6.13 shows the final result after processing is complete; by visual inspection it is clear to see that each segment is covered by the appropriate contact metal and the approximate location of the junction by the onset of periodic twinning of the p-type segment. Currently, with this process, yield is quite low from the combination of a few undesired effects. Theoretically, maximal yield of p-n junction <110> nanowires on GaAs (100) is 50% because of the bi-directional growth; it is critical that each doped segment is contact by the appropriate metal to prevent the formation of a Schottky barrier at the metal-semiconductor junctions. To reduce processing time and cost, nanowires and contacts are randomly distributed, further reducing the yield. Additionally, natural defects such as non-ideal nanowire growth, improper doping incorporation and processing error also reduce the yield. Nevertheless, monolithic lateral p-n junctions on GaAs (100) have been demonstrated using <100> planar GaAs nanowires.

Electrical testing of the p-n junction is shown in Figure 6.14. Figures of merit of the p-n junction are extracted by examining the Shockley ideal diode equation:

\[ I_D = I_S \left( e^{V_D/nV_T} - 1 \right) \tag{6.1} \]

where \( I_S \) is the saturation current (3.81903\(^{-15}\) A), \( V_D \) is the applied bias across the junction, \( n \) is the ideality factor, \( V_T \) is the thermal voltage (\( V_T = (k_B*T)/q \approx 26 \text{ mV at room temperature (300 K)} \)). Extrapolating the exponential part of \( I_D \) back to the x-axis we can determine the turn-on voltage of the diode is approximately 1.18 V. Taking the exponential term to be \( >> 1 \) (valid for
$V_D > 500 \text{ mV at } 300 \text{ k} \), we can drop the -1 and take the slope of the semilog plot, as shown in Figure 6.15 of $\ln(I_D)$ vs. $V_D$ to extract $n$, the ideality factor and use the intercept to calculate $I_S$. The ideality factor is determined to be around 2.13 from the linear region before the nanowire becomes resistive after the bands align. An ideality near 2 indicates that a larger amount of the current is due to recombination instead of diffusion. This is most likely the combination of an imperfect junction due to the reservoir effect \cite{51}, radiative recombination and increased surface recombination due to increased surface to volume ratio of the nanowire, which is typical for unpassivated nanowire p-n junction diodes \cite{48}. The ideality factor can be improved by passivating the GaAs nanowire surface to reduce surface states. Planar nanowire p-n junctions also offer an impressive rectification ratio of nearly $10^6$ measured at ± 2 V bias.
6.4 Figures

Figure 6.1 Illustration highlighting process steps to fabricate a GaAs planar nanowire MESFET. 1) Au nanoparticles are dispersed on GaAs substrates. 2) MOCVD growth is performed to grow n-type nanowires via the VLS mechanism. 3) Photolithography is used to define source and drain regions and a metallic stack of Ge/Au/Ni/Au is deposited. 4) Source and drain contacts are annealed to form AuGeNi ohmic contacts to n-type GaAs. 5) The gate region is defined by photolithography and a stack of Ti/Au is deposited to form the Schottky gate contact.
Figure 6.2  SEM micrographs of a fabricated planar nanowire MESFET. (Top) A wide view of the MESFET patterned metal regions sans nanowire; (S)ource, (D)rain, and (G)ate contacts are labeled. (Bottom) Zoomed in view of a GaAs planar nanowire bridging metallic contacts as a MESFET channel.
Figure 6.3 Family of curves, $I_{ds}$-$V_{ds}$, of a GaAs <100> planar nanowire MESFET. $V_{ds}$ is swept from 0 V to 3 V while $V_{gs}$ is stepped from -2 V to 0 V with 250 mV steps. Maximum drain current was found to be 78.1 µA/µm at $V_{gs} = 0$. 
Figure 6.4 Transfer characteristic, $I_{ds}-V_{gs}$, of a GaAs <100> planar nanowire MESFET. $V_{gs}$ is swept from -1.3 V to 0 V while $V_{ds}$ is stepped from 0.25 V to 1.25 V with 250 mV steps. A $V_{th}$ of -1.135 with SS of 182 mV/dec was extracted from this device.
Figure 6.5 A plot of the transconductance, $g_m$ of a GaAs <100> planar nanowire MESFET.

Maximum $g_m$ was found to be 36.5 $\mu$S or 103.69 mS/mm taken at $V_{ds} = 1.25$ V.
Figure 6.6 Family of curves of a GaAs <110> planar nanowire MESFET. $V_{ds}$ is swept from 0 V to 3 V while $V_{gs}$ is stepped from -2 V to 0 V with 250 mV steps. Maximum drain current was found to be 761.63 µA/µm at $V_{gs} = 0$. 
Figure 6.7 Transfer characteristic, $I_{ds}$-$V_{gs}$, of a GaAs $<110>$ planar nanowire MESFET. $V_{gs}$ is swept from -1.3 V to 0 V while $V_{ds}$ is stepped from 0.25 V to 1.25 V with 250 mV steps. A $V_{th}$ of -1.654 with SS of 224 mV/dec was extracted from this device.
Figure 6.8 A plot of the transconductance, $g_m$ of a GaAs $<110>$ planar nanowire MESFET.

Maximum $g_m$ was found to be 21.3 $\mu$S or 42.34 mS/mm taken at $V_{ds} = 1.25$ V.
Figure 6.9 (Top) Band diagram illustrating a metal-semiconductor junction where there is a mismatch of the work function of the metal and the sum of the electron affinity and the Fermi level of an n-type semiconductor ($\Phi_m > (\chi + E_F)$). (Bottom) Two terminal I-V measurement of the Schottky gate diode, $I_{gs} - V_{gs}$, of a planar GaAs $<100>$ nanowire MESFET. The extracted Schottky barrier height was found to be $\Phi_m = 460$ mV.
Figure 6.10 Comparison of simulated and measured family of curves of a planar GaAs <100> nanowire MESFET where $N_d = 3.45 \times 10^{17}$ cm$^{-3}$ and $\mu_n = 4563$ cm$^2$/V·s was used to fit the curves. Good agreement was found between the curves indicating high material quality.
Figure 6.11 a) Schematic of a simple inverting amplifier where $Q_1$ is a depletion mode N-channel planar GaAs nanowire MESFET and $Q_2$ is the drive transistor. $V_{DD}$ is set to 6 V. b) SEM micrograph of a top-down view of the multi-nanowire inverting amplifier.
Figure 6.12 Output curve of an inverting amplifier using planar GaAs nanowire MESFETs. A high peak gain of ~117 V/V was found as a result of the high output resistance of the nanowires.
Figure 6.13 SEM micrograph of a planar GaAs nanowire p-n junction. The p-type segment is easily visible by the characteristic twinning super lattice in contrast to the smooth facets of the n-type segment.
Figure 6.14 I-V characteristic, $I_D$-$V_D$, of a p-n junction planar GaAs $<110>$ nanowire diode.

Turn on voltage was extracted at a forward bias of 1.18 V.
Figure 6.15 Semi-log plot of a p-n junction planar GaAs <110> nanowire diode. An ideality factor of 2.13 was extracted from the linear portion of the curve during forward bias. A high rectification ratio of nearly $10^6$ was measured at $V_D = \pm 2V$. 
CHAPTER 7 - FUTURE DIRECTIONS FOR PLANAR NANOWIRES

7.1 Annealing Intolerability

Thin film annealing and regrowth of films is a standard technique in MOCVD growth to achieve high quality surfaces, activate dopants and to create patterned heterostructures. In attempts to anneal the planar nanowire crystal facets of n-type doped nanowires, it was apparent that nanowires lost all conductivity for even short anneal durations and conservative temperatures. Nanowires that could normally conduct µA currents for ± 2 V biases are now conducting in the pA range. Initially the source of conductivity loss was unclear; however a few potential possibilities were explored.

One possibility was that that most of the dopants lie along the outer radial edges and during high temperature treatment the out atoms rearrange and/or dopants simply diffuse out. However, attempts at protecting the surface of the nanowire using protective oxide proved unsuccessful at preventing conductivity loss. Furthermore, given the low annealing temperatures (600 °C) and durations (∼ 1 min), the out diffusion of Si atoms seems unlikely.

Another scenario investigated was the possibility of the migration of substrate traps into the nanowire itself from the epitaxial connection. Semi-insulating GaAs substrates are usually doped with deep level traps [96] such as Cr and O, which could potentially migrate into the nanowire trapping the majority of the carriers. An experiment was performed to see if growing thick buffer layers could prevent conductivity loss. A 1 µm buffer layer was grown on GaAs (100) substrate with nanowire growth subsequently grown on top, then subjected to a 1 min (anneal time is count down from when anneal temperature is reached), 600 °C anneal. Multiple samples were prepared to test the anneal at various stages of the growth and regrowth process.

Figures 7.1 and 7.2 outline the results of the experiment. Even with utilizing a buffer layer nanowires still lost conductivity and even the buffer layer itself became not conductive after the anneal. It is very unlikely that impurities from the substrate would be able to diffuse so
far in such a short period of time at a low temperature. Recently researchers have found out carbon incorporation, from the methyl groups attached to metalorganic precursors, is surprisingly high in InP VLS nanowires [97]. It is possible that the anneal activates C atoms in the lattice, which effectively compensates the intentional doping from the Si atoms. Carbon is typically activated through low temperature anneals post film growth to activate the dopants [98]. Nevertheless, solving the annealing intolerability of planar nanowires is paramount to utilize doped nanowires with any high temperature treatment.

### 7.2 Interaction between Planar Nanowires and Thin Films

As mentioned in Chapter 4, planar nanowires are in a unique growth regime where they are always within a diffusion length of Ga adatoms diffusing along the substrate surface when compared to vertical nanowires (Figure 7.3). In addition to the aforementioned ramifications of constant diffusion, planar nanowire growth can be easily combined with thin films. Miao et al. demonstrated that GaAs planar nanowires could be covered in a thin film of AlxGa1-xAs and utilize the difference in depletion widths generated from the SI substrate and the nanowire body to create a high electron mobility transistor (HEMT) using the nanowire as the active channel [62]. While covering nanowires in VPE growth (i.e. core-shell structures) has been investigated extensively, combining thin film growth of planar nanowires with selective advanced thin film growth techniques is easily achievable with the planar system. Selective area epitaxy (SAE) is a growth technique where a lithographically defined, non-reactive hard mask, usually a dielectric such as SiO$_2$ or SiN$_x$, is used to create regions of encouraged and disallowed growth [99]. Essentially, this is a bottom-up approach to defining expitaxial thin films, instead of the top-down method of etching a film to intended dimensions post-growth. The control of deposition is a result of the difference of diffusion lengths of adatoms across the different surfaces, i.e. GaAs (100) and SiO$_2$. 
A secondary effect of the increased diffusion along the SAE mask is an increased growth rate along the edges of the mask known as growth enhancement. Growth enhancement depends on the local ratio of covered to uncovered areas: for example, take a sample with a 1 \( \mu m^2 \) pad opened in oxide the center with on-oxide diffusion lengths on the order of 10^2 \( \mu m \) and compare it to a sample with an area of 100 \( \mu m^2 \) of oxide; the second sample will experience far more grown enhancement than a sample with only 10 \( \mu m^2 \) of surrounding oxide. Growth enhancement can be utilized to create regions of high adatom concentration which can be harnessed to control the rate of planar nanowire growth. Figure 7.4a outlines how to locally control the growth rate of individual nanowires by adjusting the adjacent coverage of masked regions surrounding the nanowire. Nanowires with thick surrounding coverage should grow faster from an increased local precursor surface adatom concentration; areas with thinner or no coverage would grow much slower. Additionally it may be possible to control local doping concentration and alloy percentage (in heterogeneous systems) by exploiting different adatom diffusion lengths on various mask surfaces. The potential detriment of parasitic VPE was highlighted in Chapter 5, however SAE could be utilized to locally prevent deposition of parasitic VPE around the nanowire through careful patterning in the selective mask. Figure 7.4b illustrates the potential use of a SAE mask to prevent such growth.

In addition to utilizing growth enhancement, selective growth of epitaxial films can be grown in-plane directly on as-grown nanowires. The full registry with the crystal substrate and the well-defined crystal facets allow planar nanowires to be fully integrated with thin films. Quality epitaxy on vertical nanowires can only occur on their growth substrate; once they are transferred to a host substrate, the lack of registry will create anti-phase related defects. Preliminary work has been completed on integrating selective area thin films on (100) GaAs planar nanowires. Figure 7.5 illustrates the process to create selective thin films on top of planar nanowires. First, planar nanowire growth is carried out with growth conditions (colloid size,
doping type/rates) specific to the intended application. After growth, all non-planar nanowires are removed. Subsequently, a 20 nm plasma enhanced chemical vapor deposition (PECVD) SiO$_2$ film is deposited on top of the substrate. Patterns of 20 x 20 μm$^2$ regions are opened in the oxide mask with a Transene™ buffered hydrofluoric acid etch (800 Å/min listed etch rate) to designate regions of enhanced growth. A 1:1 HCL:H$_2$O oxide etch is performed before regrowth. During regrowth, slow growth rates are preferable for good morphology and to offset the faster growth rate imposed by growth enhancement. After growth, the hard mask is removed leaving behind a selective epitaxial film over the top of the nanowires.

Figure 7.6 shows top and side views of intrinsic GaAs grown on top of the nanowires, showing great coverage and good crystalline quality in the SAE regions. SAE regions can be doped to create or enhance electrical devices. For example, with an n-type nanowire and p-type SAE regions, one can create a PNP device (BJT) or regrow n$^+$ SAE regions over the top of an n-type wire to reduce contact resistance for FETs or other electrical devices. Prototypes of these devices were fabricated (Figure 7.7); however the planar nanowire annealing intolerability rendered the nanowires depleted. Until the annealing intolerability is remedied, using planar nanowires as the active electrical part of a regrown structure is not possible and the use of high temperature treated planar nanowires is structural or passive at best (i.e. planar nanowire HEMT).

### 7.3 Lateral Heterojunctions, Hetero Epitaxy and New Material Systems

Planar nanowire research has been primarily performed on GaAs [62, 63, 87, 94, 100] with planar-like growth reports with other material systems was well [101]. The expansion of planar nanowires to other material systems is a rich area waiting to be explored. The concept of new materials can be expanded beyond simply the homoepitaxy of planar nanowires; heteroepitaxy of planar nanowires (between the nanowire body and the connecting substrate) and the introduction of lateral heterojunctions. The incorporation of heterogeneous materials
into planar nanowires will prove challenging. The problem is twofold: (1) incorporation of material into the catalyst and (2) epitaxial compatibility between the nanowire and its host substrate. It can be difficult to incorporate additional materials into the Au catalyst after it has already been saturated. Additionally, there is minimal information for the ternary Au-X-X phase system for elements of interest for nanowires, even more so for the temperatures suitable for nanowire growth. Second, while vertical nanowires are championed for their ability to accommodate more strain than 2D films [51], planar nanowires have to take account of its epitaxial connection along the length of its axis. Even if the heterojunction can withstand the lattice mismatch without generating misfit dislocation, it may not be the same for the substrate interface. Figure 7.8 shows examples of different types of potential heterojunctions for planar nanowires. The realization of heterojunction planar nanowires will lead to development of devices such as heterojunction bipolar transistors (HBT), tunneling FET (tFET), resonant tunneling diodes, and embedded quantum dots.

### 7.4 Planar Nanowire Modeling

Nanowires provide interesting modeling and simulation opportunities in research and academia. Their one-dimensional geometry combined with the VLS growth mechanism and related phenomena [60, 102] require new simulations and modeling to elucidate the underlying mechanisms. This holds true even more so for planar nanowires where even newly found theory for VLS nanowires needs to be adapted or even reformulated for planar nanowires. One particular instance is related to the growth facets for planar nanowires. The TEM work performed by Fortuna et al. [45] revealed unique crystal facets at the liquid-solid interface for planar nanowires as shown in Figure 7.9. While it has been confirmed that the $<111>B$ crystal plane is the plane where growth (nucleation of new crystal layers) occurs [87], the role of the other facets is still to be determined. Uncovering the role of these facets would provide better understanding of the mechanism of planar growth mode. In addition, the nucleation plane for
planar nanowires is not parallel to the growth direction (Chapter 4) of the nanowire when compared to out-of-plane wires. An interesting consequence is the modeling of hetero- and p-n junctions within planar nanowires. Figure 7.10 shows theoretically the physical location of ionized donors and acceptors within a <110> GaAs planar nanowire. Modeling the band structure and/or charge distribution as a function of position along the axis of the nanowire is unique and could prove to be interesting.

7.5 Multi-Junction Light Scatterer

Efficient light scattering for solar applications has been a growing area of research for energy harvesting [103-105]. Two of the main routes for efficiency loss in solar cells are from carrier recombination and inadequate absorption. One of the methods to improve absorption is to lengthen the optical pathway, the path a photon takes inside of a material, for an increased chance of absorption. One method to lengthen the optical pathway is to scatter the light, and change the angle of incidence and force the light to enter the material at a shallower angle. Nanowire arrays have been demonstrated as strong light scatterers, however solar cell designers often use the nanowire as the active material as well. Nanowires suffer from having extreme surface to volume ratios which cause rampant surface recombination and outweigh the benefits of the increased absorption. Planar nanowires however, could be utilized as passive light scatterers by texturizing the surface of a semiconductor solar cell as they should be excellent Mie scatterers. Mie scattering is when light scatters off an object that is on the same order as the incident wavelength of light. It was found recently that Mie scatterers are not only effective at scattering the light, but also have a tendency to directly couple light into the layer they reside upon [106]. Figure 7.11 highlights how planar nanowires could be integrated into solar cell: assuming a multi-junction solar cell, homoepitaxy of nanowires can be grown at the interface between each cell with dimensions and have patterned spacings targeting the absorption of the cell below it. The well-defined crystal facets allow for easy regrowth while CMP can be used to
planarize the films at each step between cells. The overall result combines the effectiveness of Mie scattering, while minimizing the increased surface area for each cell, not just the topmost cell.
Figure 7.1 Two terminal I-V curves showing the effect of annealing on the background of the buffer layer with no nanowires present. The loss in conductivity in the buffer layer after the anneal is a result from parasitic VPE deposited on the surface during the nanowire growth.
Figure 7.2 Two terminal I-V curves showing the effect of annealing on the conductivity of the n-doped nanowires. Nanowires that previously conducted in the μA range, lose nearly $10^4$ orders of current loss after annealing, rendering them insulative.
Figure 7.3 An illustration highlighting the difference of growth regime between vertical and planar nanowires. Planar nanowires experience surface adatom diffusion throughout their entire growth.
Figure 7.4 a) An illustration highlighting the potential use of oxide strips to locally control the growth rate of planar nanowires which would have been grown for the same identical length of time. b) An oxide mask could be used to prevent parasitic VPE growth in the surrounding area of a planar nanowire.
Figure 7.5 An illustration demonstrating the fabrication procedure to create SAE thin films over the top of planar nanowires.  

a) Planar nanowires are grown and subsequently, b) an oxide layer is deposited and lithographically defined. c) Regrowth occurs in the opened regions of the mask and then d) the mask is stripped and metal contacts are placed as desired. e) A side view of the finish device.
Figure 7.6 a) Angled and b) top view of GaAs regrowth on top of a $<110>$ GaAs planar nanowire.
Figure 7.7 Angled view of multiple nanowires spanning SAE regrowth with metal pads placed on top.
Figure 7.8 Potential heterostructures for planar nanowires such as a) InAs-GaSb tunneling junction and b) GaAs-InGaP HBT.
Figure 7.9 TEM images of the growth interface of GaAs nanowires on (100) revealing multiple interfaces between the nanowire and the Au seed. Adapted with permission from [1]. Copyright 2008 American Chemical Society.
Figure 7.10 a) Illustration of a p-n junction nanowires. b) Zoomed-in view of the angled junction that would occur within an abrupt p-n junction of a planar nanowire. The angle is a result of the growth plane relative to the GaAs (100) surface. c) Profile of ionized carrier concentrations along the axis of the nanowire. Even if the junction is abrupt, there is an overlap of the n and p regions relative to the nanowire body.
Figure 7.11 Illustration of using arrays of planar nanowires at each cell junction as a specific spectrum absorber for the targeted cell. Light is incident from the top of the cell.
CHAPTER 8 - SUMMARY

Planar nanowires are a potential solution to the industrial scaling issues that currently effect conventional out-of-plane nanowires. In this dissertation, we have demonstrated the growth of planar GaAs nanowires on GaAs(100), GaAs(110), and off-cut GaAs substrates. Using visual analysis and x-ray microdiffraction, we were able to elucidate the crystal facets and growth directions of planar nanowires grown on these substrates. We have found the main contributing factor to determining for planar nanowire growth direction is the relationship between the <111>B crystal direction, the common low energy growth direction for nanowires, and the growth substrate surface. Planar projection theory can be used to determine the planar nanowire growth direction by projecting the direction normal to the nucleation plane (<111>B in most cases) onto the surface of the substrate. Good agreement was found between experimentally found and calculated growth directions for (110) and off-cut substrates. A theoretical model was developed to determine the role of the diffusion of surface Ga adatoms on the planar GaAs nanowire growth rate. The model indicates that growth rate is not a function of the length of the growing nanowire, but a constant growth rate depending on growth conditions alone. GaAs nanowires were successfully patterned into arrays unidirectional nanowires using electron beam lithography with an extensive cleaning procedure. Relative planar nanowire growth direction was also perturbed by introducing obstacles in its growth path, altering its course.

The doping of planar GaAs nanowires was investigated for both n-type and p-type. N-type doping was found to be relatively uniform with little variation along the length of the nanowire. There was also minimal incorporation into the forming parasitic thin film that forms with planar nanowire growth. P-type doping of planar nanowires, with both Zn and C precursors, was used to induce twinning superlattices in planar GaAs nanowires. The twinning period was determined primarily to be a function of the Au seed diameter. The twinning
period is modulatable by adjusting gas flows during the nanowire growth. The heavily doped parasitic VPE layer that forms with Zn p-type planar nanowires was removed with a light chemical etchant and two-terminal I-V curves were taken to estimate the approximate doping concentration at specific precursor flows. At high dopant/Ga ratios, planar nanowire growth was disrupted and the formation of crawling growth modes (C doping) and pyramidal structures (Zn doping) was observed.

Finally, functional electrical devices were demonstrated utilizing planar nanowires as the active device. N-channel depletion mode MESFETs were demonstrated with planar GaAs nanowires used as the channel. Fabrication steps are thoroughly explained and performance results are discussed and compared between \(<110>\) and \(<100>\) devices. A simulation was performed to estimate the n-type doping and mobility in a selected device. A multi-planar nanowire based inverting amplifier was fabricated and demonstrated with good voltage gain. Also, a lateral nanowire p-n junction was fabricated with a high rectifying ratio.

Future directions for planar nanowires were outlined with clear steps for moving forward. Initial results were presented with integrating planar nanowires with SAE thin films. The issue of annealing intolerability is discussed while hypothesizing on the source of the conductivity degradation. Modeling opportunities for planar nanowires are discussed including thermodynamic nucleation modeling and angled junctions. Further discussion on planar nanowire heterostructures beyond p-n junctions and the passive use of planar nanowire within optical devices such as solar cells is discussed.

Planar nanowires are a promising modification of VLS nanowire growth - their conventional process compatibility, controllable growth direction, and high material quality make them attractive for electrical and optical devices. The further investigation of planar nanowires may potentially uncover new physics and phenomena while better understanding of the VLS mechanism.
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