PREDICTIVE TRANSIENT CIRCUIT SIMULATIONS OF CHARGED DEVICE MODEL
ESD EVENTS IN SYSTEM IN PACKAGE CHIPS

BY

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DISSERTATION

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ABSTRACT

This thesis focuses on obtaining circuit models to simulate the voltage stress experienced by the devices on integrated circuit components stressed by the charged device model (CDM) electro-static discharge (ESD) testers. The thesis presents a simple package modeling methodology that can be used to create a distributed model to simulate the voltage stress across internal circuit nodes or a lumped model that can be used to study the CDM reliability of primary input/output circuits on the chip. This thesis shows that three-dimensional (3D) EM simulation based package models may not be necessary, and that reasonably accurate results can be obtained using a simple 2D package extraction method. A method to model the on-die circuits and parasitic resistances of the power/ground busses is also presented.

The circuit simulations were used to (a) study domain crossing circuits in single and multi-die packages, (b) study inter-die interface circuits in the stacked die and 3D integrated circuits (3DICs) that use through-silicon vias (TSVs), and (c) estimate the peak CDM discharge current for any integrated circuit component with minimal knowledge of on-die circuits. Both the simulations and measurement results are presented in this document. The simulation results agree with the measurement results from several test chips. Therefore, the methods presented in this thesis may be used to perform circuit simulations on an integrated circuit component model before the chip is manufactured to optimize the ESD protection network, or to find ESD weaknesses in the integrated circuit.

This thesis shows that it is not necessary to use full sized ESD protection circuits at the domain crossing circuits and inter-die interface circuits. Small, secondary voltage clamps are
sufficient if the primary current-carrying paths such as the ground and power nets are designed properly. Guidelines are provided for the design of power and ground nets and the size of the protection circuits to be used at the domain crossing circuits and the inter-die interface circuits.
To My Mom Arya Shukla and Late Dad, Gurudatt Shukla
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1. INTRODUCTION

Electrostatic discharge (ESD) is the transfer of static charges between objects at different electric potentials [1]. Static charges are generated due to tribo-electric charging, ionic charging, direct charging or field-induced charging [2]. Discharge of static charges into or out of integrated circuits (ICs) can damage the internal circuits and render them unusable or degrade their performance. As the physical dimensions of the devices in the ICs are scaled down to increase the operating speed and decrease the area, the devices are becoming increasingly susceptible to damage resulting from ESD events. Therefore, three samples of a given IC are tested in the laboratory for ESD robustness at a stress level requested by the customer before delivering the ICs to them. This procedure is referred to as ESD qualification. Various models are used to simulate the ESD events that the IC may experience in the real environment. The human body model (HBM) [3], machine model (MM) [4] and charged device model (CDM) [5] are the three component level ESD test models that are used by the IC vendors. Today, IC handling is highly automated and thus CDM is the most relevant of the component-level ESD tests [3], [5]. Two types of CDM tests are used in the industry: socketed CDM (SCDM) and field-induced CDM (FICDM). A majority of the electronic industry today performs the CDM qualification tests using the FICDM method because it is a better representation of the CDM events in the real world [6]. Therefore, the work presented in this thesis focuses on modeling the FICDM events on the integrated circuits.

1.1 Charged Device Model ESD Test

During an FICDM test, a packaged chip, called a device under test (DUT), is placed upside-down on a field plate as shown in Figure 1.1. The field plate potential is raised to a
predetermined pre-charge voltage and then a pogo pin, which is attached to a ground plate, is lowered until it makes contact with a pin of the DUT. Charge flows through the pogo pin to the DUT in order to support the potential difference between the grounded component and the field plate. In reality, the discharge event starts even before the pogo pin makes contact with the DUT pin due to the spark created by the large potential difference between the pogo pin and the DUT pin. The charge flows through the lowest impedance paths that lie between the “zapped pin” and the charge storage sites throughout the component. This results in a high current stress as shown in Figure 1.2.

![Figure 1.1](image.png)

Figure 1.1 Packaged component placed upside down on the field plate of an FICDM tester. A thin insulator separates the field plate and the component. A pogo pin attached to the ground plate is lowered to make contact with each pin of the component one at a time.

There are two ways to apply the negative stress on the DUT. In one of the methods, the pogo pin is raised and returned to its original position. The DUT is still charged. The pre-charge voltage on the field plate is then reduced to 0 V. The potential difference between the field plate and the DUT is still 500 V and the DUT is now essentially at -500 V. A stress of negative polarity is then applied by bringing the pogo pin down to make contact with the device pin. The charge leaves the device to bring the DUT potential to 0 V.
Another way to apply the negative stress on the DUT is to slowly bring the potential on the field plate to 0 V with the pogo pin still in contact with the DUT. The charge on the DUT slowly bleeds away into the ground. The pogo pin is then raised to its original position. Now, the potential on the field plate is slowly brought to -500 V. The pogo pin is then lowered to make contact with the DUT again. The DUT becomes positively charged and the potential on the DUT is brought to 0 V. This method helps us conduct experiments where we can separate the stress polarity (positive and negative) on the pins to conduct detailed failure analysis.

The peak current depends upon the amount of charge stored in the IC and the impedance of the discharge path. The amount of charge is determined by the total capacitance formed between the metallic parts of the IC and the field plate. The pogo pin inductance, the resistance of the spark between the pogo pin and the DUT, and the impedance of the discharge path on the chip determine the peak current for a given amount of charge storage. The DUT is characterized before and after the CDM stress. The CDM robustness of the DUT is defined as the highest pre-charge voltage that can be used to stress all the pins of the DUT without causing a failure. Although the
DUT’s CDM robustness is qualified in terms of the pre-charge voltage, it has been shown that the peak discharge current is the true indicator of the DUT’s CDM robustness [6].

**1.2 Motivation for CDM Simulation of Circuits**

The CDM test is carried out on a packaged IC. Finding the ESD related failures after fabricating and packaging an IC costs much more than finding the same issues earlier in the design cycle, and fixing them before fabrication. Therefore, it is desirable to detect the ESD weaknesses in the IC design and fix them before fabricating the ICs. In the HBM and the MM tests, the peak current for a given pre-charge voltage is known beforehand. Designers can design and place the ESD protection circuits to minimize the stress on the circuits for each stress mode. In contrast, in the CDM test, the peak current varies from design to design, depending on the size of the die and of the package. Also, unlike in the other component level tests, during the CDM test, the path of discharge cannot be easily determined. A charge storage model needs to be created to better understand the current discharge paths and the resulting potential drop they create between the circuit nodes of interest.

The CDM discharge current has fast rise time, of the order of a few hundreds of pico seconds. The rise time dictates that transient effects have to be included while analyzing the circuit reliability. Thus, transient circuit simulations are needed to study the robustness of circuits. The circuit simulations also allow the designers to measure voltages and currents at the internal nodes, a method which is not easy to implement while testing the packaged ICs. Circuit simulations allow the chip designers to conduct what-if analysis and make well-informed decisions during the circuit, package or ESD protection network re-design. Circuit simulations also allow the analysis of the root cause of any unexpected CDM failures.
1.3 Introduction to System-in-Package Technology

Speed of communication between any two chips soldered on to a printed circuit boards (PCBs) can be increased if the interconnect delay of the channel between the chips is reduced. The interconnect delay can be reduced drastically if the two chips are integrated in a single package. Multi-die packaging technologies offer several advantages:

- Enables area and weight reduction through integration of more functionality per unit area of the PCB
- Enables higher electrical performance through reduction of interconnect delay between the dies
- Reduces the system level cost through a higher level of integration of the functional components

There are several different multi-die packaging technologies today. Some of the popular packaging technologies are:

- Multi-chip-modules (MCM): Multiple chips placed side by side connected using the bondwires or wiring inside a ceramic or plastic substrate
- Stacked-die technology: Multiple dies stacked on top of each other
- 2.5-dimensional (2.5 D) packaging: Multiple chips placed side by side and connected via wiring inside a silicon interposer
- 3D Integrated circuits (3DICs): Multiple dies stacked on top of each other and connected using through-silicon-vias (TSVs) through the substrate of the dies
- Package-on-Package (PoP): Multiple packages placed on top of each other
Multi-die packages enable integration of different components of a system in one package and therefore they are also referred to as system-in-packages. This dissertation focuses on the stacked die and 3DIC system-in-packages.

3D (three-dimensional) integration refers to a family of technologies which enable the stacking of active silicon layers with vertical connections between them. These vertical connections consist of through-silicon-vias (TSVs) or micro-bumps or both. Through-silicon-vias are metal connections which go through the silicon substrate of the die, creating connections between the backside of the die and the frontside circuits on the die [7].

3D integration is an attractive approach to stay on the semiconductor productivity roadmap. The value of 3D integration lies in increasing the transistor density in a given lateral footprint with the potential benefit of shorter electrical path lengths through the use of the shorter third-dimension (vertical stacking). An additional benefit is the intimate integration of disparate technologies such as power amplifiers with digital CMOS without having to place them on the same die.

Primarily based on the bonding method, there are three approaches for 3D stacking: bonding silicon at the wafer level, joining it at the die level (which includes die to die and die to wafer bonding) or bonding multiple dies on a wafer. Each of these approaches has advantages as well as disadvantages. Within each type of bonding method, one can either join the two dies or the wafers in face-to-face (F2F), face-to-back (F2B) or back-to-back (B2B) orientation. A single stack may mix the three types of die orientations in one stack. Figure 1.3 shows a four-tier stack with the bottommost die (Die 1) connecting to the Die 2 in B2B fashion, Die 2 connecting to Die
3 in F2F fashion and finally Die 3 connecting to the topmost die, Die 4, in F2B fashion. Reviews of the various types of 3D stacking, and their advantages may be found in recent publications [8].

An important step in any type of 3D integration is the introduction of TSVs in the fabrication sequence. For wafer to wafer bonding, TSVs may be introduced after bonding and thinning. This is an example of a via-last process. However, if TSVs are introduced in the wafers prior to bonding, it would result in a via-first or a via-middle process. For die to die bonding, or die to wafer bonding, the TSVs must be introduced in the silicon long before the dies are bonded. If the TSVs are introduced very early in the fabrication sequence, before the devices are built, this would be termed a via-first process. However, for several reasons, such as the TSV form factor and the choice of metallization, it may be more beneficial to introduce TSVs during the BEOL (backend of line) fabrication, i.e. a via-middle process. It is to be noted that the point of the introduction of the TSV plays a critical role in the choice of TSV processes, including materials and temperatures used.

Figure 1.3 A four-tier stack showing both face-to-face (F2F), face-to-back (F2B) and back-to-back (B2B) configuration of die orientation.
1.4 Background Information on the Field of Research

This thesis presents a simulation model that can be used to predict CDM failures in system-in-packages. Simulation of CDM events in the integrated circuits requires modeling the plural charge storage locations and discharge paths. The charge is stored in various metallic parts of the IC, such as the conducting parts of the package and on-chip interconnect. The discharge path for each storage site may be different. The discharge path for each storage site also differs depending on the location of the zapped pin. In order to simulate the discharge current waveform, the netlist must include elements representing the package, ESD circuits and substrate [9], [10]. If full-chip modeling is undertaken, one can also simulate the CDM waveforms at power domain crossing circuits, known as internal I/Os. These circuits may be susceptible to gate oxide damage during CDM events [11], [12]. Full-chip CDM simulation to study the power domain crossing circuits was presented in [13] but the work did not include the substrate model. The impact of the substrate resistivity on the voltage stress generated at the power domain crossing circuits was studied by presented by Shukla et al. in [14]. Their work [14] presented a methodology to predict the CDM reliability issues of the power domain crossing circuits in a single die package. This dissertation presents simulation based analysis of some of the CDM induced failures in the domain crossing circuits in two single die test chips that were not explained in [14].

This work addresses the subject of CDM reliability in more complex, multi-die packages. Predictive transient circuit simulation of CDM events in stacked die and 3DICs is the subject of this doctoral research and was first presented in [15] by Shukla et al. The CDM issue for System-in-Package (SiP) designs was mentioned in [16], but the reliability risk from a CDM discharge to an integrated circuit in a stacked die package was still largely unknown until a simulation based study was reported by [15]. The circuit simulation study was later proven to be accurate by the
measurement data [17]. Both these works presented their study on a two-tier stacked die in which the tiers were connected together using bondwires. This study laid the foundation for exploring the CDM reliability of true 3DICs. CDM reliability of 3DICs is not very well understood. A simulation based study of the CDM ESD reliability of 3DICs was first presented in [18]. No measurement data is available yet. In this thesis, a 3DIC test chip design and a test plan are also presented in addition to the simulation based predictions of CDM reliability of 3DICs. The measurement data from the test chip will be used to verify the simulation results and the hypotheses made in [18].

1.5 ESD Challenges in 3DIC

3D integration technology has opened up a plethora of options in terms of functional system integration and related architecture [19]. However, no studies have been conducted to evaluate the impact on ESD reliability. Some designers have assumed that no ESD protection is needed at the internal I/O [20], but no CDM-ESD qualification data have been provided to support this approach. One design team conducted a study on the presence of ESD during TSV processing and its impact on the gate oxide of the devices. However, this study did not investigate the stress generated at either the external interfaces or the inter-die interfaces of 3DIC during the CDM qualification tests. In a typical 3DIC stack, the connections to the external pins or balls of the package are made from only one of the dies in the stack. One may make a premature conclusion that there is no need to place any ESD protection clamps on a die not directly connected to the package pins. The absence of ESD clamps between the power and the ground nets on a die could lead to a large potential drop between the power and the ground nets depending upon the CDM charge storage locations and nature of the discharge paths.
The inter-die signal interfaces in a 3DIC could be vulnerable to over-voltage stress induced by Charged Device Model (CDM) ESD. In this work, we investigate the voltage stresses at the inter-die interfaces for different configurations of the power delivery network between the dies in the stack. We also investigate the optimum ESD strategy to protect the inter-die interfaces without penalizing the performance of the inter-die signal paths.

In a 3DIC stack with all the dies under the control of one design team, one could optimize the placement of the rail clamps and decoupling capacitors in the stack. If a process allows fine pitch TSVs distributed all over the die, one can ensure low impedance between the rail clamps on one die and the protected circuits on another die in the stack. Case studies will be presented to explore 3D ESD network design. A two-tier 3DIC test chip design is proposed to provide verification of the simulation-based case studies presented in this work.

1.6 Organization of the Document

Chapter 2 provides an overview of a complete, distributed simulation model for CDM and its individual components: the package, substrate and on-chip circuit models using an example of doubly-stacked die. Chapter 3 provides a simplified, lumped CDM simulation model that can be used to predict the peak CDM discharge of packaged electronic components. Chapter 4 presents the test chip simulation results and the corresponding measurement data from two test chips: (a) single-die packaged in a QFP of 144 pins and (b) doubly-stacked die in a BGA package. Chapter 5 presents a simulation model for 3DIC and simulation results for different scenarios of the power delivery network in the stack. A two-tier 3DIC test chip design is presented to verify the simulation based predictions. Chapter 6 concludes the dissertation with a summary of the results, design guidelines and future work.
2. FULL CHIP MODELING FOR CDM SIMULATIONS

This chapter presents the methodology used in works by Shukla et al. in [14] and [15] to setup CDM circuit simulations for both single and the multi-die components respectively. Consider a device under test (DUT) placed upside-down on the field plate of the FICDM tester as shown in Figure 2.1. The distributed capacitance between the conductors in the package and the field plate is represented by the single lumped capacitance, \( C_{\text{pkg}} \). Similarly, the capacitance between the die and the field plate is shown as \( C_{\text{die}} \). Let \( C_{\text{DUT}} \) be the sum of \( C_{\text{pkg}} \) and \( C_{\text{die}} \). The capacitance between the DUT and the ground plate is labeled \( C_{\text{G}} \). The capacitance between the field plate and the ground plate is labeled \( C_{\text{FG}} \).

Figure 2.1 A packaged component placed on the field plate of an FICDM tester.

Figure 2.2 shows an equivalent representation of the component on the FICDM tester using the three-capacitor model described in [21], [22]. Alternately, a five-capacitor model [23] can be used to model the tester. However, in this work, we use the three-capacitor model, in which the chassis capacitance is included in \( C_{\text{FG}} \), as it is sufficient to model the first peak of the CDM discharge current [23].
Figure 2.2 Electrical equivalent model of the component placed on an FICDM tester. The 1 ohm disc resistor that is used to measure the current during the discharge event is lumped into $R_{SPARK}$.

The analysis in [21], [22] shows that the total charge entering or leaving the DUT when the pogo pin contacts one of the pins of the DUT is

$$Q = C_{eff} \cdot V_{CDM} \cdot \frac{C_{DUT}}{C_{DUT} + C_G} , \quad (2.1)$$

where

$$C_{eff} = C_G + \frac{C_{FG} \cdot C_{DUT}}{C_{FG} + C_{DUT}} . \quad (2.2)$$

For a given value of “Q” and the discharge path impedance, the value of $I_{peak}$ can be estimated analytically [23] or obtained from circuit simulation. Thus, it is seen that the values of the three capacitors, $C_{DUT}$, $C_G$ and $C_{FG}$, must be known in order to estimate $I_{peak}$, although for the usual case that $C_G \ll C_{DUT}$, $C_G$ may be ignored. Note that the impedance of the discharge path includes the pogo pin and the spark.

The values of $C_{FG}$, $R_{SPARK}$ and $L_{POGO}$ can be extracted by measuring the discharge current of a calibration coin of known value of $C_{DUT}$ on a given FICDM tester. $R_{SPARK}$ is typically about 20 to 25 $\Omega$ [23]. The value of $L_{POGO}$ depends on the length of the pogo pin and is typically 4 to 6 nH [23]. The values of these parameters have negligibly small dependence on the size of the DUT. However, $C_{DUT}$ is strictly a function of the DUT size and its package type.
The three-capacitor model with a lumped representation of $C_{DUT}$ provides information about the current at the zapped pin and thus the amount of current flowing through the ESD protection circuit at the pad on the die connected to the zapped pin. Therefore, this method of estimating the peak current is sufficient to predict the reliability of I/O circuit at the pads. To estimate the stress induced by a CDM discharge event on an internal circuit, such as a power domain crossing circuit or an inter-die interface circuit, distributed modeling of the charge storage locations is needed. The distributed model of $C_{DUT}$ provides information about the current flowing from one power domain to another power domain or from one die to another die for a given pin zap. This chapter presents the distributed CDM circuit simulation model. Chapter 3 presents a simplified, lumped CDM simulation model that can be used to predict the peak CDM discharge current of micro-electronic components.

Section 2.1 presents two different methods to build a charge storage model for an IC being stressed on an FICDM tester. Section 2.2 describes a methodology to create a circuit model of multiple discharge paths in an IC. The charge storage model and the discharge path models can then be combined to create a circuit simulation netlist that can be used to study CDM reliability of power domain crossing circuits, inter-die interface circuits or other internal circuits.

### 2.1 Charge Storage Model

Figure 2.3 shows a quad-flat package (QFP) on an FICDM tester. Each pin has a capacitance coupling it to the field plate, denoted by $C_{pin-fp}$, and a capacitance coupling it to the ground plane, denoted by $C_{pin-gp}$. The die-attach plate forms capacitance $C_{die-plate-gp}$ with the ground plane. The exposed part of the die-attach plate forms capacitance $C_{die-plate-fp}$ with the field plate. A distributed charge storage model for a 48-pin QFP is shown in Figure 2.4. In a lumped three-capacitor model, all the capacitances to the field plate would be lumped to form $C_{DUT}$ and
the capacitances to the ground plane would be lumped to form \( C_G \). Preserving the distributed nature of the charge storage model along with the model of the discharge path allows us to study the current flow inside the chip when a particular pin of the package is zapped. Modeling the package level charge storage capacitances is presented in Section 2.1.1.

\[
\begin{align*}
\text{Ground Plane} \\
\text{Pogo Pin} & \quad C_{\text{pin-fp}} \quad C_{\text{die-plate-gp}} \quad C_{\text{pin-gp}} \\
\text{Field Plate} & \quad C_{\text{FG}} \quad C_{\text{pin-fp}} \quad C_{\text{die-plate-fp}} \quad C_{\text{die-fp}} \quad C_{\text{pin-fp}} \\
\text{Field Plate Dielectric} & \\
\end{align*}
\]

Figure 2.3 A quad-flat-package placed on the field plate of an FICDM tester. Capacitance between each pin and the field plate is labeled.

\( C_{\text{die-fp}} \) represents sum of the capacitance coupling from the field plate to (i) the metal interconnect on the die and (ii) the frontside of the die substrate not covered by the interconnect. Modeling of die level charge storage locations is presented in Section 2.1.2.

\subsection{2.1.1 Package Level Charge Storage Model}

Package electrical models extracted for signal integrity analysis cannot be used for CDM simulations as is. The signal integrity models model the self-impedance of the package traces or pins with respect to the ground planes in the package or the board. They do not contain the capacitances formed between the package conductors and the CDM tester plates. During the CDM test, the field plate and the ground plane are the ground reference planes. Therefore a different setup is needed to extract the package model for CDM circuit simulations. A model
containing the charge storage capacitors as shown in Figure 2.4 has to be extracted for CDM circuit simulation purposes.

![Distributed Capacitance Model](image)

Figure 2.4 Distributed capacitance model for the QFP package shown in Figure 2.3. Capacitance between each pin and the tester planes are labeled. The capacitance between the on-die metal and the die surface is shown as one lumped capacitance, \( C_{\text{die}} \).

In [8], the capacitance of the package pins and the die-attach plate were measured in the lab using a C-V meter and the measured values were used to create the distributed charge storage model. However, this method can only be used once the package is available for measurement. In many cases, it is desirable to predict the CDM reliability of a design before it is manufactured and packaged. Therefore, a package modeling methodology that creates a charge storage model given the package database is valuable. In [24], [25], 3D full-wave electromagnetic (EM)
simulations were used to extract the charge storage model of a package, culminating in circuit-level simulations of CDM current waveforms that agreed with measurement data. However, the setup time required to import the package database into the 3D EM solver tool, runtime and memory required to model large packages are prohibitive. An automated and efficient package modeling method is preferable. This work presents a simple two-dimensional (2D) package modeling methodology to model the distributed charge storage sites in a package. Next, both the 3D EM based modeling methodology and the simple 2D modeling methodology are described. In Section 2.3, a fully automated version of the 2D package modeling method to estimate the peak value of CDM discharge current is presented.

2.1.1.1 3D EM Simulation Based Package Modeling Methodology

Typical rise times (10% to 90%) of CDM discharge currents range from 50 ps to 500 ps [6], [17]. These rise times correspond to a frequency range of 700 MHz to 7 GHz. Quasi-static 3D electro-magnetic simulations are shown to be sufficient for this frequency range [26]. To model a package on an FICDM tester, at minimum, size of the field plate, size of the ground plane, length of the pogo pin, the thickness of the dielectric film on the field plate, and its dielectric constant are needed.

Figure 2.5 summarizes the steps involved in modeling a package for CDM simulation purposes using a 3D EM simulation tool. Typically, lead based packages are designed in AUTOCAD®. This applies to the popular quad-flat-package (QFP), quad-flat-no-lead (QFN), dual in line package (DIP) etc. Packages that have a substrate are designed using board design software such as Cadence® Design System’s Allegro®. AUTOCAD® is a generic software tool for creating designs of buildings, machine tools, packages, etc. and therefore does not have a standard for defining packages. Therefore, the package drawing in AUTOCAD® needs to be
cleaned up to retain only the package layers required for the modeling purpose. Package pin names, die outline, die pads and the corresponding pad names need to be defined in the AUTOCAD®. The shapes in the AUTOCAD® file need to be closed shapes. The open shapes are not imported into the EM simulation tool.

Figure 2.5 Steps involved in creating a package model using a 3D EM simulation tool starting from a package database in AUTOCAD® or Cadence Allegro®.

Figure 2.6 shows a QFN package drawing of multi-chip-module in AUTOCAD® before the comments and the text were cleaned up. The die outline of the two die are in different layers (shown by different color of the die outline), the package drawing contained many shapes, outlines, text that are not required for package modeling. The package pin numbers are outside the pin shapes. Bondwires are not drawn using a unique layer. Figure 2.7 shows the cleaned-up version of the same package drawing. Unnecessary layers have been removed. The pin names
have been moved inside the pin shapes. Both the die outlines have been moved to the same layer. All the bondwires have been drawn using the same layer.

![AUTOCAD file of a QFN package with two dies placed side by side](image)

Figure 2.6 An example of AUTOCAD file of a QFN package with two dies places side by side, referred to as multi-chip module (MCM). The AUTOCAD file contains comments, notes and several other layers not needed for modeling.

On the other hand, Cadence® Allegro® is a standard tool used for designing substrate based packages. Packages designed using Allegro® can be directly imported into most of the commercial 3D EM simulation tools. Once the package database is imported into the EM simulation software tool, we need to make sure that the pin nodes are defined at the package end as well as the die end of the each path between a package pin and the corresponding bondpad on the die.
Figure 2.7 Cleaned-up version of the AUTOCAD file of the MCM QFN package shown in Figure 2.6. Only the required layers are retained in the database. Both the die are moved to the same layer. Package pins and pads are labeled with their respective numbers.

Next, the ground plane and the field plate are added as reference planes above and below the package drawing. The field plate and the package are only separated by the field plate dielectric film. A pin node should be created on the field plate. The ground plane of the tester is assigned as the ground reference. The distance between the ground plane and the package should be equal to the length of the pogo pin. The maximum signal frequency over which the model needs to be physically accurate is chosen such that it is higher than the highest frequency component of the CDM discharge current. Based on the typical rise time($t_{\text{rise}}$) data of CDM discharge current which range from 50 ps to 500 ps [6], [17] and the relationship between the rise time and 3-dB bandwidth requirement ($\text{BW} = 0.35/t_{\text{rise}}$), 7 GHz can be chosen as the
maximum frequency for which the model needs to be valid. The simulation tool then creates a mesh for the problem and extracts a RLC model for the package consisting of capacitances between the package conductors and the tester plates, mutual capacitances and inductances between the neighboring conductors, self-inductance and resistances of nets inside the package between the package pins and the bondpads on the die. The RLC model extracted by the tool can be exported into SPICE format. The number of stages in the RLC model can be specified to the EM simulation tool.

The 3D EM simulation tools are very accurate in modeling the package. The EM simulations not only extract the capacitance model of the charge storage but also the model of the discharge paths. The model can then be combined with the on-chip model of the ESD protection network, power-ground busses and circuits of interest to create a complete circuit simulation model. However, EM simulations are expensive in terms of computational runtime and memory. Reducing the size of the FICDM tester plates in the EM simulations can reduce the runtime and memory requirements. The runtime data are presented in Chapter 4. However, the extracted value of capacitance between the ground and the field plates ($C_{FG}$) will be lower in such a simulation. $C_{FG}$ needs to be calculated separately and added to the netlist later. A simple and fast 2D capacitance extraction method is presented next for creating a charge storage model for a package placed on the FICDM tester field plate.

2.1.1.2 2D Package Modeling Methodology

We propose a simple 2D capacitance extraction method to model the capacitances between the package conductors and the field plate of the tester. To estimate the capacitance between a package conductor and the field plate, one needs to know the area of the conductor
(A_{trace}), the distance from the conductor (d_{trace-fp}) to the field plate, and the dielectric constant of the medium (\varepsilon) in between.

\[ C_{trace-fp} = \frac{\varepsilon \cdot A_{trace}}{d_{trace-fp}}. \] (2.3)

Figure 2.8 illustrates a die packaged in a ball grid array (BGA) package with a three-layer substrate placed on an FICDM tester. Trace A is on layer 1. Trace C is on both layer 1 and layer 2. Traces B and D are on layer 2. Trace E is on layer 3. The distances between the respective layers and the dielectric on the field plate are labeled D_{layer1}, D_{layer2}, and D_{layer3} respectively. The distance between the field plate and the die is labeled D_{die}. The thickness of the dielectric on the field plate is labeled t_{dielectric}. When calculating the capacitance between a segment of a trace and the tester field plate, one needs to take into account any shielding of the lower layer metal by the upper layer metal. Referring to Figure 2.8, the die and traces A and C on layer 1 are completely unshielded.

![Figure 2.8 A package with a three-layer substrate placed on the field plate of the FICDM tester.](image)

Therefore, the complete areas of the die and traces on layer 1 are used to calculate their respective capacitance with the field plate. In contrast, trace D on layer 2 is completely shielded by the die above it. Parts of trace C and trace B in layer 2 are shielded by traces on layer 1. Similarly, part of trace E is shielded from the field plate. To compute the capacitance of the traces on each layer using Equation 2.3, only the unshielded area of the traces should be taken...
into account. A layout extractor is used to perform area calculations taking into account the shielding effect by upper level metal layers.

The next step is to determine the distance between each trace and the field plate. This information can be obtained from the package cross-section provided on the package datasheet. An example for a BGA package is shown in Figure 2.9. The nominal thickness of this package, excluding the ball height, is 0.9 mm. The package substrate thickness is not shown in the package data sheet and, in fact, the package substrate may change from design to design. Therefore, the substrate thickness and the substrate stack details need to be obtained separately.

An example of the information needed for the substrate stack is given in Figure 2.10. The \( t_1 \), \( t_2 \) and \( t_3 \) denote the thickness of the respective metal layers; \( t_{21} \) and \( t_{32} \) denote the thickness of the inter-level dielectrics; \( t_{\text{sub}} \) is the thickness of the package substrate; and \( t \) is the package thickness excluding the ball height.

![Figure 2.9 Package cross-section diagram for a BGA package. The diagram shows the thickness of the package and the ball height.](image)

From Figure 2.10, one may calculate the distance from the die to the field plate, \( D_{\text{die-fp}} \), as

\[
D_{\text{die-fp}} = D_{\text{die}} + t_{\text{dielectric}},
\]

where

\[
D_{\text{die}} = t - t_{\text{sub}} - t_{\text{die}}.
\]

Similarly, the distance from layer 1 to the field plate, \( D_{\text{layer1-fp}} \), is calculated as
where

$$D_{layer1-fp} = D_{layer1} + t_{dielectric} \tag{2.6}$$

$$D_{layer1} = t - t_{sub} - t_1 \tag{2.7}$$

The distance between other layers and the field plate can be calculated similarly. The field plate dielectric thickness depends on the test standard. The JEDEC FICDM standard specifies a 0.380 mm (15 mil) thick FR-4 dielectric, whereas the ESDA standard requires a 1 or 2 mil thick dielectric material. Next, the dielectric properties of the field plate dielectric and the package need to be obtained. The package mold material dielectric constant and the package substrate dielectric constant need to be obtained from the package designer. Once the package database and a technology file containing the package stack information have been obtained, capacitance can be calculated.

![Package substrate stack diagram showing the thickness of the conductor and the dielectric layers and the overall thickness of the substrate. The die thickness and the package thickness may need to be obtained from the chip designer and the package datasheet respectively.](image)

The inputs to the package modeling tool are the package database, tester pre-charge voltage, a tech file containing the package layer stack, and the tester information. Commercial EDA tools are part of the overall tool flow, specifically, a layout extraction tool, a package design tool, a package database format conversion tool, and a circuit simulation tool.

The data flow diagram of the complete toolset is outlined in Figure 2.11. In step 1, the package database is converted into a GDSII format. In step 2, an option file is created. This file maps the package database layer names to the standard layers names used in the layout.
extraction rules deck. It also stores the values of the distance parameters, i.e., the distance of each layer from the field plate dielectric. This information is obtained from the tech file. Geometry-dependent formulas for calculating the capacitances are coded in the layout extraction rule deck. In step 3, the layout extraction tool reads the package database in GDSII format and the options file, extracts the parasitic capacitances, and then it creates a SPICE file containing the capacitors between the package metal and the field plate.

The tester parasitic capacitance $C_{FG}$ is then calculated based on the size of the field plate, ground plane, length of the pogo pin and the package height. The capacitance between the chassis and the tester plates should also be taken into account while calculating $C_{FG}$. The capacitance $C_{FG}$ is added to the SPICE file.

![Data flow diagram of 2D package extraction method.](image)

Figure 2.11 Data flow diagram of 2D package extraction method.
2.1.2 Die Level Charge Storage Model

The package database does not contain the details of the on-die metal conductors. In order to obtain a distributed model improve the modeling of the charge storage on the die, area of the on-die conductors belonging to different nets has to be estimated. Depending on the orientation of the die to the field plate, the capacitive coupling from the field plate could either be to the frontside of the die or to the backside of the die.

Figures 2.12-2.14 illustrates the different scenarios. In Figure 2.12, a die is wire-bonded to a BGA package substrate. The frontside of the die faces the field plate of the capacitor. There will be capacitive coupling between the on-die interconnect and the field plate. The resulting capacitance is labeled $C_{\text{int-die}}$. The area of the frontside of the substrate not covered by any interconnect or devices forms $C_{\text{die-sub}}$ with the field plate.

![Diagram of BGA package](image)

Figure 2.12 A BGA package containing a die wire-bonded to the package substrate is placed on the FICDM tester. Due to the orientation of the frontside of the die to the field plate, there is no capacitive coupling between the field plate and the backside of the substrate.

In Figure 2.13, a die is packaged in a QFP package in cavity-up fashion. The die is facing up. The bondpads of the die are wire-bonded to the leads of the package. When the package is placed on the field plate of the FICDM tester, the frontside of the die faced the field plate.
plate of the tester. The metal interconnect on the die forms capacitance $C_{\text{int-die}}$ with the field plate. The top of the die substrate not covered by the metal interconnect or devices forms capacitance $C_{\text{die-sub}}$ with the field plate of the tester.

Figure 2.14 shows a flip-chip package on the field plate of FICDM tester. The die is flipped on the BGA package substrate and connections to the package substrate are established through the flip-chip bumps on the die. Therefore, the backside of the die forms capacitance $C_{\text{die-sub-back}}$ with the field plate of the tester. Next, a method to estimate the capacitance $C_{\text{die-int}}$, $C_{\text{die-sub}}$ and $C_{\text{die-sub-back}}$ is presented.

Figure 2.13 A QFP package with a die wire-bonded to the leads of the package is placed on the field plate of FICDM tester. The die is orientated such that the frontside of the die is facing the field plate of FICDM tester.

Figure 2.14 A flip-chip BGA package placed on FICDM tester. The die is flipped on to the package substrate. Therefore, the backside of the substrate forms capacitance $C_{\text{die-sub-back}}$ with the field plate of FICDM tester.
(a) Estimating the Capacitance to the Frontside of the Die

To estimate the capacitance $C_{\text{int-die}}$, area of the metal interconnect on the die needs to be estimated. Power and ground metal typically forms the majority of the metal on the die. The contribution of the signal metal lines on the die can be neglected because of the relatively small area they occupy. For each power and ground net on the die, the area of the metal can be extracted using layout extraction tool and the die layout database. The distance of the frontside of the die (see Equation 2.5) can be obtained from the package stack information. The capacitance of each power and ground net can then be estimated by applying Equation 2.3 on the area of the metal. The on-die metal may be at different levels of routing. But typically the value of $D_{\text{die}}$ is much larger than the total metal stack height on the die and therefore, the differences in the distance of each metal level on the die to the field plate can be neglected. For simplicity, the estimated value of $C_{\text{die-int}}$ for each power/ground net can then be distributed among the bondpads of that particular net.

Next, the area of the substrate not covered by the metal interconnect or the devices on the die can be extracted using the die layout database. The corresponding capacitance $C_{\text{die-sub}}$ can be calculated using the simple parallel plate capacitance formula (Equation 2.3). If the design consists of multiple ground domains that connect to the substrate, the capacitance can be divided among the different ground domains such that the amount of capacitance is proportional to the area of the die belonging to the respective ground domain.

(b) Estimating the Capacitance to the Backside of the Substrate

The capacitance to the backside of the substrate, $C_{\text{die-sub-back}}$, as shown in Figure 2.14 can be calculated by using parallel plate capacitance using the area of the die, value of the dielectric
constant of the package encapsulation material and the distance from the die backside to the field plate. The capacitance $C_{\text{die-sub-back}}$ can be distributed along the backside of the die substrate. The granularity of the distributed model of $C_{\text{die-sub-back}}$ depends on the discharge path model used for the substrate. This is discussed in detail in Section 2.2.

2.1.3 Charge Storage Model for Wafer Level Chip Scale Packages

Wafer level chip scale packages (WCSP), also known as micro surface mount devices ($\mu$SMD), do not contain any kind of encapsulation. Balls are directly attached to the die to create connections to the external world. The metal re-distribution layer (RDL) is used to create connections between the balls and the pads on the die. A very thin (25 $\mu$m to 50 $\mu$m) protective insulating material is coated on the backside of the die. This coating is referred to as backside coating (BSC). Figure 2.15 shows a WCSP placed on the field plate of FICDM tester. The backside of the die is on the field plate of the tester. The die substrate is separated from the field plate of the tester only by the thin backside coating and the field plate dielectric. The field plate dielectric is about 25 $\mu$m – 50 $\mu$m in the case of ESDA standard tester and 380 $\mu$m in the case of JEDEC standard tester. Therefore, the capacitance $C_{\text{die-sub-back}}$, is significant. Such packages can be easily modeled using the 2D package modeling methodology detailed in Section 2.1.2.

Figure 2.15 A WCSP package placed on the field plate of an FICDM tester. The balls are attached to the frontside of the die and therefore the backside of the die is on the field plate of the tester.
\( C_{\text{die-sub-back}} \) can be calculated as following:

\[
C_{\text{die-sub-back}}^{-1} = \left( \frac{\varepsilon_0 \varepsilon_{\text{BSC}} A_{\text{die}}}{t_{\text{BSC}}} \right)^{-1} + \left( \frac{\varepsilon_0 \varepsilon_{\text{FPD}} A_{\text{die}}}{t_{\text{FPD}}} \right)^{-1},
\]  

(2.8)

where \( \varepsilon_{\text{BSC}} \) is the dielectric constant of BSC, \( \varepsilon_{\text{FPD}} \) is the backside coating of the field plate dielectric, \( \varepsilon_0 \) is permittivity of the free space with a value of 8.854e-12 F/m, \( t_{\text{BSC}} \) is the thickness of BSC and \( t_{\text{FPD}} \) is the thickness of the field plate dielectric and \( A_{\text{die}} \) is the area of the die. Typically, the values of \( \varepsilon_{\text{BSC}} \) and \( \varepsilon_{\text{FPD}} \) are almost the same, around 4.4. Therefore, the Equation 2.8 for \( C_{\text{die-sub-back}} \) can be simplified into Equation 2.9:

\[
C_{\text{die-sub-back}} = \left( \frac{\varepsilon_0 \varepsilon_{\text{FPD}} A_{\text{die}}}{t_{\text{BSC}} + t_{\text{FPD}}} \right).
\]  

(2.9)

During the CDM event, the capacitance \( C_{\text{die-sub-back}} \) discharges through the substrate, into the on-die ESD network. \( C_{\text{die-sub-back}} \) can be modeled as a distributed capacitance over the whole surface area of the backside of the die. This is especially true when a distributed model of the substrate is used for modeling the discharge path. This is discussed in detail in Section 2.2.

### 2.2 Discharge Path Modeling

After the charge storage sites are modeled using the methods explained in Section 2.1, discharge paths from each of the charge storage locations to the pins or balls of the package have to be modeled. Consider a chip-scale package containing two-tier stacked die shown in Figure 2.16. The capacitances formed between the conductive parts of the package and die with the field plate have to be modeled using the methods explained in Section 2.1. An overview of the discharge path model with the components of the package and the die is shown in Figure 2.17. \( R_{\text{trace}} \) and \( L_{\text{trace}} \) represent the impedance of a package trace. \( R_{\text{bw}} \) and \( L_{\text{bw}} \) represent the impedance
of a package bondwires connecting the on-die bondpads and the package traces. The details of the connections between Die1’s on-chip ESD protection network and that of Die2 are not included in Figure 2.17. These connections may exist due to a shared ground net, a shared power net, or an I/O connection between the dies. Such connections are either made by directly bonding the pads from the either die using a single bondwire or through a pair of bondwires that connect the pads on the either die to a shared bondfinger on the package substrate.

In the schematic shown in Figure 2.17, if ball 1 is zapped, the capacitance $C_{\text{trace-1}}$ charges or discharges through the pogo pin. The capacitance $C_{\text{bondpad-1}}$ discharges through the bondwire and trace impedances denoted by $L_{\text{bw-1}}$, $R_{\text{bw-1}}$, $L_{\text{trace-1}}$ and $R_{\text{trace-1}}$ respectively. The charges stored on the capacitances at other locations have to travel through the respective traces into the corresponding die’s ESD protection network, through the bondpad-1 into the zapped ball of the package. For example, a charge on $C_{\text{trace-n}}$ discharges through its trace impedance into Die2. This charge then flows through Die2’s ESD protection network into Die1’s ESD protection network and finally into the zapped ball belonging to trace1.

![Diagram of a two-tier stacked die in a BGA package](image)

Figure 2.16. A two-tier stacked die in a BGA package is placed upside down on the field plate of the CDM tester. The diagram shows the major capacitance formed between the plates of the tester and the metallic parts of the package and the die.
Figure 2.17. Schematic of the charge storage model and the discharge path model for the doubly stacked CSP package shown in Figure 2.11.

The discharge path model can be categorized into:

(a) Package level discharge path

(b) On-die discharge path model

Modeling methodology for package level discharge paths involves modeling the package traces or pins, power/ground planes and bond wires. The tools and methods required to model the package level discharge paths are different from the ones required to perform modeling of the discharge paths on the die. Modeling the on-die discharge paths involves modeling the ESD protection circuits, parasitic impedance of the on-die interconnect, decoupling capacitors between the power and the ground nets and the circuits under study. Section 2.2.1 presents the methodology of package level modeling of the discharge paths and
Section 2.2.2 presents the methodology used in this work to model the on-chip components of the discharge path.

### 2.2.1 Package Level Discharge Path Modeling

There are three methods that can be employed to obtain the model of the discharge paths in the package:

(a) 3D EM simulation methodology

(b) Use the existing package signal-integrity model

(c) Approximate inductance/resistance model based on analytical formula for bondwires and traces and leads

If the 3D EM simulation tool was used for modeling the charge storage locations as detailed in Section 2.1.1, the impedance of the traces, bondwires would have been already modeled and there is no need to model these separately. The complete package model can be then combined with the on-chip model to obtain the complete circuit schematic for CDM simulations.

If a package was modeled for signal integrity analysis, the model can be used for CDM simulation purposes. The model should contain the resistance and inductance of the bondwires, traces or leads, mutual capacitances between the neighboring pins. We have to make sure that the self-inductances of the pins or the traces are the partial self-inductances and not the loop self-inductances. Loop self-inductances are to be avoided because their values are extracted based on an assumption about the location of the ground plane that may not be applicable to the case of the package on an FICDM tester. Therefore, only the partial self-inductance values of the pins
and the bondwires should be used if available in the package datasheets. If not, Equation 2.10 and Equation 2.12 can be used to estimate the self-inductance values of the bondwires and the package pins or traces. The self-capacitance values of the pins cannot be used for CDM simulation purposes. These values would not be accurate in the case of a package placed on the FICDM tester. The charge storage model discussed in Section 2.1 should be used in place of the self-capacitances.

If neither of the above two methods are available, one can construct models for the package trace, leads and bondwires using approximate formulas.

(a) Bondwires

The partial self-inductance of a cylindrical conductor is given by Equation 2.10 [28].

\[ L_{bw} = 0.2 \cdot l \cdot [\ln(2 \cdot l/r) - 0.75] \text{ nH} \]  

\hspace{1cm} (2.10)

In Equation 2.10, \( l \) is the length of the bondwire in mm and \( r \) is the radius of the bondwire in mm. Typical diameter of the bondwires are in the range of 25 \( \mu \text{m} \) to 50 \( \mu \text{m} \). For the bondwires with typical diameter, the partial self-inductance is often approximated as 1 nH/mm. The following plot in Figure 2.18 shows that the approximation is not very far from the values obtained using Equation 2.10 for the bondwires of diameter 25 \( \mu \text{m} \) and 50 \( \mu \text{m} \).
The resistance of the bondwires can be calculated using Equation 2.11:

\[ R_{bw} = \rho \cdot l/A, \]  

(2.11)

where \( \rho \) is the resistivity of the bondwire material, \( l \) is the length and \( A \) is the cross-sectional area of the conductor. For gold, \( \rho = 2.214 \times 10^5 \Omega \cdot m \), and therefore for a bondwire with 25 µm diameter, the resistance can be approximated to be 50 mΩ/mm length of the bondwire.

(b) Rectangular traces

The inductance of rectangular traces can be calculated using the Equation 2.12 [28]:

\[ L_{trace} = 0.2 \cdot l \cdot [ln(2 \cdot l/(w + t))] + 0.5] \text{ nH}, \]  

(2.12)

where \( l \) is the length of the trace in mm, \( w \) is the width of the trace in mm and \( t \) is the thickness of the trace in mm. For a trace of width 150 µm and thickness of 35 µm, the inductance is plotted in Figure 2.19 for different trace lengths. The rule of thumb approximation of 1 nH/mm is also
plotted for comparison. The 1 nH/mm is a pessimistic approximation of the inductance of the package traces.

The resistance of the package traces $R_{\text{trace}}$ can be calculated using Equation 2.11. The mutual capacitance (e.g. $C_{m12}$) between the traces that are very close to each other needs to be modeled. This capacitance can be calculated by using the simple analytical expression in Equation 2.13 for parallel plate capacitance:

$$C_m = \frac{\varepsilon_0 \varepsilon_r A}{d},$$

(2.13)

where $\varepsilon_0 = 8.854 \times 10^{-12} \text{ F/m}$ and $\varepsilon_r$ is the dielectric constant of the package encapsulation material, $A$ is the area of the conductor walls facing each other and $d$ is the distance between the conductors. For more complicated structures that are not strictly parallel, capacitance extraction tools need to be used for calculating the mutual capacitance.
### 2.2.2 On-Die Discharge Path Modeling

The components of the on-die discharge path model can be broadly categorized into the following:

(a) ESD protection network model

(b) Parasitic impedance model of the power and the ground busses

(c) Decoupling capacitors between the power and the ground nets

(d) Substrate impedance model

If the layout of a whole die is extracted along with the parasitic resistances and capacitances of the signal, power and ground network, the number of circuit elements in the resulting netlist for a chip with a die size of 8 mm$^2$ may be on the order of tens of millions. The runtime and memory requirement for such a circuit simulation will be prohibitive. Even if one could afford to perform such a simulation, one has to make sure that the models of the devices are valid in the high voltage or current regime that the devices may operate during the CDM discharge. Therefore, at the very least, the ESD protection circuits need to be replaced by models that are valid during the ESD conditions. CDM discharge is a very fast transient event. Therefore, the ESD protection device models should capture the transient effects during the CDM circuit simulations.

(a) ESD protection network model

The simulation circuit should represent the ESD protection circuit network on the die. Typically, there is an ESD protection circuit at each pad. On a die with multiple power domains,
the ground nets are connected using anti-parallel diodes. The power domain crossing circuits are typically protected by voltage clamping circuits.

The behavior of the each ESD protection circuit used on the chip should be characterized using very fast transmission line pulsing (vfTLP) [29]. The quasi-static current-voltage (I-V) curves should be obtained. Due to the fast nature of the CDM pulse, some ESD protection circuits such as silicon controlled rectifiers (SCRs) and shallow-trench isolation (STI) diodes exhibit transient voltage overshoot before clamping the voltage to a lower value. In the case of SCRs, delayed turn-on of the SCR device leads to voltage overshoot that is higher than the quasi-static snapback voltage level. In the case of STI diodes, the diode on-resistance ($R_{on}$) reduces to a lower value after a few hundreds of pico seconds due to conductivity modulation. Therefore the transient voltage waveform exhibits a voltage overshoot during the rise time of the CDM event before the voltage is clamped to a lower, quasi-static value. Using the transient peak value of the voltage and the quasi-static I-V curves, a compact model can be obtained for the ESD protection circuit [30]. This model can then be used to represent the ESD protection circuit in the simulation.

(b) Parasitic impedance model of the power and the ground busses

The CDM discharge current mainly flows through the ESD protection network in the I/O ring and the power/ground busses connecting the ESD protection circuits. For large packages, the peak discharge current, $I_{peak}$, can be as high as 10 A at 500 V pre-charge level for packages of size in the order of 1000 mm$^2$. For such high currents, even a small parasitic resistance in the power or the ground bus can create substantial amount of voltage drop. Therefore it is important to model the resistance of the power and the ground busses correctly. One can perform parasitic
extraction of the complete power and the ground interconnect network but the resulting netlist will have a very large number of nodes and elements. Also, when extracting the ground bus, one should take care that the bulk nodes of the devices are not shorted through the substrate. A majority of the parasitic extraction tools consider the die substrate as an ideal ground plane and short all the device nodes that connect to the substrate. Such a netlist will yield a very low parasitic resistance even between the nodes of the ground bus even through the nodes are at the extreme corners of the I/O ring. There are two ways to fix this problem: (a) instruct the extraction tool not to extract the bulk nodes of the devices. However, you will have to manually assign the correct net names to the bulk nodes of the devices in the extracted netlist, or (b) instruct the extraction tool to extract the die substrate by providing the correct substrate resistivity value. This method is time consuming and can result in a huge netlist. In this work, a simplified model was used to represent the parasitic resistance of the power/ground nets.

The power and the ground bus in the I/O ring have a pre-defined width that is regular throughout the I/O ring. Therefore the value of the parasitic resistance of each power and ground bus between two bondpads can be extracted using a parasitic extraction tool or estimated using the sheet resistance values published in the PDK. A ring network can then be created to represent each power and ground bus in the I/O ring. In this work, a parasitic extraction tool, Calibre®, was used to estimate the resistance. The substrate contacts were manually removed from the section of the layout being extracted.

Majority of the chips consist of the core power and ground network in a grid structure or a collection of parallel stripes. Section of the grid or the stripe structure can be modeled using the method described in the previous paragraph and these sections can be repeated to represent the core power and ground network. The connections between the core network and the I/O ring
have to be modeled accurately in terms of connection resistances and the physical location of the connections.

Figure 2.20 shows a schematic of a representative I/O ring containing the ESD protection devices connected to each pad and interconnected by the parasitic resistance model of the power and the ground busses. The design has consists of 48 bondpads and two power domains: VDD1 and VDD2. The power nets VDD1 and VDD2 are isolated whereas VSS1 and VSS2 are connected by anti-parallel diodes (APDs) placed in the I/O ring as shown. The parasitic bus resistance of the section of the VSS1 bus between two pads is denoted by $R_{VSS1-x-y}$, where $x$ and $y$ are the two adjacent pad numbers. The parasitic resistances of the VSS2, VDD1 and VDD2 busses are similarly labeled. The on-chip circuit model connects to the package or other dies in the package (refer to Figure 2.17) at the bondpads. Because of the sharp rise time of the CDM discharge current, Abessolo-Bidzo et al. [31] suggested that the inductance of the power and ground bus on the die be modeled for circuit simulation. However, there is neither an indication that the inductance model was used in the circuit simulation nor if the results presented in [31] would have been different if the inductance was not included. In this work, only the resistance of the on-die power and ground busses was included in the circuit model. The simulation results agree with the measurement results on two test chips. Therefore, the on-chip inductance is not critical enough to be included in the simulation model.
Figure 2.20 An example circuit model of an I/O ring of a chip. The chip has two power domains: VDD1 and VDD2 which are isolated. VSS1 and VSS2 are connected using anti-parallel diodes (APDs) placed in the corners of the I/O ring. Pad2, Pad24, Pad25 and Pad48 are ground pads. Pad13 and Pad38 are power pads.

The capacitance of the power bus with respect to the substrate can also be estimated per section of the power bus between two pads. This capacitance should be included in the model as shown in Figure 2.20, labeled by $C_{dx}$, where $x$ is the pad number.

(c) Decoupling capacitance

The decoupling capacitance in each of the pad cell should be included and can be lumped into $C_{dx}$. The displacement current due to $C \cdot \frac{dv}{dt}$ flows across the decoupling capacitors.
Therefore, during the rise time of the CDM event, the potential difference between the power and the ground net is clamped to a lower value.

The decoupling capacitance in the core should be modeled and connected to the core power ground net model at their respective physical location. The entire core decoupling capacitances placed contiguously can be lumped together. If any two banks of decoupling capacitors are physically separated from each other, then the banks should be modeled separately.

(d) Substrate impedance model

The substrate impedance model needs to be included in the circuit simulations only when there is significant amount of coupling between the backside of the substrate and the field plate of the FICDM tester ($C_{\text{die-sub-back}}$ in Figure 2.14 and Figure 2.15) or substrate is the only path of discharge for any major charge storage site (e.g. $C_{\text{die-plate-fp}}$ in Figure 2.13). The orientation of the die to the field plate and the absence or presence of the die-attach plate dictate the need for the substrate impedance model.

Figure 2.12 illustrated a case where $C_{\text{die-sub-back}}$ or $C_{\text{die-plate-fp}}$ is absent. Therefore the substrate model need not be included in the CDM simulations.

Figure 2.13 showed a QFP package on the tester resulting in $C_{\text{die-plate-fp}}$. This capacitance will discharge only through the substrate, if there is no down-bonding of the die-attach plate. If the die-attach plate is down bonded using bondwires to the ground pins of the package, there is an alternate path for the capacitor $C_{\text{die-plate-fp}}$ to charge or discharge. Despite the down-bonding of
the die-attach plate, the substrate impedance model needs to be included in the CDM simulations if the value of $C_{\text{die-plate-fp}}$ is comparable to the total package-pin capacitance.

Now, consider the BGA package shown in Figure 2.1. During the CDM discharge, the capacitor $C_{\text{die-sub-back}}$ discharges through the substrate. Therefore, the substrate impedance model needs to be included in the CDM simulations. Similarly, in the case of WCSP in Figure 2.15, the capacitance $C_{\text{die-sub-back}}$ discharges through the substrate.

A distributed model of the substrate can be used for accurate representation of the substrate impedance. In such a model, the substrate is divided into a 3D grid of boxes, each represented by six resistors, as suggested in [8]. A program was written by Shukla et al. [14] to create a substrate resistor network, given the substrate size and the grid size. The grid size and the die size determine the number of nodes in the substrate model. The backside of the substrate is connected to $C_{\text{die-plate-fp}}$, and the top side of the substrate is connected to the substrate contacts of the VSS busses as shown in Figure 2.21. The substrate model in Figure 2.21 is for a design that has two ground domains that are not connected by metal on the die. However, the VSS1 and VSS2 nets are connected through the substrate underneath. The effective impedance between a node in the VSS1 domain and a node in the VSS2 domain depends on the distance between them on the die, the substrate resistivity and also the thickness of the die.
Figure 2.21 3D substrate resistor grid. X1, X2 … Xn are the substrate contacts. The resistors in the top row model the ground buses. A sample grid box with six resistors is shown on the lower-left corner.

Figure 2.21 corresponds to the particular case in which the die attach plate is connected to the die substrate using conductive glue (silver filled epoxy). If, instead, the die is attached using an insulating glue, the $C_{\text{die-attach-fp}}$ should be distributed across the bottommost grid boxes of the substrate in the x-y plane. A method to connect the substrate model to the on-die substrate contact was presented in [14]. The top-side of the substrate is connected to the substrate contacts.

In this work, substrate contacts were automatically extracted from the layout and a reduction algorithm was used to merge the substrate contacts that were in the same grid box of the substrate model. The locations of the substrate contacts were extracted using a customized layout extraction rule set. A script was written to identify the topmost grid boxes within the substrate model, as these contain all of the substrate contacts. Multiple substrate contacts contained within the same grid box were merged to form a single equivalent contact that is placed at the location of the original contact that is closest to the center of the grid box. The smaller is the grid box, the better is the accuracy of the model. However, if each substrate contact is contained in its own
grid box, the size of the grid would be too large and the model would be computationally inefficient.

The 3D model of the substrate enabled the study of the current flow in the substrate during the CDM discharge. In [14], it was found that during the CDM discharge event in the case of the high resistivity substrate with resistivity value of 2-20 Ω-cm (lightly doped), the current flows mostly vertically (in z-direction) in the substrate, into the substrate contacts and then flows laterally (in x-y direction) through the on-die ground bus metal interconnect. However, in the case of the low-resistivity substrate with resistivity value of 0.01-0.1 Ω-cm (highly doped), the CDM discharge current first flows laterally across the substrate and then exits through the substrate contacts near the zapped pin.

2.3 Model of the Circuit under Study

Including all the circuits on the die in the CDM simulation requires large computational power and memory. Therefore, only the circuits under study are recommended to be modeled in the CDM simulation netlist. Examples of circuits that are vulnerable to damage from a CDM discharge event are

- Primary input/output circuits
- Power domain crossing signal interfaces
- Inter-die interface circuits in the case of multi-die system-in-packages

Primary input/output circuits directly interface with the external world through the package pins. Therefore, when a package pin is stressed, the devices in the corresponding input/output circuit may experience over-voltage stress if the ESD protection circuit at the pad is
not well designed. Several studies have been conducted to study the CDM robustness of input/output circuits and properly design the ESD protection network for them [32], [33]. In this work, the primary focus is on the power domain crossing circuits and the inter-die interface circuits.

### 2.3.1 Power Domain Crossing Circuits or Internal I/O Circuits

Multiple power domains on a single chip are very common in modern integrated circuits and are essential building blocks of complex system-on-chip (SoC) designs. In such chips, there may be multiple signal lines that transmit information from one power domain to another power domain. Such circuits are referred to as power domain crossing circuits. Figure 2.22 shows an example power domain crossing circuit in a chip consisting of two power domains VDD1 and VDD2. The corresponding ground nets are VSS1 and VSS2, respectively. VDD1 and VDD2 are not connected on the die or package. VSS1 and VSS2 are connected on the die by two pairs of anti-parallel diodes, labeled as APD1 and APD2 in Figure 2.22.
Figure 2.22 An example of power domain crossing circuit consisting of transmitter (TX) in VDD1/VSS1 domain and receiver (RX) in the VDD2/VSS2 domain. The dashed line represents the boundary of two domains. Points A, B, C and D show the points at which the TX and the RX power/ground ports connect to the respective busses in the I/O ring.

TX and RX are placed in the core region of the chip. Resistors $R_{\text{VDD1-core}}$, $R_{\text{VSS1-core}}$, $R_{\text{VDD2-core}}$ and $R_{\text{VSS2-core}}$ represent the core power/ground net parasitic resistance between the TX/RX nodes and the points A, B, C and D in the VDD1, VSS1, VDD2 and VSS2 busses in the I/O ring. Though this diagram shows a simple single resistance model, in practice, the parasitic resistance network could be more complex. It is important to model the core parasitic power/ground network that connects the TX and RX power/ground ports to the main busses that carry the CDM discharge current in the I/O ring. One could perform parasitic extraction of the power and the ground nets and include the complete model or use a simplified model that captures the connections between the core power domain crossing circuit and the main busses in the periphery. A simplified model of the power domain crossing circuit is shown in Figure 2.23.
Figure 2.23 A simplified linear model of the power domain crossing circuit shown in Figure 2.21. The red arrows indicate the direction of the current flow during the CDM discharge event when the chip is pre-charged positive and the pin connecting to the VSS2 pad is zapped. The nodes A, B, C and D correspond to the nodes indicated in Figure 2.21. The APD shown here is an approximate representation of an APD with a perimeter that is the sum of two APDs shown in Figure 2.22.

The nodes A, B, C and D from Figure 2.22 are labeled in Figure 2.23 also. The diagram shows the direction of CDM discharge current flow when a pin connecting to the VSS2 pad is zapped (shown by the red spark symbol) after the chip is pre-charged with a positive voltage level on the FICDM tester. The total current that flows into the zapped pin, $I_{\text{CDM}}$, consists of:

- $I_1$: Current flowing from the VDD1 power net to the VSS1 net due to the package and the die level charge storage capacitances connected to the VDD1 domain

- $I_2$: Current flowing from the VSS1 ground net to the VSS2 net due to the package and the die level charge storage capacitances connected to the VSS1 domain

- $I_3$: Current flowing from the VDD2 power net to the VSS2 net due to the package and the die level charge storage capacitances connected to the VDD2 domain
• Current flowing from the VSS2 domain into the zapped pin due to the package and the die level charge storage capacitances connected to the VSS2 domain itself.

The current flowing from VSS1 domain to VSS2 domain, \( I_{APD} \), is equal to the sum of the currents \( I_1 \) and \( I_2 \). CDM discharge currents mainly flow through the power and the ground busses in the I/O ring as indicated. There is no significant current flowing through the signal line from TX to RX. However, significant potential difference can develop across the RX gate oxide due to potential difference between VDD1 and VSS1 and the current flowing across the domain, \( I_{APD} \).

Let \( V_G \) denote the potential at the gate node of the receiver (RX), \( V_{S-N} \) denote the potential at the source node RX NMOS and \( V_{S-P} \) denote the potential at the source node of RX PMOS. The voltage stress generated between the gate and the source terminals of the RX NMOS can be expressed using Equation 2.14:

\[
V_{GS-N} = V_G - V_{S-N} \approx V_A - V_C \approx V_1 - V_C. \tag{2.14}
\]

The expression can be further simplified as shown in Equation 2.15:

\[
V_1 - V_C = (V_1 - V_2) + (V_2 - V_B) + (V_B - V_C). \tag{2.15}
\]

Equation 2.15 is further expressed in terms of individual components of voltage drops across the various elements along the current discharge path as shown in Equation 2.16:

\[
V_{GS-N} \approx V_{power-clamp} + (I_1 + I_2) \cdot R_{VSS1b} + V_{APD} + I_{APD} \cdot (R_{VSS1a} + R_{VSS2a}) \tag{2.16}
\]

Equation 2.16 is a simple analytical expression for the stress generated at the RX NMOS. In practice, the CDM discharge event is a transient event with very fast rise time. Therefore, only
the transient simulations will be able to accurately predict the voltage stress across the RX NMOS gate oxide. Voltage drops $V_{APD}$ and $V_{power-clamp}$ are rise time dependent. Also, Equation 2.16 approximated $V_G$ to be equal to $V_A$, which is not an entirely correct assumption. Studies [27] have shown that the size of the PMOS in the TX circuit impacts the potential $V_G$. As the size of the PMOS in the TX circuit is increased, the value of $V_G$ becomes closer to the value of $V_A$ (the potential at the source of the TX PMOS, as shown in Figure 2.23). Therefore, the voltage stress, $V_{GS}$, increases. Larger the size of the PMOS in the TX circuit, closer $V_G$ Therefore, the entire TX and RX circuits, the power and the ground network that connect the TX and the RX circuits to the corresponding busses in the IO ring should be included in the circuit simulation netlist.

SPICE models provided with the product development kit (PDK) can be used for representing the TX and RX circuits. However, it was noticed that the gate current model parameters in the SPICE models over-predicted the gate currents at high voltage levels (> 3.2 V). The SPICE models for gate leakage currents are based on the direct-tunneling mechanism and are valid only the low voltage regime. Direct tunneling models represent the oxide potential barrier as a trapezoidal barrier which is true only in the low voltage regime. In the higher voltage regime, the potential barrier is of triangular shape. Due to the high gate current predicted by these models, the voltage stress across the RX gate oxide predicted by the circuit simulations will be very low. Therefore, it is important to turn off the gate current model parameters by setting $IGCMOD = 0$ and $IGBMOD = 0$ in both the p-type and the n-type MOSFET transistors.

To accurately model the gate tunneling current, Fowler-Nordheim gate tunneling current models [34] should be used in the simulations. A voltage controlled current source may be
connected in parallel with the gate-source of the receiver transistors, RX NMOS and RX PMOS. The gate current can be modeled as shown in Equation 2.17 [34]:

\[
J_G = A e^{-\frac{BT_{ox}}{V_{gs}}}. \tag{2.17}
\]

\(J_G\) is the gate tunneling current density. A and B are the model fitting parameters. The gate leakage currents for the NMOS and the PMOS thin oxide devices can be measured under the transmission line pulsing (TLP) [35] stress, and the mathematical model in Equation 2.17 can be fitted using MATLAB [36]. After obtaining the appropriate parameters for the measured data, the equation may be implemented in Verilog-A [37] script and the resulting Verilog-A model should be included in the netlist used for the circuit simulations.

Parasitic body diodes in the transistors can provide voltage clamping during certain polarity of stresses that bias the diodes in the forward conducting mode. Therefore, it is important to make sure that the PDK transistor SPICE models correctly describe the I-V characteristics of these diodes. If not, the diodes’ I-V characteristics should be measured under VFTLP stress and the model should be modified to match the measured I-V characteristics.

2.3.2 Inter-Die Interface Circuits

Inter-die interface circuits were shown to be vulnerable to CDM induced damage in [15], [17] even though they do not connect to the external pins of the package. Detailed discussion of the methodology to model the inter-die interface circuits for circuit simulations was presented in [15] and predictions about the CDM reliability of the inter-die interface circuits were formulated. Subsequently, measurement data from a stacked die test chip was presented in [17] that concurred with the simulation based predictions. A detailed analysis of the measurement data is presented in Chapter 4.
2.4 Chapter Summary

A methodology to create a complete CDM circuit simulation model for single-die packages as well as complex, multi-die packages was presented. An alternative to the 3D package modeling method was presented. Simple and efficient procedure to construct the charge storage model, the package and on-die discharge path model were discussed.

In Chapter 4, test chip measurement results from two test chips are presented along with the simulation based analysis. Simulations were used to predict the reliability of power domain crossing circuits and inter-die interface circuits before the tape-out of the test chips. Measurement results confirm the correctness of the simulation models presented in this chapter.
3. ESTIMATION OF PEAK CDM DISCHARGE CURRENT

Chapter 2 presented a methodology to construct a complete, distributed circuit model that could be used for studying the reliability of internal circuits of a system-in-package. However, to analyze the reliability of external I/O or the primary input/output circuits, only the peak current and the current rise time information is needed. For such purposes, distributed models of the package and die are unnecessary. In previous works [24], [25], three-dimensional (3D), full-wave electromagnetic (EM) simulations were used to extract a package model, culminating in circuit-level simulations of CDM current waveforms that agreed with measurement data. However, the setup time required to import the package database into the 3D EM solver tool, runtime and memory required to model large packages are prohibitive. Therefore, in practice, ESD designers have limited information about the amount of the CDM current that the protection network should be designed to withstand. One may estimate the expected value of I_{peak} for a given package using I_{peak} data collected for earlier packages, but this method is not always reliable. An automated and efficient package modeling method is preferable. In this chapter, for the first time, a simple, computationally efficient and fully automated method to estimate I_{peak} is presented [38]. Measurement data on several packages (presented in Chapter 4) agrees with the simulation results.

3.1 Peak Current Estimation for Packages with Encapsulation

For packages such as BGA, QFP and QFN, a simple 2D package modeling method was presented in Section 2.1.1 to obtain charge storage capacitance model. A simplified version of the methodology is used to predict the CDM I_{peak}, with results that are in good agreement with measurement data.
Refer to Figure 2.5 in Section 2.1.1. A 2D package extraction method was employed to extract capacitances of the package conductors with respect to the field plate of FICDM tester. Figure 3.1 extends the method to sum all the capacitances to form $C_{DUT}$. Steps 1, 2 and 3 are outlined in Section 2.1.1. Additional information about the resistance ($R_{ds\text{discharge}}$) and the inductance of the zapped pin and the bondwire ($L_{\text{discharge}}$) can be provided in step 2. Step 3 extracts the parasitic capacitances, and then it creates a SPICE file containing the capacitors between the package metal and the field plate. To estimate $I_{\text{peak}}$, a lumped model of $C_{DUT}$ is sufficient. In step 4, the SPICE file is read and all the capacitances with respect to the field plate are lumped to form $C_{DUT}$. Finally, in step 5, the circuit shown in Figure 3.2 is simulated to obtain the discharge current waveform. The peak value of the current, $I_{\text{peak}}$, is obtained from the simulated waveform.

Figure 3.1 Data flow diagram of automated peak current estimation tool.
3.2 Peak Current Estimation for WCSP Devices

WCSP devices do not contain package encapsulation. A ball grid array is directly attached to the top of the die. Modeling method for WCSPs was presented in Section 2.1.3. The method can be simplified to estimate $I_{\text{peak}}$. A WCSP placed on the field plate of FICDM tester is shown in Figure 3.3. The capacitance $C_{\text{die-sub-back}}$ between the field plate and backside of the substrate discharges through the substrate. Therefore, substrate impedance has to be included in the discharge path model.

Figure 3.2 Circuit schematic for estimating $I_{\text{peak}}$.

Figure 3.3 WCSP placed on the field plate of the FICDM tester.
The capacitance $C_{\text{die-sub-back}}$ can be calculated as per Equation 2.9 in Section 2.1.3. The capacitance $C_{\text{DUT}} = C_{\text{die-sub-back}}$. Substrate discharge path impedance can be lumped to form $R_{\text{discharge}}$ as shown in Equation 3.1:

$$R_{\text{discharge}} = \frac{\rho_{\text{sub-die}}}{A_{\text{die}}}$$  \hspace{1cm} (3.1)

The sequence of steps to estimate $I_{\text{peak}}$ is summarized in Figure 3.4.

3.3 Emulating the Oscilloscope Bandwidth Limitation

The bandwidth of the oscilloscope used to monitor the peak current of the chips during FICDM testing is specified as 1 GHz in the JEDEC standard and 1 GHz or 3.5 GHz in the ESDA standard. However, the CDM discharge currents have been shown to contain higher frequency components in them. Therefore, the waveform measured by a 1 GHz or 3.5 GHz oscilloscope is not the true waveform of the CDM discharge current [39]. The true waveform can be observed
only if measured by a scope of 8 GHz to 12 GHz. Therefore, it is important to know the bandwidth of the scope used to measure the CDM discharge current.

In circuit simulations, the discharge current measured through the pogo pin is not limited by any bandwidth restriction. To emulate the bandwidth limitation of the oscilloscope used for recording the waveform of the FICDM discharge current, a filter was introduced in the circuit simulation of peak current. Implementation of the filter enables a fair comparison between the simulated current waveform and the data measured by a low bandwidth oscilloscope. The user can specify the bandwidth of the oscilloscope to the simulation tool. A low pass RC filter is used to attenuate the higher frequency contents of the simulated CDM discharge current. The RC low pass filter used in this work is shown in Figure 3.5. $I_{\text{CDM}}$ is the current-controlled current source that replicates the current flowing through the pogo pin in Figure 3.2. $I_{\text{filtered}}$ is the current measured at the oscilloscope. At high frequencies, the capacitor C acts as a short and most of the current is diverted away from the resistor branch. At low frequencies, most of the current flows through the resistor.

![Figure 3.5 Low-pass RC filter implementation. A single pole RC filter was chosen for simplicity and ease of implementation. Higher-order, complex filters could be used to emulate the bandwidth limitation of the oscilloscope.](image)

The values of the components in Figure 3.5 are chosen to satisfy the Equation 3.2 based on the bandwidth limitation specified by the user. If the bandwidth of the scope used for the measurement is $f_H$. 
\[ \tau = R \cdot C = \frac{1}{2\pi f_H} \]  (3.2)

Value of one of the components \((R \text{ or } C)\) can be chosen arbitrarily and the value of the other component \((C \text{ or } R)\) can be chosen based on Equation 3.2.

### 3.4 Chapter Summary

A fully automated method to estimate the peak value of the CDM discharge current for a given packaged IC was presented for the first time. The setup time required to use the tool is very small compared to that of the 3D EM simulation based method. The measurement data from several packaged components and the tool runtime data is summarized in Chapter 4.
4. EXPERIMENTAL VERIFICATION OF CIRCUIT SIMULATION RESULTS

Design guidelines for CDM-ESD reliability of packaged integrated circuits were experimentally verified by two test chips. The experimental results demonstrate the robustness of the previously proposed ESD protection strategies for power domain crossing circuits [14] and inter-die signal paths [15]. Additionally, the experimental results show a good agreement with the circuit-level simulation of CDM-ESD reliability, demonstrating that the circuit simulations may be used to assess CDM reliability of system-in-package prior to fabrication and assembly. Section 4.1 presents the measurement data from a 90 nm test chip that was specifically designed to study CDM robustness of the power-domain crossing circuits. Section 4.2 presents a brief overview of the stacked die test chip designed to study the CDM reliability of the inter-die interface circuits and the corresponding measurement results.

4.1 Experimental Verification on 90 nm Test Chip

This section reviews and analyzes the measurement results for a test chip that was designed at the University of Illinois at Urbana-Champaign (UIUC) in collaboration with United Microelectronics Corporation (UMC). The chip was fabricated in a standard 90 nm CMOS process. The test chip I/O ring was designed at UMC; the core circuitry and some of the ESD protection devices were designed at UIUC by graduate student Nick Olson [27]. Both bare dies and packaged dies were provided to our group. The packaged dies were subjected to JEDEC FICDM testing at UMC as per the test plan provided by the UIUC. Leakage tests and functional tests were conducted by Nick Olson on the stressed and the unstressed packaged devices. The test chip design and the measurement results are presented next.
4.1.1 90 nm Test Chip Design

The die size was 4 mm x 2 mm and consisted of 64 bondpads. The dies were wire-bonded to a thin QFP package of size 20 mm x 14 mm consisting of 100 pins. The size of the die-attach plate was 6 mm x 6 mm. The package was modeled as per the 2D method described in Section 2.1.1. Table 4.1 lists the maximum and minimum lead lengths and the corresponding partial self-inductances ($L_{\text{pin}}$), capacitances to the field plate ($C_{\text{pin-fp}}$) and resistance values. The values indicated in Table 4.1 were used to construct a distributed simulation model for the package as shown in Figure 2.4.

Table 4.1 Values of the lead inductance, pin capacitance, resistance values.

<table>
<thead>
<tr>
<th></th>
<th>Lead Length (mm)</th>
<th>$L_{\text{pin}}$ (nH)</th>
<th>$C_{\text{pin-fp}}$ (fF)</th>
<th>$R_{\text{pin}}$ (Ω)</th>
<th>$C_{\text{die-plate-fp}}$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max. Value</td>
<td>10.35</td>
<td>6.4</td>
<td>76</td>
<td>92</td>
<td>460</td>
</tr>
<tr>
<td>Min. Value</td>
<td>6.04</td>
<td>3</td>
<td>46</td>
<td>52</td>
<td>460</td>
</tr>
</tbody>
</table>

The test chip contains five isolated power domains, as depicted in Figure 4.1. External I/O pins connect to pads in the VDDIO1, VDDIO2 and VDDANA domains. VDDIO1 and VDDIO2 domains contain CMOS digital I/O circuits, each of which is protected by either a snapback clamp or a dual-diode circuit. The input circuits in VDDANA are differential amplifiers, which is typical for a high-speed receiver. Detailed description of the test chip design can be found in [27]. Two versions of the test chip were fabricated; these are referred to as TC1 and TC2. There are three main differences between the two test chips: the types of rail clamps
used in the I/O domains were changed, the amount of decoupling capacitance in VDDIO2 was reduced in TC2, and some dummy logic and some domain crossing circuits were removed from TC2.

Figure 4.1. Two banks of identical cross-domain circuits were placed on the test chip. They are referred to as bank A and bank B. The figure was taken from [27].

Signal lines cross from the VDDIO1 to the VDD1 domain, from VDD1 to VDD2, from VDD2 to VDDIO1, from VDDIO2 to VDD1, and from VDD2 to VDDIO2. CDM-induced failures are expected only at the interface between the two 1 V power domains, VDD1 and VDD2. A total of 24 signal lines cross from VDD1 to VDD2. In each case, both the driver and the receiver are a CMOS inverter. There are twelve unique domain crossing circuits in bank A and these are replicated bank B; bank A and bank B are depicted in Figure 4.1. A variety of ESD clamps are placed at the 12 domain crossing circuits within one bank, as listed in Table 4.2. Interface #7 and #8 have ESD clamps at the gate of the receiver. Interface #9 has anti-parallel diodes between the driver and the receiver ground nets placed very close to the domain crossing circuits.
Table 4.2 Domain crossing interface circuits. ESD protection was 8 µm wide except for the APD whose perimeter was 75 µm. This table is borrowed from [27].

<table>
<thead>
<tr>
<th>Interface #</th>
<th>Driver Width (NMOS µm /PMOS µm)</th>
<th>ESD Protection</th>
<th>Receiver Width (NMOS µm /PMOS µm)</th>
<th>Wire Length (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>(1.2/3)</td>
<td>-</td>
<td>(0.12/0.3)</td>
<td>300</td>
</tr>
<tr>
<td>2</td>
<td>(1.2/3)</td>
<td>-</td>
<td>(0.12/0.12)</td>
<td>300</td>
</tr>
<tr>
<td>3</td>
<td>(1.2/3)</td>
<td>-</td>
<td>(0.12/1.2)</td>
<td>300</td>
</tr>
<tr>
<td>4</td>
<td>(1.2/1.2)</td>
<td>-</td>
<td>(0.12/0.2)</td>
<td>300</td>
</tr>
<tr>
<td>5</td>
<td>(1.2/12)</td>
<td>-</td>
<td>(0.12/0.3)</td>
<td>300</td>
</tr>
<tr>
<td>6 (Inverted Logic)</td>
<td>(1.2/0.3)</td>
<td>-</td>
<td>(0.12/0.3)</td>
<td>300</td>
</tr>
<tr>
<td>7</td>
<td>(1.2/0.3)</td>
<td>GCNMOS+GCPMOS</td>
<td>(0.12/0.3)</td>
<td>300</td>
</tr>
<tr>
<td>8</td>
<td>(1.2/0.3)</td>
<td>GCNMOS</td>
<td>(0.12/0.3)</td>
<td>300</td>
</tr>
<tr>
<td>9</td>
<td>(1.2/0.3)</td>
<td>Local APD</td>
<td>(0.12/0.3)</td>
<td>300</td>
</tr>
<tr>
<td>10</td>
<td>(1.2/0.3)</td>
<td>-</td>
<td>(0.12/0.3)</td>
<td>1000 (serpentine pattern)</td>
</tr>
<tr>
<td>11</td>
<td>(1.2/0.3)</td>
<td>-</td>
<td>(0.12/0.3)</td>
<td>5</td>
</tr>
<tr>
<td>12</td>
<td>(1.2/0.3)</td>
<td>-</td>
<td>(0.12/0.3)</td>
<td>1000 (straight)</td>
</tr>
</tbody>
</table>

Figure 4.2 shows the pad arrangement and the power and the ground bus structure on the die. The power and the ground bus in the I/O ring were modeled as per the method described in Section 2.2.2. In addition, the core ring consisting of all the power and the ground nets were also modeled. The metal straps that connected the core ring to the I/O ring were also modeled.
Figure 4.2 Pad arrangement and the power/ground bus structure of the 90 test chip. VSSANA is connected to VSS2 through APDs as shown in the diagram. It is isolated from the rest of the ground busses. VSS1 and VSS2 nets are connected to each other and both the nets are connected to VSSIO1 and VSSIO2 through APDs. Power nets are isolated from each other. Picture is sourced from [27] and modified.

4.1.2 FICDM Measurement Results of Power Domain Crossing Circuits

No failures were seen at the 250 V or 500 V pre-charge voltage levels. At 1000 V, some cross-domain circuits in Bank B failed, while none in Bank A failed. This result was found for both TC1 and TC2 version of the test chip. The average measured peak current for 20 zaps at 1000 V was 10.6 A. The detailed results for TC2 and TC1 are shown in Figure 4.3 and Figure 4.4 respectively. All the failures are hard failures causing a stuck-at fault at the cross-domain interface. The failure incidence is higher for TC2 than for TC1. These results suggest that the cross-domain voltage stress is higher in bank B than in bank A, and higher on TC2 than on TC1.

Refer to Figure 4.3. The three cross-domain circuits with ESD protection (interface circuits #7, 8 and 9 in Table 4.1) passed 1000 V pre-charge voltage stress. Two of these cross-
domain circuits are protected by small voltage clamps at the receiver input; the protection devices were only 8 µm wide and thus do not greatly load the driver. The third “safe” cross-domain circuit has a “local APD” type protection circuit; here, the protection devices are not on the signal path and will have no effect on circuit performance, i.e., delay. Circuit simulations had accurately predicted that the interface circuits #7, 8 and 9 would survive the CDM stress. Despite the local APD having been effective in this design, it is not recommended to use this method unless post-layout CDM circuit simulations are undertaken as part of the design process. The design parameters for implementing the local APD method of ESD protection are explained in Section 4.1.2.3 with the help of simulation results. When VDD1 pins are zapped, the only cross-domain circuit to fail is #5, with the large PMOS device in the driver. Simulations indicate that increasing the width of this device decreases its source-drain voltage drop during CDM, and consequently increases the voltage stress across the receiver gate oxide [14].

![Figure 4.3 Bank B cross-domain failure rates on TC2 for the VDD1, VSS1, I/O pins and VSS2 pin zaps. These results showed increased failure rates compared to the TC1 results. Data borrowed from [27].](image-url)
4.1.2.1 CDM Failure Differences in TC1 vs. TC2

There are three main differences between TC1 and TC2: the types of rail clamps used in the I/O domains were changed, the amount of decoupling capacitance in VDDIO2 was reduced in TC2, and some dummy logic and some domain crossing circuits were removed from TC2. These last changes were made to free up room for standalone test structures. It is assumed that the cross-domain voltage stress is higher on TC2 since more failures occur on those chips. CDM simulations confirm this conjecture and indicate that the cause for this difference is that the capacitance of the VDD1 domain on TC2 is 35% lower than on TC1. Reduced capacitance in the VDD1 domain increases the voltage drop between VDD1 and VSS1 leading to higher stress across the receiver at the domain crossing [14].

4.1.2.2 Bank A vs. Bank B

The dramatically different failure rates between the bank A and bank B circuits are attributed to the difference in the ground bus routing and the corresponding change in ground bus resistance. The lumped models for a bank A and bank B interface circuit are shown in Figure...
Figure 4.5 and Figure 4.6, respectively. Circuit simulation results in Figure 4.7 show that indeed a larger voltage stress is experienced by the bank B receiver. Circuit simulations also show that the worst case stress occurs when the VSS2 pins are zapped, consistent with the measurement results. For domain crossing circuits in bank A, the receiver ground connects to the VSS2 bus in the inner bus ring at node E, and $V_{GS}$ of the receiver NMOS is given by:

$$V_{GS}^A \approx V_A - V_E$$  \hspace{1cm} (4.1)

$$V_A - V_E = (V_A - V_B) + I1 \cdot R_{VSS1b} + I2 \cdot R_{VSS1a} + V_{APD} + I4 \cdot R_{VSS2a} - (I5 \cdot R_{VSS2b})$$  \hspace{1cm} (4.2)

In bank B, the receiver grounds connect to the VSS2 bus at node D in the pad ring, and the receiver NMOS $V_{GS}$ is given by:

$$V_{GS}^B \approx V_A - V_D$$  \hspace{1cm} (4.3)

$$V_A - V_D = (V_A - V_B) + I1 \cdot R_{VSS1b} + I2 \cdot R_{VSS1a} + V_{APD} + I4 \cdot R_{VSS2a}.$$  \hspace{1cm} (4.4)

Equations 4.2 and 4.4 indicate that the receivers in bank B experience stress that is larger by the amount $I5 \cdot R_{VSS2b}$. The value of $R_{VSS2b}$ is layout and floorplan dependent; it depends on the power/ground bus routing from the core circuitry to the inner bus ring and the distance from that connection point to the pad being zapped.
Figure 4.5 Cross-domain circuit in Bank A. VSS2 pad at point “D” is zapped. The receiver source is connected to point “E” in the I/O ring. The amount of stress is lowered by the amount $I_3 \cdot R_{VSS2b}$.

Figure 4.6 Cross-domain circuit in Bank B. The receiver source is connected to point “D” in the I/O ring. The receiver sees higher stress compared to the receiver shown in Figure 3.5.
Figure 4.7 Comparison of the voltage stress ($V_{gs}$) at the receiver NMOS in Bank A vs. Bank B when Pin 12, a VSS2 pin was zapped after the component was pre-charged to positive 500 V. Through simulations, Pin 12 was found to generate the highest stress across the Bank B receiver.

4.1.2.3 Impact of Local APD

Figure 4.8 shows a schematic a domain crossing circuit with the receiver, driver, the APDs, and the lumped ground bus resistance to the VSS pad. The effect of bus resistance R1 and R2 is shown in Figure 4.9. The voltage stress is for a peak current of 3 A flowing from driver domain to the receiver domain. For this protection strategy to be effective, the resistances R1 and R2 have to be very low. Other parameters such as the size of the local APD, size of the I/O ring APD and the bus resistance between the I/O ring APD and the local APD ($R_{VSS1-core}$ and $R_{VSS2-core}$) also impact the stress at the receiver. Therefore, careful transient simulations are needed to verify that the stress seen by the receiver is not enough to damage the oxide at the desired CDM stress level.

In the 90 nm test chip the local APD perimeter was 75 µm. The resistances between the local APD and the NMOS source nodes were about 1.5 Ω each (R1 + R2 = 3 Ω). The resulting voltage stress was less than NMOS $BV_{ox}$ of 5.2 V even at 1000 V pre-charge ($I_{peak} = 10.6$ A) as inferred from the measurement results. It is recommended that $R_{con}$ be less than 1 Ω and APD
perimeter be 25 µm to increase the area savings. This protection strategy was employed on the 65 nm test chip.

Figure 4.8 Cross-domain circuit protected by an additional APD in the core physically placed very close to the cross-domain circuit. R1, R2, RVSS1a and RVSS2a are the important resistances that determine the stress across the receiver. If RVSS1a and RVSS2a are too large, the local APD is not sufficient to protect the receiver gate oxide.

Figure 4.9 Effect of parasitic resistance connecting the driver and receiver transistors to the local APD terminals for various perimeters (42 µm, 126 µm and 210 µm) of the diodes in the local APD. Perimeter of APD in the I/O ring is 210 µm. Rvss1-core and Rvss2-core are 6 Ω each. This is the parasitic resistance to the APD in the I/O ring.

4.1.3 FICDM vs. Wafer Level Test Measurement Results

In N. Jack’s work [40], primary inputs in the VDDANA domain were stressed on wafer level testers such as WCDM and VFTLP testers. The pins were also stressed on FICDM tester at UMC. N. Jack [40] found that the failure currents were lower on the wafer level testers than
those on FICDM tester. The study [40] suggested that the differences in the failure currents were potentially caused by the filtering of the transient current waveform by the long leads present in the 90 nm test chip package. The inputs in the analog domain were protected by ESD protection devices that exhibit transient voltage overshoots when conducting currents with fast rise time (few hundred pico seconds). Therefore, the study suggested that though the current measured at the pogo pin had a fast rise time (~250 ps), the rise time probably degraded to about 600 ps at the pad. The ESD protection device experienced a 600 ps rise time instead of 250 ps. Whereas in the case of the bare die, the current pulse is applied right at the pad and the rise time the device experiences is expected to be 250 ps. Slower rise time at the ESD protection device in the case of FICDM tester was attributed to be the primary reason for the lower voltage stress and therefore, the higher failure current.

Table 4.3 compares the failure current values for the two input pads after the FICDM and the wafer level test methods. The data was taken from [40]. The polarity of the stress is such that the discharge current enters the chip. Input 1 was protected by STI diodes and Input 2 was protected by SCR protection device. Simulations were used to compare the voltage stress and the current rise time at the bondpads corresponding to Input 2.

Table 4.3 Comparison of the failure currents for Input 1 and Input 2 after FICDM and Wafer level CDM stress tests. Capacitively coupled transmission line pulsing (CCTLP) stress results on the packaged and the bare die are also compared in the table.

<table>
<thead>
<tr>
<th>Input Pad</th>
<th>ESD Protection Device</th>
<th>JEDEC FICDM (Packaged)</th>
<th>WCDM (Bare Die)</th>
<th>CCTLP Packaged</th>
<th>CCTLP Bare Die</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input 1</td>
<td>STI Diodes (60 μm perimeter)</td>
<td>10.6 A</td>
<td>3.8 A</td>
<td>5.75 A</td>
<td>5 A</td>
</tr>
<tr>
<td>Input 2</td>
<td>DTSCR (25 μm width)</td>
<td>5.7 A</td>
<td>1.2 A</td>
<td>1.2 A</td>
<td>1 A</td>
</tr>
</tbody>
</table>
FICDM circuit simulations were performed with negative pre-charge voltages stressing the package pin corresponding to Input 2. Both the lumped and the distributed package lead model were used for the simulations. The 1-stage model refers to a lumped RLC model for the package leads. The 3-stage and 5-stage models refer to the models where each package lead was represented by a 3-stage π model and a 5-stage π model respectively. Current at the pogo-pin and the current at the bondpad on the die are plotted in Figure 4.10 through Figure 4.12. The simulations results indicate no degradation in the rise time (measured 10%-90% of peak value). The peak current measured at the pogo pin is the same as that at the bondpad.

Figure 4.10 Current waveform at the pogo pin and at the pad simulated using a lumped RLC model for the package pin being zapped. There is no significant difference in the rise time or peak current for the waveform at the pad compared to that at the pogo pin.
Kireev et al. [41] modeled the package traces as transmission lines and studied the differences between the peak current at the pogo pin and that at the bondpad. Their study indicated that there was no change in the rise time of the current. However, they modeled the traces as 50 Ω transmission lines. This may not be accurate in the case of the packaged device placed on the field plate of FICDM tester. In this context, the true AC grounds are the field plate.
and the ground plate of FICDM tester. Therefore, package trace characteristic impedance needs to be modeled treating the FICDM tester plates as the reference ground planes. For the 90 nm test chip, the characteristic impedance for the package lead was calculated and found to be around 300 Ω. FICDM circuit simulations were repeated with the 50 Ω and 300 Ω transmission line model and the results are plotted in Figure 4.13 and Figure 4.14. Simulations indicate no degradation in the rise time.

Figure 4.13 Simulation plots of current at the pogo pin and that at the pad simulated with the package pin modeled as a transmission line with $Z_0 = 50$ Ω.
Figure 4.14 Simulation plots of current at the pogo pin and that at the pad simulated with the package pin modeled as a transmission line with $Z_0 = 300 \, \Omega$.

Table 4.3 also reports the failure currents of CCTLP stress on the packaged test chip and compares it with the bare die. The FICDM failure current is only 20% higher for Input 2 and 15% higher for Input 1. Considering the variation in oxide breakdown voltages, the differences in the failure currents can be considered as negligible. Simulation results and the CCTLP measurement results seem to indicate that there is no degradation in the rise time the current. Therefore, this study concludes that the rise time degradation may not be the factor causing the differences between the failure current levels after FICDM and those after WCDM tests. Further investigation is suggested through additional experimental verification through test chips. It is also suggested to re-stress the analog input pins of the 90 nm test chip on commercial FICDM tester.

4.2 Experimental Verification on 65 nm Test Chip

Shukla and Rosenbaum [15] presented a circuit simulation methodology and simulation results on a hypothetical test chip to analyze the CDM-ESD reliability of wire-bonded stacked-die components. It was found that the design of the power delivery network greatly affects the
CDM-ESD reliability of wire-bonded stacked-die components. Subsequently, a 65 nm test chip was designed by Nick Olson [17], graduate student at University of Illinois at Urbana-Champaign. The chip was packaged in either a single die or doubly stacked die configuration. The signal flow through the test chip was such that the locations of circuits failing due to CDM stress can be identified [15].

### 4.2.1 Description of the 65 nm Test Chip

A 2 mm x 2 mm test chip was designed in a 65 nm low power CMOS process. The dies were packaged in a 7 mm x 7 mm BGA package either alone or in a doubly stacked configuration. The on-die pads were connected to the package substrate using wire bonds. In the stacked-die components, the die-to-die signal connections were made by wire bonding directly between the two die. An overview of the design is given in Figure 4.15.

In the stacked parts, there are four signal lines running from the top die to the bottom die and four running from the bottom to the top; these interfaces are labeled TB1 through TB4 and BT1 through BT4, respectively. Based on circuit simulations, a different protection scheme was selected for each of these interfaces, as summarized in Table 4.4.
As indicated in Figure 4.15, there are two power domains on each die. Power domain crossing circuits are known to be susceptible to CDM-induced damage. There are power domain crossing circuits on seven of the datapaths that traverse each die. A variety of ESD protection circuits were placed at the domain-crossing circuits; these are listed in Table 4.5.
Table 4.5 ESD protection at the domain-crossing interfaces. Local APD denotes anti-parallel diodes placed on the ground busses local to the driver and receiver. The pass gate descriptor is NMOS/PMOS width.

<table>
<thead>
<tr>
<th>Path</th>
<th>Name</th>
<th>Local APD</th>
<th>Local Clamp</th>
<th>Series Resistor</th>
<th>Local Decoupling Capacitor</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Control</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>2</td>
<td>Pass Gate</td>
<td>None</td>
<td>None</td>
<td>2.5/5µm pass gate</td>
<td>None</td>
</tr>
<tr>
<td>3</td>
<td>Dual Diode 1</td>
<td>None</td>
<td>6.5/12.5µm dual diode</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>4</td>
<td>VSS2b</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>5</td>
<td>Dual Diode 2</td>
<td>None</td>
<td>25µm dual diode</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>6</td>
<td>Local APD</td>
<td>25µm</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
<tr>
<td>7</td>
<td>Dual Diode + Resistor</td>
<td>None</td>
<td>25µm dual diode</td>
<td>25Ω</td>
<td>None</td>
</tr>
<tr>
<td>8</td>
<td>Local Decap</td>
<td>25µm</td>
<td>None</td>
<td>None</td>
<td>30pF each side</td>
</tr>
</tbody>
</table>

4.2.2 Measurement Results

4.2.2.1 Measurement of Stand-Alone Devices for Compact Modeling

Gate oxides of stand-alone thin oxide NMOS and PMOS transistors were subjected to VFTLP stress and the breakdown voltages (BV$_{ox}$) were recorded for these transistors in the inversion and the accumulation stress modes. The BV$_{ox}$ values are shown in Figure 4.16 and Figure 4.17.

![Figure 4.16 Gate oxide breakdown voltage of four samples of NMOS measured with a 5 ns VFTLP stress in the inversion and the accumulation mode. The spread of the BV$_{ox}$ values is indicated by the background color. The average BV$_{ox}$ value of the four samples is indicated by the dashed line.](image)
Figure 4.17 Gate oxide breakdown voltage of four samples of PMOS measured with a 5 ns VFTLP stress in the inversion and the accumulation mode. The spread of the $B_{V_{ox}}$ values is indicated by the background color. The average $B_{V_{ox}}$ value of the four samples is indicated by the dashed line.

The transient and quasi-static I-V characteristics of the APDs used in the I/O ring were measured. Measured I-V characteristics are shown in Figure 4.18. VFTLP pulses with 2.5 ns width and 100 ps rise time were used to characterize the APD. One can see significant voltage overshoot at high current levels. The test chip consisted of two pairs of APDs in the I/O ring. Full chip simulations indicated that roughly 35% of $I_{\text{peak}}$ flows through each pair of APD when a pin in the VSS2 domain is stressed. For an $I_{\text{peak}}$ of 8 A with 100 ps rise time, the currents through the each APD is roughly 2.5 A. At 2.5 A, the peak voltage drop across the APD is around 4.5 V. The quasi-static voltage drop is about 2.5 V. Therefore, it is important to characterize the overshoot voltage in the diodes carrying high currents. The I-V plots were used to obtain diode compact model [30] that accurately predicted the peak voltage drop before the manifestation of conductivity modulation.

Figure 4.19 shows the transient and quasi-static voltage drops across the 25 µm perimeter diode in the local APD. These diodes are in the core region. Simulations show that the peak
current through these diodes does not exceed 1 A even for a CDM discharge with an $I_{\text{peak}}$ of 16 A at the stressed pin. Therefore voltage overshoot is not a concern for these diodes.

![Graph 1](image1.png)

**Figure 4.18** Transient peak and quasi-static I-V characteristic of the diode in the I/O ring APD. Transient overshoot voltage is significant at high current levels.

![Graph 2](image2.png)

**Figure 4.19** Transient and quasi-static I-V characteristics of the 25 µm perimeter diode in the local APD.
4.2.2.2 Inter-Die Interface Circuits

Circuit simulation of a hypothetical component, consisting of stacked die in a CSP, indicated that a small ESD protection device placed at the receiver input is sufficient to protect the inter-die interface circuits, provided the ground nets of the die are connected together at the package level [15]. The pre-silicon simulations results, shown in Figure 4.20, indicated that even the receiver at TB3 will survive the CDM testing.

![Figure 4.20](image-url)

Figure 4.20 $V_{gs}$ of the input transistors in the inter-die receivers located on the bottom die. The peak voltage stress is well below the oxide breakdown voltage.

Test chip measurements show that none of the inter-die interface circuits were damaged by CDM stressing of any ball up to +/- 2000 V, corresponding to a peak discharge current of about 11.5 A. Even interfaces BT3 and TB3 which have small dual-diodes at the receiver (25 μm perimeter), no series resistor, and no protection at the driver, are not damaged by the CDM stress. This clearly demonstrates that full-sized ESD protection devices were not needed, nor was a series resistor. As these extra elements limit the bandwidth and thus the data rate, it is advantageous to eliminate them.
A custom-configured CDM tester was then used to stress the units at a higher current up to 15 A. TB4 failed at this current level. From Table 4.4, this path has a full size ESD protection at the driver and a very small pair of ESD diodes at the receiver. The simulations had predicted that TB4 was more likely to fail prior to other paths that have protection only at the receiver as shown in Figure 4.20. TB4 consists of a transmitter with full-sized ESD protection diodes and a receiver with only a small secondary diode protection with no series resistor. Therefore, a higher amount of current enters through the full-sized ESD protection diodes at the transmitter through the signal interface line into the small diodes at the receiver. The higher currents through these diodes led to higher voltage drop across the gate oxide in the receiver NMOS. TB2/BT2 and TB3/BT3 interfaces do not consist of ESD protection diodes at the transmitter. Even though TB1/BT1 interfaces consist of full-sized ESD protection at the transmitter, the series resistor at the receiver prevents flow of any substantial amount of current.

4.2.2.3 Impact of Stacking on the CDM Stress

The peak discharge current measured during FICDM testing, I_{peak}, can be roughly modeled as a function of the pre-charge voltage and three capacitances, C_{DUT}, C_G, and C_{FG}, shown in Figure 4.21 (a). C_{DUT} has two components: C_{die}, the capacitance between the die stack and the field plate, and C_{pkg}, the capacitance between the conductive portions of the package and the field plate. As shown in Figure 4.21(b) and Figure 4.21(c), for a fixed package height, T_{pkg}, and package area, only C_{DUT} varies with the number of die in the stack. This change is mitigated if the dies are thinned before stacking. In this work, the die packaged singly were 250 μm thick, whereas those packaged in a double-stack were 150 μm thick. Furthermore, the C_{pkg} portion of C_{DUT} was larger than the C_{die} portion, and C_{pkg} is invariant with the number of die in the stack. As a result, I_{peak} was not expected to vary significantly between the single die and two die
components. Simulations predicted that the peak discharge current for the doubly stacked test chips would only be around 15% higher than for the single die components. This is less than the 20% (or more) zap to zap variation in $I_{\text{peak}}$ obtained during FICDM testing at a constant pre-charge voltage. Therefore, it was not expected that a significant difference would be observed between the $I_{\text{peak}}$ values for single and two die components.

The average peak currents recorded during CDM testing at each of the pre-charge voltages are plotted in Figure 4.22. There is no significant difference in the peak current between the single die and the stacked die components, in agreement with the simulation results.

Figure 4.21(a) Three-capacitor model for a device on a FICDM tester. $C_{FG}$ is the capacitance between the field plate and the ground plate. $C_{DUT}$ is the capacitance formed by the DUT with the field plate. $C_G$ is the capacitance between the DUT and the ground plate. (b) Single-die package on a CDM tester. (c) Two die are offset stacked in the same package. $T_{\text{pkg}}$ remains the same in both cases. Due to die thinning, $T_{\text{die2}}$ is comparable to $T_{\text{die1}}$; therefore $C_{\text{die1}} \approx C_{\text{die2}}$. 
Figure 4.22 Average peak CDM current vs. precharge voltage. The $I_{\text{peak}}$ values for the single-die components are virtually indistinguishable from those for the stacked-die components. 6-GHz and 8-GHz oscilloscopes were used to measure the current waveforms. This plot was borrowed from [17].

4.2.2.4 Reliability of Domain Crossing Circuits: Single Die

The stress at the on-die domain-crossing circuits was also simulated prior to chip tape-out. For single-die components, the simulation results shown in Figure 4.23 suggested that the domain-crossing circuits on signal paths 1, 2 and 6 would fail when the peak discharge current is around 10 A. Additional simulations indicated that none of the other paths would fail even at 20 A. These predictions were made assuming that the gate breakdown voltage, $B\text{V}_{\text{ox}}$, of an NMOS biased in inversion is at least 5.4 V, a result obtained from 100 ns TLP testing of MOS gate oxides.
Figure 4.23 Voltage stress at the on-die cross-domain receivers along signal paths 1, 2, and 6 – plot of receiver NMOS Vgs. Positive CDM zap at a VSS2 ball. The peak discharge current is 10 A. Path 1 has no ESD protection at the receiver.

The experimental results for the single-die components are tabulated in Table 4.6. Only paths 1, 2 and 6 failed during CDM testing, a finding predicted by the circuit simulations. Domain crossing circuit, Path 1, failed at a +1000V pre-charge voltage, or a peak current of 8 A, which is a little lower than that predicted by the simulations, but is not unexpected given the variability of the oxide breakdown voltage. At CDM stress currents of 11 A and above, there were higher incidences of failures on paths 1, 2 and 6, in accordance with the simulation-based predictions. Simulations were also correct in predicting that the Path 1 would see higher stress than paths 2 and 6. The predictions were supported by the measurement results which show that Path 1 failed at 8 A, whereas paths 2 and 6 started failing at higher stress currents.
Table 4.6 Failures induced in the single-die components at the domain-crossing interface circuits. Failures were seen for CDM pre-charge voltages as low as 1000 V. The least robust circuit was the control circuit (#1) with no ESD protection. “Both” in the stress polarity column indicates that the functional and the leakage tests were conducted after both the positive and the negative CDM tests were done. Otherwise, the functional and the leakage tests were conducted after each polarity of the test at the indicated pre-charge voltage. Table taken from [15].

<table>
<thead>
<tr>
<th>Path</th>
<th>Failure Rate #Fail/#Tested Pos.:Neg.</th>
<th>Pre-charge Voltage</th>
<th>Stress Polarity</th>
<th>Stress Location</th>
<th>ESD Protection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1/3</td>
<td>1000</td>
<td>Both</td>
<td>All pins</td>
<td>No ESD</td>
</tr>
<tr>
<td>1</td>
<td>3/3</td>
<td>1500</td>
<td>Both</td>
<td>All pins</td>
<td>No ESD</td>
</tr>
<tr>
<td>2</td>
<td>3/3</td>
<td>1500</td>
<td>Both</td>
<td>All pins</td>
<td>Pass Gate</td>
</tr>
<tr>
<td>6</td>
<td>3/3</td>
<td>1500</td>
<td>Both</td>
<td>All pins</td>
<td>Local APD</td>
</tr>
<tr>
<td>1</td>
<td>1/2</td>
<td>2000</td>
<td>Positive</td>
<td>Output</td>
<td>No ESD</td>
</tr>
<tr>
<td>6</td>
<td>1/2</td>
<td>2000</td>
<td>Negative</td>
<td>Output</td>
<td>Local APD</td>
</tr>
<tr>
<td>1</td>
<td>2/3:1/1</td>
<td>2000</td>
<td>Positive/Negative</td>
<td>VDD2</td>
<td>No ESD</td>
</tr>
<tr>
<td>2</td>
<td>1/3</td>
<td>2000</td>
<td>Negative</td>
<td>VDD2</td>
<td>Pass Gate</td>
</tr>
<tr>
<td>6</td>
<td>2/3</td>
<td>2000</td>
<td>Positive</td>
<td>VDD2</td>
<td>Local APD</td>
</tr>
<tr>
<td>1</td>
<td>2/3:2/2</td>
<td>2000</td>
<td>Positive/Negative</td>
<td>VSS2</td>
<td>No ESD</td>
</tr>
<tr>
<td>2</td>
<td>1/3</td>
<td>2000</td>
<td>Negative</td>
<td>VSS2</td>
<td>Pass Gate</td>
</tr>
<tr>
<td>6</td>
<td>2/3:2/2</td>
<td>2000</td>
<td>Positive/Negative</td>
<td>VSS2</td>
<td>Local APD</td>
</tr>
</tbody>
</table>

Pin and polarity stress separation were done only at 2000 V or 12 A stress level. The results are summarized in Table 4.7. Failures were observed for both positive and negative CDM zaps. Prior to tape-out, simulations had indicated lower voltage stress for the negative zaps and therefore, failures were not expected for the negative zaps.

Table 4.7 Measured failures at 12 A (2000 V) FICDM stress. Pin and polarity stress separation occurred only at 2000 V. The failures that were not reproducible through circuit simulations are highlighted by bold, italicized text in red color.

<table>
<thead>
<tr>
<th>Pin Stressed</th>
<th>Domain Crossing</th>
<th>VDD2</th>
<th>VSS2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path 1 (Control)</td>
<td>POS/NEG</td>
<td>POS/NEG</td>
<td></td>
</tr>
<tr>
<td>Path 2 (Pass Gate)</td>
<td>NEG</td>
<td>NEG</td>
<td></td>
</tr>
<tr>
<td>Path 6 (Local APD)</td>
<td>POS</td>
<td>POS/NEG</td>
<td></td>
</tr>
</tbody>
</table>
After analyzing the measurement results and measuring the transient I-V characteristics of stand-alone APDs, the on-die circuit models were updated with the correct transient I-V models. Simulations were performed with the improved models. The results are presented next.

Figure 4.24 shows the simulated voltage stress across the receiver NMOS gate oxide in Path 1 for a VSS2 pins stress. For positive stress of 9 A, the voltage stress is higher than BV_{ox-inv}. The measurement results indicated failures at 8 A with a failure rate of 1/3. The simulation results are in agreement with the measurement results. For negative zap of 9 A stress, the voltage stress is only slightly lower than the BV_{ox-acc} value. Measurement results indicated failures after the negative stress of 11 A. There is no information about failures at negative stress of 8 A. Given the variability in the oxide breakdown voltages, it is safe to say that the simulations results correctly indicate that failures are possible for the negative stress of -11 A.

![Figure 4.24 Simulation plots for the positive and negative zaps on package ball K6 (VSS2 ball). The peak voltage stress for the positive zap of 9 A peak current stress is above the BV_{ox-inv} of NMOS device. The peak voltage stress for the negative zap of 9 A peak current stress is very close to the BV_{ox-acc} of NMOS device.](image)
Figure 4.25 shows the simulated transient voltage plots of the voltage stress across the PMOS gate oxide at the receiver of Path 1 circuit for a VSS2 pin stress. Based on the peak voltage stress values, one can safely conclude that VSS2 pin stresses did not cause any failures in the PMOS gate oxide. The failures in Path 1 due to VSS2 pin stresses are in the NMOS, as shown in Figure 4.24. Next, a possibility of a failure in the PMOS gate oxide is investigated for VDD2 pin zaps.

Figure 4.25 Simulated transient plots of $V_{gs}$ voltage stress across the PMOS gate oxide for positive and negative zaps on a VSS2 pin. The voltage stress is not severe enough to break the oxide at +/- 9 A. At 12 A (not shown in the plot), the positive zap may produce failures in the receiver PMOS.

Plots of simulated transient voltage stress across the PMOS gate oxide of Path 1 circuit during a zap on VDD2 pin are shown in Figure 4.26. Simulations indicate that PMOS in the receiver in Path 1 might have failed even at 6 A stress of positive polarity. Failures are possible even for negative zaps on the VDD2 pin as indicated by the simulation results, but at a slightly higher current. Measurement data with pin-specific stresses are available only at an $I_{peak}$ of 12 A as shown in Table 4.7. From Table 4.7, VDD2 pin zaps of positive and negative 12 A stress caused failures in Path 1. The simulation results agree very well with the measurement results at
12 A. However, based on the data from all-pin stress at lower currents, we know that Path 1 did not fail at 4 A but failed at 8 A. Therefore, the failures at 8 A could either be due to stress on VSS2 pins breaking the receiver NMOS oxide or that on VDD2 pins breaking the receiver PMOS oxide.

Simulated voltage stress across the receiver NMOS on Path 6 is plotted in Figure 4.27 for different peak current stresses. Simulations indicate that failures are possible at stresses higher than 9 A with positive stress polarity. Whereas, for negative stress polarity, the simulated voltage stress is not large enough to cause the gate oxide breakdown in the receiver NMOS gate oxide. Refer to Table 4.7. Measurement results indicate that there were failures after negative zaps on the VSS2 pins. Simulation results indicate otherwise. This discrepancy needs to be investigated further. Initial investigation shows that the body diode in the driver NMOS clamps the voltage across the body-drain terminals to a very low value (1 V) and the local APD clamps the voltage between the driver source and the receiver source to a low value (2 V). Therefore, the peak
voltage stress across the receiver NMOS gate-source terminals clamps to a value of 3 V as indicated by the simulation results. Performing circuit simulation with the RF model for the body diode of the driver resulted in higher voltage stress across the receiver gate oxide. However, the simulated I-V plots of the RF model of the body diode do not match with the measured I-V characteristics of the body diode. The RF model of the body diode is not accurate for large signal analysis and therefore not the correct model for use in CDM circuit simulations. Contradictions were also found between the measurement data and simulation results in the case of Path 2 (receiver protected by transmission gate circuit). Simulation results are discussed next.

Figure 4.27 Voltage stress across the receiver gate-source terminal in the domain crossing circuit protected by a local APD (Path 6). Simulations indicate failures for the positive zap. However, simulations do not show significant voltage stress for the negative zaps. Peak voltage stress for the negative zaps is encircled in the plot and the values are much lower than $BV_{\text{ox-acc}}$ of NMOS device.

Figure 4.28 shows transient voltage plots of receiver NMOS $V_{\text{gs}}$ at Path 2. For positive zaps, the voltage stress is not large enough to cause gate oxide breakdown. This is in agreement with the measurement results in Table 4.7. However, simulations also indicate that voltage stress is not large enough to cause failures during negative zap, in contrast to measurement results. The
voltage is clamped by the body diodes of the transmission gate circuit during both the positive and the negative polarity stresses. The parasitic body diodes in the transmission gate circuit are shown in Figure 4.29.

To summarize, in the case of Path 2 and Path 6, negative stress failures were not explainable by circuit simulations. In both of these cases, simulations indicated that the body diodes of the transistors in the driver circuit clamp the voltage to a low value. However measurement data indicated failures. Even though CDM circuit simulations using the RF model of the transistors in the driver circuit show higher voltage stress, the RF model is not physically accurate in the high voltage regime. Therefore, further investigation should involve characterizing the parasitic body diode of the actual driver circuit or the transmission gate under VFTLP stress. Physical failure analysis of the failure sites on the 65 nm single die test chip may also provide valuable insight into future research direction.

![Figure 4.28 Plots of simulated V_{gs} of the NMOS in the receiver of the domain crossing circuit protected by the transmission gate circuit (Path 2). Positive zaps of even 11 A does not produce enough voltage stress to break the oxide. Similarly, negative stress does not produce high enough voltage stress to break the oxide in accumulation mode. However, measurement results indicated failures only after negative stress on the VSS2 pin at 12 A stresses.](image)
Figure 4.29 (a) Body-to-drain and body-to-source diodes of the transistors in the transmission gate circuit are shown in red. The bulk nodes of the PMOS and the NMOS are connected to VDD2 and VSS2 respectively. (b) Equivalent representation of the transmission gate circuit. The circuit acts as local dual diode protection circuit at the receiver. \( R_{\text{gate}} \) is the channel resistance of the transmission gate.

### 4.2.2.5 Reliability of Domain Crossing Circuits: Single Die vs. Stacked Die

For the stacked-die components, simulations prior to tape-out predicted that the domain crossing circuits will see failures at peak currents of 15 A or higher. Typically, such high discharge currents are not observed at the commonly accepted pre-charge voltage level of 250 V even when large packages are stressed [6]. This implies that domain crossing circuits in the stacked die components are very robust if the individual dies share the discharge current during the CDM event. Sharing of the discharge current leads to a lower amount of current flow across the domain and thus resulting in a lower stress across the receiver gate oxides [15].

In the stacked die components, only Path 1 failed at 2000 V or 12 A of peak discharge current as indicated in Table 4.8 with a failure rate of 1/3. Figure 4.30 compares the domain crossing circuit failures in the stacked die with those in the single die package test chips. There is a lower number of failures in the stacked die test chip compared to the single die test chip.
Table 4.8 Failure induced in the stacked-die component at the cross-domain interface. The control circuit without any ESD protection (#1) is the only circuit that failed, failing after 2000 V CDM stress.

<table>
<thead>
<tr>
<th>Cross-domain</th>
<th>Failure Rate</th>
<th>Die Location</th>
<th>Stress Polarity</th>
<th>ESD Protection</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1/3</td>
<td>Top</td>
<td>Both</td>
<td>None</td>
</tr>
</tbody>
</table>

Figure 4.30 Comparison of the failures in the domain crossing circuits in the single die test chip versus that in the stacked die test chip.

Simulations indicated lower amount of current flowing across the domain in the case of stacked die test chip. This is because the capacitance between the package metal and the field plate, which is the largest component of $C_{DUT}$, is divided almost equally between the two die. The sharing of the current is further facilitated by the package-level ground net connections, as illustrated in Figure 4.31. For the specific case of a positive zap on a VSS2T ball shown in the figure, the maximum voltage stress across the receiver NMOS gate oxide on the top die is roughly equal to

$$V_{gs-stacked} \approx V_{power-clamp} + V_{APD} + 0.375 \times I_{peak} \times (R_{VSS1} + R_{VSS2}).$$  (4.5)
In contrast, refer to Figure 4.32 for the case of single die test chip. When a VSS2 ball is zapped, the voltage stress would be given by

\[
V_{gs\text{-}single} \approx V_{power\text{-}clamp} + V_{APD} + 0.75 \cdot I_{peak} \cdot (R_{VSS1} + R_{VSS2}).
\]  

(4.6)

Figure 4.31 Current flowing across the domain crossing circuit on the top die of the stacked die test chip is half of current that flows across the domain in the single die test chip.

Figure 4.32 Current flowing from the VSS1 domain to the VSS2 domain in the single die test chip when a pin belonging to VSS2 net is zapped. The current is twice the amount of current that flows across the domain on a die in the stacked die test chip.

From Equations 4.5 and 4.6, it is clear that \( V_{gs\text{-}stacked} \) is lower than \( V_{gs\text{-}single} \). The lower number of failures in the stacked die components confirms that due to sharing of the discharge
current, stress across the domain crossing circuits on each die is lower than that in the case of single-die component for the same peak current, in accordance with the simulation results.

4.3 Experimental Verification of the Peak Current Simulation Methodology

The methodology presented in Chapter 3 was applied to several designs to simulate $I_{\text{peak}}$. The simulated $I_{\text{peak}}$ values were compared with the measurement results on those designs. The results are listed in Table 4.9. The runtime was less than a minute for all of these designs. In all simulations, the appropriate tester standard and the bandwidth of the oscilloscope were specified. The measured current values listed in the table are the average of several pin zaps with three zaps per pin. The simulation results for all the designs are within 15% of the measured $I_{\text{peak}}$, except for the design labeled “UIUC Test Chip” and the WCSP version of Design D. In “UIUC Test Chip,” only 77 of the 144 balls were bonded to the die causing the measured $I_{\text{peak}}$ to be lower than the simulated $I_{\text{peak}}$. The traces connected to the floating balls of the package do not contribute to the $I_{\text{peak}}$. These traces only modify the capacitance of the neighboring traces that are bonded to the die and thus modifying the total charge storage by a small amount. The simulation tool can be enhanced to account for the details of die to package bonding. A marker layer could be used in the package layout-database to indicate the floating pins or traces, and the tool could be directed to neglect the capacitance contribution from such pins or traces. A case study is presented in Section 4.3.1 to illustrate the impact of the floating traces on the $I_{\text{peak}}$.

In the case of Design D, the QFN version of the design resulted in a higher $I_{\text{peak}}$ than did the WCSP version, even though the size of the QFN package is larger. In the case of WCSP version, the die is directly placed on the tester, separated from the field plate only by a very thin dielectric sheet (ESDA standard). This leads to a higher $C_{\text{DUT}}$ and thus a higher $I_{\text{peak}}$ for the WCSP version of this component. The simulator correctly predicted a higher $I_{\text{peak}}$ for the WCSP
version but the predicted value is off by about 24%. As the tool correctly predicted $I_{\text{peak}}$ for other WCSP components, there is no good explanation for the quantitative discrepancy between measurement and simulation and thus the measurement will be repeated.

As mentioned above, the $I_{\text{peak}}$ prediction methodology usually provides good results for WCSP devices. Figure 4.33 compares the measured and the simulated $I_{\text{peak}}$ for four additional WCSP devices, demonstrating that the simulated $I_{\text{peak}}$ is within 15% of the measured value.

![Figure 4.33 Comparison of the measured and simulated $I_{\text{peak}}$ for WCSP devices. Both the measurements and simulations were band-limited at 8 GHz.](image)

Table 4.10 compares simulation results with the measurement data for another design. Die X was originally in a QFN package. The product team wanted to migrate to a BGA package for thermal reliability reasons. The tool was used to estimate the peak current if Die X were to be placed in the BGA package instead of the QFN package. To provide confidence in this “what-if” simulation, the tool was used to estimate $I_{\text{peak}}$ of an existing BGA-based product, Die Y. The good correlation between the simulation and the measurement results for Die Y provided confidence in the predicted value of $I_{\text{peak}}$ for the case that Die X is placed in the BGA package. It
is predicted that the CDM stress will increase when Die X migrates from the QFN to the BGA package. The tool also captures the effect of change in the die size for the same package; for the same BGA package, note the difference in the \( I_{\text{peak}} \) value for Die Y versus that for Die X.

The lumped \( C_{\text{DUT}} \) model based peak current estimation method provides good correlation between the measurement and simulation results. Next, this method is compared to the more elaborate distributed \( C_{\text{DUT}} \) model. The distributed model based simulation requires more setup time because the distributed charge storage capacitances need to be connected together using the on-die and package level discharge paths. In Section 4.3.1 it is explored whether the on-chip resistances, ESD protection devices and the impedance of the package leads and traces have any impact on the peak value or the rise time of the discharge current.

Table 4.9 Comparison of simulation results and the measured peak current on several designs at a pre-charge level of 500 V. The oscilloscope bandwidth is 3 GHz unless otherwise indicated.

<table>
<thead>
<tr>
<th>Design</th>
<th>Package</th>
<th>FICDM Tester</th>
<th>Simulation</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>UIUC Test Chip</td>
<td>144 pin BGA (7 mm x 7 mm)</td>
<td>JEDEC</td>
<td>4.8 A</td>
<td>4 A</td>
</tr>
<tr>
<td>Design A</td>
<td>337 pin, 12 layer BGA (16 mm x 16 mm)</td>
<td>ESDA</td>
<td>7.9 A</td>
<td>8.1 A</td>
</tr>
<tr>
<td></td>
<td>144 pin TQFP (20 mm x 20 mm)</td>
<td>ESDA</td>
<td>10.3 A</td>
<td>10.1 A</td>
</tr>
<tr>
<td>Design B</td>
<td>WCSP (4.9 mm x 4.9 mm)</td>
<td>JEDEC</td>
<td>3.85 A</td>
<td>3.5 A</td>
</tr>
<tr>
<td>Design C</td>
<td>QFN</td>
<td>JEDEC</td>
<td>2.24 A</td>
<td>2.34 A</td>
</tr>
<tr>
<td>Design D</td>
<td>WCSP (3.7 mm x 3.7 mm)</td>
<td>ESDA</td>
<td>5.6 A (1 GHz)</td>
<td>4.5 A (1 GHz)</td>
</tr>
<tr>
<td></td>
<td>QFN (6 mm x 6 mm)</td>
<td>ESDA</td>
<td>2.8 A (1 GHz)</td>
<td>2.9 A (1 GHz)</td>
</tr>
</tbody>
</table>
Table 4.10 Predictive simulation of $I_{\text{peak}}$ for Die X in the BGA package. Simulation results for other combinations of the die and the package agree with the simulation results.

<table>
<thead>
<tr>
<th>Pre-Charge (V)</th>
<th>500</th>
<th>750</th>
<th>1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>Die X in QFN package</td>
<td>Simulation</td>
<td>7.4 A</td>
<td>11.2 A</td>
</tr>
<tr>
<td></td>
<td>Measurement</td>
<td>7.7 A</td>
<td>11.3 A</td>
</tr>
<tr>
<td>Die Y in BGA package</td>
<td>Simulation</td>
<td>8.7 A</td>
<td>12.8 A</td>
</tr>
<tr>
<td></td>
<td>Measurement</td>
<td>8.9 A</td>
<td>13 A</td>
</tr>
<tr>
<td>Die X in BGA package</td>
<td>Simulation</td>
<td>9.4 A</td>
<td>13.5 A</td>
</tr>
<tr>
<td></td>
<td>Measurement</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

The capacitances associated with the fringing fields at the periphery of the device are not included in the $C_{\text{DUT}}$ estimation methodology. This is expected to be significant only for WCSP components, where it could be as high as 15% of the parallel plate capacitance. The overall good results, obtained using the current methodology, do not provide motivation to add in this additional, usually small, component of $C_{\text{DUT}}$. Furthermore, it is noted that the lumped $C_{\text{DUT}}$ model will tend to overestimate $I_{\text{peak}}$, so excluding the fringing field capacitance may introduce a compensating error. The next section contains a comparison of lumped and distributed $C_{\text{DUT}}$ modeling.

4.3.1 Lumped vs. the Distributed Simulation Model for Peak Current Prediction

The simulated transient current waveform obtained using the distributed $C_{\text{DUT}}$ model of 90 nm test chip used in Section 4.1 and those obtained using the lumped $C_{\text{DUT}}$ models of the same test chip are compared with the measured current waveform in Figure 4.34. Recall that only 64 out of the 100 pins of the package were connected to the die in the 90 nm test chip. Two
versions of the lumped $C_{DUT}$ model were constructed: (a) “Isim-lumped-NoFloatingPins” was obtained using the capacitance contribution only from the pins connected to the die and (b) “Isim-lumped-AllPins” was obtained considering the capacitance contribution from all the pins in the package. The lumped $C_{DUT}$ model in (a) was constructed manually by ignoring the capacitance contribution from the floating pins.

![Comparison of the measured current waveform with those simulated with the distributed $C_{DUT}$ and the lumped $C_{DUT}$ model.](image)

The peak current value and rise time of the simulated current waveform obtained using the distributed model agree very well with those of the measured current waveform. The lumped $C_{DUT}$ model constructed using all the pins overestimates the $I_{\text{peak}}$ by about 18% relative to the measured value, whereas the lumped $C_{DUT}$ model constructed using only the connected pins of the package predicts an $I_{\text{peak}}$ that is only a 8% higher than the measured value.

The lumped models are also observed to produce a higher peak current than the distributed model. This occurs because the lumped models connect all the charge storage sites, with no impedance between them. Thus, they provide a pessimistic, worst-case value of the peak
current. However, the lumped $C_{DUT}$ model that accurately captures the information about the floating pins and traces in the package produces a closer match to the measured current.

It is important to note the rise time and the peak current value of the measured discharge current varies by 15 to 20% for a given part and a pin. This suggests that the error introduced by lumped rather than distributed modeling is negligible. For CDM simulation purposes, the first peak and the rise time of the discharge current are the important parameters that determine the voltage stress on the circuits on the die. From Figure 4.34, the full-width of the first current pulse (measured between zero crossings) of the measured waveform is observed to be larger than that of the simulated waveforms by about 200 ps. This minor difference in the pulse width is not a significant factor in determining the reliability of the circuits on the die. The error in the simulated pulse width is attributed to the discharge path inductance and resistance models, specifically the spark gap resistance.

Overall, the lumped model is sufficiently accurate for the purpose of projecting CDM reliability, especially if one considers that the time and effort required to setup the distributed model and simulation runtime are much higher than for the lumped $C_{DUT}$ model. Finally, the lumped $C_{DUT}$ model, unlike the distributed model, does not require knowledge of the on-chip ESD network and bus resistance models. The spark gap resistance changes from zap to zap depending on the approach speed and the geometry of the pin being zapped [39]. The rise time and the peak current values of the measured discharge currents vary by 15 to 20% for a given part and a pin. The values assumed in this simulation are based on the $I_{\text{peak}}$ measurements on calibration coins [39].
As a final check on the correctness of the model, the total charge entering (or exiting) the component is obtained from both measurement and simulation. Charge is obtained by integrating the current waveform measured at the discharge pin. The results are shown in Figure 4.35. The measured charge is identical to that obtained using the lumped model constructed considering all the pins of the package, whereas the distributed $C_{DUT}$ model and the lumped model without the floating pins underestimate the total charge by about 15%. This difference is attributed to the fringing field capacitance, which is neglected in all the models. Adding the fringe capacitance would likely result in a more accurate representation of the total charge stored by the distributed $C_{DUT}$ model and the lumped $C_{DUT}$ model that was constructed by considering only the bonded pins of the package. In contrast, the lumped $C_{DUT}$ model constructed considering all the pins of the package would over-predict the total charge storage if the fringe capacitance were included.

Figure 4.35 Plots of charge calculated by integrating the measured and the simulated current waveforms. The total charge is almost the same.
4.4 Chapter Summary

Simulation results showed good agreement with the measurement results on both the 90 nm and 65 nm test chips. Simulation based analysis helped us better understand some of the surprising measurements observed at the domain crossing circuits on the 90 nm test chip.

A small voltage clamp (1/20th of the size used at the I/O pads) with no series resistor is sufficient to protect the receiver at the power-domain crossing circuits. A suitable ESD protection circuit for an inter-die interface consists of small voltage clamps (1/10th of the size used at I/O pads) placed at the receiver input. There is no need for a series resistor. This protection strategy is specific to the case that the ground nets of the two die are connected together at the package level.

In a stacked die component, if the dies are thinned to maintain the stack height, stacking more die does not significantly increase the amount of charge. Therefore, the peak CDM discharge current does not increase. This means that the external pads for a stacked die component require the same protection as in a single-die component.

The peak current estimation methodology showed good correlation with the measurement results on several test chips. The method can be applied very easily to estimate the peak current for a given chip design and the ESD protection network can be designed accordingly.
5. CDM RELIABILITY OF 3D INTEGRATED CIRCUITS

Modeling and circuit-level simulation of the CDM events in wire-bonded stacked die components were introduced in Chapter 2. The test chip measurement data were presented in Chapter 4 to provide authenticity to the simulation results. A brief overview of 3D integration technology was provided in Section 1.3. In this chapter, the simulation methodology is extended to 3D components containing through-silicon vias (TSVs). This is the first time a simulation based analysis has been conducted on a 3DIC component. The work was presented at the 2011 3DIC conference held in Japan in 2012 [18].

Figure 5.1 shows a three-tier 3DIC on an FICDM tester. The majority of the charge is stored on the package conductors and the backside of the topmost die in the stack as shown in the figure. After the charge storage locations are determined and the corresponding capacitor model is derived, one can then model the discharge path from these capacitors to the grounded ball of the package. After a CDM zap on a package ball connected to the bottom die, negative charge will be stored on the unshielded conductors of the component. Red arrows show the current flow during the zap. Charge reaches the top die substrate through the VSS net TSV. To avoid ESD-induced damage, there must be a safe, low-impedance path from the VSS net to the pad on the bottom die that is being zapped. Charge stored on the topmost die has to find its path through the ground bus network consisting of the on-die busses and the TSVs to the grounded ball. The charge stored on the unstressed pins and traces of the package will enter the bottommost die and flow through the on-die ESD network, into the grounded ball. Figure 5.2 shows the possible discharge current paths for the component shown in Figure 5.1. An important ESD research question pertaining to 3DICs is whether the inter-die interfaces are safe during ESD events. This question will be further explored in the next section.
5.1 CDM Hazards at Inter-Die Interface

Figure 5.1 3D-IC on an FICDM tester. Face to back die stacking is assumed and a package ball connected to the bottom die is grounded (zapped) by the pogo pin.

The inter-die signal interfaces do not necessarily lie on any of the main ESD current paths. Therefore, in a 3D-IC, the inter-die signal interfaces may not require the same ESD protection as do the external signal pads. One might assume that no ESD protection is needed at the inter-die signal interfaces, especially if the external package pins are directly connected only to a single die in the 3DIC.
Figure 5.2 Circuit-level model of the ESD zap illustrated in Figure 5.1. Current flows from the coupling capacitances ($C_{\text{die}}$, $C_{\text{trace}}$) to the grounded pin through paths that include the top die’s Si substrate, the power and ground busses, and the ESD protection devices (diodes, rail clamps).

However, even in this case, the static charge will flow through all the dies and one should not assume that there is no ESD hazard at the inter-die interfaces. In the specific case of FICDM testing, static charge is stored on the top die and will make its way through the die stack to or from the external pins, as illustrated in Figure 5.1 and Figure 5.2. In [15], it was shown that, for wire-bonded stacked die components, ESD protection is indeed needed at the inter-die signal interfaces; however, if the ground nets for all the dies are connected together at the package level, smaller protection devices can be used at the inter-die signal interfaces than at the external signal pads [15], [17].

Today, most stacked die components use the same I/O cells at both the inter-die signal interfaces and the external signal pads, primarily for reasons of design reuse. Thus, in many
stacked die components, the inter-die signal interfaces (“internal I/O”) are unnecessarily loaded by large ESD protection devices.

The first 3D-ICs in mass production are likely to be DRAM products [42]. In the case of 3D-DRAM, a complete redesign of the I/O circuits is undertaken to achieve power savings [43] and an increased data rate [20]. Some designers have assumed that no ESD protection is needed at the internal I/O[20], but no FICDM stress results have been provided to support this approach. In this section of the document, the CDM-induced voltage stress at internal I/O in 3D-IC is analyzed.

Figure 5.3 shows the schematic representation of the circuit model used for transient CDM simulations. This model corresponds to the 3DIC component shown in Figure 5.1. Figure 5.3 also shows the circuit model for the inter-die interface circuit. The model is specific for the case where the VDD and VSS busses of the dies are connected together using TSVs. This specific case is discussed in Section 5.1.1. In Section 5.1.2, the impact of isolated ground nets on the CDM reliability of the inter-die interfaces is also analyzed.
5.1.1 3D-IC with a Single Ground Bus

In a 3D-IC, the inter-die signal interfaces are not the primary points at which static charge enters or exits the component; therefore, it is not necessary to design full-sized ESD protection circuits at these interfaces if an alternate low-impedance path is provided to move static charge between the dies. If the component contains just a single ground bus, then the ground bus network provides a conduit for static charge. However, the voltage stress at an inter-die receiver may still be severe enough to damage the gate oxide of the receiver if the power delivery network (PDN) between the dies is not designed carefully. A specific example will be used to
study the stress at an inter-die receiver: a 3D-IC containing two die stacked face to back and in which the bottom die is flip-chip attached to the package substrate. The case considered is that of a CDM zap to an external signal pin. An example of the resulting schematic is shown in Figure 5.4(a); as the complete circuit model is quite huge, only a portion is shown in the figure. The gate dielectric of the receiver NMOS will be stressed if its $V_{GS}$ exceeds the process $V_{DD}$. To determine the value of $V_{GS}$, it is more convenient to use a lumped version of the circuit model, as shown in Figure 5.4(b).

![Figure 5.4](image_url)

Figure 5.4 Signal interface between two die. When an external pin on the same die as the receiver is zapped, charge stored on the substrate of the top die (Die 2) flows to its VSS and through the TSV network into the VSS bus of Die 1. (a) The ground net is represented as a distributed, 3D resistive network. (b) Flattened, lumped model. Each resistor represents the transfer resistance between two nodes in the net. These figures are borrowed from [18].
Using this model, the receiver NMOS $V_{GS}$ may be estimated by the following sum

$$V_{GS} \approx V_{clamp} + I \cdot (R_1 + R_2 + R_3) + I \cdot R_{TSV}.$$  (5.1)

In Equation 5.1, $V_{clamp}$ is the voltage drop across the “rail clamp” circuit; a rail clamp is a protection circuit that provides a path between VDD and VSS for positive ESD current, and rail clamps are part of the normal on-chip protection network in CMOS chips. In Equation 5.1, the term $I \cdot (R_1 + R_2 + R_3 + R_{TSV})$ represents the potential difference between the VSS bus local to the transmitter and the VSS bus local to the receiver. From Figure 5.4(a), these VSS nodes are connected via the on-chip, multi-branch resistive bus networks and the TSV impedances; however, in Figure 5.4(b), the relevant portion of the VSS network is represented by just four transfer resistances, $R_1$, $R_2$, $R_3$ and $R_{TSV}$. One might reasonably assume that a component with a well-designed ground bus network would have a negligibly small potential drop between the various nodes of the VSS net. However, the effective impedance between two points in this network may be significantly higher during ESD than during normal operation, due to the different boundary conditions.

Under normal operating conditions, all the external VSS pins of the component are connected to ground. During FICDM testing, at most one VSS pin is connected to the grounded pogo pin; the other pins are floating. This can result in a very non-uniform distribution of current throughout the VSS bus grid during ESD testing.

An example is provided to illustrate the concept of a transfer resistance and also to show that the type of package strongly impacts the CDM current distribution. Figure 5.5 shows a simple resistive mesh that is intended to represent the VSS bus wiring on a bottom die. Some ESD current is injected from an upper die into this mesh at node X. The transfer resistance
between node X and ground is defined as $V_X / I_{ESD}$. If just one of the VSS pads is connected to ground, the transfer resistance is $\frac{7}{8} \cdot R$, whereas if all four VSS pads are connected to ground, the transfer resistance has a much smaller value, $\frac{3}{8} \cdot R$. From this example, one may conclude that if a package contains a lead frame, such as in a QFN package, then zapping a single VSS pin will ground just a single VSS pad, resulting in large transfer resistances between points in the VSS mesh. However, if the package contains a multi-layer substrate, as in some BGA packages, the various VSS pins might be connected to a single ground plane. In this case, the various VSS pads are at virtually the same potential when just one pin is zapped, reducing the transfer resistance between points in the VSS mesh. In summary, the design of the ground bus network, on both the die and package level, will affect the ESD stress at inter-die signal interfaces.

![Image](image_url)

Figure 5.5 Mesh structure distributes the ground bus throughout the die. VSS pads are connected at the four corners. The resistance of each branch is assumed to be “R”. At node X, ESD current is injected into the mesh from the upper die.

The voltage stress at an inter-die signal interface may be simulated and the need for an ESD protection circuit evaluated. Figure 5.6 contains a representation of a vertical data channel connecting a two-stack wide-I/O DRAM and its controller; this is roughly modeled after [20]. The box labeled “ESD protection” may contain a primary protection circuit (which consists of
large protection devices), a series resistor and a secondary protection circuit (which consists of small protection devices); it may contain a series resistor and a secondary protection circuit; it may contain just a secondary protection circuit. These three options are illustrated in Figure 5.7 (a)-(c).

Figure 5.6 Model of two-stack wide-I/O DRAM plus DRAM controller with TSV and microbump interconnection. Parasitic elements associated with the TSV and microbumps are included. Series inductance of TSV may be ignored at frequencies of current interest (e.g., 200 MHz). Figure taken from Rosenbaum et al.[18].

Figure 5.7 A variety of ESD protection circuit topologies are considered for inter-die signal interfaces. Dual-diode protection circuits are illustrated here but other options exist, including MOS and SCR-based protection circuits. (a) Primary ESD protection circuit, series resistor and secondary ESD protection circuit. The secondary protection devices are typically 1/10 the size of those used in the primary protection circuit. (b) Series resistor and secondary protection circuit. (c) Secondary protection alone. Figure taken from Rosenbaum et al. [18].

To investigate the voltage stress on inter-die receivers, a model is constructed of a 3D component that contains bi-directional inter-die data channels, such as shown in Figure 5.6. The 3D component is closely modeled upon a small SiP component the authors designed, modeled and tested previously [15]. The component contains two identical dies of size 2 mm x 2 mm, which are stacked and interconnected using TSVs. The dies are housed in a 7 mm x 7 mm BGA.
package with 169 balls. ESD rail clamp circuits are placed around the periphery of both dies in a typical ring fashion, with power and ground busses interconnecting them. Static charge storage throughout the component is dictated by the model of the coupling capacitances between the tester and the component; roughly half of the static charge is stored on the VSS net, and 25% on the VDD net. The remaining 25% is uniformly distributed among the signal nets of the package. Bi-directional inter-die signal interfaces were placed at the center of the dies. Four such interfaces are included in the component model. One interface does not include any ESD protection. At the second interface, the ESD protection circuit of Figure 5.7(a) is instantiated at both sides of the interface. The third interface is protected by the circuit shown in Figure 5.7(b), and the fourth interface is protected by the circuit shown in Figure 5.7(c). The primary ESD protection circuit (Figure 5.7(a)) consists of a 300 µm perimeter upper diode and a 200 µm lower diode. The series resistor (Figure 5.7(a) and Figure 5.7(b)) is 50 Ω. The secondary ESD protection circuit (Figure 5.7(a)-(c)) contains two diodes, each of which has a 25-µm perimeter. The CDM tester pre-charge voltage is 1500 V and a VSS ball is zapped (grounded). The large pre-charge voltage was selected to ensure that the peak discharge current and the resulting stress are comparable to that experienced by large components tested at moderate pre-charge voltages (e.g., 500 V).

As shown in Figure 5.8, simulations indicate that the full-sized ESD protection network (Figure 5.7(a)) provides only marginally better voltage clamping at the inter-die receiver than is provided by a small secondary protection circuit alone (Figure 5.7(c)). This is the result of the interface lying off the main discharge path; the protection circuit need not sink much ESD current, it simply needs to provide voltage clamping. Figure 5.8 also shows the simulated voltage stress for the case of no ESD protection circuit at the inter-die I/O. To avoid gate dielectric
breakdown in modern processes, $V_{GS}$ must be kept below about 4 V. The simulation results suggest that this cannot be done in the absence of an ESD protection circuit unless the effective resistance between the transmitter and the receiver ground nodes ($R_1 + R_2 + R_{TSV} + R_3$ in Figure 5.4 (b)) is kept below 1 Ω in totality.

![Diagram](image)

Figure 5.8 Circuit simulation of CDM-ESD in a 3DIC with a single ground bus; voltage stress at the inter-die receiver is plotted. Stress is an increasing function of the ground net transfer resistances (Figure 5.4). In these simulations, the ESD clamps are diodes.

The simulation results show that one has two options for achieving ESD reliability: placing voltage clamping devices at the inter-die signal interfaces or tightly controlling the impedance of the ground net. The latter approach is feasible if the existing ESD rule checking tools are modified. New checks would need to be implemented to calculate the effective transfer resistance between the transceiver VSS nodes. Existing voltage drop analysis tools could be enhanced to perform these checks using the relevant boundary conditions, as described earlier in this section.
5.1.2 3D-IC with Multiple Ground Busses

5.1.2.1 Ground Busses Connected at the Package Level

If the inter-die signal interface has its transmitter and receiver connected to different ground busses, but these ground busses are connected together in the package, then the voltage stress at the receiver is a function of the impedance from the package ground to an on-chip VSS bus. Better CDM reliability is expected if the chip-to-package connections are made using C4 solder bumps rather than bondwires.

CDM simulations provide quantitative insight as to how the inter-die stress magnitude varies with the die to package connection. First considered is the case of bond-wire connections. Figure 5.9(a) shows the die-stack assumed for the simulations. Most of the charge is stored on the package conductors, the substrate of the topmost die, and the part of the bottom die that is not shielded from the tester field plate by the upper die. Figure 5.9(b) shows a simplified schematic of the inter-die signal interface that was used in the simulations. As shown in the figure, the transmitter, located on Die 2 or Die 3, lies within the VDD2/VSS2 power domain; the receiver, located on Die 1, is in the VDD1/VSS1 power domain. This inter-die interface does not include an ESD protection circuit. Although VSS1 and VSS2 are isolated on the die level, each VSS1 bond-pad is connected to a VSS2 bond-pad by means of bonding to a single bond-finger in the package. There are four VSS1 pads and four VSS2 pads in total. VDD1 and VDD2 are isolated on both the die and package levels.
Figure 5.9 (a) Cross-section of a 3D-IC in which the die to package connections are made using bondwires. (b) Inter-die signal interface: the driver on Die 2 is in the VDD2 domain and the receiver on Die 1 is in the VDD1 domain. Pairs of VSS1 and VSS2 pads are connected together at the package. An external signal pin is zapped.

The worst case stress at the inter-die receiver occurs when an external signal pin is zapped (the I/O circuit connected to this pin lies within the VDD1 domain). In Figure 5.10, $V_{GS}$ of the receiver NMOS transistor is plotted as a function of the peak CDM discharge current; this is equivalent to a plot of $V_{GS}$ as a function of the tester pre-charge voltage. For a 10 A discharge, the peak $V_{GS}$ is 6 V, which is likely to rupture the gate dielectric. $V_{GS}$ is large primarily because there is a large potential difference between the VSS1 and VSS2 nets which, in turn, is the result of the “$L \cdot \frac{dt}{dt}$” voltage drop across the bondwires [15]. The $L \cdot \frac{dt}{dt}$ term is significant because the rise time of the CDM discharge current is on the order of 100-200 ps.
5.1.2.2 Ground Busses Isolated at the Package Level

If the inter-die signal interface has its transmitter and receiver connected to different ground busses, and these busses are not connected together in the package, then a protection circuit must be inserted between the two busses. The protection circuit between different VSS busses is usually implemented as a pair of anti-parallel diodes (APD). Such protection circuits are found in most SoC designs; in 3D-IC, one needs to consider the best die on which to implement the APD. Figure 5.11 provides a schematic representation of the ESD current path for
a CDM zap to an external signal pin. The ESD analysis for this case is similar to that presented in Section 5.1.1, except that the transfer resistance between the transmitter and receiver grounds is larger in this case and it includes the APD impedance. Consequently, the ESD hazard at the inter-die signal interfaces will be greater for this type of ground bus network and it is highly recommended that an ESD clamp be included at the input of any inter-die receiver.

In Figure 5.11, the APD were arbitrarily shown as having been placed on the bottom die. The placement of the APD on the top or bottom die is a design variable that may have an impact on the overall ESD reliability of the part and will be investigated via experimental verification on the 3DIC test chip presented in the next section.

5.2 Impact of the Placement of TSVs and Power Clamps in a 3D Stack

In this section, a simulation based study is presented to explore whether the number of power clamps within a power domain spanning multiple dies in a 3D stack can be optimized. In particular, we explore whether or not the number of clamps can be reduced on a die that is not directly connected to package pins. In Section 4.2, it was shown that stress current distributes
over the multiple dies in a stack thus reducing current stress experienced by each die in the stack. Therefore, it may be possible to reduce the number of clamps on some of the dies in the stack.

A synthetic test case representing a 3DIC stack shown in Figure 5.12 was created for circuit simulations. The 3DIC stack consists of two dies stacked in front-to-back configuration. The bottom die is flipped on a BGA package substrate. The connections between the dies are made using the TSVs that go through the substrate of Die 1. Each die is 2 mm x 2 mm. Die 1 has 100 bump pads that connect to the 100 package balls. Both the dies share the power and the ground nets: VDD and VSS. The I/O ring and the core power/ground bus structure are shown in Figure 5.13. There are 15 VDD pads on Die 1. The cells at the VDD pads contain active power clamps. The core power and ground network is a grid of size 10 x 10 and each arm of the grid is about 150 μm in length. The core grid metal lines are considered to be 10 μm wide and made up of the top level metal. Inter-die receivers are labeled RX1 and RX2, shown at their respective locations in the grid. Their power and ground ports are connected to the nearest grid nodes. The corresponding drivers on Die 2, TX1 and TX2, are considered to be placed vertically right above the receivers.

Figure 5.12 3DIC consisting of two dies stacked in face-to-back configuration. Die 2 is flipped on the backside of Die 1. Die 1 is flipped on top of the BGA package substrate. TSVs create connections between Die 2 and Die 1.
Figure 5.13 Pad arrangement and the power/ground bus structure on the die. Core grid is shown only for VDD but the simulation model contains the grid for both VDD and VSS nets. Pads are labeled 1 through 100 in counter-clockwise direction.

Two different arrangements of TSV arrays are considered next, as shown in Figure 5.14.

The TSV arrangements shown in Figure 5.14 is replicated for both VDD and VSS nets.

Figure 5.14 Power/Ground TSV arrangement options analyzed in this section.
The TSV model used for the circuit simulations is shown in Figure 5.15. The simulation model assumed $R_{TSV}$ of 24 mΩ [20] and $L_{TSV}$ of 0.1 nH. A more accurate model would consist of $C_{TSV}$ as shown in Figure 5.16. $C_{TSV}$ was neglected to reduce the complexity of the simulation model. Including $C_{TSV}$ necessitates the modeling of the substrate of the die that contains the TSV. At high frequencies (rise time of the CDM discharge event), $C_{TSV}$ provides a path through which displacement current can enter the substrate. This current is collected by the substrate contacts, eventually making its way into the ground bus network on the die. In the case of high resistivity substrates, the amount of current is not expected to be significant. However, for low resistivity substrates, it may be important to model $C_{TSV}$. In the simulations presented in this thesis, the substrate was assumed to be of high resistivity (20 Ω-cm) and therefore $C_{TSV}$ was not included in the TSV model. It is recommended that $C_{TSV}$ be included in the TSV model in the case of low-resistivity substrates.

![Electrical model of the TSV used in the circuit simulations](image)

Figure 5.15 Electrical model of the TSV used in the circuit simulations presented in this section.

Refer to Figure 5.12. When the component is placed on the field plate of FICDM tester, the field plate forms a capacitance with the backside of Die 2. The traces in the package form capacitances with the field plate. When one of the package balls is contacted by the pogo pin, the
capacitance formed with the backside of Die 2 discharges through the substrate of Die 2, into the VSS network of Die 2. The discharge current then flows into the VSS network of Die 1 through the TSV network of the VSS net, making its way to the zapped package ball. The charge coupled to the package traces enters Die 1, flows through the ESD network into the zapped package ball.

Figure 5.16 A more accurate electrical model consisting of $C_{TSV}$ in addition to the series resistance and inductance.

Package ball corresponding to pad 1 was zapped to initiate CDM discharge at different pre-charge levels. The resulting voltage drops across the receiver NMOS gate-source terminals are plotted in Figure 5.17. The voltage stress is higher at the NMOS in RX1 compared to that at RX2. This is because RX1 is located closer to the zap point. The source of the NMOS at RX1 is at the closer to the lowest potential compared to the rest of the nodes in the components. The TSV arrangement A is better for RX1. The power and the ground TSVs are very next to the inter-die driver and the receiver in this arrangement. Therefore, the potential drop between the
driver and the receiver source is lower. RX2 is located away from the zap location and therefore, sees very low voltage stress. Arrangement “B” is slightly better for RX2.

![Graph showing voltage stress across NMOS gate-source terminals in receiver RX1 and RX2 for TSV arrangements A and B.](image)

**Figure 5.17** The voltage stress across the NMOS gate-source terminals in the receiver RX1 and RX2 for TSV arrangements A and B.

To summarize, the inter-die interface signal TSV, driver and receiver should be placed closer to the power/ground TSV network. The driver and the receiver power/ground nodes should be connected to the TSV network with minimum interconnect resistance.

Next, the impact of removing the power clamps on Die 2 is studied. For this study, the case of NMOS of RX1 with TSV arrangement “A” is chosen. This case was chosen because (a) RX1 experiences higher voltage stress compared to RX2, and (b) RX1 with TSV arrangement “A” is a more realistic scenario than RX1 with TSV arrangement “B”. The voltage stresses at the NMOS of RX1 on Die 1 are compared in Figure 5.18 for two cases: (i) when both Die 1 and Die 2 consist of power clamps and (ii) when only Die 1 consists of power clamps. Because of the orientation of Die 2 away from the field plate of the FICDM tester, there is no charge coupled to VDD nets on Die 2. All the charge is coupled to the backside of the substrate of Die 2. This charge flows through the VSS network of Die 2 into Die 1 through the TSV network of VSS net.
Therefore, removing the power clamps from Die 2 does not lead to significant increase in the voltage drop between VDD and VSS on Die 2. Therefore, the voltage stress at RX1 does not increase significantly.

Figure 5.18 Comparison of the voltage stress at the receiver RX1 on Die 1 with TSV arrangement “A” when both the dies have power clamps with that when only Die 1 has power clamps.

To summarize, if there is no charge coupled to the VDD net of a die in a 3DIC stack, the number of power clamps may be reduced on that die or potentially removed without significant risk to the circuits on the die. However, the VDD and VSS nets of the die should be well connected to the other dies in the stack that have power clamps between VDD and VSS. TSV network and the on-die power/ground network should be well designed to maintain very low resistance between the die and rest of the dies in the stack. In this study only doubly-stacked 3DIC was used as a test case. Studies need to be conducted on die stack with higher number of dies and other stacking scenarios. For example, if the charge coupled to the VDD net on Die 2 is significant, removal of power clamps is expected to increase the voltage drop between VDD and VSS significantly.
5.3 3DIC Test Chip Design

In the previous section, simulation based predictions about the CDM reliability of 3DICs were made. In this section, a 3DIC test chip design for the verification of simulation results is presented. First, the purpose of the test chip is stated. A brief overview of the 3D integration process is presented next. In Section 5.3.3, the test chip architecture and the logic design is described. Section 5.3.4 provides a brief overview of the test plan for the test chip. The test chip implementation has been completed but the fabrication is on hold indefinitely.

5.3.1 Test Chip Purpose

The purpose of this test chip is multi-fold. First, CDM reliability of 3DICs is largely unknown. There is no published data available on the CDM qualification results of 3DICs. Based on the discussions with our industry partners, semiconductor industry is very much interested in knowing if there are any ESD issues that may affect adaptation of 3D integration technologies. 3DIC design space is fairly new and there are various architectures being proposed to take advantages of the vertical stacking with very small footprint and lower signal transmission delays between the dies in the stack. However, no silicon data is available on the ESD reliability of 3DICs. The test chip will be the first in the industry to specifically study ESD robustness of 3DICs. Second, simulation based study on the CDM reliability of 3DICs was first presented by Rosenbaum et al. [18]. The test chip will implement several of the proposals made in [18] and verify the simulation results. The modeling and simulation methodology can be improved based on the measurement results of the test chip. Third, the test chip will also investigate ESD protection for high speed SSTL IO at the external interfaces of the chip.
5.3.2 3D Integration Process Overview

Tezzaron-Globalfoundries 3DIC two-die (“two-tier”) fabrication process is used to implement the test chip on a multi-purpose wafer through MOSIS. Each individual wafer will be fabricated in GlobalFoundries 130 nm process. The two-tier stack will be integrated using Tezzaron’s stacking process. Tezzaron process uses face-to-face (F2F) wafer level bonding process. The cross-section of the stack is shown in Figure 5.19.

![Figure 5.19 Two-tier wafer level stacking process from Tezzaron. The top wafer is flipped on top of the bottom wafer and bonded using a top level copper metal layer on either die under low pressure. The topmost metal layer geometries act as glue. Once the two wafers are bonded, the top die is thinned to expose the TSVs on the backside of the wafer. Picture on the right shows the BEOL with the TSV. TSV or the super-contact is connected to M1 (Metal 1) of BEOL. M6 or the topmost level is used to created wafer-to-wafer bonds for the F2F stacking.]

The TSVs used in this process are known as super-contacts and are made of tungsten instead of copper. Tezzaron uses via-middle process (explained in Section 1.3) to create super-contacts. The super contacts are etched after the FEOL but before the Metal 1 layer. The super contacts are only 6 μm long and 1.25 μm in diameter. Therefore the substrate of the wafer with super contacts has to be thinned to about 6 μm. There is about 6 μm of BEOL on the wafer and therefore the wafer is about 12 μm thick. The wafer is thinned after bonding to the un-thinned
wafer as shown in Figure 5.19. Therefore, there is no need for a carrier wafer to make sure the thin wafer does not bend and create stress in the devices.

After the super-contacts are exposed on the backside of the thinned wafer, one layer of backside metal is deposited to make contact with the super contacts. One can then either wirebond from the pads on the backside metal or create bumps for flip-chip packaging.

5.3.3 Test Chip Architecture and Circuit Design

The two-tier test chip will be integrated as per the process outlined in Section 5.2.2. Each die in the stack is 5 mm by 5 mm. External interfaces are on backside of the thinned top die provide access to the power, ground and the external signals. The stack will be packaged in a 144 pin QFP measuring 20 mm x 20 mm. Wirebond connections will be made between the package leads and the bond pads on the backside of the top die. The cross-section of the test chip is shown in Figure 5.20. The low speed data paths of the test chip are designed to operate at 200 MHz and the high speed sections of the test chip are designed to operate at 2 Gbps. The I/O cells translate the external signals from 3.3 V to 1.5 V. There are five I/O power (3.3 V) domains, five core power (1.5 V) domains and five ground nets in the test chip.

Figure 5.20 Shows the test chip cross-section. The two-tier stack will be packaged in a 144-pin QFP. Tier 0 is not thinned. Tier 1 is thinned and contains the super-contacts to connect the Tier 1 devices to the backside metal pads. The backside metal pads connect to the leads of the package using wire bonds.
The test chip has implemented inter-die interfaces with different types of ESD protection circuits, driver sizes and the ground net connections (power delivery networks) between the dies. There are three different types of ground net connections between the dies as outlined below:

(a) VSS and VDD of either die connected to each other with F2F connections between the dies. The VDD1/VSS1 domain is dedicated for this experiment. Both bi-directional and uni-directional inter-die interfaces are implemented in the VDD1 domain. Uni-directional interfaces are implemented in either direction.

(b) VDD4 (TIER 0) and VDD5 (TIER1) are isolated. VSS4 (TIER 0) and VSS5 (TIER 1) are connected together on the package lead frame. Uni-directional interfaces in either direction are implemented in this set of data paths.

(c) Isolated VDD nets; VSS of Tier 0 connecting to VSS of Tier1 on the die using anti-parallel diodes. VDD2 (TIER 0) and VDD3 (TIER1) are isolated. VSS2(TIER 0) and VSS3 (TIER 1 ) are connected using anti-parallel diodes placed on the bottom die. Uni-directional interfaces in either directions are implemented in this set of data paths.

These three types of ground net connections allow us to verify the CDM reliability of inter-die interfaces subject to different power delivery network designs explored in Section 5.1. Each of the three power domain pairs described above host inter-die interfaces between the two dies. The die floorplan with different power domains is shown in Figure 5.21.
Figure 5.21 Floorplan of the top and the bottom die showing the power domain plan on each die. VSS1 of the top die and VSS1 of the bottom die are shorted together using F2F connections. VSS2 and VSS3 are connected only through APDs on the bottom die. VSS4 and VSS5 are connected at the package level only.

To detect post-CDM stress failures at the inter-die interface circuits without having to do a physical failure analysis, circuit logic has been implemented. The circuit logic will enable us to perform electrical characterization of the inter-die interface circuits before and after CDM stressing. A behavioral change in the inter-die interface circuit post CDM stress will indicate that the circuits have been damaged during the CDM qualification. The circuit logic is described in Figure 5.22.
Figure 5.22 Logic diagram of data paths from the external I/Os on the top die (T7-T10) to the VDD2 domain, crossing the die into the VDD3 domain and finally connecting to the external pins through bottom die I/Os (B7-B10). The logic also allows signals to be passed from bottom die to the top die. The multiplexers and the de-multiplexers allow the signal to pass from any of the external I/Os into any of the inter-die tests. The path redundancy allows us to detect failures at the inter-die interfaces post CDM-stress. Here, the paths between the VDD2 and VDD3 domains are shown. There are two more sets of data paths between: (a) VDD1 of the top die and VDD1 of the bottom die and (b) VDD5 of the top die and VDD4 of the bottom die.

Figure 5.22 shows only one set of data paths that carry signals from VDD2 to VDD3 domain and vice versa. There are two more sets of data paths: (a) from VDD1 of top die to the VDD1 of the bottom die (b) VDD5 domain of the top die to the VDD4 domain of the bottom die. The multiplexers and the de-multiplexers are controlled by setting bits in a shift register. There are three shift registers in the test chip; one for each set of data paths. A shift register implemented in VDD2/VDD3 domain is shown in Figure 5.23. The bits D1-D10 control the multiplexers and de-multiplexers shown in Figure 5.22.
Figure 5.23 Shift register in the VDD2/VDD3 domain. The bits control the MUXes and the DE-MUXes in VDD2 and VDD3 domain shown in Figure 5.22. There are four external pads per shift register: RST3 resets the bits to predetermined bit pattern, CLK3 is the strobe for shifting in data, DIN3 is the data input and DOUT3 is the serial out pin to verify correctness of the shift register contents.

The list of ESD experiments at the inter-die interfaces is provided in Table 5.1 and Table 5.2 for each of the power domains. These experiments will help us verify the simulation based predictions made in Section 5.1.

Table 5.1 List of ESD experiments implemented at the inter-die interfaces in VDD1 domain and those between VDD4 and VDD5 domains. These experiments are implemented at the bi-directional interfaces as well as the uni-directional interfaces.

<table>
<thead>
<tr>
<th>Test</th>
<th>ESD Protection</th>
<th>TX Size</th>
<th>RX size</th>
<th>$R_{bus}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>No ESD</td>
<td>Wp/Wn = 1.5 FO1</td>
<td>FO4</td>
<td>2 Ω</td>
</tr>
<tr>
<td>2</td>
<td>Dual Diode (12.5 µm)</td>
<td>Wp/Wn = 1.5 FO1</td>
<td>FO4</td>
<td>2 Ω</td>
</tr>
<tr>
<td>3</td>
<td>No ESD</td>
<td>Wp/Wn = 1.5 FO8</td>
<td>FO4</td>
<td>2 Ω</td>
</tr>
<tr>
<td>4</td>
<td>No ESD</td>
<td>FO8</td>
<td>FO4</td>
<td>&lt; 0.5 Ω</td>
</tr>
</tbody>
</table>
Table 5.2 List of experiments at the inter-die interfaces in VDD2/VDD3 domain crossing.

<table>
<thead>
<tr>
<th>Test</th>
<th>ESD Protection</th>
<th>TX Size</th>
<th>RX Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>No ESD</td>
<td>Wp/Wn = 1.4</td>
<td>FO4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FO1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Dual Diode (10 µm/5 µm)</td>
<td>Wp/Wn = 1.4</td>
<td>FO4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FO1</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>*GGNMOS /GGPMOS (10 µm)</td>
<td>Wp/Wn = 1.4</td>
<td>FO4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FO1</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>No ESD</td>
<td>Wp/Wn = 1.4</td>
<td>FO4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FO8</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>No ESD; VM between INPUT and RX-VSS</td>
<td>Wp/Wn = 1.4</td>
<td>FO4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FO1</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>No ESD; VM Between INPUT and RX-VDD</td>
<td>Wp/Wn = 1.4</td>
<td>FO4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>FO1</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Minimum size antenna diode (VSS to input only)</td>
<td>FO8</td>
<td>FO4</td>
</tr>
<tr>
<td>8</td>
<td>Design-kit antenna diode</td>
<td>FO8</td>
<td>FO4</td>
</tr>
</tbody>
</table>

The primary inputs and outputs are implemented using bi-directional I/Os available from the design kit standard cell library. The I/O cells are located both on the top and the bottom die. However, all external connections have to go through the top die and the bondpads are present only on the backside of the top die. Therefore, feedthru I/O cells were created on the top die to provide connections from the bondpads to the bottom die I/O cell. The I/O rings for the top and the bottom die are shown in Figure 5.24. The external signal are in the VDDIOx (x = 1 to 5) domain (3.3 V) and are level shifted to VDDx (1.5 V) level. Low speed paths in the VDD1 domain and the signal paths in the VDD2, VDD3, VDD4 and VDD5 domains are designed to operate at 200 MHz. There is a high speed section in the VDD1 domain. These high speed I/Os
are implemented using serial stub transmission line (SSTL) standard and operate at 2 GHz. The high speed section of the I/O ring is shown in Figure 5.24.

To study the impact of reduction in the number of power clamps on the die not connected to the package directly (simulation study presented in Section 5.2), the VDD1 domain in the top die contains 10 power clamps whereas the VDD1 domain on the bottom die has only three power clamps. Higher number of failures in the receivers of the inter-die interfaces placed on the top die would indicate increase in the voltage drop between VDD and VSS on the bottom die due to reduced number of power clamps.

![Diagram](image)

Figure 5.24 I/O ring of the top and the bottom die. There are five 3.3 V domains (VDDIO1-VDDIO5) and five 1.5 V domains (VDD1-VDD5) in the test chip. The I/O and the core voltage domain partitions are shown in the diagram.

### 5.3.4 Test Plan

MOSIS will deliver 40 stacked parts. There will be 35 packaged parts and five bare dies (stacked). The 35 packaged parts will be split into various groups based on the stress pin classification. A test board will be designed to carry out functional characterization of the test
chip data paths. Leakage data at all the pins will be characterized. The 35 packaged parts will be subject to FICDM qualification tests. Post FICDM tests, the parts will be characterized again to check for changes in the functionality or leakage at the pins. A data path will be considered failed if the operating frequency changes by more than 30% or leakage at a pin increases by more than 10 μA.

Originally, the test chip was originally planned to be taped out in October 2012 but was delayed until January 2013. The tape-out date of the multi-purpose wafer has now been postponed indefinitely. If an opportunity to tape-out the design arises in the future, it will be taken to completion by my colleagues in the research group. If a different 3DIC integration process or fabrication process is chosen, the test chip will have to be laid out again. However, the logic design of the circuits and the set of ESD experiments can be implemented in the new fabrication process.
6. CONCLUSIONS AND FUTURE WORK

6.1 Conclusions

Various modeling methods for CDM circuit simulations were presented. The advantages and disadvantages of each of the methods were discussed. It was shown that the distributed models of the charge storage sites and discharge paths are required to simulate the voltage stress at the internal circuits such as domain crossing circuits or inter-die interface circuits. A simplified 2D package modeling method was presented. Methods to obtain simplified models for the discharge paths in the package and die were also presented. The resulting models were used to perform transient CDM circuit simulations on two test chips and the measurement data were compared with the simulation results.

Simulation results agreed with most of the measurement data except for the negative FICDM stress failures at the domain crossing circuits protected by (a) local APD and (b) transmission gate circuit. Further research is required to investigate the miscorrelation and the suggestions are documented in Section 6.2.

Based on the simulation results and experimental verification, we can conclude that a small voltage clamp (1/20 of the size used at the I/O pads) with no series resistor is the efficient method to protect the receiver at the power-domain crossing circuits. Any other methods that completely avoid placing any ESD protection circuit at the receiver would require careful full chip modeling with special attention to modeling the locations that the driver and receiver circuits connect to in the power/ground bus network of the chip.

It was first shown using circuit simulations that small secondary voltage clamps are sufficient to protect the inter-die interface circuits when the ground nets of the two dies are
connected together at package level. Later, test chip measurement data were presented and the measurement data agreed with the simulation results. It was shown that stacking multiple dies in the same package does not necessarily increase the FICDM stress current for a given pre-charge voltage. It was also shown that the domain crossing circuits in stacked die components are more robust compared to those in single die components.

Measurements results in [40] on the 90 nm test chip revealed that the analog inputs of the chip failed at lower stress currents on the wafer level testers than when stressed on FICDM tester. The work [40] hypothesized that the differences may have been caused by the degradation in the rise time of FICDM current pulse when it travels from the pogo pin, through the package leads or traces to the on-die bondpad. However, circuit simulations did not show any degradation in the rise time of the FICDM current pulse. Therefore, further research is suggested in Section 6.2 to identify the root cause for the differences.

The peak current estimation methodology showed good correlation with the measurement results on several test chips. The method can be applied very easily to estimate the peak current for a given package. Knowing the value of the expected peak current stress for a component, the ESD protection network of the chip can be designed efficiently. It was shown that the lumped $C_{DUT}$ model is sufficient for this purpose and provides very good match with the measurement results in terms of the rise time and the peak value of the current. Distributed $C_{DUT}$ model is not necessary for peak current prediction.

In 3D components that contain a single ground net, use of ESD protection devices at the inter-die signal interfaces can be avoided if the 3D ground bus network is designed such that
during an ESD event, the transfer resistance between the transmitter and the receiver nodes is sufficiently small, on the order of tenths of an Ohm.

In components that contain multiple ground nets, an ESD path must be provided by package-level connections between the grounds or by placing APDs between the grounds. For the case of a component with package-level connections between its ground nets, C4 solder bump attach of the die stack to the package provides better CDM reliability than does bondwire attach. Package ground planes are expected to improve CDM reliability. With an APD placed between two isolated ground nets in the stack, the voltage stress at the inter-die interfaces is expected to be high enough to require the use of protection devices.

It is possible to optimize the placement and number of power clamps within a power domain of a 3DIC die-stack. Design of the TSV network of the power and ground nets, orientation of the dies in the stack and placement of the inter-die interface circuits with respect to the TSV network of the power/ground nets determine whether or not the number of power clamps can be reduced on a die that’s not directly connected to the package. Simulation results presented in this thesis show that it is possible to reduce the number of power clamps in some scenarios. Experimental verification is needed to verify the hypothesis.

6.2 Future Work

Miscorrelations between the simulation and measurement results need to be investigated further. To correctly reproduce the negative stress failures in the domain crossing circuits, it is suggested to model the body diodes of the actual transistors in the driver circuit under VFTLP stress. Physical failure analysis of the failure locations is advised. Failure analysis may aid future research direction.
To investigate the miscorrelation between the wafer level testers and FICDM tester, additional test chip based experimental verification is advised. Primary inputs protected by rise-time sensitive ESD protection circuits should be designed with different package level trace lengths. Voltage monitors may also be used to detect the peak voltage stress during CDM stress. Parts of the 90 nm test chip that are in working condition may also be re-stressed on FICDM tester to re-verify the failure currents at the inputs of the analog domain.

Though the 3DIC test chip layout presented in this work may not be used directly for manufacturing in other fabrication and 3D stacking processes, the circuit design and the experiments presented in this work may be ported to a newer 3DIC fabrication process if an opportunity becomes available in the future. The simulation based hypothesis may be verified on a new test vehicle.

In this thesis, simplified models were used to represent the parasitic resistances of the on-die power/ground network. This method may be error-prone. It is advisable to employ automated parasitic extraction tools. However, faster transient simulation tools are required to solve the huge netlists resulting from the complete parasitic extraction of the power/ground nets. CAD tools are required to automatically replace the ESD protection circuits and circuits of interest in the extracted netlist by their corresponding compact models.
REFERENCES


[26] V. Jandhyala, “Next-generation three-dimensional full-wave electromagnetic solver hybridization for large-scale signal integrity, power integrity, and EMI modeling.”


