OPTIMUM GATE ARRANGEMENTS FOR AN MOS STANDARDIZED LAYOUT

BY

DAVID HAROLD ROBBINS

B.S., University of Illinois, 1972

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 1975

Urbana, Illinois

OPTIMUM GATE ARRANGEMENTS FOR AN MOS STANDARDIZED LAYOUT

BY

DAVID HAROLD ROBBINS

B.S., University of Illinois, 1972

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 1975

Urbana, Illinois

UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

THE GRADUATE COLLEGE

May, 1975

WE HEREBY RECOMMEND THAT THE THESIS BY

DAVID HAROLD ROBBINS

ENTITLED OPTIMUM GATE ARRANGEMENTS FOR AN MOS STANDARDIZED LAYOUT

BE ACCEPTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF MASTER OF SCIENCE

Director of Thesis Research

Head of Department

Committee on Final Examination†

Chairman

† Required for doctor's degree but not for master's.

D517

UNIVERSITY OF ILLINOIS
Urbana-Champaign Campus
The Graduate College
330 Administration Building

FORMAT APPROVAL

To the Graduate College:

The format of the thesis submitted by David Harold Robbins for the degree of Master of Science is acceptable to the department of Electrical Engineering.

May 7, 1975
Date

(Signed) Harold D. Webb
Departmental Representative

TABLE OF CONTENTS

ACKNOWLEDGMENT

The author wishes to thank Dr. Wataru Mayeda for his many contributions. Thanks are also due to Kathy Cloward for the typing of this paper.

Special thanks go to the author's wife, Barbara, for her support and encouragement.

The author also acknowledges the spirit of revelation through which all knowledge comes.

1. INTRODUCTION

Optimization of size is an important topic of research in the engineering of digital circuits. The field effect transistor (FET) is making an important contribution in this area. In this paper, the basic properties of the FET which pertain to digital circuits will be examined. The problems associated with the physical layout of large integrated circuits using FETs will also be discussed and a standardized method of layout will be reviewed. A simple procedure for optimizing chip area when using this standardized layout method will be developed and illustrated.

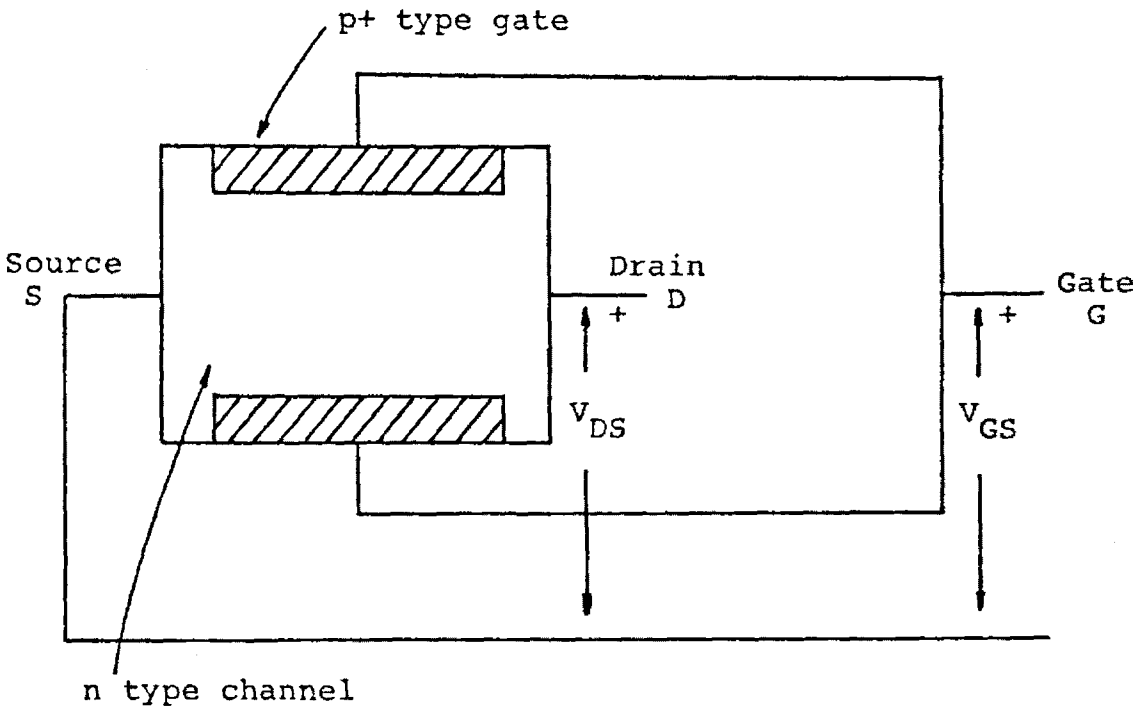
2. INTRODUCTION TO MOS DIGITAL CIRCUITS

Much of semiconductor research in recent years has concentrated on the development of the metal oxide semiconductor field effect transistor (MOSFET). Although its fabrication process is difficult to control, the MOSFET offers many characteristics which are more favorable than the conventional bipolar transistor. These characteristics are especially important to digital circuits.

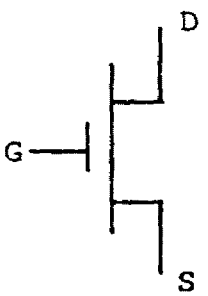
The MOSFET is a voltage controlled current device. Since its operation depends on the flow of majority carriers only, it is called a unipolar transistor [1]. In contrast, conduction in bipolar transistors is a function of both majority and minority carriers.

The structure of an n-channel FET is shown in Figure 1. The region of n-type material between the two gate regions is the channel through which the majority carriers move from source to drain. The width of this channel varies with changes in the voltage difference between the gate and source (V_{gs}). The effective channel width decreases as V_{gs} becomes increasingly reverse biased.

Because of its structural simplicity, the MOSFET is easy to integrate into complex digital circuits [2]. Unlike its bipolar counterpart, MOS integrated circuits (ICs) usually consist only of transistors. This is possible since the FET can be operated as both a load and a driver. Resistors, capacitors and diodes as functional elements are usually



a) An n-channel MOSFET



b) Circuit symbol

Figure 1. The MOSFET structure.

unnecessary [3].

The chip area required for a MOSFET is only about five percent of that needed by a bipolar junction transistor [2]. Thus, MOS digital circuits exhibit a higher gate density (gates/mm^2) than bipolar. This is extremely important in the production of large scale integrated (LSI) circuits.

The necessity of a high degree of process control has hindered the development of MOS technology [2]. Only in recent years has FET fabrication become economically competitive with the highly developed bipolar processes.

MOSFETs are either p-channel or n-channel. The difference is not only in the type of material used for the channel, but also in the kind of majority carrier by which conduction is effected. Current flow in the p-channel FET is due to holes, while that of n-channel is a function of electrons.

The hole mobility of silicon is less than half the electron mobility [4]. This means n-channel devices are inherently faster than p-channel. As a result of its lower mobility, a p-channel FET has twice the on resistance of an equivalent n-channel. As a result, higher density circuits are possible with n-channel MOS.

The switching speed of a MOSFET is limited primarily by the internal RC time constants [1]. The capacitance involved is directly proportional to the junction area. The junction area of an n-channel FET is smaller than a p-channel since a higher packing density is possible. Thus, n-channel switching speeds are higher.

unnecessary [3].

The chip area required for a MOSFET is only about five percent of that needed by a bipolar junction transistor [2]. Thus, MOS digital circuits exhibit a higher gate density (gates/mm^2) than bipolar. This is extremely important in the production of large scale integrated (LSI) circuits.

The necessity of a high degree of process control has hindered the development of MOS technology [2]. Only in recent years has FET fabrication become economically competitive with the highly developed bipolar processes.

MOSFETs are either p-channel or n-channel. The difference is not only in the type of material used for the channel, but also in the kind of majority carrier by which conduction is effected. Current flow in the p-channel FET is due to holes, while that of n-channel is a function of electrons.

The hole mobility of silicon is less than half the electron mobility [4]. This means n-channel devices are inherently faster than p-channel. As a result of its lower mobility, a p-channel FET has twice the on resistance of an equivalent n-channel. As a result, higher density circuits are possible with n-channel MOS.

The switching speed of a MOSFET is limited primarily by the internal RC time constants [1]. The capacitance involved is directly proportional to the junction area. The junction area of an n-channel FET is smaller than a p-channel since a higher packing density is possible. Thus, n-channel switching speeds are higher.

unnecessary [3].

The chip area required for a MOSFET is only about five percent of that needed by a bipolar junction transistor [2]. Thus, MOS digital circuits exhibit a higher gate density (gates/mm^2) than bipolar. This is extremely important in the production of large scale integrated (LSI) circuits.

The necessity of a high degree of process control has hindered the development of MOS technology [2]. Only in recent years has FET fabrication become economically competitive with the highly developed bipolar processes.

MOSFETs are either p-channel or n-channel. The difference is not only in the type of material used for the channel, but also in the kind of majority carrier by which conduction is effected. Current flow in the p-channel FET is due to holes, while that of n-channel is a function of electrons.

The hole mobility of silicon is less than half the electron mobility [4]. This means n-channel devices are inherently faster than p-channel. As a result of its lower mobility, a p-channel FET has twice the on resistance of an equivalent n-channel. As a result, higher density circuits are possible with n-channel MOS.

The switching speed of a MOSFET is limited primarily by the internal RC time constants [1]. The capacitance involved is directly proportional to the junction area. The junction area of an n-channel FET is smaller than a p-channel since a higher packing density is possible. Thus, n-channel switching speeds are higher.

An important MOS characteristic is the threshold voltage (V_t). This is the V_{gs} potential required to initiate conduction. Early MOSFETs required a high V_t, which made larger power supply voltages necessary. The use of ion implantation has reduced V_t and made MOS devices even more desirable [5].

Reduced voltage levels increase packing density and lower voltage swings during switching. This increases speed. MOS device reliability is also increased with reduced voltage levels since breakdown voltages are less likely to be achieved [6].

As a result of its low threshold voltage, n-channel FETs can be made compatible with transistor-transistor logic (TTL) and operate from a single five volt supply. However, TTL compatibility comes at the expense of reduced speed since higher voltages are required to optimize switching times [6].

Although n-channel characteristics are superior to p-channel, the production of n-channel gates is much more difficult to control. The drift of MOS characteristics with time and temperature has been a problem, and the physics of the device tends to create conditions which turn it on prematurely [2]. However, most MOS producers now have an n-channel process and manufacturing is becoming economically competitive.

3. AN MOS LAYOUT METHOD

Although much of MOS research has been directed toward the development of memories, n-channel logic circuits are also being realized. The result is a system in which both logic and memories are fabricated with one n-channel process, yielding a truly homogeneous LSI technology.

The most time consuming phase of the design of complex LSI circuits is the completion of a suitable layout. One author estimates an average of one man-hour per transistor is required for the planning, drawing, changing and checking of random logic areas [2].

Present layout techniques consist of custom design and standardized patterns [7]. Custom designed circuits yield high density products at the expense of many man-hours. Layouts for large MOS memories are developed using this method since the optimum use of chip area is critical.

Standardized patterns reduce layout turnaround times and can allow for some design automation. However, lower density layouts usually result with standardized patterns. This design method can reduce development costs for circuits in which highest density is not required.

Weinberger has proposed a method which combines the advantages of standardization and relatively high density and is applicable to n-channel MOS circuits [7]. This method is most effective when the circuit to be realized consists of NOR gates only. Although other logic elements are possible,

the use of NOR gates allows the pattern to be more easily automated.

Figure 2 illustrates the physical structure of an n-channel MOS positive logic NOR gate. It consists of three n+ channel diffusions on a p substrate. One diffusion connects to V_{DD} (the positive power supply) and one to ground. The third is a gate output diffusion. A load device, which is always on due to the voltage V_{gg}, is formed between the V_{DD} and output diffusion regions. Input and output lines and gate interconnections consist of metalized paths. Only one layer of metalization is required and all paths are parallel. These paths are also called signal nets [7].

When a high voltage, representing a logical 1, is present on a line connected to an input device, the device is turned on and conduction between V_{DD} and ground is initiated. The output voltage of the gate is then low, or logical 0. If the voltages on the lines to each input device are low, the output voltage level is near V_{DD}.

A one-dimensional array of NOR gates is called the basic pattern [7]. Because of its symmetry, gates may be added to the left or right to increase its size. Furthermore, mirror images of the basic pattern may exist above or below a block of the basic pattern by sharing a common V_{DD} or ground diffusion. The basic pattern, with a possible layout of the function $Y=A \oplus B$, is shown in Figure 3.

An IC chip could be realized using a single block of the basic pattern. Depending on circuit requirements, several

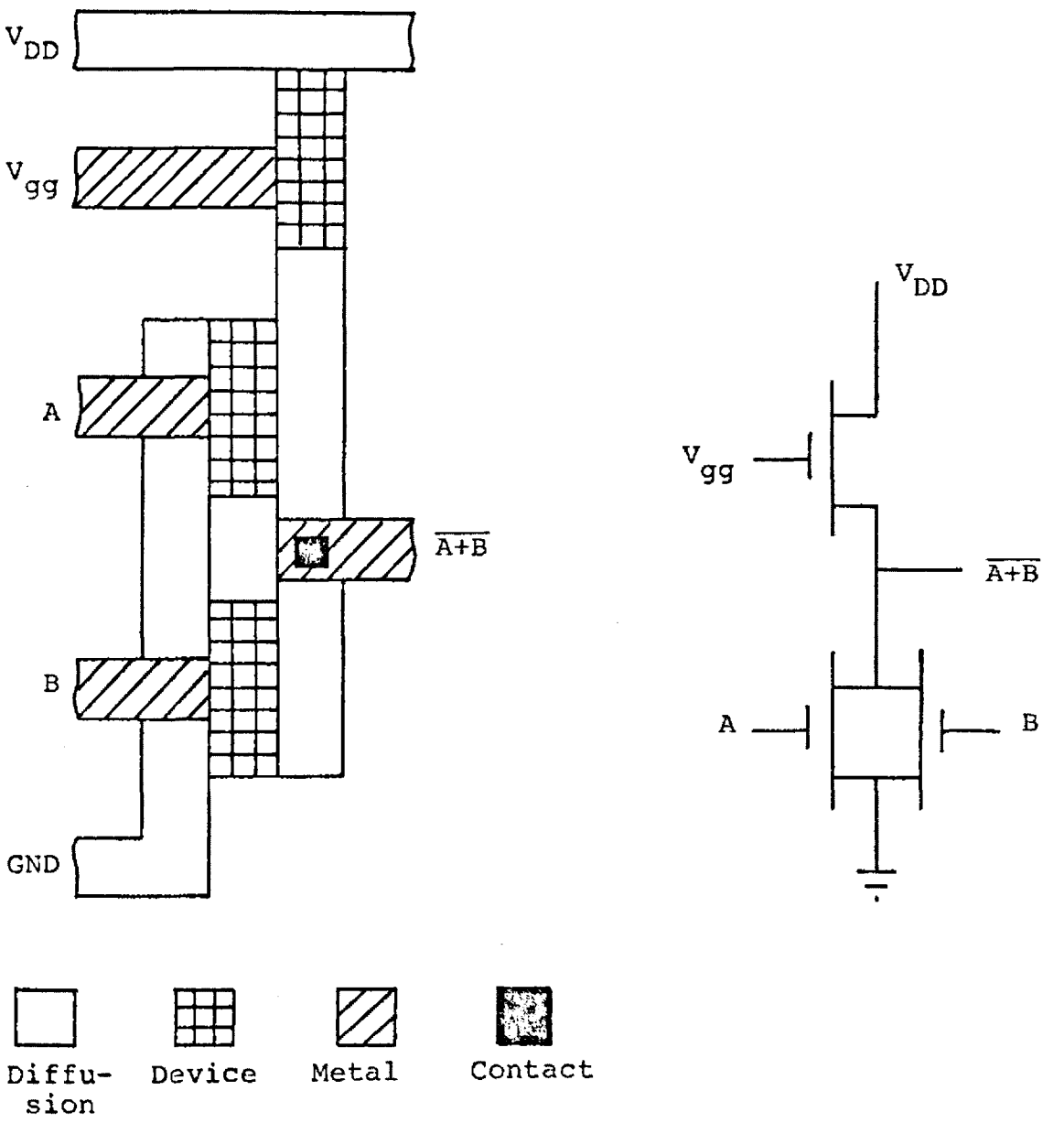


Figure 2. A positive logic MOS NOR gate.

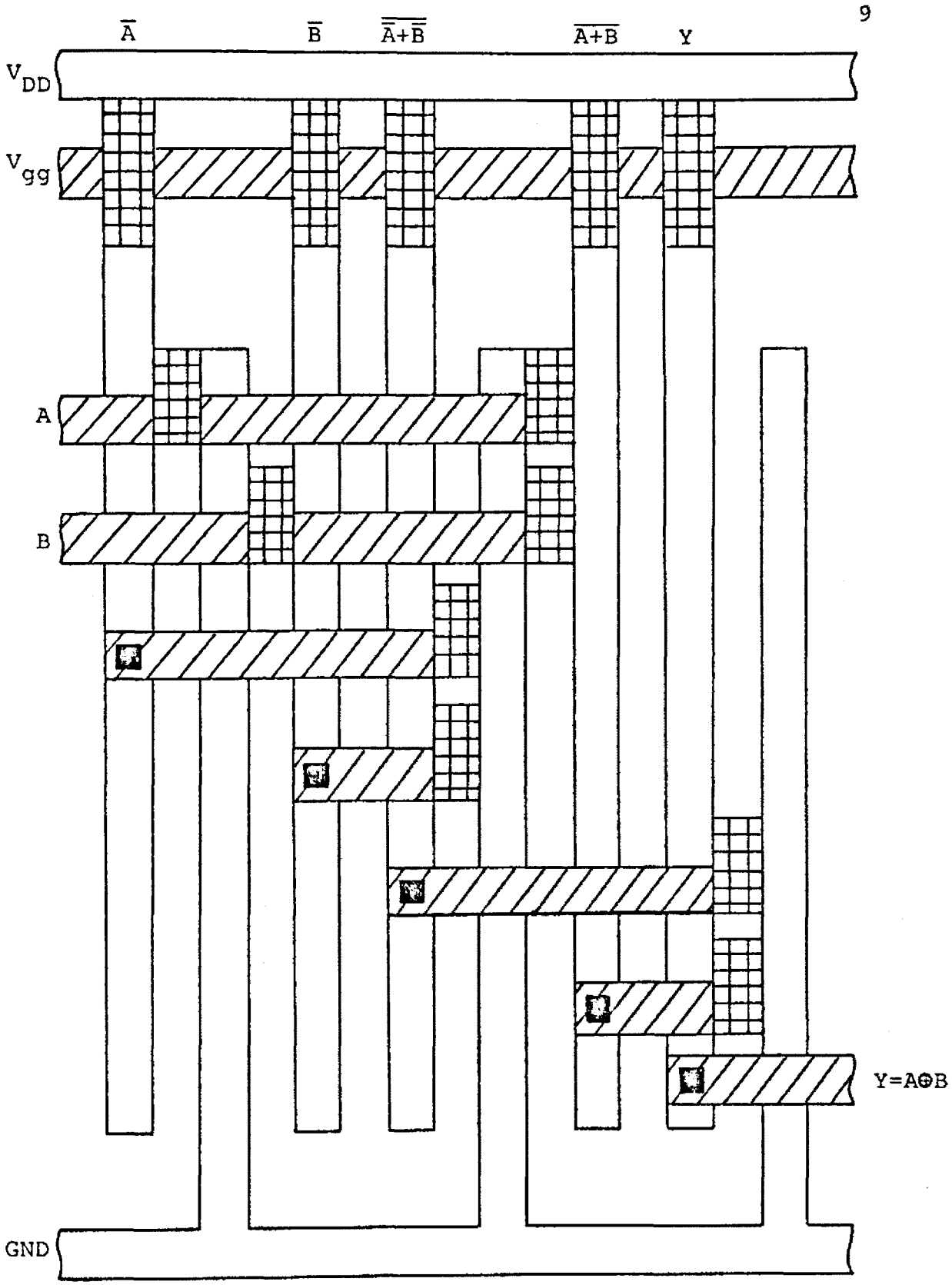


Figure 3. A possible layout for the function Y=A⊕B using the basic pattern.

blocks could be used and laid out in a variety of arrangements.

This layout scheme then, provides several advantages. Not only is the interconnection pattern within the layout simplified, but also signal paths are all parallel, which eliminates the necessity of several layers of metalization. Individual circuit requirements can usually be satisfied since the basic pattern is adaptable to many arrangements.

4. OPTIMIZATION PRELIMINARIES

The standardized pattern described previously yields higher density circuits if the gates are carefully ordered. The purpose of this paper is to describe a simple method of gate ordering which will maximize density.

It is assumed that all inputs into the basic pattern will enter from the left and all outputs out of the basic pattern will exit on the right. Inputs generated within the basic pattern and outputs which do not exit the basic pattern may be in either direction.

Definition 1: An analysis model is a simplified representation of an actual layout. A gate input is depicted by a '1' and an output by an '*'. Signal nets appear as horizontal lines.

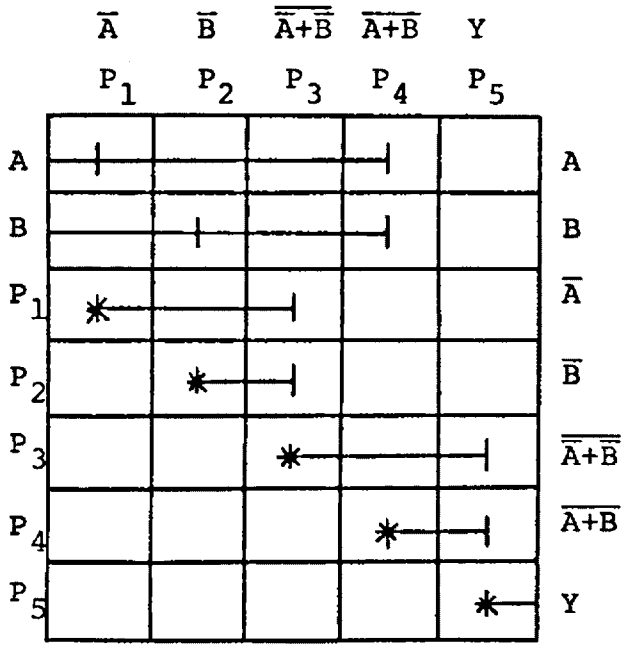
An analysis model for the layout in Figure 3 is given in Figure 4a.

Definition 2: A primitive layout is any layout on the basic pattern in which not more than one gate output appears in any row.

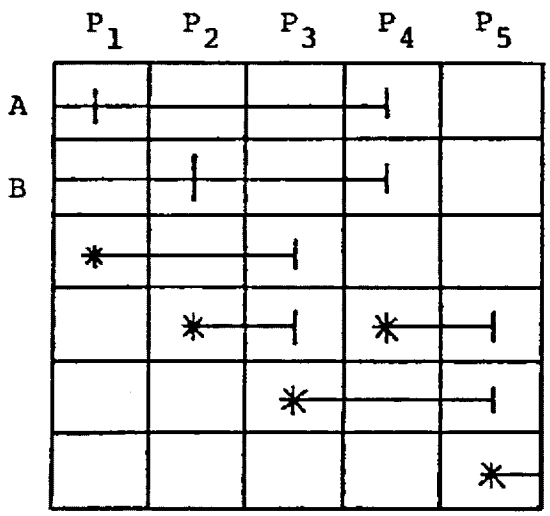
Figure 4a illustrates a primitive layout. The layout in Figure 4b is not primitive since the fourth row contains two gate outputs.

An important measure of the efficiency of a layout is the length of the signal nets. The following three definitions pertain to the measure of signal nets.

Definition 3: A waste cell is an empty cell in the



a) Primitive layout



b) Nonprimitive layout

Figure 4. Examples of analysis models.

analysis model through which a signal net passes.

In the primitive layout shown in Figure 4a, the cells in column $\overline{B}$ which are common to rows A and $\overline{A}$ are waste cells.

Definition 4: The waste Ψ of a given layout is the sum of the waste cells for that layout.

For the layout in Figure 4a, $\Psi = 6$.

Each gate in the analysis model is designated as P_i. For a system of n gates, i is an integer between 1 and n.

Definition 5: $\Delta\Psi(P_i,P_j)$ is the change in Ψ when the columns representing gates P_i and P_j are interchanged.

For example, consider the evaluation of $\Delta\Psi(P_1,P_3)$ for the layout shown in Figure 4a. This is most easily accomplished by computing the change in the number of waste cells in each row when P_1 and P_3 are interchanged. The results of each row are then added to yield $\Delta\Psi(P_1,P_3)$. In row A, a waste cell is eliminated in column P_3 but another is generated in P_1, producing a net change of 0. No waste cells are created or removed in rows B, $\overline{A}$, $\overline{B}$, $\overline{A+B}$ or Y. Thus, the change in these rows is 0. A change of 2 in row $\overline{\overline{A}+\overline{B}}$ occurs since the length of the signal net in that row is increased by 2 cells when P_1 and P_3 are interchanged. Therefore $\Delta\Psi(P_1,P_3) = 2$.

In finding $\Delta\Psi(P_3,P_4)$, rows A, B and $\overline{\overline{A}+\overline{B}}$ give a change of -1 each since signal nets are reduced in these rows. Rows $\overline{A}$, $\overline{B}$ and $\overline{A+B}$ each yield a change of 1 due to increasing signal nets. No waste cell change occurs in row Y because the cells involved are empty. Since the sum of the row changes is 0, this implies $\Delta\Psi(P_3,P_4) = 0$.

As Ψ is reduced, more empty cells are created and signal nets become shorter. This allows for the possibility of more rows being combined. The combining of rows reduces the y dimension of the basic pattern and hence the area. This in turn, increases the density. Therefore, Ψ will be minimized in order to maximize density.

An arrangement of gates is designated as π_i. For example, for a four gate system, the arrangement $P_1P_2P_3P_4$ might be defined as π_0 or the ordering $P_2P_4P_1P_3$ be called π_1.

Theorem 1: If a system in which a gate arrangement π_0 yields the minimum waste Ψ_{min}, then $\Delta\Psi(P_i,P_j) \geq 0$ for all gates P_i and P_j.

Proof: Assume there exists some P_i and P_j such that $\Delta\Psi(P_i,P_j) = -c$, where c is a positive constant. Interchanging gates P_i and P_j yields a new arrangement π_c. $\Psi(\pi_c) = \Psi_{min} - c$. This implies $\Psi(\pi_c) < \Psi_{min}$. This is a contradiction since Ψ_{min} is the minimum waste for this set of gates by definition. Therefore, $\Delta\Psi(P_i,P_j) \geq 0$ for all gates P_i and P_j.

QED

The converse of Theorem 1 will now be proven.

Theorem 2: If an arrangement π_0 of n gates has $\Delta\Psi(P_i,P_j) \geq 0$ for every pair of gates P_i and P_j, then $\Psi(\pi_0) = \Psi_{min}$.

Proof: Assume there exists some arrangement π_1 of these same n gates so that $\Psi(\pi_1) = \Psi_{min}$. For each arrangement π_0 and π_1, there are $n(n-1)/2$ gate pairs, the interchange of which yields $\Delta\Psi \geq 0$. The intersection of these gate pairs, denoted by $\pi_1 \wedge \pi_0$, gives a set of conditions which must hold in order

for $\Delta\Psi \geq 0$ for each pair of interchanges. The remaining $\pi_1 + \pi_0 - 2(\pi_1 \wedge \pi_0)$ pairs represent a set of single interchanges which transform π_0 to π_1 and π_1 to π_0. This set of pairs is called $\overline{\pi_1 \wedge \pi_0}$.

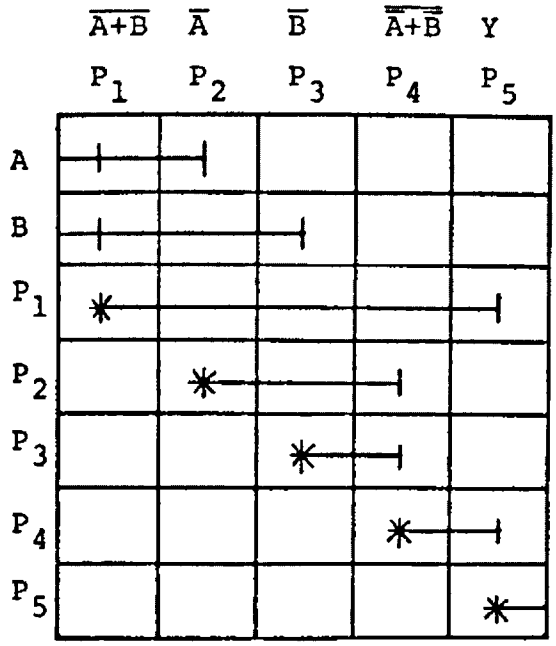
Theorem 2 is shown to be true by proving $\Psi(\pi_0) = \Psi(\pi_1)$ by finite induction. From the set $\overline{\pi_1 \wedge \pi_0}$, there exist a pair of gates P_i and P_j which are neighbors in the arrangement π_1. The interchange of these gates does not violate $\pi_1 \wedge \pi_0$. Assume P_i and P_j are interchanged and the new arrangement is called ${}_1\pi_1$. $\Delta\Psi(P_j,P_i) \geq 0$ in ${}_1\pi_1$ since $\pi_1 \wedge \pi_0$ is satisfied. $\Delta\Psi(P_i,P_j) \geq 0$ in π_1 by initial assumption. Because $\Delta\Psi(P_j,P_i) \geq 0$, $\Delta\Psi(P_i,P_j) \geq 0$ and $\Delta\Psi(P_j,P_i) = -\Delta\Psi(P_i,P_j)$, this implies $\Delta\Psi(P_i,P_j) = \Delta\Psi(P_j,P_i) = 0$. Therefore, $\Psi({}_1\pi_1) = \Psi(\pi_1)$. This is the first case.

Assume $\Psi({}_k\pi_1) = \Psi(\pi_1)$. Again, there exists an interchange in ${}_k\pi_1$ which does not violate $\pi_1 \wedge \pi_0$. This interchange is from the set $\overline{\pi_1 \wedge \pi_0}$. The change in Ψ for this interchange is 0. Hence, $\Psi({}_{k+1}\pi_1) = \Psi({}_k\pi_1) = \Psi(\pi_1)$.

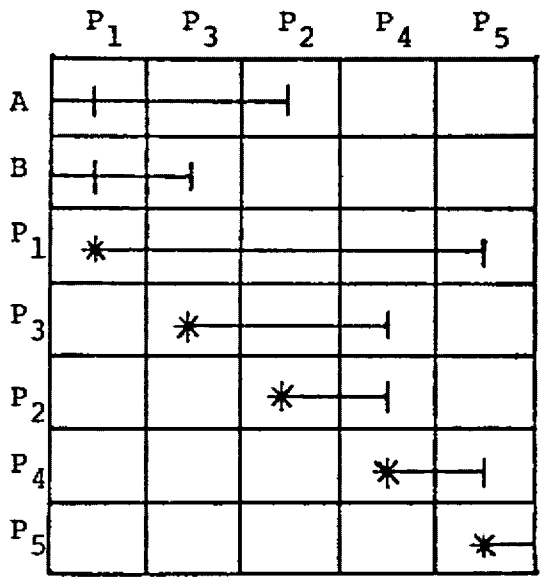
Since a set of neighbor interchanges in $\pi_1 \wedge \pi_0$ transforms π_1 to π_0 and since no change in waste results from these interchanges, this implies $\Psi(\pi_0) = \Psi(\pi_1) = \Psi_{min}$.

QED

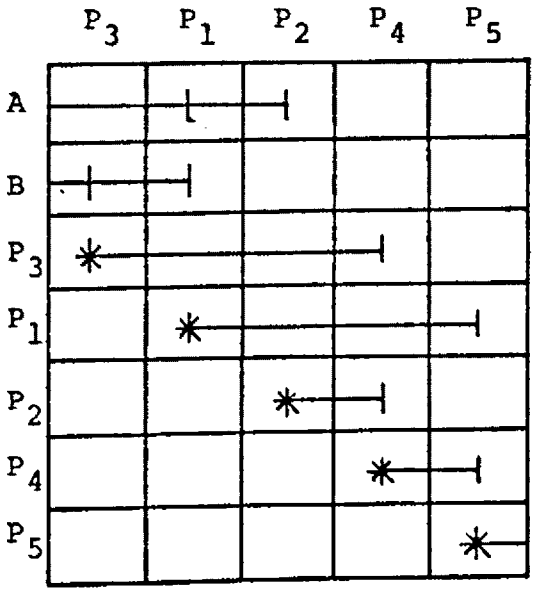
The results of Theorem 2 are illustrated by the following example. For the system $Y = A \oplus B$, let $P_1 = \overline{A+B}$, $P_2 = \bar{A}$, $P_3 = \bar{B}$, $P_4 = \overline{\bar{A}+\bar{B}}$ and $P_5 = Y$ (see Figure 5). Define $\pi_0 = P_1P_2P_3P_4P_5$ and $\pi_1 = P_3P_1P_2P_4P_5$. These are different gate arrangements in



a) Arrangement π_0



b) Arrangement $_1\pi_0$



c) Arrangement $_2\pi_0$

Figure 5. Illustration of Theorem 2 results.

which $\Delta\Psi \geq 0$ for all gates P_i and P_j in each arrangement.

For π_0,

$$(P_i,P_j) = \{P_1,P_2;\ P_1,P_3;\ P_1,P_4;\ P_1,P_5;\ P_2,P_3;\ P_2,P_4;\ P_2,P_5;\ P_3,P_4;\ P_3,P_4;\ P_4,P_5\}$$

and for π_1,

$$(P_i,P_j) = \{P_3,P_1;\ P_3,P_2;\ P_3,P_4;\ P_3,P_5;\ P_1,P_2;\ P_1,P_4;\ P_1,P_5;\ P_2,P_4;\ P_2,P_5;\ P_4,P_5\}$$

$$\pi_0 \wedge \pi_1 = \{P_1,P_2;\ P_1,P_4;\ P_1,P_5;\ P_2,P_4;\ P_2,P_5;\ P_3,P_4;\ P_3,P_5;\ P_4,P_5\}$$

$\pi_0 \wedge \pi_1$ implies P_1 is left of P_2, P_1 is left of P_3 and so on. (P_2,P_3) and (P_1,P_3) represent neighbor interchanges which transform π_0 to π_1 without violating $\pi_0 \wedge \pi_1$. Therefore the following is true.

$$_1\pi_0 = P_1P_3P_2P_4P_5 \qquad \Psi(_1\pi_0) = \Psi(\pi_0)$$

$$_2\pi_0 = P_3P_1P_2P_4P_5 \qquad \Psi(_2\pi_0) = \Psi(_1\pi_0) = \Psi(\pi_0) = \Psi(\pi_1)$$

As a result of Theorem 2, Ψ_{min} is unique for a given set of gates although the gate arrangement yielding Ψ_{min} may not be.

Using the properties of Theorem 1 and Theorem 2, a procedure for obtaining a minimum waste layout is developed in the next section.

5. OPTIMIZATION PROCEDURE

A result of Theorem 1 is that the interchange of any two neighboring columns of a minimum waste layout must produce a $\Delta\Psi \geq 0$.

Definition 6: The condition in which $\Delta\Psi(P_i,P_j) \geq 0$ for all neighboring gates P_i and P_j is called the neighbor property.

Part 1 of a two part process for obtaining an optimum gate arrangement consists of finding a gate ordering which has the neighbor property.

The neighbor property is necessary but not sufficient to insure $\Delta\Psi(P_i,P_j) \geq 0$ for every pair of gates P_i and P_j. In order to guarantee $\Delta\Psi \geq 0$ for the interchange of any two columns, each pair of gates not already tested in Part 1 is compared. This is Part 2.

The process for obtaining a minimum waste layout begins by assigning each gate some value P_i. An initial gate ordering is chosen at random and a primitive layout, using an analysis model, is made. The following algorithm is then used.

Part 1:

A. The gates in neighboring columns are compared. If the interchange of the gates in these columns would yield a nonpositive change in Ψ, the interchange is made. Otherwise, no exchange results. This process begins with the gates in columns 1 and 2. The procedure is then applied to the gates in columns 2 and 3,

and then 3 and 4 and so on until all neighboring gates have been compared. One cycle is thus completed.

B. If no interchanges were made, go to Part 2.

C. Otherwise, neighboring gates are again compared and processed as described in A., with the following modification in interchange rules. If, for some pair of gates P_i and P_j, $\Delta\Psi(P_j,P_i) = 0$ and P_i and P_j were interchanged on the previous cycle because $\Delta\Psi(P_i,P_j) = 0$, P_j and P_i are interchanged only if

1. Another interchange was made during the previous cycle, or
2. A new $\Delta\Psi = 0$ interchange is possible.

D. If an interchange was made during the previous cycle, the procedure is repeated as described in C. This cyclic process of gate comparing coupled with interchange decisions continues until no negative interchanges and no new $\Delta\Psi = 0$ interchanges exist. When this is accomplished, go to Part 2.

Part 2:

Each pair of gates not already compared by the previous procedure is now compared. An interchange is made only if Ψ would be reduced.

The steps of this procedure are illustrated by two examples in the following section.

6. EXAMPLES

Example 1: Obtain a minimum waste layout for the single output function $Y = \overline{C+D} + \overline{\overline{A}+\overline{B}}$. The initial layout is shown in Figure 6a. Table 1 lists the gate comparisons and interchange decisions for each step of Part 1 of the minimization. Analysis models for Part 1 are shown in Figures 6 and 7.

The gates in columns 1 and 2 are first compared, yielding $\Delta\Psi(P_1,P_2) = 3$. This indicates Ψ will increase if P_1 and P_2 are exchanged. Thus, no interchange is made. The gates in columns 2 and 3 are now tested. Interchanging P_2 and P_3 reduces Ψ since $\Delta\Psi(P_2,P_3) = -1$. The new primitive layout is showr in Figure 6b.

The gates in columns 3 and 4 are now compared. Since P_2 is in column 3 and P_4 is in 4, $\Delta\Psi(P_2,P_4)$ is computed and is found to be 0. Because this represents a new $\Delta\Psi = 0$ interchange, the exchange is made. Figure 6c illustrates the primitive flow table after this exchange.

The first cycle of gate comparisons is completed by evaluating $\Delta\Psi(P_2,P_5)$. The value of $\Delta\Psi$ is found to be 3, so no interchange is made.

Because an interchange was made during this cycle, the procedure begins again with the first two columns. The remaining comparisons and decisions for Part 1 are shown in Table 1. The comparison calculations for Part 2 are given in Table 2. The preceding calculations indicate $\Delta\Psi(P_i,P_j) \geq 0$ for all gates P_i and P_j. Therefore, by Theorem 2, this gate arrangement produces minimum waste. The minimum waste layout is shown in Figure 8.

TABLE 1. Calculations and interchange decisions for Part 1 of Example 1.

(P_i, P_j) UNDER TEST	$\Delta\Psi(P_i, P_j)$	SWITCH P_i AND P_j	FIGURE
P_1, P_2	3	no	6a
P_2, P_3	-1	yes	
P_2, P_4	0	yes	6b
P_2, P_5	2	no	6c
End of Cycle			
P_1, P_3	0	yes	
P_1, P_4	-1	yes	6d
P_1, P_2	1	no	7a
P_2, P_5	2	no	
End of Cycle			
P_3, P_4	-1	yes	
P_3, P_1	0	yes	7b
P_3, P_2	1	no	7c
P_2, P_5	2	no	
End of Cycle			
P_4, P_1	1	no	
P_1, P_3	0	yes	
P_1, P_2	1	no	7d
P_2, P_5	2	no	
End of Cycle			
P_4, P_3	1	no	
P_3, P_1	0	no	
P_1, P_2	1	no	
P_2, P_5	2	no	8
End of Cycle			

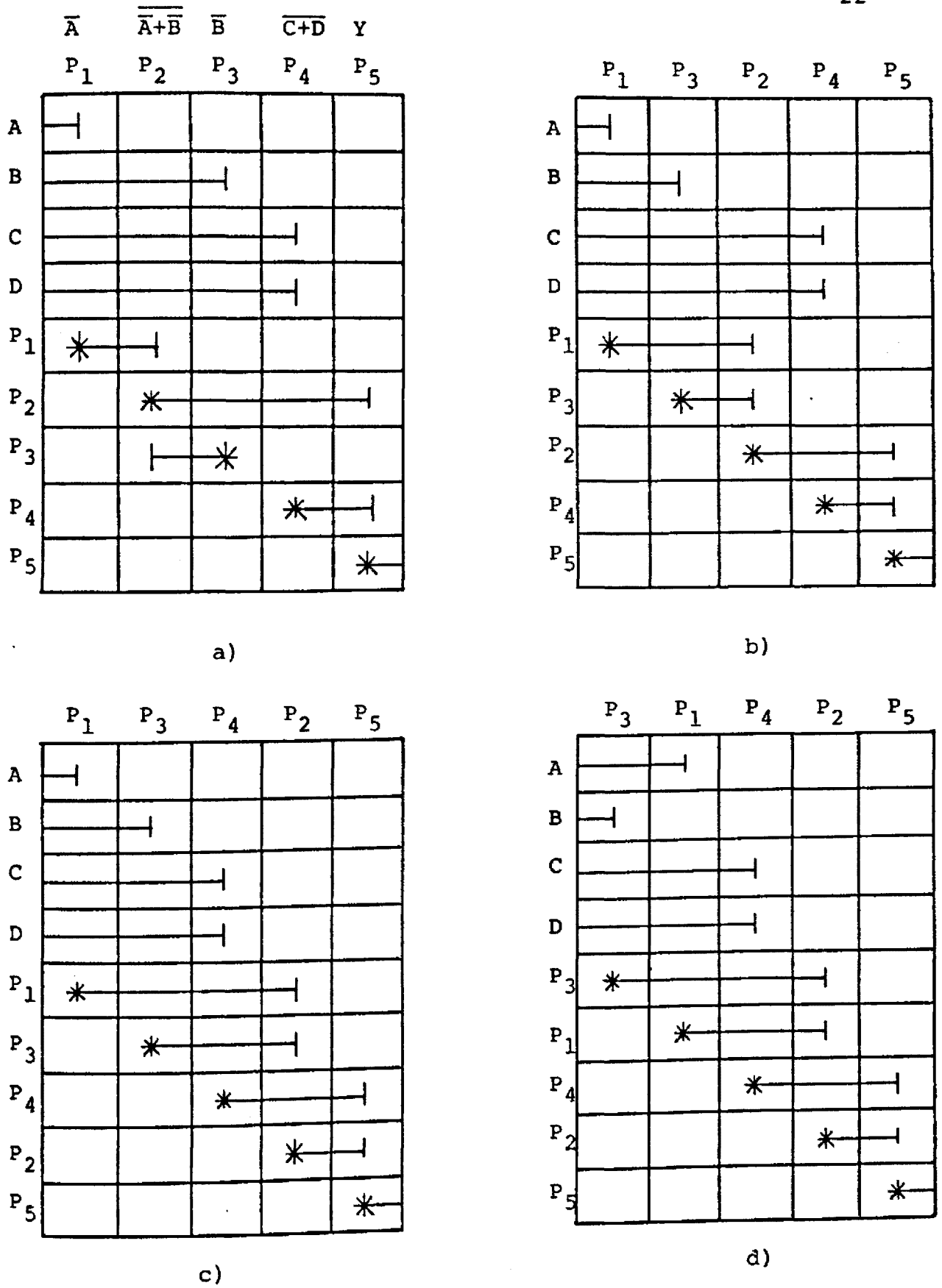


Figure 6. Analysis models for Example 1.

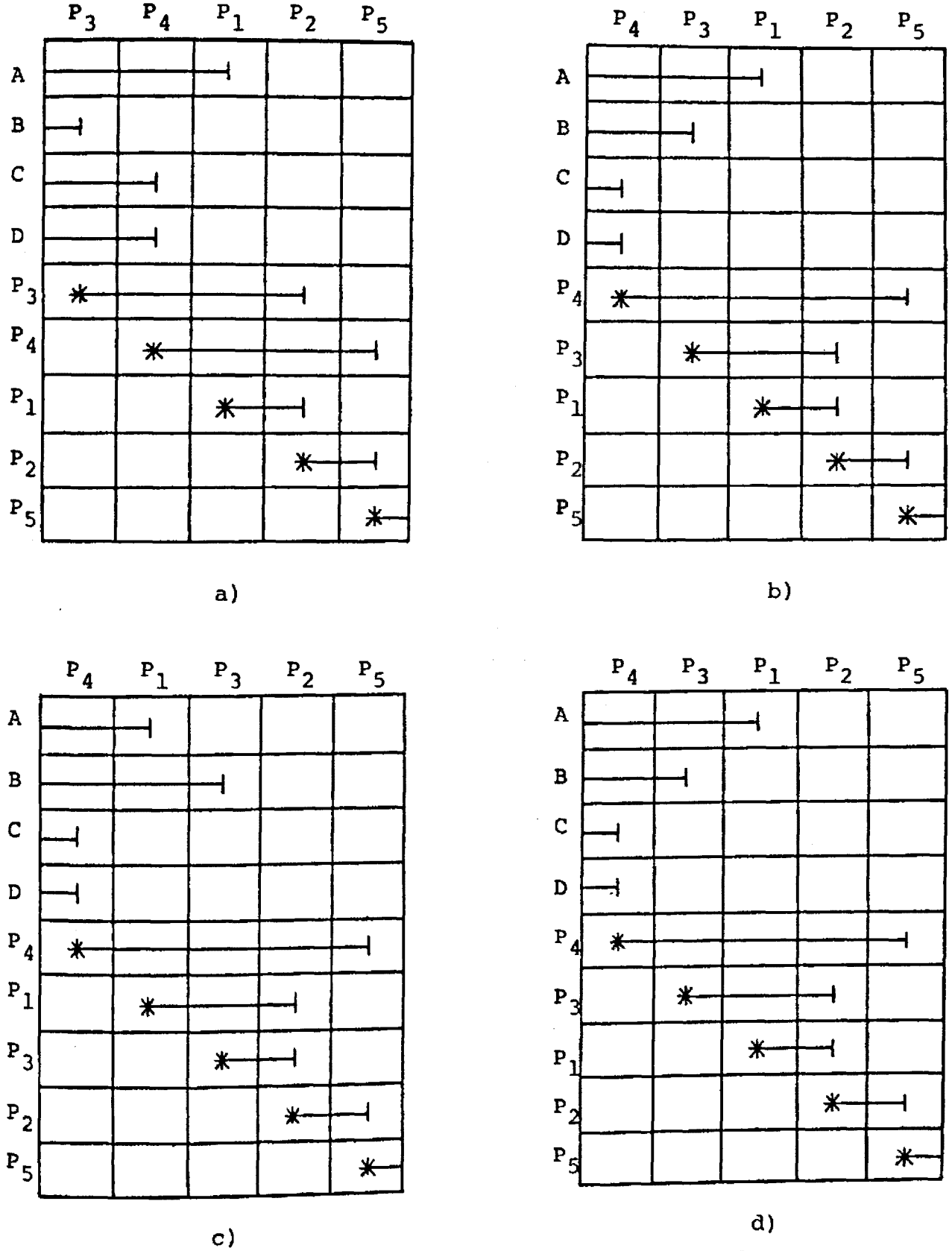


Figure 7. Analysis models for Example 1.

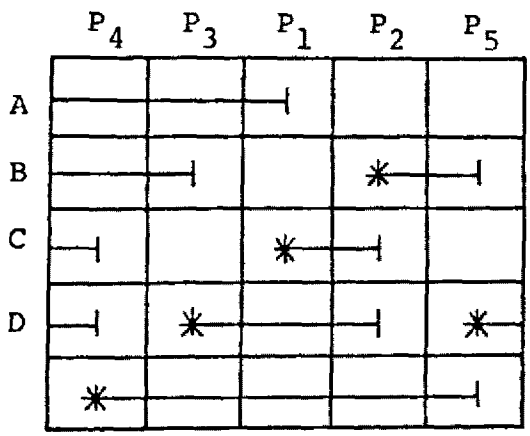


Figure 8. Minimum waste layout for Example 1.

TABLE 2. $\Delta\Psi(P_i,P_j)$ Calculations for Part 2 of Example 1.

	P_4	P_3	P_1	P_2
P_3	1			
P_1	2	0		
P_2	6	4	1	
P_5	14	3	2	2

Example 2: Find a minimum waste layout for the multiple output system $Y_1 = A+\bar{B}$ and $Y_2 = \overline{B+C}$. The procedure is the same as was illustrated by the first example. Part 1 calculations and interchange decisions are given in Table 3. Table 4 contains the calculations of Part 2.

The initial arrangement is shown in Figure 9a and the minimum waste layout is illustrated in Figure 10c.

TABLE 3. Calculations and interchange decisions for Part 1 of Example 2.

(P_i, P_j) UNDER TEST	$\Delta\Psi(P_i, P_j)$	SWITCH P_i AND P_j	FIGURE
P_1, P_2	0	yes	9a
P_1, P_3	1	no	9b
P_3, P_4	-1	yes	
End of Cycle			
P_2, P_1	0	yes	9c
P_2, P_4	0	yes	9d
P_2, P_3	3	no	10a
End of Cycle			
P_1, P_4	-1	yes	
P_1, P_2	1	no	10b
P_2, P_3	3	no	
End of Cycle			
P_4, P_1	1	no	
P_1, P_2	1	no	
P_2, P_3	3	no	10c
End of Cycle			

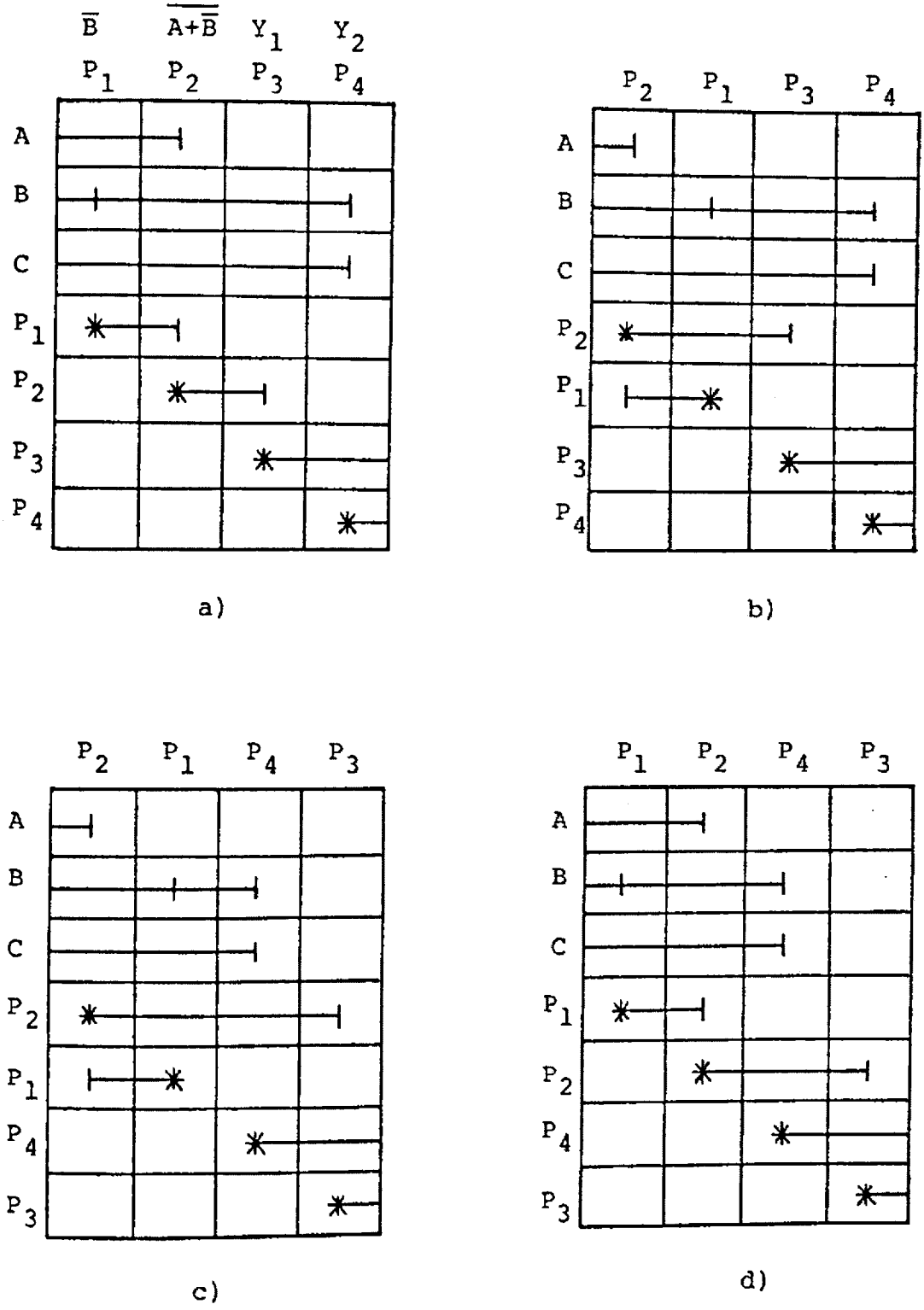
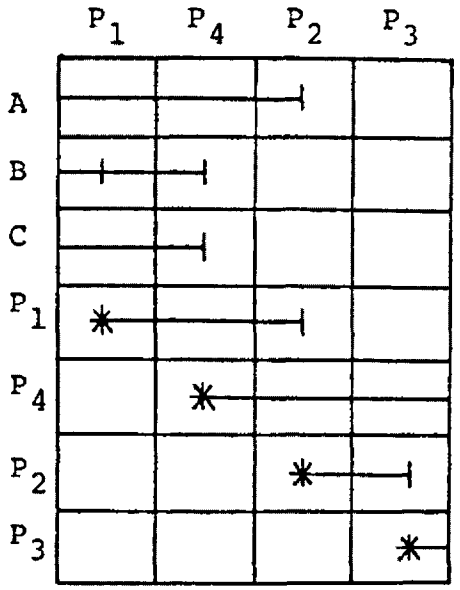
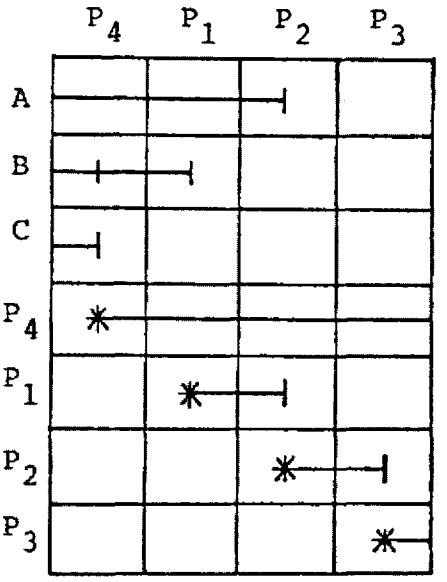


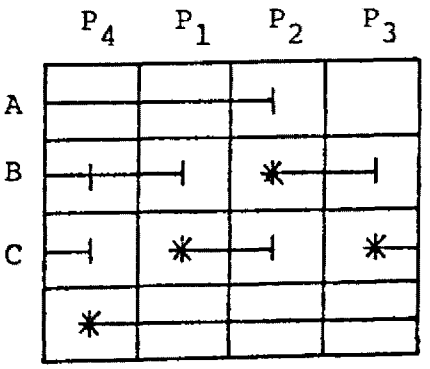
Figure 9. Analysis models for Example 2.



a)



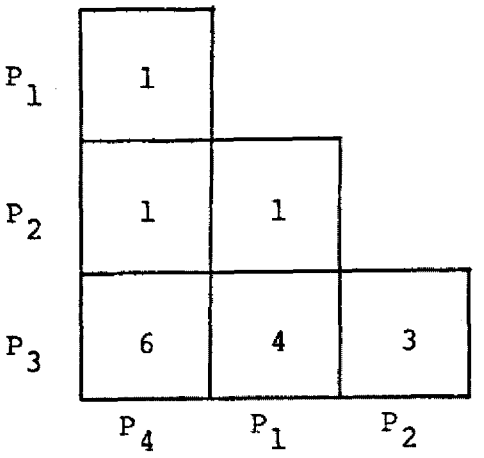
b)



c) Minimum waste layout

Figure 10. Analysis models for Example 2.

TABLE 4. $\Delta\Psi(P_i,P_j)$ Calculations for Part 2 of Example 2.



7. CONCLUSION

The importance of the MOSFET in digital circuits has been discussed and a standardized layout pattern which has the potential of providing for reasonably high density circuits has been reviewed.

A method for optimizing circuit density has been developed. This procedure is both simple and easy to program. This is important for the automation of layout design.

Part 1 of the process often yields a minimal or near minimal solution. This part provides a systematic method for interchanging gates which gives a gate arrangement having the neighbor property. Since the neighbor property is necessary but not sufficient to insure an optimum solution, Part 2 is necessary. This consists of comparing the remaining gate pairs and interchanging those that would reduce the waste.

Further research should examine methods which could reduce the number of calculations required by Part 2.

REFERENCES

[1] J. Millman and C. Halkias, Integrated Electronics: Analog and Digital Circuits and Systems. New York: McGraw-Hill, 1972.

[2] F. Faggin, "The role of technology in microcomputer design and evolution," Circuits and Systems, vol. 7, no. 5, pp. 4-13.

[3] R. H. Crawford, MOSFET in Circuit Design, New York: McGraw-Hill, 1967.

[4] L. Altman, "Improved n-channel processes make their move in memories, Electronics, May 8, 1972, p. 106.

[5] R. J. Huber et al., "Simplified n-channel process achieves high performance," Electronics, March 7, 1974, pp. 117-122.

[6] R. Abbott, H. Gopen, T. Rowe, and D. Bryson, "N-channel goes to work with TTL," Electronics, May 8, 1972, pp. 107-110.

[7] A. Weinberger, "Large scale integration of MOS complex logic: A layout method," IEEE J. Solid-State Circuits, vol. SC-2, pp. 182-190, December 1967.