Ultra Thin Solar Cells

by

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Thesis topic:

Ultrathin Silicon Solar Cells

Abstract

Top-down approaches for the fabrication of semiconductor micro/nano scale elements consist of a series of strategies that use lithographically patterned wafers for generating semiconducting structures in forms ranging from wires, ribbons, bars and platelets. Recently, the use of top-down approaches for applications in large area flexible electronics has generated a great deal of interest due to the ability to integrate certain structural forms with thin plastic sheets. This report will describe (i) the research topic and goals of this work, (ii) procedures for the fabrication of silicon microstructures, (iii) initial solar cell results, (iv) stretchable PV, (v) high voltage mini module.

i) Introduction

During the last half century, aggressive reductions in the critical dimensions (i.e., channel lengths and dielectric thicknesses) of transistors in microelectronic systems have led to enormous increases in speed, functionality and computing capacity. Over the last ten years, a much different class of electronics, sometimes referred to as “macro electronics” or “large-area electronics”, has emerged and has generated a great deal of interest [1]. A common example of a macro electronic system is flat-panel display that uses thin film transistor (TFT)-on-glass technology for active matrix pixel addressing. The success of such large area displays could lead to new applications of macro electronics, including flexible photovoltaic systems, paper-like displays, and conformal structural health monitors, in which lightweight, flexible substrates facilitate system transport and use [1,2]. These possibilities create substantial interest in materials

and fabrication techniques that enable electronic devices to be formed, in scalable ways, directly on flexible substrates such as metal foils or ideally on thin sheets of plastic. The main challenge for macro electronics is that the characteristics of the plastic substrates and the large area requirements often impose limitations on materials choices and fabrication processes (i.e., high temperature processing steps). The broad goals of this research are as follows: **(i)** Develop top-down fabrication strategies for generating single crystal micro/nano scale elements from bulk wafers **(ii)** Build technologically and/or scientifically relevant systems and devices that incorporate these microstructures as active components. This thesis will explore a combination of theoretical and experimental studies for the development, characterization and optimization of silicon microstructures for photovoltaic applications.

ii) Fabrication of semiconductor micro/nano scale elements

There are two general approaches for the fabrication of semiconducting micro/nano scale objects: The "bottom-up" approach and the "top-down" approach. The bottom-up approach relies heavily on chemically synthetic procedures used to generate nano wires by exploiting the highly favored reaction between gaseous precursor composed of semiconducting materials and catalytic nano particles [3-5]. An impressive array of unusual hetero structured nano wires with interesting properties has been demonstrated by the bottom-up approach[4,6-8]. Other advantages are that large quantities of material can be formed and very small dimensions can be obtained.

Recently, an alternative approach that uses photo-lithographically patterned substrates to etch, slice and cave semiconducting microstructures from a source wafer, commonly referred to as top-down strategies, has emerged[9-13]. An attractive feature of this approach is that wafer-scale procedures, including doping technologies, dielectric materials and device layouts can be

readily exploited. Also, these approaches take advantage of processing procedures used by the semiconductor industry. In is simplest form, top-down fabrication uses source wafers with embedded sacrificial layers (i.e., SiO_2) such as silicon on insulator (SOI) [12]. In this case the sacrificial layer is selectively etched away by hydrofluoric acid, which subsequently releases the silicon microstructures from the source wafer. The SOI approach is attractive because of its simplicity, however, it is cost prohibitive for systems that require electronics to distribute over large areas. Therefore, complimentary approaches that utilize bulk wafers (i.e., less expensive) are of special interest.

In one such approach, anisotropic chemical etching of bulk silicon (111) wafers can generate single crystal silicon ribbons, platelets and bars [9-11]. Our initial work demonstrated that a series of vertical and horizontal etches on bulk Si (111) wafers could be implemented to fabricate thin Si ribbons [10,11]. These approaches, however, had the following disadvantages: (i) The ribbons showed a high degree of surface roughness, which could introduce problems for printing these structural forms onto plastic substrates or interface problems for dielectric materials. (ii) The structures exhibited large thickness variations and defects. (iii) The problem is not robust and the spatial dimensions of features that can be generated are limited. Recently, we have extended this work in two important ways. First, the newly refined procedure increases the level of control over the dimensions and morphologies of the fabricated structures. Second, and most interesting, the optimized procedure allows the ability to produce new microstructures (i.e. thick silicon bars and platelets) whose geometries can be exploited in other research areas.

Figure 1 depicts the fabrication sequence. The process begins with patterning lines of resist perpendicular to the Si $(1\,\bar{1}\,0)$ planes and then etching trenches into the exposed silicon (Figure 1C). The key innovation of this work is the KOH refining step (Figure 1D) which turns a

non-ideal rough surface into a smooth surface with rectangular features. Interestingly, these

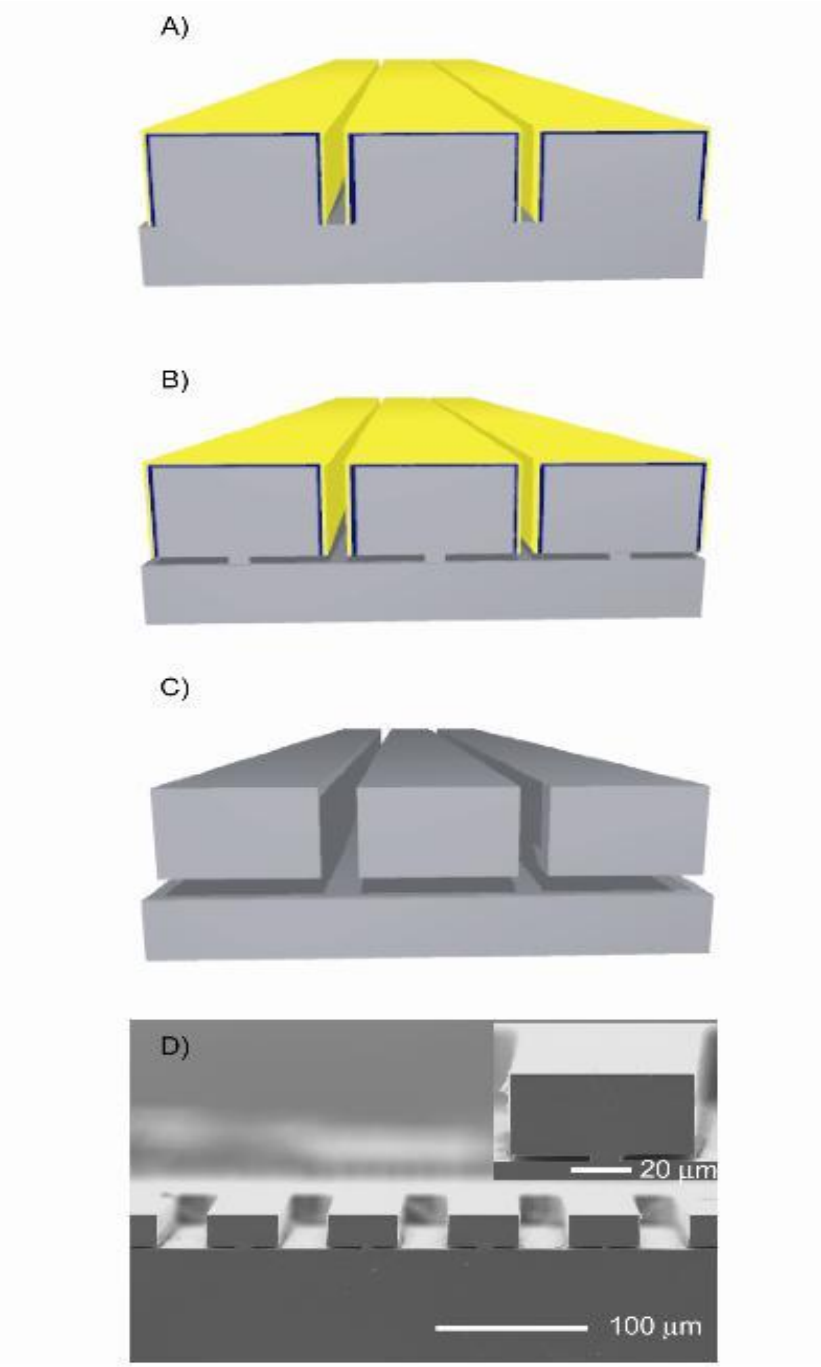

Figure1. SOG

rough surfaces were one of the main disadvantages of our previous work. Depositing a resist layer (SiO_2 (~60 nm)/Si_3N_4 (~300 nm) on all of the silicon surfaces followed by electron beam evaporation of metal and then removing the unprotected SiO_2/Si_3N_4, readies these surfaces for anisotropic undercut. The Si $(1\,\bar{1}\,0)$ etch fronts proceed in a horizontal fashion until they meet to complete the undercut and release freestanding single crystal silicon nano/microstructures. By carefully controlling the processing parameters, ribbons, platelets and bars with dimensions between 100 nm and the size of the wafers (thickness and diameters) can be formed inflexible and stretchable configurations [9]. Collectively, these results provide a promising route for fabrication of silicon structural form factors for applications in flexible large area electronic systems.

iii) Fabrication of Silicon microbar (μb) Solar Cells

Single crystal silicon represents the dominant cell material for PV devices. The current trend in Si PVs is to reduce the amount of silicon usage, because the use of high quality silicon wafers contributes a substantial fraction (~ 50 %) to the overall cost of mono-Si solar modules. Therefore, there is a significant interest in reducing the thickness of conventional "bulk" silicon solar cells. For example, current bulk silicon devices have an average thickness of 300 μm and recently various attempts have been demonstrated that reduce this thickness to 150 μm, however, it is impractical to handle and process wafers in this thickness range using conventional fabrication strategies [14]. Current research in silicon PV focuses on developing thin film PV devices, preferably from low cost materials or processing methods [14,15]. For instance, implementing the processing procedures depicted in Figure 1 for the fabrication of Si microbar solar cells represent one possible route. Introducing a spin-on dopant (boron or phosphorus) step in the process flow leads to the fabrication of thin strips of single crystal silicon solar cell devices.

These microstructures can also be manipulated with ease and printed onto virtually any substrate by using established soft stamping techniques [16]. The key aspects of our work include (i) dramatic reduction and efficient use of silicon wafers, thereby possibly reducing the total cost of silicon PVs, (ii) development of lightweight, mechanically flexible modules, (iii) printing sparse arrays of thin Si μb solar cells combined with micro-optics for the fabrication of concentrator systems and transparent PV modules. Related Si thin-film technologies have been demonstrated [17,18]. Figure 2 shows representative μb silicon solar cell strips fabricated bulk wafers. As a consequence of our optimized fabrication strategies [9] excellent control over the thicknesses of our Si devices can be obtained. Our initial results are promising with individual Si μb devices demonstrating efficiencies as high as 10 % under AM 1.5 conditions. Figure 3 and 4 show the calculated efficiency, Voc and Jsc values plotted as a function of thickness for our devices. The results illustrate the potential use of solar grade silicon at ultrathin thickness, thereby providing a possible overall cost reduction by employing nonelectronic grade starting materials.

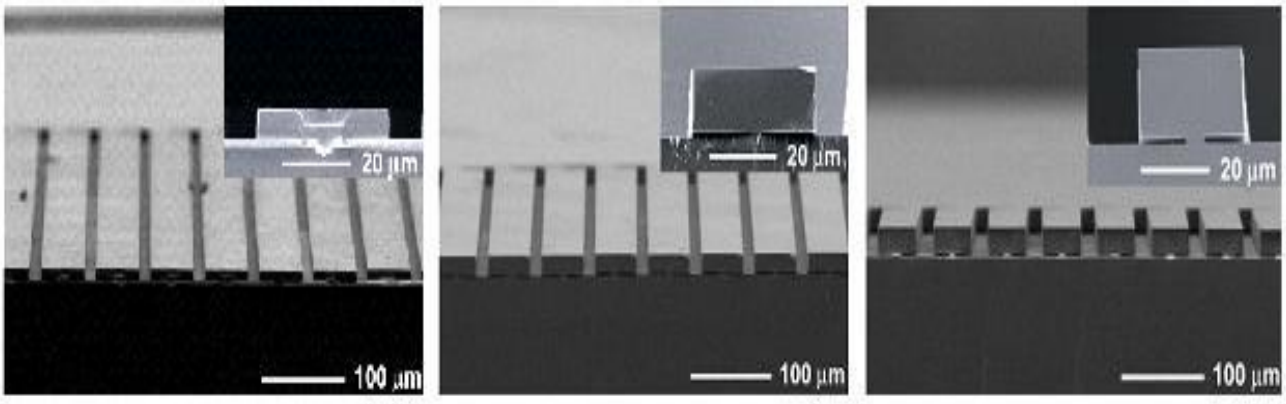

Figure 2. Si μb-cells with different thickness

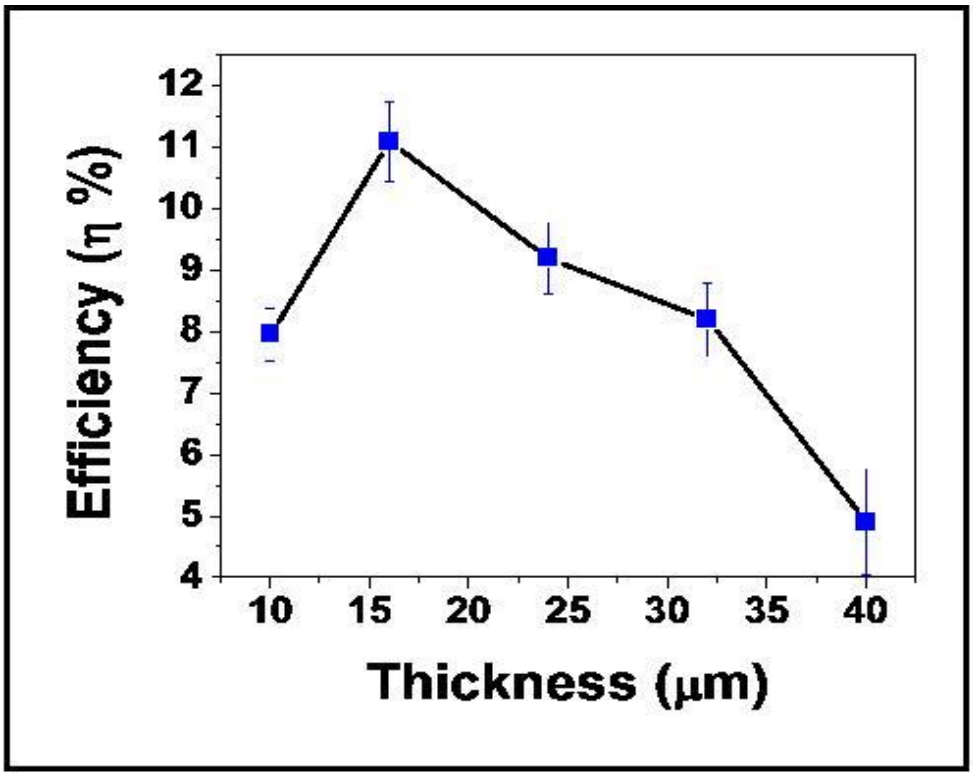

Figure 3. Efficiency vs thickness

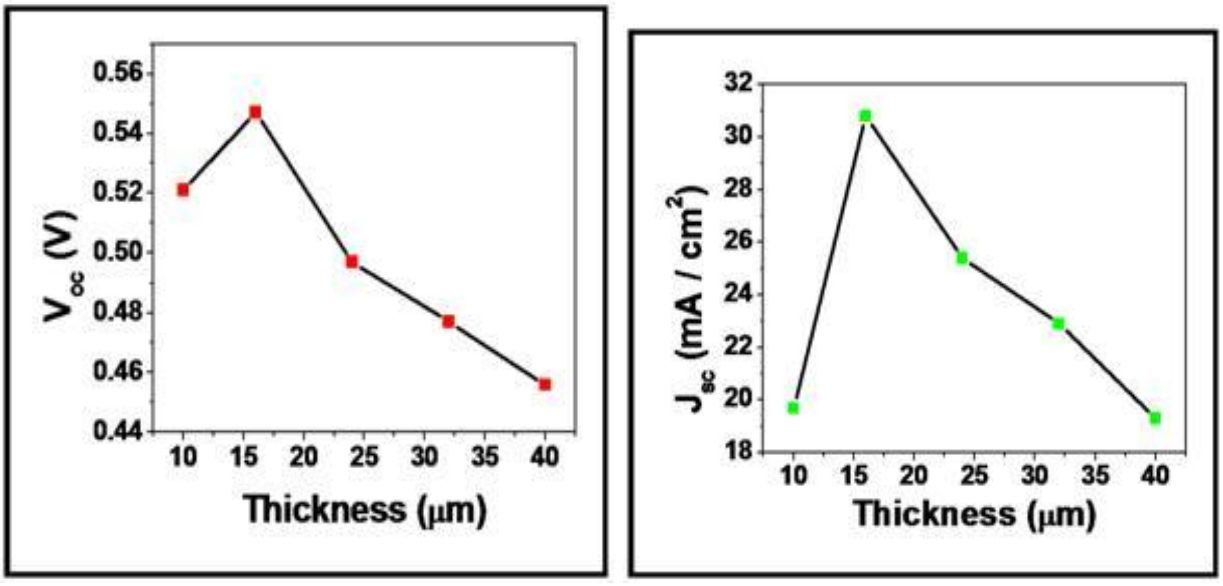

Figure 4. Voc and Jsc vs device thickness

iv) Stretchable PV

For the stretchable PV device, metal interconnection between cells determines the prestrain. For example, the prestrain of an electronic cloth would be ~ 25%, so if we can create a system that can be subjected to strains larger than 25% of the prestrain, we could bend and stretch the electronic cloth without changing its function. Our initial work centered on the ability to control the width and height of our devices and calculate the prestrain present in our interconnects. Figure 5 depicts our first design / attempt to achieve a stretchable solar fabric. This design, however, suffered from cracks and or breaks along the length of the interconnect area, so a new design was created.

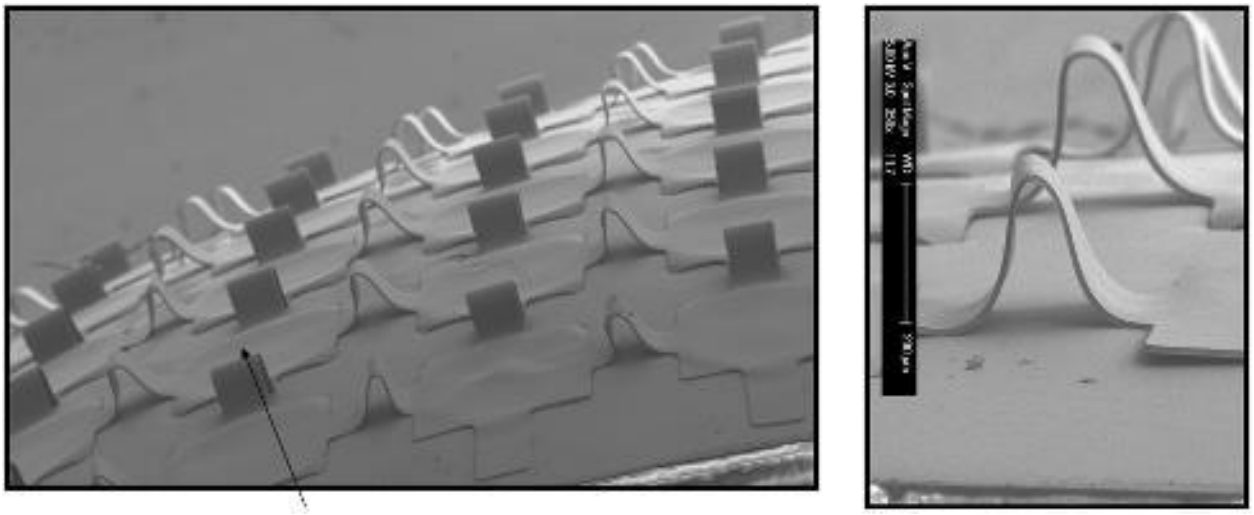

Figure 5. Old design of ultra thin microbar structures for PV

The process for our new design begins with establishing the width and length of our interconnect bridges. The width of our old design was 200 μm and the length was 400μm. However, the prestrain came out to be about 20%, which did not exceed the design limitation of 25%. So, we have changed our design to a width of 300 μm and length of 800 μm. Basically, after we increased the length and decreased the width of our interconnects, we were able to get higher

prestrain levels of about 27%. Figure 6 shows our images of our new and improved design. Thus, this device is more suitable for applications that require large levels of stretching and flexibility.

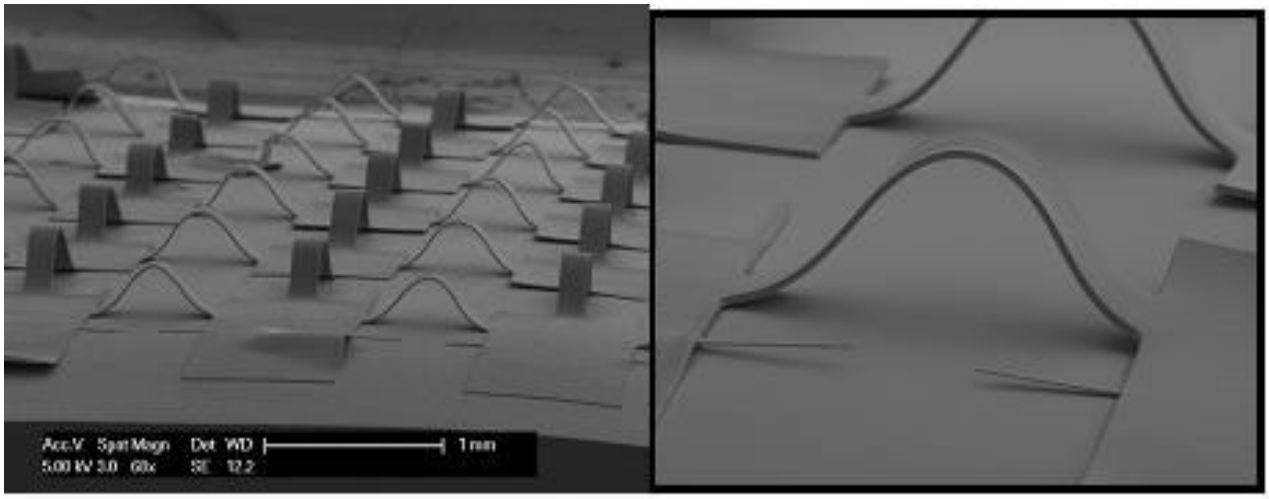

Figure 6. Old design of ultra thin microbar structures for PV

v) High Voltage mini module

Some applications require let's say European regular house output voltage is 220 V in order for electronics to run. Conventional systems for this are really large and require multiple stacks of large area cells. However, now we can create small (several microns squared) modules that produce high voltages. There is a cost advantage for creating the same amount of voltage as conventional cells but at much smaller areas. Also, we will create flexible modules in this case as well which will enable the use of this modules in systems that require some amount of flexibility. In order to fabricate high voltaic mini module, we use the method called alternating window opening. Using of different masks, we open the windows and perform Boron and Phosphorus doping. Figure 8 describes how the high voltaic mini module looks like. The stack of n-type and p-type doping is connected in series, so this design produces high voltage, which is about 200V and 300V. Basically, built in potential of p-n junction is about 0.6V. Therefore, series of built in potential of these p-n junctions produce high voltage.

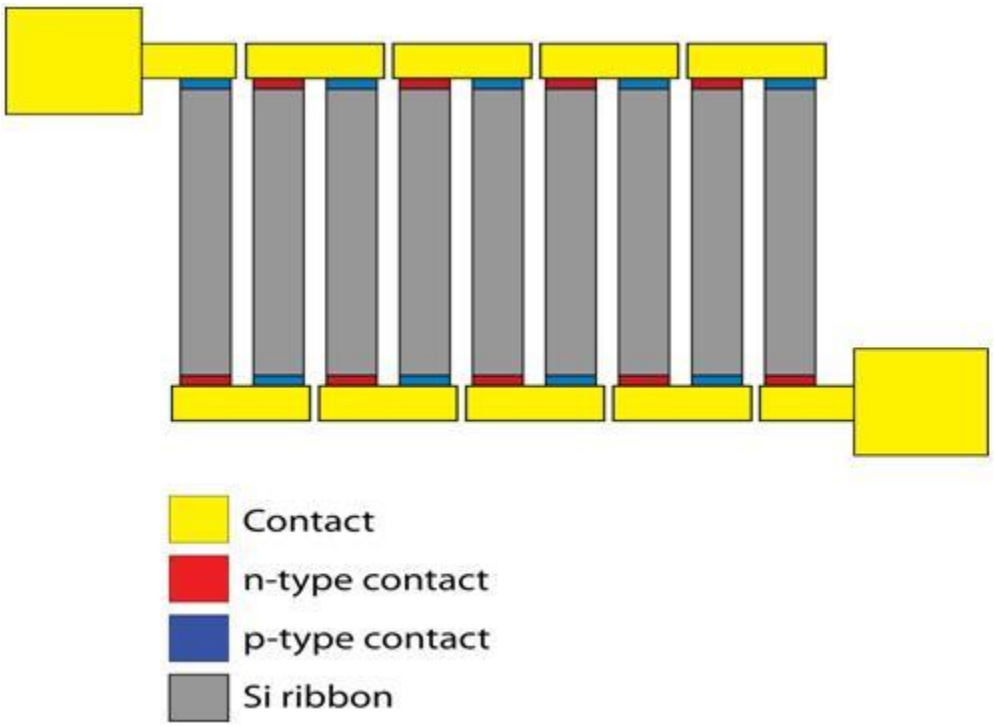

Figure. 7 High voltaic mini module cell layout

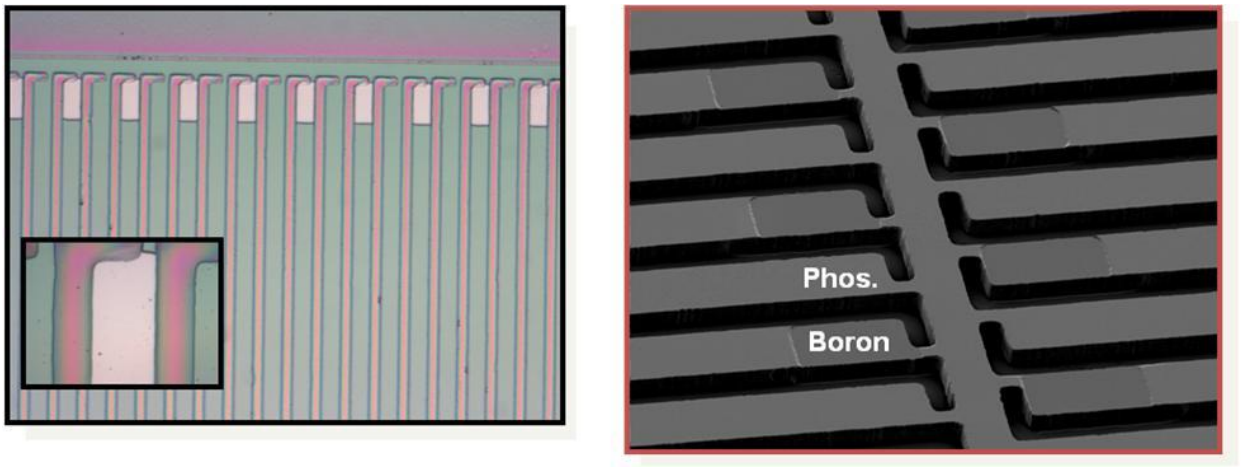

Figure 8. Alternating window opening

Figure 8 depicts representative high voltaic mini module cells used alternating window opening.

vi) Future Research Plans

- Further investigate the use of Si (111) structures for photovoltaic applications
- Study the effect of antireflective coatings, surface texturization and metals contacts on cell performance metrics.
- Investigate silicon wafers of varying purity (collaboration with Dow).
- Develop a high-voltage minimodule.
- Investigate and develop light trapping / surface texturization schemes for Si (111) surface.
- Model Si (111) solar cell design and current voltage characteristics by PC1D software and diode fit models.

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