HIGH-FIELD TRANSPORT IN TWO-DIMENSIONAL GRAPHENE AND MOLYBDENUM DISULFIDE

BY

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DISSERTATION

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ABSTRACT

My research focuses on the study of nanoscale transistor physics, particularly that of atomically-thin two-dimensional (2D) crystals such as graphene and molybdenum disulfide (MoS$_2$). The excellent electrical and thermal properties of 2D materials like graphene have attracted much attention for potential applications in integrated-circuit technology. Understanding high-field transport in a semiconductor material is crucial not only from the perspective of fundamental device physics, but also for achieving practical device applications. Unfortunately, many of the early measurements on these materials, especially graphene, were focused on low-temperature and low-field physics.

Motivated by the above, we investigate electrical transport in graphene across a wide range of temperatures (including near and above room temperature) up to high electric fields ($> 1$ V/µm) typical of modern transistors. For our measurements, we carefully engineered test structures to obtain uniform potential and heating along the channel, and we developed simple yet practical models for heating and high-field drift velocity in graphene, including the roles of both temperature and carrier density. We find that transport in supported-graphene devices does not resemble that of ideal graphene, indicating that interactions with the underlying SiO$_2$ play a role in limiting high-field transport.

We sought to understand the intrinsic electrical and thermal properties of graphene, by examining devices freely suspended across microscale trenches. We study the coupled electrical and thermal transport in suspended graphene at high-fields, extracting both high-field drift velocity and thermal conductivity at breakdown of graphene up to higher temperatures than previously possible (300-2200 K). We also directly measure the temperature rise due to self-heating in an electrically biased suspended graphene device via Raman thermometry.
Lastly, we investigate the electron transport properties of few-layer MoS$_2$ transistors. We observe a strong temperature dependence of low-field mobility as well as strong self-heating effects during high-field operation. Interestingly, we observe high-field negative differential conductance (NDC) at low temperature and high bias. Our high-field electrical measurements, combined with detailed modeling and simulations, allow us to provide insight into the high-energy band structure of MoS$_2$.

As the scaling of transistor lengths approaches 10 nm, it becomes necessary to investigate novel materials for future nanoscale electronics. The atomically-thin body of 2D materials makes them robust against short-channel effects, which could enable scaling down to sub-10 nm MOSFET channel lengths. Additionally, these materials may prove useful for new applications that take advantage of their inherent 2D nature.
To my grandparents for emphasizing the importance of education, and to my brothers for their continuing guidance.
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CHAPTER 1: INTRODUCTION

1.1 Power Dissipation and Scaling in Integrated-Circuit Technology

The ability to consistently scale down the size of a transistor in integrated-circuit (IC) technology has been the crowning achievement of the semiconductor industry for the last several decades. This trend in scaling, commonly referred to as Moore’s Law [1], has resulted in the doubling of the number of silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) for a given area approximately every two years [2], as shown in Fig. 1.1. The obvious result of scaling is an increase in functionality due to the increased number of transistors per unit area, but another benefit from scaling is the enhanced performance of the individual transistor.

However, as feature sizes of silicon transistors approach the nanometer scale, transistor performance no longer scales in proportion with device dimensions, particularly channel length, $L$. The trends of power supply voltage, $V_{DD}$, and threshold voltage, $V_T$, for transistors with shorter channel lengths exemplify this issue, such that $V_{DD}$ no longer scales proportionally with $L$, and $V_T$ no longer scales proportionally with $V_{DD}$ [3]. This occurs due to a tradeoff between circuit speed versus leakage current when adjusting $V_{DD}$ and $V_T$, where scaling down the threshold voltage may improve switching speed but will also cause an exponential increase in the “off” current.

The inability to scale down $V_{DD}$ proportionally with $L$ causes a problem with respect to power dissipation. The static power of a transistor circuit may be defined by its leakage current and supply voltage where $P_{\text{STATIC}} = I_{\text{LEAK}} V_{DD}$. The dynamic or switching power of a transistor circuit is given by $P_{\text{DYN}} = CV_{DD}^2 f$, where $C$ is the circuit’s total equivalent capacitance charged and discharged in a clock cycle and $f$ is the clock frequency. Both the static and dynamic power increase with increasing $V_{DD}$; thus, $V_{DD}$ not scaling with $L$ has caused the power density of pro-
Figure 1.1: Scaling of MOSFET gate lengths through the decades in production-stage ICs as of 2010 (solid red circles) and International Technology Roadmap for Semiconductors (ITRS) targets (open red circles). The corresponding increase in the number of transistors per processor (blue stars) is shown on the right axis [2].

Processors to increase exponentially over time, as shown in Fig. 1.2. Therefore, future scaling is limited by the rate at which heat can be removed from the circuit [4, 5]. Furthermore, the increasing use of IC technology has made reducing power dissipation in integrated electronics essential, as the U.S. information technology infrastructure uses up to 10% of national electricity today, a figure that may triple by 2025 [6]. In addition, PCs in corporate offices are responsible for CO₂ emissions equivalent to that of approximately 5 million cars. Based on simple estimates, even a 2x more energy-efficient transistor would lower nation-wide power use by over 10 GW. Thus, developing low-power nanoscale devices will affect energy consumption by society as a whole, and has great environmental implications as well.

It is also important to point out that, as scaling has become more difficult with each new process cycle, novel device structures are needed in order to improve short-channel performance. The most prominent examples of novel device structures are multiple gate field-effect transistors
(FETs), often referred to as FinFETs [7] or Tri-Gate FETs [8, 9]. These device structures take advantage of improved electrostatics in order to continue transistor scaling. This motivates research that investigates the use of atomically thin materials as the channel material for transistors, as 2D materials present the opportunity for ideal electrostatics and are optimal for the ultimate ultra-thin body FET [10, 11]. This concept will be expanded upon further in Chapter 2.

1.2 Graphene

Graphene is a two-dimensional (2D) crystal of carbon atoms arranged in a hexagonal structure (see Fig. 1.3a,b), where each atom is bonded to its nearest neighbor by a strong covalent sp² bond. Each atom also shares a π bond with its three nearest neighbors, which results in a band of filled π orbitals (valence band) and a band of empty π* orbitals (conduction band). The thickness of a single sheet of graphene is 0.34 nm. The electronic band structure of graphene is shown in Fig. 1.3c,d. From the diagram, we see that the Dirac point (K or K') is where the va-
Figure 1.3: (a) Hexagonal lattice of graphene, which consists of two interpenetrating triangular lattices [12] and (b) corresponding Brillouin zone. The distance between adjacent carbon atoms is 1.42 Å and the distance between carbon atoms in different layers (i.e., graphene thickness) is 3.4 Å. (c) Band structure of graphene showing ab initio (solid lines) and tight binding (dashed) calculations [13]. Graphene has six Dirac (K and K’) points and a linear dispersion relationship around them. (d) Angle-resolved photoemission spectroscopy (ARPES) data along symmetry directions in Brillouin zone for graphene [14]. (e) Phonon energy dispersion graphene determined theoretically (lines) from ab initio calculations and experimentally (solid circles) from high-resolution electron energy-loss spectroscopy (HREELS) [15]. Phonon dispersion for bulk graphite is also shown for comparison (open circles) [16].
lence and conduction bands meet. Also, the bands are symmetrical around the Dirac point with a linear dispersion relation described by $E = \hbar v_F k$, where $v_F \approx 10^8 \text{ cm/s}$ is the Fermi velocity, $\hbar = h/(2\pi)$ is the reduced Planck constant, and $k$ is the 2D momentum. The symmetry of the conduction and valence bands around the Dirac point indicates that electrons and holes should have equal mobilities, unlike in typical semiconductors like Si, Ge, or GaAs where mobilities are asymmetric, with hole mobility being particularly low. Despite the attention gained by graphene for future applications in integrated-circuit technology due to its excellent electrical [17, 18] and thermal properties [19], as well as its impressive mechanical strength [20] and relatively high optical phonon energies of ~180 meV (see Fig. 1.3e), the absence of a band gap makes it unsuitable for conventional digital transistors because of low on/off ratios.

### 1.3 Molybdenum Disulfide

The attractiveness of 2D materials for use in next-generation nanoelectronic devices has resulted in the study of other materials besides graphene. For example, there has been a growing interest in studying the electronic properties of 2D layered transition-metal dichalcogenides (TMDs) of the form MX$_2$ where M = metal and X = S, Se, or Te [21-23]. Like graphite [24], layered TMDs consist of stacked 2D atomic layers weakly bound by van der Waals forces, and thus, like graphene from graphite, atomically-thin TMD layers may be isolated from bulk TMD crystals. TMDs have been studied for decades but their behavior as single- and few-layer atomically thin materials is new. Among the family of TMDs, molybdenum disulfide (MoS$_2$) has received special emphasis. Monolayer MoS$_2$ with thickness $t \approx 6.5$ Å has a large direct band gap of ~1.8-1.9 eV [25, 26] (see Fig. 1.4), whereas bulk MoS$_2$ has an indirect band gap of 1.2 eV [27]. The presence of a band gap in MoS$_2$, unlike in graphene, has resulted in field-effect transistors (FETs) with high on/off ratios ($\sim 10^8$) and low sub-threshold swing ($SS \approx 70$ mV per decade) [21,
Room-temperature mobility is typically of the order of $10^2 \text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$, which makes it comparable to mobility in ultra-thin Si [28]. Typical transistors from exfoliated MoS$_2$ flakes only exhibit $n$-type conduction, and as a result, in Chapter 5 we focus on electron transport in MoS$_2$. Although beyond the scope of this study, we point out that $p$-type conduction has been observed in MoS$_2$ [29] under certain conditions and in other TMDs [30].

1.4 Device Fabrication of Graphene and MoS$_2$ Field-Effect Transistors

We fabricate graphene devices by two methods, one by mechanically exfoliating graphene from natural graphite, the other by chemical vapor deposition (CVD) growth on Cu substrates. With the standard “tape method,” graphene is mechanically exfoliated onto a substrate of $\sim300$ nm (or $\sim90$ nm in some cases) of SiO$_2$ with a highly doped Si substrate ($p$-type, $5\times10^3 \text{ } \Omega\text{-cm}$). The tape residue is then cleaned off by annealing at 400 °C for 120 min with a flow of Ar/H$_2$ (500/500 sccm) at atmospheric pressure. Monolayer graphene flakes are then identified with an optical microscope and confirmed via Raman spectroscopy, as shown in Fig. 1.5a [32]. The process is similar for exfoliating MoS$_2$ except that natural graphite is replaced with a molybdenite crystal. An example of the characteristic Raman spectrum for MoS$_2$ is shown in Fig. 1.5b. Also, for MoS$_2$ devices, unless stated otherwise, we use few-layer MoS$_2$ flakes where flake...
thickn ess is confirmed via atomic force microscopy (AFM) with $t \approx 4$ nm (i.e., ~6 layers) being typical.

Graphene growth by CVD is performed by flowing CH$_4$ and Ar gases at 1000 °C and 0.5 Torr chamber pressure, which results primarily in monolayer graphene growth on both sides of the Cu foil [34]. One graphene side is protected with a ~250 nm thick layer of polymethyl methacrylate (PMMA) while the other is removed with a 20 sccm O$_2$ plasma reactive ion etch (RIE) for 20 seconds. The Cu foil is then etched overnight in aqueous FeCl$_3$, leaving the graphene supported by the PMMA floating on the surface of the solution. The PMMA + graphene bilayer film is transferred via a glass slide to a HCl bath and then to two separate deionized water baths. Next, the film is transferred to the SiO$_2$/Si substrate and left for a few hours to dry. The PMMA is removed using a 1:1 mixture of methylene chloride and methanol, followed by a one hour Ar/H$_2$ anneal at 400 °C to remove PMMA and other organic residue.

After we have exfoliated, or transferred for the case of CVD graphene, onto the SiO$_2$/Si substrate, we pattern a rectangular graphene channel using e-beam lithography and an O$_2$ plasma etch. For MoS$_2$ devices, instead of an O$_2$ plasma etch we define rectangular channels using a

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**Figure 1.5:** (a) Raman spectrum showing the G and 2D bands of monolayer graphene. A single Lorentzian (red) is fitted to the 2D peak [32]. (b) Raman spectrum of MoS$_2$ device showing characteristic $E_{2g}^1$ and $A_{1g}$ peaks [33]. Scans here correspond to a 633 nm laser line.
XeF$_2$ etch consisting of 2 cycles at 60 s/cycle and XeF$_2$ pressure = 3 Torr [35]. Another e-beam lithography step is used to define the electrodes, which typically consist of ~0.5 nm of Cr and ~40 nm of Pd for supported graphene-based devices, ~1 nm of Cr and ~80 nm of Au for suspended devices, and ~35 nm of Au (i.e., no underlying “sticking” layer) for MoS$_2$-based devices.

For the suspended graphene study discussed in Chapter 4, the suspension process is as follows. First, we etch away ~200 nm of the underlying 300 nm SiO$_2$ [36]. The sample is then placed in 50:1 BOE for 18 min followed by a deionized (DI) water bath for 5 min. Isopropyl alcohol (IPA) is squirted into the water bath while the water is poured out so that the sample always remains in liquid. After all the water has been poured out and only IPA remains, the sample is put into a critical point dryer (CPD). Following the CPD process we confirm suspension using scanning electron microscopy (SEM) or AFM. All electrical measurements for all studies discussed here, unless specified otherwise, are performed in vacuum (~10$^{-5}$ Torr) at the stated background temperature ($T_0$).
CHAPTER 2: REVIEW OF HIGH-FIELD TRANSPORT IN GRAPHENE AND MOLYBDENUM DISULFIDE

2.1 Practical Device Operation and High-Field Transport

Understanding high-field transport is not only important from a scientific point of view, but it is essential for achieving practical applications. This can be further expounded upon by comparing the long-channel model versus the short-channel model for a typical FET. The basic long-channel MOSFET equation for calculating drain current \( I_D \) is given by [37]

\[
I_D = \mu C_{ox} \frac{W}{L} \left[ \left( V_G - V_T - \frac{1}{2} V_D \right) V_D \right]
\]

(2.1)

where \( \mu \) is the carrier mobility, \( L \) and \( W \) are the channel length and width, respectively, \( C_{ox} \) is the gate oxide capacitance, \( V_G \) is the gate voltage, \( V_T \) is the threshold voltage, and \( V_D \) is the drain voltage. Using the long-channel model, when \( V_D \geq V_G - V_T \) the inversion layer at the drain is effectively in “pinch-off” as shown in Fig. 2.1, and \( I_D \) no longer rises with an increase in \( V_D \). The saturation current \( I_{Dsat} \) is defined by the drain voltage at the pinch-off point (i.e., \( V_D = V_G - V_T \))

\[ \text{Figure 2.1: Schematic of a typical long-channel MOSFET, shown in this case at the onset of saturation such that the pinch-off point is at the drain side of the channel} \ [3]. \]
and given by

\[ I_{D\text{sat}} = \mu C_{ox} \frac{W}{2L} (V_G - V_T)^2 \]  

(2.2)

where we see that \( I_{D\text{sat}} \) increases quadratically with overdrive voltage \( (V_{GT} = V_G - V_T) \) and is inversely proportional to \( L \). For short-channel MOSFETs, the long-channel analysis, which assumes constant carrier mobility, is no longer applicable as much higher electric fields are present in short-channel transistors. These higher fields result in the drift velocity \( (v_d) \) of carriers in short-channel devices approaching a limiting value known as the saturation velocity \( (v_{sat}) \). This leads to current saturation occurring in a short-channel transistor at much lower voltages than one would predict if using the long-channel model \([3, 38]\). Consequently, for short-channel MOSFETs the saturation current is given by

\[ I_{D\text{sat}} = v_{sat} W C_{ox} (V_G - V_T - V_{D\text{sat}}) \]  

(2.3)

where \( V_{D\text{sat}} \) is the drain voltage at the onset of current saturation. For increasingly shorter gate lengths \( (L \rightarrow 0) \), we can estimate the maximum drain current as

\[ I_{D\text{max}} = v_{sat} W C_{ox} (V_G - V_T) \]  

(2.4)

where \( I_{D\text{max}} \) increases linearly, not quadratically, with overdrive voltage \( (V_{GT}) \) and the term \( C_{ox}(V_G - V_T) \) is an approximation of the 2D carrier density \( (n) \) in the channel. Figure 2.2 shows a comparison of the high-field behavior for long- and short-channel devices discussed here, and further emphasizes that with increased scaling and higher electric fields in modern transistors, improved understanding of high-field transport (i.e., the energy dissipation mechanisms that determine \( v_{sat} \) for a given material) is critical for enhancing practical device operation.

The 2D devices discussed in later chapters for the work presented here are in effect a hybrid of long-channel and short-channel transistors. Channel lengths are typically a few microns
(i.e., longer than the sub-100 nm lengths commonly associated with short-channel transistors), but by applying a sufficiently high gate bias to these devices, the channel does not approach pinch-off when operating under high drain-source voltages. Thus, current saturation behavior is due to velocity saturation effects as discussed above for short-channel devices. Additionally, we are careful to avoid the formation of significant non-uniform fields along the channel.

Detailed knowledge of the coupling of high-field transport with self-heating is also necessary when discussing practical device operation. As mentioned in Section 1.1, the ability to effectively remove heat from ICs is a limiting factor for future scaling. At high fields, the charge carriers (e.g., electrons in conduction band) accelerate and gain energy, or “heat up.” Mechanisms that may limit electron transport include electrons scattering with other electrons, phonons, interfaces, defects, and impurities. These scattering events not only determine $v_{\text{sat}}$, but when electrons scatter with phonons, electrons can lose energy to the lattice and effectively raise the temperature of the lattice (i.e., Joule heating or self-heating) [4, 39, 40]. Consequently, it is im-

**Figure 2.2:** (a) Current-voltage characteristics for a MOSFET with $L = 0.25 \, \mu m$ and $W = 9.5 \, \mu m$. The solid lines are experimental curves while the dashed line is the long-channel approximation with velocity saturation effects ignored [38]. (b) Model predictions for MOSFET saturation current versus channel length without velocity saturation (dashed) and with velocity saturation (solid) [37].
important to account for self-heating effects when investigating high-field transport, as the electronic properties of a material may vary drastically with temperature. For example, the saturation velocity in Si decreases with rising temperature due to an increase in phonon scattering [41]. Analysis of the temperature dependence of high-field transport in graphene and MoS$_2$ will be given in later chapters.

2.2 Review of High-Field Transport in Graphene

A review of previous studies of high-field transport in graphene is presented now, while in Chapters 3 and 4 we continue this discussion and present our original work and analysis of high-field behavior in graphene. Discussion is limited to monolayer graphene, ignoring bilayer and few-layer graphene as well as graphene nanoribbons (GNRs), which are beyond the scope of this study. We also only give attention to steady-state transport, ignoring high-frequency response. First, we focus on simulation results for ideal graphene and then include analysis of substrate effects and experimental data.

A detailed review of the current theoretical understanding of electron transport in graphene has recently been presented by Fischetti et al. [42]. We will summarize some of the key points from this study, as well as other theoretical works, as they pertain to our discussion of high-field transport. We initially give attention to phonon-limited transport in ideal graphene, as shown in Fig. 2.3. We point out that the electron drift velocity appears to peak at \( \sim 2 \times 10^7 \text{ cm/s} \) at 1 V/\( \mu \text{m} \) for \( n = 10^{13} \text{ cm}^{-2} \) at 300 K. The onset of negative differential velocity (NDV) at 0.3-0.5 V/\( \mu \text{m} \) for lower carrier densities is an intriguing observation, and in this case, is attributed to electrons gaining enough energy at high electric fields to populate the flatter regions of the Brillouin zone, causing a degradation of the drift velocity. The appearance of NDV has been presented in previous simulations as well.
Akturk and Goldsman [43], using a Monte Carlo simulator, show peak drift velocities for intrinsic graphene as high as $4.6 \times 10^7$ cm/s and slight NDV for fields above ~10 V/µm. Shishir and Ferry [44] show similar peak velocities and NDV for $n \leq 2 \times 10^{12}$ cm$^{-2}$ at fields above ~0.5 V/µm. Chauhan and Guo [45] show carrier velocity as a function of electric field up to 1 V/µm with $v_{\text{sat}}$ near $4 \times 10^7$ cm/s, but no NDV is observed. However, the carrier density is fixed at $5.29 \times 10^{12}$ cm$^{-2}$ in their simulations so it is uncertain if NDV would have been observed at lower densities. The calculated drift velocity vs. electric field for these works is shown in Fig. 2.4. The variation among different theoretical works for transport in ideal graphene may, at least in part, be associated with the different choices made for deformation potentials, band structures, and phonon dispersions. Therefore, drawing qualitative, rather than quantitative, conclusions may be more appropriate from these simulation studies. For example, a clear observation in [42] and [44] is the decrease in high-field drift velocity with increasing carrier density, which is an interesting
phenomenon considering typical non-degenerate semiconductors like Si have a constant $v_{\text{sat}}$ (e.g., $\sim 10^7$ cm/s for Si at 300 K) [41]. Graphene has no band gap, and thus is a degenerate semiconductor where the dependence of saturation velocity on carrier density is due to the degeneracy of carriers and the Pauli exclusion principle [46].

Continuing the discussion of the carrier-density dependent electron transport in graphene, we note that Ferry in his simulations [47] used an impurity density that increased with carrier density, indicating that this increasing impurity density was the only way to match the experimental data in [32] and [48]. It is plausible that a change in impurity density may occur during measurements due to the application of a high gate field and subsequent motion of impurities within the oxide. Another explanation is that a more dynamic form of screening, as proposed in [49], is necessary to properly understand the dependence of transport on carrier density. For future analysis of experimental work, we note that a constant impurity density (independent of gate voltage) is assumed.

**Figure 2.4:** Calculated drift velocity vs. electric field from Monte Carlo simulations from (blue solid) Akturk and Goldsman [43], (red dashed) Shishir and Ferry [44], and (green dotted) Chauhan and Guo [45]. The blue line corresponds to intrinsic graphene. The red dashed lines vary in carrier density from $5 \times 10^{11}$ to $10^{13}$ cm$^2$ from top to bottom. The multiple green dotted lines have impurity densities of $n_{\text{imp}} = 0$, $10^{11}$ cm$^2$, and $10^{12}$ cm$^2$ from top to bottom.
Returning to the previously mentioned high-field NDV in graphene shown in several theoretical studies [42-44, 50], Fang et al. suggest that the inclusion of electron-electrons (e-e) scattering actually removes the NDV effect [46]. Because high-energy electrons exchange their momentum and energy with low-energy electrons, e-e scattering weakens the backscattering effect that would lead to NDV [46]. Another effect not yet discussed is carrier multiplication due to interband tunneling and e-e scattering [51, 52]. If the Fermi level is near the Dirac point we could expect Zener tunneling and/or impact ionization to generate electrons and holes, especially at high fields, and increase the carrier concentration. Experimental works have shown that it is very difficult to obtain saturation of high-field current in graphene transistors [32, 53-56], a characteristic credited to the lack of a band gap in graphene that facilitates ambipolar transport and the easy transition from electron-dominated to hole-dominate transport (or vice-versa) during high-field operation. Transport models have been developed that use a phenomenological term to account for the current up-kick associated with ambipolar transport [57, 58], but we emphasize that if the Fermi level is near the Dirac point then tunneling and impact ionization effects may also play a role in the observed current up-kick [51, 52]. For the original experimental work discussed in later chapters, we typically operate at high electron densities in a unipolar regime, thus simplifying our transport analysis.

We now turn to substrate effects, a necessary discussion in light of the fact that a majority of the experimental work on graphene (including Chapter 3 here) has been performed with graphene on SiO₂/Si substrates. Although it is beyond our focus here, we also note that graphene on hexagonal boron nitride (h-BN) is gaining increasing attention due to the observation of improved device performance [59]. An additional scattering process that limits electrical transport in supported graphene is scattering with charged impurities [60]. Substrate impurities that remain
after the fabrication of graphene transistors [61-63] play a significant role in limiting the low-field mobility of graphene transistors [64], but do not significantly affect high-field transport [55, 65]. Additionally, we expect that if a graphene transistor is used in the future for nanoscale electronics, then it will most likely be a top-gated transistor with a high-κ insulator as the top-gate dielectric [66, 67]. Detailed models have been provided for analyzing the effect of charged impurity scattering and its dependence on the surrounding dielectric environment [68-71], but as we are primarily concerned with high-field transport here, we will move on to a more relevant scattering process.

For insulators like SiO$_2$ and HfO$_2$ there are bulk dipoles associated with the ionicity of the metal-oxide bonds. These dipoles generate fringing fields on the substrate surface such that the frequencies of these dipoles are typically determined by the bulk longitudinal optical phonons of the insulator. Electrons in close proximity to the substrate surface may interact with these surface optical (SO) phonons via a process commonly referred to as remote-phonon scattering. For Si inversion layers, remote-phonon scattering has been investigated [72, 73], where it was found to have a small effect on the drift velocity in the regime just beyond Ohmic transport, but it was not strong enough to affect the saturation velocity [74], which is determined by the bulk Si optical phonons. In supported graphene, it is reasonable to consider electrons interacting strongly with SO phonons considering electrons are essentially confined to the graphene sheet, and the gap between the graphene and substrate is small, ~0.3-0.4 nm [75]. Furthermore, recent work shows that graphene may even emit longitudinal out-of-plane acoustic phonons into the substrate, representing an energy dissipation mechanism in the vertical direction [76].
When discussing remote-phonon scattering in graphene, Ong and Fischetti [49, 77, 78] indicate the importance of considering dynamic screening and the charge density response of graphene due to the electric field created by SO phonons. Figure 2.5 shows the remote-phonon-limited mobility ($\mu_{\text{RP}}$) in graphene as a function of carrier density for various supporting substrates. The mobility is calculated by accounting for the hybrid interface phonon-plasmon (IPP) modes formed from the hybridization of the SO phonons with graphene plasmons [49]. We see from the plot that $\mu_{\text{RP}}$ is saturating and weakly dependent on $n$ at high carrier densities since most of the remote phonons are dynamically screened. The observed behavior agrees with the findings of Zou et al. [67], who extract $\mu_{\text{RP}}$ showing a slight increase with carrier density for a graphene transistor with HfO$_2$ as the top-gate dielectric. More importantly for our discussion here, we are interested in the effect of remote-phonon scattering on high-field transport.

The experimental works of Meric et al. [54, 55] suggest that current saturation in a gra-
phene transistor may be observed due to remote-phonon scattering, or more specifically, scattering with the low-energy SO phonon of SiO$_2$ ($\hbar\omega_{\text{OP}} = 55$ meV) [79]. We use the term “low-energy” here for comparison to the graphene (zone-edge) optical phonon with energy $\hbar\omega_{\text{OP}} = 160$ meV [80]. Furthermore, Barreiro et al. [53] also suggest that the calculated current (from the analytic model described below) using a phonon energy of 149 meV overestimates the experimentally observed current in the high-field limit. Unfortunately, these works do not account for self-heating effects in their analysis, which we know is evident in graphene transistors at high currents and high fields [81-85] and may be necessary to explain high-field transport in graphene [56, 65, 86, 87]. Our original work in Chapter 3 will discuss this topic in more detail and help elucidate the behavior of high-field transport in supported graphene.

Figure 2.6 shows the extracted drift velocity from experimental $I$-$V$ data [32, 53, 55, 56] as a function of electric field. Comparison of these curves is difficult as they correspond to different values of carrier density and temperature as well as different device structures. Nevertheless, we are able to highlight some key features of high-field transport in graphene. Saturation velocity in graphene, even at high carrier densities $>10^{13}$ cm$^{-2}$, appears to be larger than $10^7$ cm/s, (i.e., larger than $v_{\text{sat}}$ in Si at room temperature). Figure 2.6 also shows the decrease in high-field drift velocity with increasing carrier density, as mentioned above and shown in previous theoretical works. Similarly, the high-field drift velocity decreases with increasing temperature, which is an expected trend if we assume high-field transport is limited by emission of optical phonons. Further discussion concerning the behavior of high-field drift velocity in graphene is provided in Section 3.5.
Lastly, in the interest of providing a thorough review, we quickly introduce the analytic models from Barreiro et al. [53], Freitag et al. [83], and Fang et al. [46]. These models assume that current saturation, or rather velocity saturation, in graphene is caused by a single optical phonon of energy $\hbar \omega_{\text{OP}}$. The first model [53], as shown in Fig. 2.7a, approximates the high-field electron distribution with two half-disks such that positive-$k_x$ electrons are populated to an energy $\hbar \omega_{\text{OP}}$ higher than negative-$k_x$ moving electrons. The assumption here is that the inelastic process of emitting an OP causes the electron to instantly backscatter. The second model [83] shown in Fig. 2.7b assumes that for a given electron density defined by $n = k_F^2 / \pi$, the high-field
transport regime simply consists of electrons within a $\pm \hbar \omega_{OP}/(2v_F)$ window around the Fermi energy $E_F$, such that $E_F = \hbar v_F k_F = \hbar v_F (\pi n)^{1/2}$. The last model (Fig. 2.7c) considers a low-energy disk ($k_l$) and a high-energy disk ($k_h$) defined by $\omega_{OP}/v_F = k_h - k_l$, such that if an electron travelling along the $k_x$-direction reaches the high-energy circle, then it instantly emits an OP and backscatters.

The “streaming” model accounts for carrier degeneracy in graphene by assuming that the occupation of the low-energy circle is so full that the Pauli exclusion principle prohibits an electron with energy less than $E_h = \hbar v_F k_h$ to emit an OP, which forces the distribution function to be squeezed and elongated along the direction of the electric field.

We emphasize that these models are more suited for empirical fitting than for providing physical insight into high-field transport in graphene. It is known that even small changes in the
electron distribution can significantly affect charge transport, and thus, these models most likely oversimplify the distribution of carriers during high-field operation. Therefore, the apparent agreement between these simple models and reported trends for high-field drift velocity in graphene is fortuitous (accidental). The “streaming” model from Fang et al. [46] most closely resembles the electron distribution in $k$-space from Monte Carlo simulations [45] so we choose to use it in Section 3.5 to empirically fit our graphene high-field transport measurements.

2.3 Review of High-Field Transport in MoS$_2$

High-field transport in MoS$_2$ has received little attention from the community studying electrical transport in 2D materials. While physical breakdown of monolayer MoS$_2$ at high field has been reported [88], a solid understanding of high-field transport in mono- and few-layer MoS$_2$ is presently unavailable. Fiori et al. provide a simple model for high-field transport in few-layer MoS$_2$ [89], but in this study contact resistance and self-heating effects are ignored. Additionally, they do not conduct measurements at high enough electric fields and carrier densities or across a wide enough range of temperatures to provide insight into the high-energy band structure of MoS$_2$. This insight may prove useful considering the few-layer MoS$_2$ band structure is not well known as evidenced by some disagreement among existing band structure calculations [26, 31, 90-95]. A thermal analysis of MoS$_2$ field-effect transistors (FETs) would also be important, particularly the effect of self-heating on high-field operation which is expected to play a significant role in applications intended on flexible substrates [96, 97]. Our work in Chapter 5 will provide a detailed analysis of high-field transport in few-layer MoS$_2$ transistors on SiO$_2$.

2.4 Ultimate Device Scaling and High-Field Transport

Before concluding this review section, we comment on the future direction of nanoscale electronics and the usefulness of high-field measurements. The continuation of scaling and de-
Development of short-channel transistors with gate lengths below 10 nm means that charge transport in devices will approach a quasi-ballistic regime [98, 99]. Understanding of more conventional diffusive transport physics may remain important [100, 101], but in terms of ballistic transport, accurate knowledge of the band structure and effective mass(es) as well as which valleys are populated during device operation will be essential in determining the number of modes of transport, and ultimately, the current carrying ability of these transistors [102]. Analysis of high-field transport in 2D materials provides practical and essential insight into the high-energy band structure of these materials, as exemplified in Chapter 5 for few-layer MoS$_2$.

Additionally, the introduction of FinFETs into state-of-the-art integrated-circuit technology has emphasized the need to improve electrostatics for highly-scaled devices. Electrons in intrinsic 2D materials (e.g., graphene and MoS$_2$) are confined by ionic potentials rather than band discontinuities so they may offer the only solution to scaling the thickness of semiconducting bodies. We consider the scaling of double-gate (DG) MOSFETs and point out that in order to avoid short-channel effects, the scale length ($\lambda$) cannot be smaller than the thickness of the channel ($t_{ch}$) or two times the thickness of the insulator ($2t_i$) [3]. High-$\kappa$ gate insulators are limited by tunneling to $\sim$2.5 nm, while monolayer graphene and monolayer MoS$_2$ are only 0.34 nm and 0.65 nm thick, respectively. Consequently, the insulator thickness would be the limiting factor in terms of ultimate scaling of a DG MOSFET when using an intrinsically 2D channel material. The minimum $\lambda$ is $\sim$5 nm resulting in a minimum channel length of $\sim$5-10 nm ($L_{\text{min}} \approx 1.5\lambda$), representing the possibility of a sub-10 nm transistor with a 2D body.
CHAPTER 3: MOBILITY AND HIGH-FIELD DRIFT VELOCITY IN GRAPHENE ON SILICON DIOXIDE

3.1 Introduction

In this study, we measure mobility in the $T = 80$-$500$ K range and high-field drift velocity at fields $F \approx 1$ V/μm in monolayer graphene on SiO$_2$, both as a function of carrier density. We also introduce simple models including the proper electrostatics, and self-heating at high fields [81]. As mentioned previously in Chapter 2, the inclusion of self-heating effects is necessary for proper analysis of high-field transport in graphene transistors. We find that mobility and high-field drift velocity decrease with rising temperature, and also show a slight decrease with rising carrier density above $2 \times 10^{12}$ cm$^{-2}$. The relatively straightforward approach presented can be used for device simulations or extended to graphene on other substrates.

We fabricated four-probe back-gated graphene structures on SiO$_2$ as described in Section 1.4. We focus on data from two devices with oxide thicknesses $t_{ox} = 300$ nm ($L = 4$ μm and $W = 7$ μm) and $t_{ox} = 90$ nm ($L = 4$ μm and $W = 2.2$ μm), where the thinner 90 nm oxide results in a higher gate capacitance, allowing us to obtain a wider range of carrier densities experimentally, and also resulting in improved heat dissipation that helps mitigate instability at high-fields. We note that the fabrication of the second device with $t_{ox} = 90$ nm did not require the additional e-beam lithography step of patterning the graphene channel with an O$_2$ plasma since the original graphene flake was already rectangular. Also, after numerous high-field measurements on this device, an outside electrode was damaged, requiring the subsequent use of two-probe measurements using the inner electrodes. We extract contact resistance $R_C$ by comparing the four-probe measured resistance ($R_{4pp}$) with the two-probe measured resistance ($R_{2pp}$), i.e., $R_C = (R_{2pp} - R_{4pp})/2$. We then determine a temperature-dependent contact resistance $R_C = 0.3T_0 + 48$ Ω, where $T_0$ is the background temperature and the linear dependence of $R_C$ on $T_0$ agrees with a previous
For analysis of two-terminal measurements we simply redefine the bias across the inner channel region as \( V_{23} = V_D - 2I_D R_C \) (similarly \( V_G \) relative to the ground electrode is reduced by \( I_D R_C \)). Extracted transport properties from four-probe measurements and two-probe measurements (accounting for contact resistance) are identical. A schematic and optical image of the device structures used here are shown in Figs. 3.1a,b.

3.2 Charge Density Model

To obtain mobility and drift velocity from conductivity measurements, we model the carrier density including gate-induced \( (n_{cv}) \), thermally generated \( (n_{th}) \) carriers, electrostatic spatial inhomogeneity \( (n^*) \) and self-heating at high fields. Previous mobility estimates using only \( n_{cv} \) could lead to unphysically high mobility \( (\mu \rightarrow \infty) \) near the Dirac voltage \( (V_G = V_0) \) at the minimum conductivity point.

First, we note the gate voltage imposes a charge balance relationship as

\[
 n_{cv} = p - n = -C_{ox} V_{G0} / q 
\]  

(3.1)

where \( C_{ox} = \varepsilon_{ox}/t_{ox} \) is the capacitance per unit area (quantum capacitance may be neglected here \([104, 105]\)), \( \varepsilon_{ox} \) is the dielectric constant of SiO\(_2\), \( q \) is the elementary charge, and \( V_{G0} = V_G - V_0 \) is
the gate voltage referenced to the minimum conductivity point. Next, we define an average Fermi level $E_F$ such that $\eta = E_F/k_B T$, leading to the mass-action law [104]

$$p_n = n_{th}^2 \frac{\mathcal{Z}_i(\eta) \mathcal{Z}_i(-\eta)}{\mathcal{Z}_i^2(0)}$$

(3.2)

where $n_{th} = (\pi/6)(k_B T/\hbar v_F)^2$ is the thermal carrier density, $v_F \approx 10^8 \text{ cm/s}$ is the Fermi velocity, and $\mathcal{Z}_i(\eta)$ is the Fermi-Dirac integral with $\mathcal{Z}_i(0) = \pi^2/12$. We also point out that in the $T \to 0 \text{ K}$ limit, the Fermi level may be approximated as $E_F = \pm \hbar v_F (\pi C_{ox} |V_{G0}|/q)^{1/2}$ where the upper (lower) sign corresponds to the electron-doped, $V_{G0} > 0$, (hole-doped, $V_{G0} < 0$) regime.

Next, we account for the spatial charge (“puddle”) inhomogeneity of graphene due to substrate impurities [61-63]. The surface potential can be approximated [105] as a periodic step function whose amplitude $\pm \Delta$ is related to the width of the minimum conductivity plateau [64] as given by the residual carrier puddle density ($n^*$) due to charged impurities in the SiO$_2$ ($n_{\text{imp}}$). The charged impurity density at the SiO$_2$ surface is determined based on the approach discussed in Adam et al. [64] and given by $n_{\text{imp}} = B C_{ox} |d\sigma/dV_{G0}|^{-1}$ where $B = 5 \times 10^{15} \text{ cm}^{-2}$ is a constant determined by the screened Coulomb potential in the random phase approximation (RPA) [106] and $d\sigma/dV_{G0}$ is the slope of the low-field conductivity $\sigma = (L/W)(I_{14}/V_{23})$. The slope is determined by a linear fit to $\sigma$ around the maximum of $|d\sigma/dV_{G0}|$ as shown in Fig. 3.2. The value of $n_{\text{imp}}$ used here for each sample is based on conductivity measurements at 80 K, where low-field mobility is limited by Coulomb scattering [60]. From Eq. (10) of [64], we determine $n^* \approx 0.297 n_{\text{imp}} \approx 2.63 \times 10^{11} \text{ cm}^{-2}$ and $n^* \approx 0.287 n_{\text{imp}} \approx 2.89 \times 10^{11} \text{ cm}^{-2}$ in the samples with $t_{ox} = 300 \text{ nm}$ and 90 nm, respectively, (averaged over the electron- and hole-doped regimes), where $n^*$ is the residual carrier puddle density representing the width of the minimum conductivity plateau. From $n^*$, we obtain a surface potential variation $\Delta \approx \hbar v_F (\pi n^*)^{1/2}$ of 59 and 63 meV and $\Delta V_0 \approx q n^*/C_{ox}$ of 3.66 and 1.21 V for our two samples, respectively. The extracted values for the sur-
face potential variation are similar to a previous study (~54 meV) [105] and to scanning tunneling microscopy results (~77 meV) [63].

The total carrier density can be determined numerically by averaging Eqs. (3.1) and (3.2) for the regions of ±Δ, but this does not yet yield an analytic expression. In order to simplify this, we note that at low charge density (η → 0) the factor Ξ_1(η) Ξ_1(-η)/Ξ_1^2(0) in Eq. (3.2) approaches unity. Meanwhile, at large |V_{G0}| and high carrier densities the gate-induced charge dominates, i.e. \( n_{cv} \gg n_{th} \) when \( η \gg 1 \). Finally, we add a correction for the spatial charge inhomogeneity discussed above, resulting in a minimum carrier density of \( n_0 = [(n* / 2)^2 + n_{th}^2]^{1/2} \). Consequently, solving Eqs. (3.1) and (3.2) with the approximations given here results in an explicit expression for the concentration of electrons and holes

\[
n, p \approx \frac{1}{2} \left[ \pm n_{cv} \pm \sqrt{n_{cv}^2 + 4n_0^2} \right] \quad (3.3)
\]

where the lower (upper) sign corresponds to electrons (holes). Equation (3.3) can be readily used

\[\text{Figure 3.2: Conductivity vs. back-gate voltage at 80 K for devices of interest with (a) } L = 4 \, \mu m, \ W = 7 \, \mu m, \ \text{and } t_{ox} = 300 \, nm \text{ and (b) } L = 4 \, \mu m, \ W = 2.2 \, \mu m, \ \text{and } t_{ox} = 90 \, nm. \ The \ red \ dashed \ lines \ correspond \ to \ linear \ fits \ to \ the \ interval \ around \ the \ maximums \ in } \left| \frac{d\sigma}{dV_{G0}} \right|. \ The \ slopes \ of \ these \ lines \ are \ used \ to \ calculate \ n_{imp} \ in \ accordance \ with \ [64].\]

\[\text{Figure 3.2: Conductivity vs. back-gate voltage at 80 K for devices of interest with (a) } L = 4 \, \mu m, \ W = 7 \, \mu m, \ \text{and } t_{ox} = 300 \, nm \text{ and (b) } L = 4 \, \mu m, \ W = 2.2 \, \mu m, \ \text{and } t_{ox} = 90 \, nm. \ The \ red \ dashed \ lines \ correspond \ to \ linear \ fits \ to \ the \ interval \ around \ the \ maximums \ in } \left| \frac{d\sigma}{dV_{G0}} \right|. \ The \ slopes \ of \ these \ lines \ are \ used \ to \ calculate \ n_{imp} \ in \ accordance \ with \ [64].\]
in device simulations and is similar to a previous empirical formula [54], but derived here on more rigorous grounds. We note Eq. (3.3) reduces to the familiar \( n = C_{ox}V_{G0}/q \) at high gate voltage, and to \( n = n_0 \) (puddle regime) at \( V_G \approx V_0 \). Figure 3.3 displays the role of thermal and “puddle” corrections to the carrier density at 300 K and 500 K. These are particularly important near \( V_{G0} = 0 \) V, when the total charge density relevant to transport \((n + p)\) approaches a constant despite the charge neutrality condition imposed by the gate \((n - p = 0)\). At higher temperatures \((k_B T \gg \Delta)\) the spatial potential variation becomes less important due to thermal smearing and larger \( n_{th} \).

### 3.3 Low-Field Mobility

Using the aforementioned model for calculating the carrier density in a graphene device, low-field (~2 mV/µm) mobility is obtained as \( \mu = \sigma/q(p + n) \), where the conductivity is given by \( \sigma = (L/W)I_{14}/V_{23} \). Figure 3.4 shows measurements of conductivity vs. \( V_{G0} \) for temperatures rang-
ing from 80 to 450 K. Mobility is shown as a function of carrier density in Fig. 3.5 for both devices of interest at various temperatures and for both the electron-doped and hole-doped regimes. Mobility values shown here are similar to previously reported Hall mobility values for graphene [71]. Although not universal, the mobility at 300 K and above appears to peak at $\sim2\times10^{12}$ cm$^{-2}$ and then decrease at higher carrier densities. A universally observed effect is the decrease in mobility with increasing temperature at high carrier densities [105], as shown in Fig. 3.6. The dependence of mobility on carrier density and temperature suggests the dominant scattering mechanism changes from Coulomb to phonon scattering at higher densities and temperatures [105].

 Inspired by empirical approximations for Si device mobility [107], the electron mobility can be fit as (dashed line in Figs. 3.5a and 3.6a)

$$
\mu(n,T) = \frac{\mu_0}{1 + \left(\frac{n}{n_{\text{ref}}}\right)^{\alpha}} \times \frac{1}{1 + \left(\frac{T}{T_{\text{ref}}} - 1\right)^{\beta}}
$$

(3.4)

where $\mu_0 = 4650$ cm$^2$V$^{-1}$s$^{-1}$, $n_{\text{ref}} = 1.1\times10^{13}$ cm$^{-2}$, $T_{\text{ref}} = 300$ K, $\alpha = 2.2$ and $\beta = 3$ for the $t_{\text{ox}} = 300$
Not all samples measured displayed the dip in mobility at low charge density, so we did not force a mobility fit below $2 \times 10^{12}$ cm$^{-2}$. We also point out that the empirical Eq. (3.4)
only applies to mobility at or above room temperature. Before concluding our analysis of low-field mobility, we comment on sample-to-sample variation and uncertainty in the extracted mobility, especially at low charge densities. A possible cause of sample-to-sample variation is the spatial inhomogeneity of the “puddle” regime that is not accurately predicted by the simple ±Δ potential model. With respect to uncertainty in our method for mobility extraction, Adam et al. [64] noted that for the extracted $n_{\text{imp}}$ the predicted plateau width is approximate within a factor of two. This leads to uncertainty in determining $\Delta V_0$, and thus uncertainty in the charge density and extracted mobility values. However, this uncertainty is only notable around the Dirac point, where the potential ripple contributes to the total carrier density. This limits the “confidence region” in Figs. 3.5, where we only show carrier densities greater than $0.85 \times 10^{12}$ cm$^{-2}$. In Fig. 3.7 we estimate the mobility uncertainty at lower charge densities around the Dirac point, such that the upper and lower bounds result from a potential ripple of $\Delta V_0/2$ and $2\Delta V_0$, respectively.

An additional source of uncertainty arises from our use of inner voltage probes that span the width of the graphene sheet. The advantage of such probes is that they sample the potential...
uniformly across the entire graphene width, unlike non-invasive edge-probes which may lead to potential non-uniformity particularly at high fields. However, full-width probes themselves introduce a few uncertainties in our measurements, which are minimized through careful design as described here. One challenge may be that, even under four-probe measurements, the current flowing in the graphene sheet could enter the edge of a voltage probe and partially travel in the metal. To minimize this effect, we used very narrow inner probes of 300 nm, which is narrower than the typical charge transfer length between graphene and metal contacts (~1 μm) [109]. In addition, we employed very “long” devices, with $L = 4 \mu m$ between the inner probes. Thus, the resistance of the graphene between the inner electrodes is much greater than both the resistance of the graphene under the metal contact and that across the narrow metal contact itself.

Another challenge stems from the work function mismatch between the Cr/Pd electrodes and that of the nearby graphene. This leads to potential and charge non-uniformity in the graphene near the contacts. Previous theoretical work has calculated a potential decay length of ~20 nm induced by Pd contacts on graphene [110]. Experimental photocurrent studies have estimated that doping from Ti/Pd/Au contacts can extend up to 0.2-0.3 μm into the graphene channel [111].
although the study had a spatial resolution of only 0.15 μm. Regardless, the potential and charge disturbance is much shorter than the total channel length of our devices ($L = 4 \mu m$). We estimate at most a ~10% contribution to the resistance from charge transfer at our metal contacts. The error is likely to become smaller at higher charge densities ($>2 \times 10^{12} \text{ cm}^{-2}$) where the graphene charge more strongly screens the contact potential, and at high fields where the graphene channel becomes more resistive itself.

3.4 Thermal Analysis

Before turning our attention to high-field drift velocity measurements, we must present a thermal analysis of the supported-graphene device structure. As discussed in Section 2.2, analysis of high-field measurements in graphene poses challenges due to Joule heating effects that must be taken into account. We estimate the average device temperature due to self-heating via the thermal resistance network, as shown in Fig. 3.1a [5],

$$\Delta T = T - T_0 \approx P\left( R_B + R_{ox} + R_{Si} \right)$$

(3.5)

where $P = I_{14}V_{23}$, $R_B = 1/(hA)$, $R_{ox} = t_{ox}/(\kappa_{ox}A)$, and $R_{Si} \approx 1/(2\kappa_{Si}A^{1/2})$ with $A = LW$ the area of the channel, $h \approx 10^8 \text{ Wm}^{-2}\text{K}^{-1}$ the thermal conductance of the graphene-SiO$_2$ boundary [112], $\kappa_{ox}$ and $\kappa_{Si}$ the thermal conductivities of SiO$_2$ and the doped Si wafer, respectively. At 300 K for our geometry $R_B \approx 10^4 \text{ K/W}$, or $\approx 2.8 \times 10^{-7} \text{ m}^2\text{K/W}$ per unit of device area, where $R_B$ is simply the total thermal resistance calculated by summing the individual thermal resistance components in series. The thermal resistance value of $10^4 \text{ K/W}$ actually applies to both devices of interest here, since although the device with $t_{ox} = 90 \text{ nm}$ benefits from improved heat dissipation through the thinner oxide to the substrate, it has a smaller channel area that balances out this effect. The thermal resistance of the 300 (90) nm SiO$_2$ ($R_{ox}$) accounts for ~84 (71)% of the total thermal resistance,
while the spreading thermal resistance into the Si wafer ($R_{Si}$) and the thermal resistance of the graphene-SiO$_2$ boundary ($R_{B}$) account for only ~12 (19)% and ~4 (10)%, respectively. We note that the roles of $R_{Si}$ and $R_{B}$ are more pronounced for the smaller device on a thinner oxide. The thermal model in Eq. (3.5) can be used when the sample dimensions are much greater than the SiO$_2$ thickness ($W, L \gg t_{ox}$) but much less than the Si wafer thickness [5].

The average graphene temperature during high-field measurement will be estimated by Eq. (3.5). We note that the thermal resistance $R_{th}$ depends on temperature through $\kappa_{ox}$ and $\kappa_{Si}$, where we obtain $\kappa_{ox} = \ln(T_{ox}^{0.52}) - 1.687$ and $\kappa_{Si} = 2.4 \times 10^4/T_0$ by simple fitting to the experimental data in [113] and [114], respectively. Based on the thermal resistance model, we estimate the average oxide temperature as $T_{ox} = (T_0 + T)/2$, and the temperature of the silicon substrate as the background temperature $T_0$. This allows for a simple iterative approach to calculating the graphene temperature rise ($\Delta T$) during a measurement.

Lastly, we discuss the temperature non-uniformity around the inner voltage probes, which may act as local heat sinks. Analysis here focuses on the device with $t_{ox} = 300$ nm but can be applied to the thinner oxide device as well. The thermal resistance “looking into” the metal voltage probes can be estimated as $R_{C,th} = L_T/\kappa_mA$, where the thermal healing length $L_T = (t_m t_{ox} \kappa_m/\kappa_{ox})^{1/2} = 685$ nm, $t_m = 40$ nm is the metal thickness, $t_{ox} = 300$ nm is the SiO$_2$ thickness, $\kappa_m \approx 50$ Wm$^{-1}$K$^{-1}$ is the Pd metal thermal conductivity, $\kappa_{ox} \approx 1.3$ Wm$^{-1}$K$^{-1}$ is the oxide thermal conductivity (at 300 K), and $A = t_m W_c$ is the cross-sectional area of the contact with $W_C = 300$ nm. We obtain $R_{C,th} \approx 10^6$ K/W based on the device geometry here (primarily due to the narrow inner contacts being only ~300 nm wide), which is about two orders of magnitude greater than the thermal resistance for heat sinking from the large graphene sheet through the oxide, i.e., $R_{th} \approx$
10^4 \text{K/W at 300 K. Thus, heat flow from the inner metal contacts is negligible.}

3.5 High-Field Transport and Velocity Saturation

We now focus on high-field electrical measurements and analysis of high-field transport in our graphene transistors. To minimize charge non-uniformity and temperature gradients along the channel at high field [81], we bias the device at high |V_G| and avoid ambipolar transport, i.e., \(V_{GS} - V_0\) and \(V_{GD} - V_0\) have the same sign [54]. For example, in the electron-doped regime we apply a negative bias across the outer electrodes \((V_{14} < 0)\) such that the effective gate voltage increases during the measurement, thus causing the electron density to increase. This bias setup, which is opposite of a typical bias one would use for a practical n-type transistor when trying to achieve pinch-off and current saturation, is appropriate here since we are investigating the unipolar high-field transport physics of graphene. Figure 3.8 shows a comparison of \(|I_{14}|\) vs. \(|V_{23}|\) for cases where the applied drain bias across the outer electrodes \((V_{14})\) is negative (lines) and positive (crosses). As expected, we see relatively higher currents when \(V_{14} < 0\) due to the increase in carrier density during high-field operation. The analysis below pertains to data obtained with \(V_{14} < 0\). We also indicate that to ensure no sample degradation due to high field stress and strong self-heating, we checked that low-field \(\sigma-V_G\) characteristics were reproducible after each high bias measurement.

The drift velocity extracted from our measurements is \(v_d = I_{14}/(Wqn_{23})\) where \(n_{23}\) is the average carrier density between terminals 2 and 3, the background temperature is held at \(T_0 = 80\) K or \(T_0 = 300\) K, and temperature in the channel is \(T = T_0 + \Delta T\) due to self-heating. Figure 3.9a shows the high-field electrical measurements at 80 K for the device with dimensions \(L = 4\ \mu\text{m}, W = 2.2\ \mu\text{m},\) and \(t_{ox} = 90\) nm. We estimate the temperature rise \(\Delta T\) in Fig. 3.9b during high-field operation based on the thermal model discussed above. Figure 3.9c shows the extracted drift velocity
versus electric field \((F)\), whereas Fig. 3.9d shows \(v_d\) versus both \(F\) and carrier density \((n, \text{where } n \gg p \text{ here})\). At high-fields \((F > 0.5 \text{ V}/\mu\text{m})\) transport is no longer in the Ohmic regime since \(v_d\) does not linearly increase with \(F\), representative of the carrier drift velocity beginning to exhibit a tendency towards saturation. In Fig. 3.10 we further analyze the velocity-field relationship and fit the drift velocity by

\[
v_d(F) = \frac{\mu F}{\left[1 + \left(\frac{\mu F}{v_{\text{sat}}}\right)^\gamma\right]^\frac{1}{\gamma}}
\]  

(3.6)

where \(\mu\) is the low-field mobility and \(\gamma \approx 1.5\) provides a good fit (dashed lines in Fig 3.10) for the carrier densities and temperatures in this work. The bounded shaded regions in Fig. 3.10 correspond to upper and lower estimates for the drift velocity at high fields when using \(\gamma \approx 1\) and \(\gamma \approx 2\), respectively, which have been used previously when fitting Eq. 3.6 to high-field transport data in graphene [32, 54]. More specifically, we use \(\gamma \approx 2\) for fitting to our device with \(t_{\text{ox}} = 300 \text{ nm}\).
The larger value of $\gamma = 2$ that produces a good fit for the data corresponding to the sample with $t_{\text{ox}} = 300 \text{ nm}$ could be representative of the device having a relatively stronger temperature dependence for low-field mobility. Another possibility is the device undergoing relatively more significant self-heating during high-field operation, which makes sense since we reached slightly higher input powers for the larger device. For simplicity we let $\mu$ in Eq. (3.6) be constant for an individual bias sweep, but we know from Fig. 3.6 that mobility varies with temperature and that

**Figure 3.9:** (a) High-field electrical measurement showing current vs. voltage at $T_0 = 80$ K for $V_{G0} = 10–50$ V for device with dimensions $L = 4 \mu$m, $W = 2.2 \mu$m, and $t_{\text{ox}} = 90$ nm. (b) Estimated temperature rise ($\Delta T$) during high-field operation for the measurements in (a). (c) Corresponding velocity-field curves showing the transition from Ohmic behavior (i.e., linear $v_d$-$F$ relationship) to the high-field regime where $v_d$ trends towards saturation. (d) Drift velocity plotted vs. electron density and electric field, where we observe a slight decrease in the high-field drift velocity (for equivalent lateral field values) as the density increases.

The larger value of $\gamma = 2$ that produces a good fit for the data corresponding to the sample with $t_{\text{ox}} = 300 \text{ nm}$ could be representative of the device having a relatively stronger temperature dependence for low-field mobility. Another possibility is the device undergoing relatively more significant self-heating during high-field operation, which makes sense since we reached slightly higher input powers for the larger device. For simplicity we let $\mu$ in Eq. (3.6) be constant for an individual bias sweep, but we know from Fig. 3.6 that mobility varies with temperature and that
the device heats up during high-field operation, and thus, it follows that a larger value of $\gamma$ may simply imply increased self-heating effects.

Figure 3.11 exemplifies the temperature dependence of $v_d$, and ultimately $v_{sat}$, by showing the extracted velocity-field values (circles), along with the fits (dashed lines) using Eq. (3.6), from measurements taken at $T_0 = 80$ K (blue) and 450 K (red). As expected, we clearly see a decrease in the carrier velocity at higher temperatures. Therefore, we introduce a temperature-dependent factor to the single-phonon-limited models for saturation velocity discussed in Section 2.2 [46, 53, 83], such that $v_{sat}(T) = v_{sat,T=0}(1 + N_{OP})$, where $N_{OP} = 1/[\exp(\hbar\omega_{OP}/k_B T) - 1]$ is the OP occupation. This factor is qualitatively similar to that in Si [41, 115, 116], and due to the OP scattering (emission) rate being proportional to $(N_{OP} + 1)$ [108]. If the graphene zone-edge OP with $\hbar\omega_{OP} = 160$ meV [80] is assumed dominant, then the model only predicts a decrease in $v_{sat}$ of ~2% between ~200 K and ~500 K. However, if we use assume an OP with lower energy plays a role in limiting high-field transport, e.g., the substrate OP in SiO$_2$ with energy $\hbar\omega_{OP} = 55$ meV [79], then a ~24% decrease in $v_{sat}$ is predicted between ~200 K and 500 K. The latter is more
agreeable with the data in Fig. 3.11. We expect transport in supported-graphene devices to be non-deal and affected by the surrounding environment. Thus, if high-field transport is not only limited by the intrinsic phonons of graphene, we must consider other dissipation mechanisms to also play a role, such as remote-phonon scattering (see Section 2.2).

As mentioned previously, we expect \( v_{\text{sat}} \) in graphene to decrease with increasing carrier density, an effect due to graphene’s unique energy band structure [42, 46]. In Figure 3.12, we plot \( v_{\text{HF}} \) vs. electron density, where \( v_{\text{HF}} \) is used here to denote a drift velocity value at an electric field that is 0.5 V/\( \mu \)m or greater. In Fig. 3.12a we show the extent of our experimental measurements for both devices in this study by displaying the extracted \( v_{\text{HF}} \) at the highest fields obtainable such that the device integrity was maintained and low-field \( \sigma-V_G \) characteristics were reproducible. In order to compare carrier velocities at equivalent fields, Fig. 3.12b plots the corresponding \( v_{\text{HF}} \) at \( F = 1 \) V/\( \mu \)m using the fits obtained with Eq. (3.6). We caution against extrapolating further than \( F = 1 \) V/\( \mu \)m because the increase in electron density at higher fields must also be estimated. Combined with strong self-heating effects, this makes estimates at higher fields diffi-

![Figure 3.11](image-url)

**Figure 3.11:** Drift velocity vs. field at background temperatures of (blue) \( T_0 = 80 \) K and (red) 450 K for \( V_{G0} = 20 \) V, device with dimensions \( L = 4 \) \( \mu \)m, \( W = 2.2 \) \( \mu \)m, and \( t_{\text{ox}} = 90 \) nm. Circles (extracted \( v_d \)) and dashed lines (fits) are as in Fig. 3.10. Estimated temperature \( (T = T_0 + \Delta T) \) at the peak extracted \( v_d \) values are 175 K and 490 K for the \( T_0 = 80 \) K and 450 K curves, respectively.
Figure 3.13 compares the results from Fig. 3.12b with the analytic model by Fang et al. [46] discussed in Section 2.2 and shown in Fig. 2.7c. The model estimates saturation velocity as a function of carrier density assuming a “streaming” electron distribution, as shown in the inset of Fig. 3.13. This model for \( v_{\text{sat}} \) is limited by inelastic emission of OPs, and thus, we consider two dominant phonon mechanisms in Fig. 3.13. As before, we consider \( \hbar \omega_{\text{OP}} = 55 \) meV (lower dashed, SiO\(_2\) substrate OP [79]) and \( \hbar \omega_{\text{OP}} = 160 \) meV (upper dashed, graphene OP [80]) and assume \( T_0 = 300 \) K for both (see discussion of temperature-dependent \( v_{\text{sat}} \) above). The model limited by SiO\(_2\) phonons slightly underestimates \( v_{\text{HF}} \) while the model with graphene OPs overes-
mates the measured $v_{HF}$. Considering the remote-phonon-limited mobility from Fig. 2.5 is shown to be slightly increasing with increasing carrier density [42], while the extracted $v_{HF}$ decreases with increasing carrier density, it appears remote-phonon scattering contributes to limiting $v_{sat}$ but may not be the dominant scattering mechanism. We provide a reminder that this simple “streaming” model for $v_{sat}$ should be viewed as an empirical equation, considering it is likely an oversimplification of the electron distribution in the high-field regime. However, it is still useful for graphene device simulations if calibrated to experimentally extracted values. For example, the data from Fig. 3.13 can easily be fit using an intermediate OP energy, $\hbar\omega_{OP} \approx 75$ meV. A summary of the high-field drift velocity values shown in Figs. 3.12 and 3.13, along with values
Before concluding, we estimate from the graphene band structure [42] that the energy-dispersion relationship around the Dirac point remains linear up to at least ~1 eV. If a significant proportion of the electron population during our high-field measurements is reaching the flatter non-linear region, where electrons move slower, then we could attribute some of the velocity saturation effects observed in our study to this. Using the typical quadratic expression for estimating electron temperature ($T_e$) [117], where $T_e = T[1+(F/F_C)^2]$ with $F_C$ corresponding to the critical field at which hot electron effects begin, we calculate the electron energy to be less than

### Table 3.1: High-Field Drift Velocity in Graphene on SiO$_2$

<table>
<thead>
<tr>
<th>Device Dimensions</th>
<th>$T_0$</th>
<th>$\gamma$</th>
<th>$n$ $(10^{12}$ cm$^{-2}$)*</th>
<th>$v_{HF}$ $(10^7$ cm/s)*</th>
<th>$v_{sat}$ $(10^7$ cm/s)$\dagger$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$L = 4$ µm, $W = 7$ µm, $t_{ox} = 300$ nm</td>
<td>80 K</td>
<td>2</td>
<td>2.1</td>
<td>2.1</td>
<td>2.55</td>
</tr>
<tr>
<td></td>
<td>300 K</td>
<td>2</td>
<td>3.7</td>
<td>1.8</td>
<td>2.22</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>2.7</td>
<td>1.8</td>
<td>2.02</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>4.0</td>
<td>1.5</td>
<td>1.72</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5.4</td>
<td>1.4</td>
<td>1.52</td>
</tr>
<tr>
<td>$L = 4$ µm, $W = 2.2$ µm, $t_{ox} = 90$ nm</td>
<td>80 K</td>
<td>1.5</td>
<td>3.2</td>
<td>2.0</td>
<td>2.59</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5.6</td>
<td>1.7</td>
<td>2.10</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>8.0</td>
<td>1.5</td>
<td>1.81</td>
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<td></td>
<td></td>
<td></td>
<td>10.4</td>
<td>1.3</td>
<td>1.60</td>
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<td></td>
<td></td>
<td></td>
<td>12.6</td>
<td>1.2</td>
<td>1.42</td>
</tr>
<tr>
<td></td>
<td>450 K</td>
<td>1.5</td>
<td>3.0</td>
<td>1.8</td>
<td>2.45</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>5.4</td>
<td>1.3</td>
<td>1.81</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>7.8</td>
<td>1.1</td>
<td>1.42</td>
</tr>
</tbody>
</table>

*calculated values at $F = 1$ V/µm obtained from fits using Eq. (3.6) with power-law coefficient $\gamma$

$\dagger$Fitting parameter from Eq. (3.6)

for $v_{sat}$ obtained from fits to Eq. (3.6), is provided in Table 3.1.
50 meV for measurements from Fig. 3.9. Here we use $F_C = 0.5 \text{ V/µm}$, which is a relatively conservative estimate [52]. Therefore, it is unlikely that many electrons in our transport measurements approach the flatter non-linear region of the band structure, indicating that other scattering mechanisms (see above) are most likely responsible for the observed high-field behavior. Nevertheless, it is plausible that electrons at high fields in graphene devices on more ideal substrates (e.g., hexagonal boron nitride [59]), or suspended graphene devices, may be able to gain enough energy to populate the non-linear regime and contribute to velocity saturation.

3.6 Conclusions

In summary, we examined mobility and high-field drift velocity in graphene on SiO$_2$, including the roles of carrier density and temperature. The results indicate that high-field transport in graphene on SiO$_2$ does not exhibit exclusively intrinsic behavior, suggesting that additional scattering mechanisms (e.g., remote-phonon scattering with the substrate) contribute to limiting high-field drift velocity in graphene. Similarly, charged impurities on the substrate play a role in limiting low-field mobility, especially at low carrier densities. Improving the graphene-substrate interface is a necessary step to improve graphene device performance and reach the intrinsic transport limits of this 2D material. Lastly, the models introduced here are simple yet practical, and can be used in future simulations of graphene devices operating up to high fields.
CHAPTER 4: HIGH-FIELD ELECTRICAL AND THERMAL TRANSPORT IN SUSPENDED GRAPHENE

4.1 Introduction

As discussed in Chapters 2 and 3, the transport properties of atomically-thin graphene are affected by interactions with adjacent materials. Therefore, in order to understand the intrinsic electrical and thermal properties of graphene, it is necessary to study devices freely suspended across microscale trenches [118-125]. Compared to devices on typical substrates like SiO$_2$, the intrinsic mobility of electrons and holes in graphene is increased by up to a factor of ten [32, 118-120], and the thermal conductivity by about a factor of five when suspended. However, previous electrical transport studies of suspended graphene have only examined low-field and low-temperature conditions. Also in light of the fact that high-field measurements carried out on suspended carbon nanotubes (CNTs) had previously revealed a wealth of new physical phenomena, including negative differential conductance [126, 127], thermal light emission [128], and the presence of non-equilibrium optical phonons [126, 129], we have sufficient motivation to investigate high-field behavior in suspended graphene. Furthermore, since we expect even more significant self-heating in suspended devices than supported devices due to the lack of a heat dissipation pathway to an underlying substrate, we give particular attention to the coupled high-field electrical and thermal transport.

The approach used here, where we examine suspended graphene devices at high fields as well as at high temperatures, enables us to extract both the high-field drift velocity of charge carriers and the thermal conductivity of graphene up to higher temperatures than previously possible (>1000 K) [130]. Our systematic study includes experimental analysis of 15 samples combined with extensive simulations, including modeling of coupled electrical and thermal transport and modeling of graphene-metal contact effects. We uncover the important role that thermally gener-
ated carriers play in such situations, and also discuss important high-field transport properties at elevated temperatures up to device breakdown.

A schematic of a typical suspended graphene device is shown in Fig. 4.1a. To assess the broadest range of samples, we fabricated such devices using both mechanically exfoliated graphene and graphene grown by chemical vapor deposition (CVD). The suspension process is as

**Figure 4.1:** (a) Schematic of suspended graphene device. The color scale indicates the temperature of a suspended device during high-field current flow in vacuum (here calculated for the sample corresponding to Fig. 4.2a,b, with applied power $P = 1.2$ mW). Scanning electron microscopy (SEM) images of: (b) suspended graphene grown by chemical vapor deposition (CVD), and (c,d) suspended exfoliated graphene samples. All SEM images taken at a 70° tilt with respect to the substrate. (e) AFM image of suspended exfoliated graphene where the dashed blue line corresponds to the (f) height vs. distance trace. The initial SiO$_2$ thickness is 300 nm, of which approximately 200 nm is etched during the suspension process.
described in Section 1.4. After fabrication we confirm suspension via scanning electron microscopy (SEM) and atomic force microscopy (AFM), as shown in Figs. 4.1b-f. In order to avoid damaging the graphene from e-beam irradiation during SEM [131], we only image “dummy” devices or use low acceleration voltages (~1 kV) to conduct SEM prior to making measurements. Some devices show a small amount of “wrinkling” (see, e.g., Fig. 4.1d), possibly leading to some of the sample-to-sample variability described in Section 4.6. We note that the CVD graphene samples underwent a vacuum anneal at 200 °C after the suspension process. Typically, device performance improved after this anneal but we also noticed several devices would break. Due to the fragility and relatively limited number of exfoliated graphene devices, we did not perform this additional annealing step with the exfoliated graphene samples.

4.2 Electrostatics and Low-Field Mobility

Figure 4.2a shows a typical resistance ($R$) vs. back-gate voltage ($V_G$) measurement for a suspended exfoliated graphene device with length $L \approx 1.5 \mu$m and width $W \approx 850$ nm, in vacuum ($\sim 10^{-5}$ Torr) at room temperature. For all measurements, we limit the back-gate voltage to $|V_G| \leq 10$ V to avoid collapsing the suspended channel [132, 133]. The as-fabricated devices do not immediately exhibit the “clean” electrical behavior one might associate with freely suspended graphene [118-120]. Although the channel is not in contact with the substrate, some residue from processing remains on the device, and this can be removed or minimized through a current annealing technique [118, 120]. In this process, we sweep the drain voltage ($V_D$) to increasingly higher values until the Dirac voltage ($V_0$) appears within the narrow usable $V_G$ window ($|V_G| \leq 10$ V) and the electrical characteristics of the device stabilize (Fig. 4.2a).

We note that increases or decreases in resistance that do not always correspond to changes in $V_0$ are often seen during the annealing process. Although we expect the removal of impuri-
ties to affect the graphene resistivity, we believe these shifts are often caused by a change in the contact resistance. For cases when the device resistance increases substantially we find that the graphene channel has undergone partial breakdown (see Sections 4.6 and 4.7). We took care to avoid using such devices when extracting transport properties.

Figure 4.2b displays the room temperature effective mobility ($\mu_0$) of the device from Fig. 4.2a. There is some uncertainty in the mobility extraction because the carrier density is not well known at low-field, in part due to limited knowledge of the residual doping density $n^*$. Thus, Fig.
4.2b displays the effective mobility at several residual doping levels \([84]\) \(n^* = 10^9, 10^{11}\), and \(2 \times 10^{11}\) cm\(^2\). Nevertheless, the estimated mobility is above \(15,000\) cm\(^2\)V\(^{-1}\)s\(^{-1}\) at room temperature, consistent with previous work \([120]\), which pointed out such values are limited by flexural phonons in suspended graphene at all but the lowest temperatures \((T \geq 10\) K).}

Interestingly, we note that significantly above room temperature the carrier density in the suspended graphene channel becomes dominated by thermally generated carriers \((n_{th})\) and independent of gate voltage as shown in Fig. 4.2c. The gate capacitance \((C_G)\) is determined by the series combination of the air gap \((t_{\text{air}} \approx 200\) nm\) and the remaining SiO\(_2\) \((t_{\text{ox}} \approx 100\) nm\), where \(C_{\text{air}} = \varepsilon_{\text{air}}\varepsilon_0/t_{\text{air}},\) \(C_{\text{ox}} = \varepsilon_{\text{ox}}\varepsilon_0/t_{\text{ox}},\) and \(C_G = (C_{\text{air}}^{-1} + C_{\text{ox}}^{-1})^{-1}\). We obtain \(C_G \approx 4\) nF/cm\(^2\), which means at \(V_{G0} = V_G - V_0 = 10\) V we estimate that the gate voltage induces \(n_{cv} = C_G V_{G0}/q \approx 2.5 \times 10^{11}\) cm\(^{-2}\) carriers; however, at 1000 K the total population of thermally generated carriers (electrons plus holes) is dominant, \(2n_{th} = 2(\pi/6)(k_B T/hv_F)^2 \approx 1.8 \times 10^{12}\) cm\(^{-2}\), and increasing quadratically with temperature, where \(k_B\) is the Boltzmann constant, \(\hbar\) is the reduced Planck constant, and \(v_F \approx 10^8\) cm/s is the graphene Fermi velocity. These trends are illustrated in Fig. 4.2c at temperatures ranging from 300 to 2000 K, calculated using the charge-density model described in Section 3.2.

Before discussing high-field measurements, we must first address the issue of contact resistance in our devices. Contact resistance in the CVD graphene devices is determined using the transfer length method (TLM). In Fig. 4.3 we plot \(R \cdot W\) versus \(L\) and extract \(R_C W \approx 1100\) \(\Omega\)-um from the linear fit (dashed line). We use the resistance value at breakdown for extracting contact resistance. The spread in \(R \cdot W\) values that results in a poor linear fit in Fig. 4.3 may be associated with the difficulty in determining \(W\) after breakdown, along with other causes of sample-to-sample variation discussed below. Therefore, we let \(R_C W = 200\) to 2000 \(\Omega\)\(-\)\(\mu\)m (typical values for “good” and “bad” contacts respectively) for extracting the upper and lower bounds of average...
carrier velocity and thermal conductivity shown later in Figs. 4.5 and 4.7. We use TLM to extract contact resistance for the exfoliated devices, but due to the limited amount of breakdown data, we use resistance values from low-field measurements of devices of varying length from the same sample. The average $R_C W$ for the exfoliated graphene devices in this work is $\sim 1800 \, \Omega \cdot \mu m$. We vary $R_C W$ by 50% to provide bounds in Figs. 4.5 and 4.7 similar to the case with CVD graphene. A possible reason for the exfoliated graphene having a larger contact resistance than that of the CVD graphene is the additional anneal in vacuum at 200 °C that the CVD graphene samples underwent, but the exfoliated graphene did not.

4.3 High-Field Electrical Measurements and Drift Velocity at Breakdown

We now turn to our high-field transport measurements of suspended graphene devices. Figure 4.4a displays the measured current density ($I/W$) as a function of average electric field along the channel $F \approx (V_D - 2IR_C)/L$, up to irreversible electrical breakdown of suspended exfoliated (red) and CVD-grown (blue) graphene devices, in vacuum ($\sim 10^{-5}$ Torr) at room temperature. Some devices show linearly increasing current at low fields followed by saturation-like behavior at high fields, while other devices show linear (and sometimes superlinear) current

\[ \text{Figure 4.3: } R \cdot W \text{ vs. } L \text{ for multiple CVD graphene devices taken at the breakdown point in vacuum. The dashed line is a linear fit where the y-intercept corresponds to } 2R_C W \approx 2200 \, \Omega \cdot \mu m. \]
throughout.

To understand this behavior, in Fig. 4.4b we use our self-consistent electrical–thermal simulator of graphene [81, 82, 134] to model $I/W$ versus $F$ up to suspended graphene device breakdown. The model used to provide the simulations shown is based on applying the suspended device geometry to the models developed in previous works [32, 135]. First, the gate capacitance $C_G$ is calculated as described above. Second, we simulate a suspended channel region by setting the thermal conductance to the substrate to zero, but we still allow for heat loss to the substrate underneath the contacts. Third, we adjust our model of drift velocity saturation in order to more accurately represent a suspended graphene sheet. Substrate effects should no longer limit transport at high fields so we assume the saturation velocity ($v_{sat}$) is determined by the zone-edge optical phonon (OP), $\hbar\omega_{OP} = 160$ meV [80]. We also use a Fermi velocity that is dependent on carrier density due to changes in the linear energy spectrum near the neutrality point for suspended graphene, $v_F(n) \sim v_0[1 + \ln(n_0/n)/4]$, where $v_0 = 0.85 \times 10^6$ m/s and $n_0 = 5 \times 10^{12}$ cm$^{-2}$ [136]. Fourth, the thermal generation of carriers, $n_{th} = a(\pi/6)(k_B T/\hbar v_F)^2$, is given a slightly stronger than $T^2$ dependence above room temperature (although it decays back to a $T^2$ dependence at high $T$) by introducing $\alpha = 1 + e^{-(T/T_0-1)/2}\sqrt{T/T_0-1}$, where $T_0 = 300$ K. This empirical fit is used to account for the possible electron-hole pair generation from optical phonon decay [85] and/or Dirac voltage shifting that may occur during high-field device operation. Lastly, we add a contribution to the carrier density near the contacts ($n_C$) to account for the modification of the graphene electronic structure by the metal contacts, such that $n_C = 10^{11}$ cm$^{-2}$ at the contact but exponentially decreases away from the contact with a decay length of ~200 nm [111].
For the simulated curves in Fig. 4b we varied the room-temperature low-field mobility ($\mu_0$) from 2,500 to 25,000 cm$^2$/V·s along with the temperature dependence of the mobility ($\mu \sim T^{-\beta}$ where $\beta$ varies from 1.5 to 2.5). This is meant to represent the range of “dirty” to “clean” devices that we measured experimentally. We accordingly vary the room-temperature thermal conductivity ($\kappa_0$) from 2000 to 3000 Wm$^{-1}$K$^{-1}$ and the breakdown temperature ($T_{BD}$) from 1420 to 2860 K, respectively. Thus, we are able to replicate the different types of curves observed experimentally. We find that devices showing saturation-like behavior at high fields typically have higher $\mu_0$ and stronger mobility dependence on temperature (i.e., $\mu(T) \sim T^{-\beta}$ where $\beta \approx 2.5$), being essentially “cleaner” and less disordered. Conversely, devices not showing saturation-like behavior have relatively low $\mu_0$ and a weaker temperature dependence ($\beta \approx 1.5$), which most likely corresponds to higher residual doping and disorder [118, 137, 138]. The superlinear current rise in such devices is due to the sharp increase in thermally generated carriers ($n_{th}$) as the device heats up. We note that overall the $I$-$V$ behavior of suspended graphene devices is markedly different from that of suspended carbon nanotubes [126-129]. Suspended carbon nanotubes show negative
differential conductance (NDC) and a current drop at high-fields due to strong one-dimensional (1D) phonon scattering as the device heats up. By contrast, the linearly increasing density of states in 2D graphene leads to enhanced thermal carrier generation as the device heats up, which prevents the appearance of NDC.

Next, in Fig. 4.5 we extract the carrier drift velocity from our high-field transport data in Fig. 4.4, near the physical device breakdown. As discussed previously, the carrier density for our suspended devices has little to no gate dependence at high temperature reached at high fields, due to device self-heating. The maximum carrier drift velocity at the breakdown (BD) point is $v_d = I_{BD}/(qWn_{tot})$, where $n_{tot} = 2[(n^*/2)^2 + n_{th}^2]^{1/2}$ is the carrier density [32] including residual doping ($n^* \sim 2 \times 10^{11}$ cm$^{-2}$) and thermal carrier generation, $n_{th}$. The latter dominates at the elevated temperatures in the middle of the channel. We note that the temperature profile, and thus, the car-

![Figure 4.5: Charge carrier high-field drift velocity at breakdown and high temperature ($T_{avg} \approx 1200$ K) along the suspended graphene channel. The dashed line is a simple estimate of $v_{sat}$ in intrinsic graphene at such temperature and average carrier density (see text). Exfoliated (red) and CVD (blue) graphene devices. Samples are ordered by increasing $(I_{BD}/W)/F_{BD}$, representative of increasingly “cleaner” devices as shown in Fig. 4.4b. Lower bounds, symbols, upper bounds correspond to models with breakdown temperatures of 2860, 2230, and 1420 K respectively. The estimation for the breakdown temperature is described below with our thermal analysis. Some uncertainty also comes from imprecise knowledge of the device width $W$, which is also discussed later in the text.](image-url)
carrier density and drift velocity, varies strongly along the channel near the BD point. However, because we cannot precisely model this profile for every device measured, we instead estimate the average drift velocity at breakdown, which is evaluated for an average carrier density along the channel, \( \langle n_{\text{tot}} \rangle \approx 4 \times 10^{12} \text{ cm}^{-2} \) and \( T_{\text{avg}} \approx 1200 \text{ K} \), based on the thermal analysis discussed below.

Figure 4.5 displays the drift velocity at breakdown from all samples, arranged in increasing order of \( (I_{\text{BD}}/W)/F_{\text{BD}} \), which our simulations (Fig. 4.4b) suggest will rank them from most to least disordered. These data represent the high-field velocity (i.e., near breakdown and approaching the saturation velocity) in intrinsic graphene, as all measurements reached fields greater than 1 V/μm. We also point out that the transport regime observed here is not identical to our previous work in Chapter 3 on SiO2-supported graphene. Here, the high-field measurement can only be carried out in an ambipolar, thermally intrinsic regime \( (n \approx p \approx n_{\text{th}}/2) \), whereas previous work for substrate-supported devices focused on unipolar (e.g. \( n \gg p \)) transport.

The maximum velocity values at breakdown \( (v_{\text{BD}}) \) seen here for sample numbers 13–15 are very close to the saturation velocity predicted by the previously discussed (see Sections 2.2 and 3.5) simple model by Fang et al. [46], when transport is only limited by graphene optical phonons (OPs) with energy \( \hbar \omega_{\text{OP}} = 160 \text{ meV} \), that is, \( v_{\text{sat}} \approx 2.7 \times 10^{7} \text{ cm/s} \) for the average charge density and temperature estimated here \( (4 \times 10^{12} \text{ cm}^{-2} \text{ and } 1200 \text{ K}, \text{ respectively}) \). However, we point out that the analytic model is based on unipolar, not ambipolar transport; as such the value for \( v_{\text{sat}} \) given here should be seen more as a guide than a fixed fundamental value. Nevertheless, similar saturation velocities have been predicted for clean, intrinsic graphene by extensive numerical simulations at comparable fields and carrier density [44, 46, 139]. However, the average high-field velocity at breakdown observed across our suspended samples is lower, \( v_{\text{BD}} = (1.7 \pm 0.6/-0.3) \times 10^{7} \text{ cm/s} \), similar for exfoliated and CVD-grown graphene, at the average carrier densi-
ties and temperatures reached here. The average value remains a factor of two higher than the saturation velocity at elevated temperature in silicon ($v_{\text{Si}} = 8 \times 10^6 \text{ cm/s at } \sim 500 \text{ K}$) [41], but we suspect that variability between our samples is due to the presence of disorder and some impurities [45], which also affect the low-field mobility. In addition, depending on the level of strain built-in to these suspended samples and how the strain evolves at high temperature, flexural phonons [120, 138] may also play a role in limiting high-field transport. It is apparent that future computational work remains needed to understand the details of high-field transport in graphene under a wide variety of temperatures and conditions, including ambipolar versus unipolar transport, impurities, and disorder.

4.4 Thermal Analysis

Now we discuss the thermal analysis of our suspended graphene devices during high-field operation. While the breakdown temperature of graphene in air is relatively well-known as $T_{\text{BD,air}} \approx 600 \text{ °C} = 873 \text{ K}$ (based on thermogravimetric analysis [140, 141] and oxidation studies [142]), the breakdown temperature of graphene in probe station vacuum ($10^{-5} \text{ Torr}$) was not well understood before the start of this study. To estimate this, we compare similar devices taken up to electrical breakdown in air and in vacuum conditions. In both cases, we can assume heat transport is diffusive in our suspended devices at high temperature based on the subsequent discussion. Following Pop et al. [135], we can estimate the phonon mean free path at 1000 K as $\lambda \approx (2\kappa/\pi)/(G_b-\kappa/L) \approx 21 \text{ nm}$, where $\kappa = 310 \text{ Wm}^{-1}\text{K}^{-1}$, $G_b = 9.6 \text{ GWK}^{-1}\text{m}^{-2}$ is the ballistic conductance per cross-sectional area (at 1000 K), and $L = 1$ to $3 \mu\text{m}$ is the range of our sample lengths. Thus, we always have $\lambda \ll L$ and phonon transport is diffusive at these high temperatures. Also indicative of diffusive phonon transport is the fact that we do not observe a dependence of $\kappa$ on sample size. Now we can write the heat diffusion equation as
\[
\frac{d^2 T}{dx^2} + \frac{P}{\kappa LWt} - \frac{2g}{\kappa t} (T - T_0) = 0
\]

(4.1)

where \(\kappa\) is the thermal conductivity and \(t = 0.34\) nm is the thickness of graphene, \(g = 2.9 \times 10^4\) Wm\(^{-2}\)K\(^{-1}\) is the thermal conductance per unit area between graphene and air [124], and \(g \approx 0\) in vacuum. Here the power dissipation is \(P = I(V - 2IR_C)\) within the suspended graphene channel, and the temperature of the contacts at \(x = \pm L/2\) is assumed constant, \(T_0 \approx 300\) K (the small role of thermal contact resistance is discussed below). Assuming that \(\kappa\) is a constant (average) along the graphene channel, we now compare breakdowns in air and vacuum and estimate the graphene device breakdown temperature.

In Fig. 4.6a-c we show examples of the electrical breakdown of suspended graphene devices in vacuum (~10\(^{-5}\) Torr), air, and O\(_2\) environments. Device failure in vacuum occurs instantaneously corresponding to a sudden drop in current over a very narrow range of voltage. However, breakdown in air and O\(_2\) is a more gradual process where the current degrades over a relatively wide voltage range. We expect that the very low O\(_2\) partial pressure in vacuum allows for the suspended device to reach higher temperature without oxidation degrading the device. This is consistent with previous studies of substrate-supported carbon nanotubes [143] and graphene nanoribbons [144]. Conversely, in air and O\(_2\) oxidation may occur sporadically at lower temperatures (< 1000 K) due to the much greater availability of O\(_2\). We also note that the breakdown location observed by SEM (Figs. 4.6d-f) is in the center of the graphene channel, corresponding to the position of maximum temperature predicted by our thermal model here.

To estimate the breakdown temperature of suspended graphene devices in vacuum, we compare breakdowns in air and vacuum. In air, solving for \(T(x)\) from the heat diffusion equation above results in
such that the breakdown temperature is given by

\[
T(x) = T_0 + \frac{P}{m^2 kLWt} \left( 1 - \frac{\cosh(mx)}{\cosh(mL/2)} \right) \tag{4.2}
\]

Figure 4.6: \( I_D \) vs. \( V_D \) and corresponding SEM images, taken at a 70° tilt with respect to the substrate, of suspended graphene broken in (a,d) vacuum, (b,e) air, and (c,f) \( O_2 \). Breakdown in vacuum is relatively sudden and less gradual than breakdown in air or \( O_2 \).

\[
T_{RD,air} = T_0 + \frac{P_{BD,air}}{m^2 kLWt} \tag{4.3}
\]

where \( m = (2g/kt)^{1/2} \) and \( \zeta = 1 - 1/\cosh(mL/2) \). In vacuum, heat loss due to convection and radiation is negligible. With respect to heat loss due to radiation, the power loss is estimated by \( P_{rad} = \sigma e A(T^4 - T_0^4) \), where \( \sigma = 5.67 \times 10^{-8} \text{ Wm}^{-2}\text{K}^{-4} \) is the Stefan-Boltzmann constant, \( e \sim 2.3 \% \) is the emissivity of graphene and assumed equal to the absorption from [145], \( A = 2 \mu\text{m}^2 \) is an upper limit for the area of the graphene channel, and \( T = 1300 \text{ K} \) is an upper limit for average temperature along the channel. We estimate \( P_{rad} \approx 7.4 \text{ nW} \), which is several orders of magnitude less than the electric power that is dissipated. Consequently, we use \( g = 0 \) which results in
\[ T(x) = T_0 + \frac{PL}{8\kappa Wt} \left( 1 - \left( \frac{2x}{L} \right)^2 \right) \]  \hspace{2cm} (4.4)\\

and

\[ T_{BD,vac} = T_0 + \frac{P_{BD}L}{8\kappa Wt}, \]  \hspace{2cm} (4.5)

Although electrical breakdown of graphene in air is often gradual and consisting of a series of partial breaks, as shown above in Fig. 4.6b, we can carefully choose the breakdown points from our measurements, and assuming \( \kappa_{air} \approx \kappa_{vac} \), we estimate \( T_{BD,vac} \approx 2230 \) K.

We acknowledge some uncertainty in assuming \( \kappa_{air} \approx \kappa_{vac} \), but note that the devices used for this comparison underwent similar processing. We expect graphene in vacuum to be relatively “clean”, especially after current annealing, and have a higher thermal conductivity than that of graphene in air, but devices in vacuum operate at a higher average temperature, which would cause a decrease in thermal conductivity. Quantitatively evaluating these competing effects is difficult, particularly the cleanliness of a sample, thus we aim to provide upper and lower bounds for our estimate of \( T_{BD,vac} \). We estimate a lower bound for \( T_{BD,vac} \) by using \( g = 0 \) as a lower limit for the heat transfer coefficient in air [124], and \( T_{BD,air} \approx 400 \) °C to account for the tendency of partial breakdown in air. We estimate an upper bound for \( T_{BD,vac} \) by using \( g = 10^5 \) Wm\(^{-2}\)K\(^{-1}\) in air, the theoretical upper limit based on kinetic theory [124], and the typical \( T_{BD,air} \approx 600 \) °C. Thus, the extreme lower and upper bounds for \( T_{BD,vac} \) are 1420 and 2860 K respectively. The lower limit appears to be a conservative estimate since the breakdown power scaled with device dimensions is typically about three times higher in vacuum than in air. The upper limit is comparable to the 2800 °C (i.e., 3073 K) previously estimated as the breakdown temperature of suspended graphitic nanoribbons under Joule heating [146]. Also, suspended CVD graphene has been reported to be thermally stable up to at least 2600 K [147]. However, we note these previous studies were
performed in a transmission electron microscope (TEM), which is capable of obtaining lower vacuum levels than our probe station, accounting for samples likely reaching higher temperatures.

Having estimated a range for \( T_{BD,vac} \), we turn to more detailed thermal modeling in order to extract \( \kappa(T) \) from the electrical breakdown data. In general, we expect the thermal conductivity decreases with increasing temperature above 300 K, consistent with the case of carbon nanotubes, graphite and diamond \[135\]. Therefore, we write \( \kappa = \kappa_0(T_0/T)^\gamma \) above room temperature and solve the one-dimensional heat diffusion equation, obtaining

\[
T(x) = \left( T_0^{1-\gamma} + \frac{PL(1-\gamma)}{8\kappa_0T_0Wt} \left( 1 - \left( \frac{2x}{L} \right)^2 \right) \right)^{\frac{1}{1-\gamma}}
\]  

(4.6)

where \( \kappa_0 \) and \( \gamma \) are fitting parameters, \( \kappa_0 \) being the thermal conductivity at \( T_0 = 300 \) K. (A similar analytic solution was previously proposed for suspended carbon nanotubes, albeit with a different functional form of the thermal conductivity \[148\].) The breakdown temperature is maximum in the middle of the suspended graphene, at \( x = 0 \)

\[
T_{BD,vac} = \left( T_0^{1-\gamma} + \frac{P_{BD}L(1-\gamma)}{8\kappa_0T_0Wt} \right)^{\frac{1}{1-\gamma}}
\]  

(4.7)

where for \( T_{BD,vac} \approx 2230 \) K we obtain \( \gamma \approx 1.9 \) and \( \gamma \approx 1.7 \) for our exfoliated and CVD-grown graphene samples, respectively.

Figure 4.7 shows the extracted thermal conductivity of each sample at \( T = 1000 \) K for devices measured in vacuum. The lower bounds, circles, and upper bounds are based on \( T_{BD,vac} = 2860, 2230, \) and \( 1420 \) K, respectively, the widest range of breakdown temperatures in vacuum estimated earlier. The average thermal conductivities at 1000 K of the exfoliated and CVD graphene samples are similar, \( \kappa = (310 \pm 200/\pm 100) \) W m\(^{-1}\)K\(^{-1}\). Of this, the electronic contribution
is expected to be <10%, based on a Wiedemann–Franz law estimate \[144\]. The result suggests that lattice phonons are almost entirely responsible for heat conduction in graphene even at elevated temperatures and under high current flow conditions. The average values of thermal conductivity found here are slightly lower than those of good-quality highly oriented pyrolytic graphite (534 W m\(^{-1}\)K\(^{-1}\) at \(T = 1000\) K) \[149\], but the latter is consistent with the upper end of our estimates. The extrapolation of our model to room temperature yields an average \(\kappa_0 \approx 2500\) W m\(^{-1}\)K\(^{-1}\) at 300 K, as shown in Fig. 4.8 and consistent with previous work on freely suspended graphene \[121-125\].

Figure 4.8 plots thermal conductivity as a function of temperature, showing that previously reported studies \[121-125\] (most near room temperature) fall on the same trend as this work at high temperature. However, our model of high-temperature thermal conductivity of suspended graphene suggests a steeper decrease (\(\sim T^{-1.7}\) weighed between exfoliated and CVD samples) than that of graphite (\(\sim T^{-1.1}\)). The difference is likely due to the flexural phonons of isolated graphene, which could enable stronger second-order three-phonon \[150\] scattering transitions (\(\sim T^2\))
scattering rate at high temperature) in addition to common first-order Umklapp phonon-phonon transitions (~$T$ scattering rate). Second-order three-phonon processes involve the virtual combination of two phonons into a virtual state, and the splitting of the virtual phonon into two new phonons. For this reason, this process is also sometimes referred to as four-phonon scattering. Similar observations as shown here were also made for silicon [151], germanium [152], and carbon nanotubes [153, 154] at high temperatures but not in isolated graphene until now.

Now we return to our thermal modeling to discuss the issue of thermal contact resistance.

Figure 4.8: Suspended graphene thermal conductivity above room temperature estimated from this work (lines) and that of previous studies (symbols). Shaded regions represent the average ranges of values for exfoliated (red) and CVD (blue) graphene from this work. The weighted average thermal conductivity for our samples is ~2500 Wm$^{-1}$K$^{-1}$ at room temperature and ~310 Wm$^{-1}$K$^{-1}$ at 1000 K, with a steeper drop-off than graphite, attributed to second-order three-phonon scattering (see text).
and estimate the temperature rise at the contacts [134] due to Joule heating during high-field current flow. The thermal resistance for heat flow from the suspended graphene channel into the metal contacts can be approximated by [155]

\[
R_{C,th} = \frac{1}{hL_{T}W_{C}} \coth \left( \frac{L_{C}}{L_{T}} \right)
\]

(4.8)

where \( h \) is the thermal interface conductance per unit area for heat flow from the graphene into the SiO\(_2\) or Au, \( W_{C} \) is the width of the graphene under the contact, and \( L_{C} \) is the metal contact length. The thermal transfer length \( L_{T} = (\kappa t/h)^{1/2} \) corresponds to the distance over which the temperature drops by \( 1/e \) within the contact [134]. Typical contact lengths are on the order of microns while \( L_{T} \approx 50 \text{ nm} \); thus, we have \( L_{C} \gg L_{T} \) and we can simplify \( R_{C,th} \approx (hL_{T}W_{C})^{-1} \approx (W_{C})^{-1}(h\kappa t)^{-1/2} \). Heat dissipation at the contacts consists of parallel paths to the underlying SiO\(_2\) substrate and the top metal contact, where \( h_{g-ox} \approx 10^8 \text{ Wm}^{-2}\text{K}^{-1} \) and \( h_{g-Au} \approx 4 \times 10^7 \text{ Wm}^{-2}\text{K}^{-1} \) [156, 157], respectively. The total thermal resistance for one contact is given by \( R_{C,th} = (R_{C,ox}^{-1} + R_{C,Au}^{-1})^{-1} \). The temperature rise at the contacts is estimated as \( \Delta T_{C} = T_{C} - T_{0} = R_{C,th}P_{BD}/2 \) (where \( P_{BD} \) is the input electrical power at the breakdown point), which is only 10s of Kelvin. Including thermal contact resistance for the analysis when estimating \( T_{BD, vac} \) above would change the extracted values by less than 4%.

**4.5 Raman Spectroscopy of Electrically Biased Suspended Graphene Transistor**

Prior to now, we have inferred the temperature of graphene devices primarily through simulations of our device structures and comparison with electrical data. Therefore, for thoroughness and to supplement our thermal modeling, we briefly discuss experimental work where we directly measured the temperature of functioning graphene devices using a thermometry method based on Raman spectroscopy [83, 158]. Raman thermometry relies on the temperature-
dependent shift of graphene 2D and G bands (see Fig. 4.9a), which downshift with increasing temperature as a result of anharmonic phonon coupling [159]. This technique has been used in the past to measure the thermal conductivity of suspended graphene devices [121, 123-125] and power dissipation in SiO₂-supported graphene devices [84, 85]. However, no studies presently exist on the Raman thermometry of suspended graphene devices heated by electrical bias.

We have calibrated this temperature dependence by placing graphene devices in a temperature-controlled stage and measuring the peak position of the 2D band as a function of tem-
For the temperature regime discussed here, we assume a linear relation between peak position and temperature such that $\chi_{2D} \approx -0.047 \text{ cm}^{-1}/K$. Figure 4.9c shows the increasing temperature in an electrically biased suspended graphene device as the power is increased. We note that the experimental setup for performing Raman spectroscopy while operating the device requires ambient conditions. Therefore, in Fig. 4.10 we use Eq. (4.2) to extract the thermal conductivity of the device from our Raman thermometry data. We observe a slight decrease in thermal conductivity from $\kappa \approx 800$ to 500 Wm$^{-1}$K$^{-1}$ as the temperature increases from $\sim 300$ K to 650 K. The extracted $\kappa$ here is on the lower end when compared to the data shown in Fig. 4.8 for suspended graphene, not surprisingly, considering these Raman thermometry measurements were performed in ambient conditions and we were unable to implement
the standard practice of annealing in vacuum and performing subsequent measurements in vacuum, without exposure to air. Nevertheless, we are able to directly measure the temperature increase in a device through self-heating effects and obtain reasonable values for graphene thermal conductivity with the Raman thermometry technique discussed here.

4.6 Variability

We now comment more on the observed variability between samples and on the role of graphene-metal contact resistance. First, even after high-temperature current annealing, polymer residue from processing may remain on the samples, increasing the scattering of both charge and heat carriers [160]. This sample-to-sample variation can contribute to the spread in extracted carrier velocity and thermal conductivity in Figs. 4.5 and 4.7, respectively. In this respect, it is likely that our samples yielding higher carrier velocity and higher thermal conductivity (e.g., sample no. 13 in Figs. 4.5 and 4.7) are the “cleanest” ones, most closely approaching the intrinsic limits of transport in suspended graphene. Second, some edge damage occasionally seen after high-current annealing affects our ability to accurately determine the sample width, W. The value used for W influences all our calculations, and its uncertainty is incorporated in our error analysis here. Third, several of the CVD graphene samples in the study had W < 200 nm, and edge scattering effects are known to limit transport in narrow ribbons [144, 161]. However, we saw no obvious dependence of thermal conductivity, carrier velocity, or breakdown current density (I_{BD}/W) on sample width when comparing “wide” and “narrow” devices. We thus expect that variation among samples due to edge scattering is smaller than other sources of variation.

4.7 Suspended Graphene Nanoconstriction

We recently mentioned above that a source of variability may be edge damage after high-current annealing. We see from the SEM image after device breakdown in vacuum (Fig. 4.6d)
that the edges of the graphene channel are damaged (i.e., twisted or burned away) during the breakdown process. Burning away of the edges may also occur before breakdown during the current annealing process and result in the formation of a graphene nanoconstriction \[162\]. Here we show the behavior of a suspended CVD graphene device \((L = 1 \mu m)\) with a nanoconstriction formed by excessive current annealing. We note that this device was not used for extracting data in previous parts of this study.

Figure 4.11: (a) Measured current vs. gate voltage at \(T = 80–300 \text{ K}\) of a suspended CVD graphene nanoconstriction formed by current annealing. (b) Electrical transport measurements at \(T = 150 \text{ K}\) under varying bias \(V_D = 50–1000 \text{ mV}\). High on/off > \(10^6\) is observed for \(V_D \leq 200 \text{ mV}\), while an increase in bias to \(V_D = 1000 \text{ mV}\) results in on/off < 10. (c) Temperature dependence of the minimum current at \(V_D = 200 \text{ mV}\). Effective bandgap of \(E_g \sim 0.35 \text{ eV}\) is extracted assuming thermal activation, \(I_{\text{min}} \sim \exp(-E_g/2k_B T)\).

Figure 4.11a displays the measured \(I_D-V_G\) of a nanoconstriction device at \(T = 80–300 \text{ K}\) for \(V_D = 200 \text{ mV}\), showing high on/off > \(10^3\) at room temperature and >\(10^9\) at \(T = 80 \text{ K}\). In Fig. 4.11b we vary the drain bias at \(T = 150 \text{ K}\) to show that the effective band gap and on/off is di-
minished at high fields. We observe high on/off $> 10^6$ for $V_D \leq 200 \text{ mV}$, but a low on/off $< 10$ when we increase the bias to $V_D = 1 \text{ V}$. At low bias and low temperature we observe discrete conductance peaks (e.g., $V_D = 50 \text{ mV}$ and $T = 150 \text{ K}$ in Fig. 4.11b). It has been suggested that the regions of the graphene channel that connect the narrow nanoconstriction to the wider graphene sheet may actually be confined longitudinally (i.e., along the length of the channel) and behave as quantum dots in series [162]. Thus, the conductance peaks correspond to resonant tunneling through the quantized energy levels of these quantum dots. In Fig. 4.11c we assume thermal activation, $I_{\text{min}} \sim \exp(-E_g/2k_B T)$, to extract an effective band gap of $E_g \sim 0.35 \text{ eV}$ and corresponding width of $\sim 12 \text{ nm}$, where $W = 2\pi\hbar v_F/E_g$ [104]. This width extraction may be an underestimate since the aforementioned quantum dot regions may increase the effective band gap. Unfortunately, the device broke before we were able to image and measure the nanoconstriction width.

### 4.8 Conclusions

In summary, we fabricated suspended graphene devices and carefully analyzed their high-field electrical and thermal transport. The electrical transport is entirely dominated by thermally generated carriers at high temperatures ($>1000 \text{ K}$), with little or no control from the substrate “gate” underneath such devices. The maximum high-field breakdown velocity recorded is $>3\times 10^7 \text{ cm/s}$, consistent with theoretical predictions for intrinsic transport limited only by graphene optical phonons. However, average extracted drift velocities are lower (although remaining a factor of two greater than in silicon at these temperatures), due to sample-to-sample variation. We estimated the breakdown temperature of graphene in $10^{-5} \text{ Torr}$ vacuum to be $\sim 2230 \text{ K}$, which combined with our models, yields an average thermal conductivity of $\sim 310 \text{ W m}^{-1}\text{K}^{-1}$ at 1000 K for both exfoliated and CVD-grown graphene. The models show thermal conductivity dependence as $\sim T^{-1.7}$ above room temperature, a steeper drop-off than that of graphite, suggest-
ing stronger effects of second-order three-phonon scattering. The Raman thermometry technique implemented here provided a direct measurement of the temperature rise of a suspended graphene device due to self-heating at high bias. Our study also highlights remaining unknowns that require future efforts on electrical and thermal transport at high field and high temperature in graphene.
CHAPTER 5: VELOCITY SATURATION AND HIGH-FIELD NEGATIVE DIFFERENTIAL CONDUCTANCE IN TWO-DIMENSIONAL MOLYBDENUM DISULFIDE TRANSISTORS

5.1 Introduction

We continue to emphasize that understanding high-field electrical transport in nanomaterials is essential for many applications including transistors and photodetectors, especially when we consider that the analysis of high-field electrical measurements can provide insight into the high-energy band structure of a material. As discussed in Section 2.3, despite the increasing amount of interest given to studying the electrical and optical properties of 2D materials [23, 163], little is known about high-field transport in 2D MoS$_2$ [88, 89], particularly as a function of temperature and carrier density. We also note that some properties of 2D MoS$_2$ films are more similar to Si than graphene, both in terms of low-field electron mobility [32, 164, 165] and the presence of an energy band gap (~1.2 eV for bulk and few-layer [25]) which is desirable for both digital transistor and photodetector applications [166]. Demonstrations of MoS$_2$ for potential use in future nanoscale electronics include the fabrication of integrated circuits based on bilayer MoS$_2$ transistors [167] as well as MoS$_2$ transistors fabricated on flexible substrates [96, 97]. In addition, the thinness of MoS$_2$ (1 layer = 6.5 Å) could enable scaling transistors to sub-10 nm dimensions [168].

A thermal analysis of MoS$_2$ field-effect transistors (FETs) is important, specifically the effect of self-heating on high-field operation, which is expected to play a significant role in applications intended on flexible substrates [96, 97]. Given that mobility and saturation current densities in MoS$_2$ are relatively low compared to graphene, it is possible others have assumed that power densities in MoS$_2$ FETs do not reach high enough values to cause significant heating. However, our work here shows that Joule heating may play an important role in high-field transport in MoS$_2$. 
In this study we investigate MoS$_2$ transistors from 80-500 K as a function of carrier density and, by comparison with theoretical models, we uncover new transport physics at high electric fields. We examine device channel lengths from $L = 0.4$-$7 \, \mu$m and thicknesses $t_{ch} \approx 0.7$-$6 \, \text{nm}$. At a combination of low temperature and high carrier density, we observe negative differential conductance (NDC) at high field, i.e. the current reaches a peak and then decreases at higher voltages. This behavior is repeatable across multiple devices and sweep conditions. Comparison with our theoretical models suggests that NDC in 2D MoS$_2$ is caused by a combination of self-heating and complex band structure effects enabling transport through more than one conduction band.

The schematic of a typical measured device is shown in Fig. 5.1a, along with an SEM image in Fig. 5.1b. As described in Section 1.4, all devices here are based on MoS$_2$ flakes mechanically exfoliated onto $\sim$90 nm of SiO$_2$. Metal contacts consist of 35 nm thick Au electrodes. In order to remove residues potentially left over from processing and improve device behavior, we perform a post-fabrication anneal in vacuum ($\sim 10^{-5}$ Torr) at 300 °C for 1 hour and then allow devices to cool overnight. Figure 5.1c shows drain current ($I_D$) versus gate voltage ($V_G$) before and after a vacuum anneal. Additional characterization by AFM is shown in Figs. 5.1d,e.

5.2 Low-Field Mobility

Before exploring high lateral field transport, we carefully establish the low-field behavior of the devices of interest. Figure 5.2 shows the measured $I_D$ versus $V_G$ for a MoS$_2$ FET in vacuum at various $T_0$. As before with our studies of graphene, we use $T_0$ to denote background temperature, and $T$ for the higher device temperature during high-field operation. In the electron-accumulation regime ($I_D$ linear with $V_G$ and $V_G > V_T$, where $V_T$ is the threshold voltage estimated as shown in Fig. 5.1c) we observe decreasing $I_D$ as $T_0$ rises, consistent with stronger phonon scat-
tering. This point is further emphasized by the temperature dependence of the electron field-effect mobility ($\mu_{FE}$) shown in Fig. 5.3. Accounting for contact resistance $R_C$, $\mu_{FE} = g'_m L (WC_{ox} V_D)$ where $g'_m = dI_D/dV_G$ in the accumulation regime, $C_{ox} \approx 38 \text{ nF/cm}^2$ is the oxide capacitance, $V_D' = V_D - 2I_D R_C$, and $V_{GS} = V_G - V_S$ with the true source potential $V_S = I_D R_C$. The estimated $R_C W \approx 2.6 \text{ k}\Omega \cdot \mu\text{m}$ is based on device fitting with our simulations discussed below and is comparable to previous results for MoS$_2$ with Au contacts [168]. The error bars in Fig. 5.3 arise from uncertainty in $R_C$, consistent with measurements on multiple devices. At 80 K the contact resistance accounts for ~25% of the total device resistance, but this contribution decreases at higher temperatures (e.g., ~10% and <5% at 300 and 500 K, respectively) and high fields. Additional discussion of contact resistance is provided in Section 5.3.
The strong temperature dependence of mobility observed in Fig. 5.3, particularly above ~150 K, is caused by increased phonon scattering at higher temperatures. These observations are consistent with studies of bulk MoS$_2$ [164] and multilayer MoS$_2$ FETs of thickness about an order of magnitude greater than ours [22]. Fitting the extracted data against our Boltzmann transport equation (BTE) model described in Section 5.5, we can estimate the contributions to mobility from charged-impurity ($\mu_{\text{imp}}$), acoustic phonon ($\mu_{\text{AC}}$), and optical phonon ($\mu_{\text{OP}}$) scattering mechanisms. For our device of interest (blue circles and line in Fig. 5.3), $\mu_{\text{OP}}$ ($\sim T^{2.4}$) appears dominant near and above room temperature, although other samples may have a slightly different temperature dependence ostensibly due to different impurity or defect densities. We note that $\mu_{\text{OP}}$ includes analysis of both homopolar and polar optical phonons (HOP and POP). Below ~150 K the mobility peaks and becomes limited by charged-impurity scattering ($\mu_{\text{imp}} \sim T$) in this model and others [22].

**Figure 5.2:** Measured current $I_D$ vs. gate voltage $V_G$ for a MoS$_2$ device ($L = 1.5$ $\mu$m, $W = 1.3$ $\mu$m, $t_{\text{ch}} \approx 4$ nm, $V_D = 0.2$ V) at background temperatures $T_0 = 120$ K (blue, solid), 300 K (red, dashed), and 500 K (green, dotted). Data is shown for both log (left) and linear (right) axes.
The second set of experimental data (magenta squares) in Fig. 5.3 is from the device shown in Fig. 5.1b,d. We have already mentioned that for the first device the mobility falls as $\sim T^{-2.4}$ at high temperatures due to scattering with optical phonons (OPs), and similar to data for bulk MoS$_2$ [164]. However, for the second device we see a slightly weaker temperature dependence ($\sim T^{-1.6}$), similar to a previous result on monolayer MoS$_2$ [170]. Sample-to-sample variation is most likely the cause of this discrepancy, as varying crystal quality and processing residue have previously been shown to affect transport in 2D materials [130]. Specifically for MoS$_2$, defects in the crystal (e.g., sulfur vacancies [169, 171]) may play a role in affecting charge transport. Nonetheless, the stronger temperature dependence is consistent with measurements.
performed on bulk MoS$_2$ crystals, and thus have been correlated with the intrinsic phonon-limited properties of this material [164].

5.3 High-Field Negative Differential Conductance and Transistor $I$-$V$ Model

We now turn to high-field measurements of our MoS$_2$ devices. In Fig. 5.4a we show

**Figure 5.4:** Measurements and modeling of negative differential conductance (NDC) in MoS$_2$ transistors. (a) Measured $I_D/W$ vs. $V_D$ at ambient $T_0$ of 80 to 500 K from top to bottom and $V_{GT} = V_G - V_T \approx 30$ V (corresponding to electron density $\sim 7 \times 10^{12}$ cm$^{-2}$). Forward and reverse $I_D$-$V_D$ sweeps are plotted for all data sets (arrows indicate sweep direction), showing repeatability with minimal hysteresis. (b) Transistor model (dashed lines) using Eq. (5.3) shows good fit to the measured data [subset of data in (a) replotted as circles]. (c) Model (dashed lines) and measured data (circles) at $T_0 = 80$ K for varying overdrive $V_{GT} = 28, 23, 18$ V. Inset shows the average temperature rise of the MoS$_2$ channel due to self-heating $\Delta T$, calculated using Eq. (3) at $V_{GT} = 28$ V.
measured $I_D/W$ vs. $V_D$ also has a strong dependence on $T_0$ for the first device discussed in Fig. 5.3 (blue circles and lines). At $T_0 = 80$ K we obtain peak $I_D/W = 280 \mu$A/µm (at $V_D = 6$ V for our device $L = 1.5$ µm), while at 300 and 500 K the peak currents are 138 and 56 µA/µm (at $V_D = 9$ V), respectively. Interestingly, below 200 K we observe NDC at high bias, i.e. the current increases with drain voltage until it peaks, then decreases with further increasing voltage. The data in Fig. 5.4a show highly repeatable, forward and reverse $I_D$-$V_D$ sweeps (as indicated by arrows), eliminating hysteresis as a possible cause of the observed NDC. We ensured no sample degradation due to high-field stress by checking that low-field $I_D$-$V_G$ characteristics were reproducible after each high bias measurement.

In order to understand the intriguing NDC feature, we first set up a simple transistor model using a modified long-channel approximation [3]. Because the MoS$_2$ body is only a few layers thick ($t_{ch} < 6$ nm), we assume the entire body is in accumulation (i.e., electron-doped) for large $V_{GT}$. Note that we are only probing the accumulation regime in this work. This is the case because we are interested in high-field transport of MoS$_2$ when the channel is conductive and highly populated with electrons. For the device of interest, we choose a minimum $V_{GT} \approx 20$ V such that we operate in the accumulation regime and avoid pinch-off effects during high-field measurements. Most data in Fig. 5.4, is shown at $V_{GT} \approx 30$ V, where NDC is more apparent due to the high carrier density, $n \approx C_{ox}V_{GT}/q = 7 \times 10^{12}$ cm$^{-2}$.

The electron density in the channel is calculated as $n = t_{ch}N_D e^{\phi(x)/k_B T}$, where $N_D \approx 10^{16}$ cm$^{-3}$ is the intrinsic doping of the MoS$_2$ based on previous capacitance-voltage measurements [22] for MoS$_2$ flakes obtained from crystals from the same manufacturer (carrier density is dominated by the gate-induced accumulation layer so the estimate for the intrinsic doping is not important, i.e., $V_{GT} \gg q t_{ch}N_D/C_{ox}$ even for $N_D \approx 10^{18}$ cm$^{-3}$), $x$ is the direction along the channel.
with \( x = 0 \) and \( x = L \) being the positions of the source and drain edge, respectively, \( \psi(x) \) is the amount of band bending relative to the flat band condition \((V_{GS} = V_{FB})\), and \( V(x) \) is the drain-induced potential along the channel with \( V(x = L) - V(x = 0) = V_D - 2I_D R_C \). Equivalently, the electron density can be determined by \( n = C_{ox} [V_{GS} - V_{FB} - \psi(x)]/q + t_{ox} N_D \), where the oxide capacitance \( C_{ox} = \varepsilon_{ox}/t_{ox} \approx 38 \text{ nF/cm}^2 \) and \( V_{GS} = V_G - V_S \) with the source potential defined as \( V_S = I_D R_C \). Combining the two equations for carrier density above allows us to calculate

\[
V(x) = \psi(x) - \frac{k_B T}{q} \ln \left[ \frac{C_{ox} (V_{GS} - V_{FB} - \psi(x))}{q t_{ch} N_D} \right] + 1
\]  

(5.1)

where the drain current is defined by

\[
I_D = q \mu \frac{W}{L} \int_{\psi_s}^{\psi_D} n(x) \frac{dV}{d\psi} d\psi
\]

(5.2)

and \( dV/d\psi \) is found from Eq. (5.1). We can now obtain

\[
I_D = \mu \frac{W}{L} C_{ox} \left[ (V_{GS} - V_T) (\psi_D - \psi_S) - \frac{1}{2} (\psi_D^2 - \psi_S^2) \right]
\]

(5.3)

where \( \psi_D \) and \( \psi_S \) are the potential of the MoS\(_2\) channel at the drain and source, respectively, \( \mu = v_d(F)/F \) is the mobility accounting for electron drift velocity effects at high electric fields \( F \), and the threshold voltage is defined as \( V_T = -\left( \frac{k_B T}{q} + \frac{q t_{ch} N_D}{C_{ox}} V_{FB} \right) \). We note that the mobility \( \mu \) can be taken out of the integral in Eq. (5.2) because we assume an effective mobility for average gate and drain fields [3], such that \( v_d(F) \) is described by

\[
v_d(F) = \mu_{FE} F + v_{sat} \left( \frac{F}{F_C} \right)^\gamma
\]

(5.4)

where \( \mu_{FE} \) is the low-field mobility described above, \( v_{sat} \) is the saturation velocity discussed below, and \( \gamma = 2 \) and the critical field \( (F_C) \) are fitting parameters \( (F_C \text{ ranges from 3.2 to 20 V/\mu m}) \).
from $T_0 = 80$ to $500$ K) that provide reasonable agreement with the experimental data. The functional form of Eq. (5.4) is the same as that used for GaAs in [172], although here we use $\gamma = 2$ instead of $\gamma = 4$, which is representative of NDC in MoS$_2$ being less severe than in GaAs. We repeat that all measurements shown here are carried out in strong electron accumulation conditions ($V_{GT} > V_D > 0$, where $V_{GT} = V_G - V_T$ is the gate voltage overdrive) such that we do not reach pinch-off. Thus, the observed current saturation is associated with velocity saturation effects, not channel depletion near the drain.

Returning to Eq. (5.3), we are able to determine $\psi_D$ and $\psi_S$ in our simulations by equating

$$C_{ox} (V_{GS} - V_{FB} - \psi(x)) = q t_{ch} N_D \left[ e^{q(\psi(x) - V(x))/k_BT} - 1 \right]$$

with input parameters $V_G$ and $V_D$ and letting $V_{FB} \approx V_T$. We can assume $V_{FB} \approx V_T$ since $V_{GT} \gg q t_{ch} N_D / C_{ox}$, as mentioned above, and the thermal voltage $k_B T / q \ll V_{GS}$ (i.e., we are only concerned with $V_{FB}$ and $V_T$ relative to the gate voltage such that $V_{GT} \approx V_{GS} - V_{FB}$). Lastly, we emphasize that an iterative, self-consistent approach is used to incorporate contact resistance effects such that the potential drop across the channel, $V(x = L) - V(x = 0) = V_D - 2I_D R_C$, and the source potential, $V_S = I_D R_C$, are continuously updated for each bias condition until a stable solution is found. This iterative, self-consistent approach also applies to the thermal modeling and self-heating effects discussed later in Section 5.4. In Figs. 5.4b,c we show the results of the transistor model (dashed lines) that fit our measured data (symbols).

The lumped transistor $I$-$V$ model assumes a constant field in the channel, which is a valid assumption if the carrier density does not vary significantly from source to drain. Typically for high-field measurements the drain voltage is large enough to cause the carrier density near the drain to significantly decrease ($V_{GD} \ll V_{GT}$). However, as stated above $V_{GT} > V_D$ for all our measurements such that we do not reach pinch off. We further validate our constant field approx-
imation by comparing the simple transistor model to a self-consistent, electro-thermal MoS₂ simulator, which is based on a finite-element drift-diffusion (DD) approach adapted from our previous simulator used to model graphene [87]. The DD simulation calculates the voltage, field, electron density, and temperature at each point along the channel in the direction of current flow, while assuming the device is uniform in the width direction perpendicular to current flow. For the lumped transistor model, once we have already calculated \( I_D \) we are also able to estimate these properties along the channel by letting [3]

\[
I_p, x = q \mu W \int_{\psi_s}^{\psi_c} \frac{dV}{d\psi} d\psi.
\]  

(5.5)

Figure 5.5 shows good agreement between the two models and validates our use of a constant field in the transistor I-V model.

### 5.4 Thermal Modeling and Raman Thermometry

Next, we briefly discuss the thermal analysis of our MoS₂ devices. The \( I_D - V_D \) simulations described above were calculated self-consistently with a thermal model of the 2D devices. We estimate the temperature profile using the heat diffusion equation [82, 130]

\[
\frac{d^2 T}{dx^2} + \frac{p'}{\kappa W_{t, ch}} - \frac{g}{\kappa W_{t, ch}} (T - T_0) = 0
\]  

(5.6)

where \( T(x) \) is the temperature at position \( x \) along the channel, \( \kappa \approx 52 \text{ Wm}^{-1}\text{K}^{-1} \) is the in-plane thermal conductivity of few-layer MoS₂ [173], \( p' = I_D F(x) \) is the Joule heating rate per unit length, and \( g \approx 14.6 \text{ Wm}^{-1}\text{K}^{-1} \) is the thermal conductance to the substrate per unit length (estimated here using the thermal resistance model discussed in Section 3.4), at 300 K. The inset of Fig. 5.4c shows an example of the calculated average temperature rise (\( \Delta T \)) during high-field operation such that \( \Delta T > 100 \text{ K} \) for \( V_D > 7 \) in this case, at ambient \( T_0 = 80 \text{ K} \). Also, a temperature
Figure 5.5: Comparison between lumped transistor $I$-$V$ model (blue, dashed) and DD MoS$_2$ simulator (red, solid). Device dimensions are identical to the device of interest ($L = 1.5 \, \mu m$, $W = 1.3 \, \mu m$, $t_{ch} \approx 4 \, nm$) and calculations here correspond to $T_0 = 80 \, K$ and $V_{GT} = 28 \, V$. (a) Simulated $I_D$ vs. $V_D$ shows good agreement. At $V_D \approx 5 \, V$, we plot (b) channel potential $V(x)$, (c) electric field $F(x)$, (d) electron density $n(x)$, and (e) temperature $T(x)$. The blue dotted lines in (c) and (e) correspond to the average value along the channel calculated with the transistor model. Results show good agreement between both simulations and validate our use of a constant field in the transistor $I$-$V$ model.
profile \( T(x) \) is shown in Fig. 5.5e for a device at \( V_D \) 5 V. When evaluating Eq. (5.4) above we include the temperature dependence of \( \mu_{FE} \), which is shown in Fig. 5.3 and discussed previously. We also include the temperature dependence of saturation velocity as \( v_{sat} = v_0/(1 + N_{OP}) \) where \( v_0 = 2.2 \times 10^6 \) cm/s and \( N_{OP} = 1/[\exp(h \omega_{OP}/k_B T) - 1] \) is the OP occupation with \( h \omega_{OP} = 48 \) meV [174]. The factor of \( 1/(1 + N_{OP}) \) accounts for the decrease in \( v_{sat} \) at higher temperatures due to increased OP scattering, similar to previous models for graphene [32] and silicon [41].

Our study highlights the current dearth of knowledge with respect to MoS\(_2\) thermal properties, especially in-plane thermal conductivity \( \kappa \) for few-layer samples. Although in our work we have used the estimate for MoS\(_2\) thermal conductivity from [173], we note it is obtained from Raman studies of suspended few-layer MoS\(_2\) prepared using a high-temperature vapor-phase method. However, our transistor simulations are not very sensitive to the in-plane \( \kappa \) of MoS\(_2\), because most heat flows into the substrate for devices of dimensions employed in this work. This is also true for graphene devices with dimensions \( >0.3 \) \( \mu \)m [87] and even more applicable to MoS\(_2\) which has a significantly lower thermal conductivity than graphene. Additionally, we could not find measurements in the literature for MoS\(_2\)-SiO\(_2\) thermal boundary resistance (\( R_B \)), hence we used values determined for the graphene-SiO\(_2\) thermal coupling [112, 156].

Fortuitously, despite the lack of knowledge with respect to MoS\(_2\) thermal properties, we find that at all temperatures of interest \( \geq 90\% \) of the thermal conductance from the device into the substrate, \( g \approx 1/[L(R_B + R_{ox} + R_{Si})] \), is determined by the \( \sim 90 \) nm SiO\(_2\) thermal resistance. \( [R_{ox} = t_{ox}/(A\kappa_{ox}) \) where \( A = L \cdot W \) is the surface area of the channel and \( \kappa_{ox} \) is the thermal conductivity of SiO\(_2\)] and the Si substrate thermal resistance (\( R_{Si} \)) [32]. For example, at 300 K we find that \( R_B \approx 5 \times 10^3 \) K/W, \( R_{ox} \approx 4 \times 10^4 \) K/W, and \( R_{Si} \approx 4 \times 10^3 \) K/W, here for \( t_{ox} = 90 \) nm, and device area \( A = L \cdot W = 1.95 \) \( \mu \)m\(^2\) where \( L = 1.5 \) \( \mu \)m and \( W = 1.3 \) \( \mu \)m. Therefore, our thermal analysis
provides a good estimate for the temperature rise in the devices during operation. As described in Section 3.4, we also account for the temperature dependence of the thermal resistance through $\kappa_{\text{ox}}$ and $\kappa_{\text{Si}}$, where $\kappa_{\text{Si}}$ is the thermal conductivity of Si. For example, $g \approx 14.6 \text{ Wm}^{-1}\text{K}^{-1}$ at 300 K but decreases to $g \approx 7.9 \text{ Wm}^{-1}\text{K}^{-1}$ at 80 K (at 80 K, $g$ is 94% dominated by the underlying SiO$_2$ and Si thermal resistance). We note that the thermal resistance at the MoS$_2$-Au contacts, although not playing a significant role here, is accounted for by following the approach described in Section 4.4.

Before concluding our thermal analysis, we briefly describe a recent attempt to directly measure the temperature rise in a MoS$_2$ transistor due to self-heating at high-fields by employing the same Raman thermometry technique described in Section 4.5. The only difference here is that we use a 488 nm laser line instead of a 633 nm laser line and that we are able to make electrical measurements to the device while it is in a temperature-controlled stage at $5\times10^{-2}$ Torr. Figure 5.6a shows the temperature calibration of the A$_{1g}$ peak, resulting in $\chi_{A_{1g}} = -4.9\times10^{-3}$ cm$^{-1}$/K if we assume a linear relation [173]. Figure 5.6b shows the estimated temperature rise ($\Delta T$) in the device during electrical measurements at $T_0 = 80$ K. We compared the extracted $\Delta T$ from Raman thermometry (circles) to the calculated $\Delta T$ using our simple thermal resistance network (dashed lines). The calculations underestimate the extracted values when we use the same boundary thermal conductance value as for graphene-SiO$_2$, i.e., $h = 10^8$ Wm$^{-2}$K$^{-1}$, but show agreement when we let $h = 10^7$ Wm$^{-2}$K$^{-1}$. Lastly, we comment that the temperature sensitivity of the A$_{1g}$ Raman peak position here is relatively small (an order of magnitude less sensitive than that of the 2D Raman peak position in graphene) so further investigation is needed to clarify if the peak shifts during device operation are solely due to self-heating, and thus, whether or not they are accurate estimates of the lattice temperature rise in the MoS$_2$ channel.
5.5 Boltzmann Transport Equation Model

The temperature rise due to self-heating and its effect on electron transport help explain our observed NDC behavior. Similar effects have been observed in suspended carbon nanotubes, where NDC was attributed to strong self-heating and scattering of electrons by non-equilibrium OPs [126]. However, it is apparent that self-heating is a necessary but not sufficient condition for the measurable NDC in MoS$_2$. Equation (5.4) and BTE simulations below suggests that a negative differential velocity is also needed in order to fully reproduce the experimental data. To understand the physical cause of such drift velocity behavior, we perform numerical simulations using the BTE, summarized in Fig. 5.7. We calculate drift velocity as a function of field including self-heating, the scattering mechanisms described below, and a simplified two-valley band structure. We use the shifted Fermi-Dirac distribution function while balancing momentum and energy gained from the field with that released by scattering [175]:
\[
f = \left[ \exp \left( \frac{E_k - h k_x v_d - E_F}{k_B T_e} \right) + 1 \right]^{-1}
\]

(5.7)

\[ qnF = -\sum_k k S(f_k) \]

(5.8)

\[ qnF \cdot v_d = -\sum_k E_k S(f_k) \]

(5.9)

where \( E_k \) is the electron energy in the parabolic approximation, \( k_x \) the quasi-momentum in the direction of current flow, \( E_F \) the Fermi level, \( T_e \) the electron temperature, \( q \) the elementary charge, \( n \) the carrier density, \( k \) the full electron quasi-momentum, and \( S(f_k) \) the scattering integral. \( S(f_k) \) includes impurity scattering calculated with Thomas-Fermi screening theory [176]. AC phonons with deformation potentials 4.5 eV for the lower valley (LV) and 2.8 eV for the upper valley (UV) [91], HOPs with deformation potentials 8 eV/Å for intra-valley scattering in the LV and 14 eV/Å for intra-valley and inter-valley scattering in the UV, and POP scattering assuming Fröhlich deformation potential with dielectric constants \( \varepsilon_0 = 7.6 \) and \( \varepsilon_\infty = 7.3 \) [22]. Both HOP and POP energies are \( \hbar \omega_{OP} \approx 48 \text{ meV} \), as in the transistor model described earlier. The effective mass is assumed to be isotropic, \( m_{LV} = 0.45 m_0 \) in the 2-fold degenerate LV and \( m_{UV} = 0.7 m_0 \) in the 6-fold degenerate UV (\( m_0 \) is the bare electron mass), which is similar to theoretical first-principle calculations [90, 91]. The energy difference between valleys is a fitting parameter in our calculations \( (\Delta E = E_{UV} - E_{LV} \approx 130 \text{ meV}) \) and reasonable agreement could be obtained with slightly different \( \Delta E \), given a corresponding change in effective mass.

Figure 5.7a displays the calculated dependence of \( v_d \) on electric field (lines), comparing it to values extracted from the experimental data in Fig. 5.4 (symbols). The role of the UV is evaluated in Fig. 5.7b, where we see that both valleys and self-heating are needed to obtain notice-
negative differential velocity at $T_0 = 80$ K. We do not observe negative differential velocity for calculations without self-heating and calculations with only one valley. We have used a range of phonon deformation potentials and different relative positions of the UV and LV in our simulation ($\Delta E$), but we were unable to obtain a reasonable agreement with the experimental transport data without a 6-fold degenerate UV (with stronger scattering) above a 2-fold degenerate LV.
Thus, the lower and upper valleys of our model appear to correspond to the conduction band valleys in MoS$_2$ at the K and Q points, respectively [31, 91]. (The Q point is located approximately halfway along the $\Gamma$-K axis.) Although this relative valley positioning has been previously obtained in some theoretical work [93, 94], it is in contrast with other theoretical estimates [90, 92] predicting the 6-fold degenerate Q valley being lower for few-layer MoS$_2$. Figure 5.7c shows the representative two-valley band structure of our model as well as the distribution function for electrons in each valley, where in this case $F = 3 \text{ V}/\mu\text{m}$ and $T_0 = 80 \text{ K}$.

**5.6 Contact Resistance and High-Field NDC**

Before concluding our study, we discuss in more detail the role on contact resistance in our devices and provide additional data on high-field NDC in MoS$_2$. Figure 5.8a shows the measured low-field $I_D$ versus $V_D$ in the accumulation regime ($V_{GT} \approx 20 \text{ V}$) for the device of interest from above. At $V_D$ below a few hundred millivolts we see nonlinear behavior such that the resistance of the device is decreasing with increasing $V_D$. This nonlinear behavior is more pronounced below room temperature. We attribute the nonlinearity to small Schottky barriers at the metal-MoS$_2$ interface of the Au contacts. Assuming the contact resistance ($R_C$) at large $V_{GT}$ is dominated by thermally assisted tunneling (TAT) [177], increasing $V_D$ results in increased band bending at the contacts, and thus, increased TAT. Below room temperature higher $V_D$ is needed to increase the band bending and tunneling current until $I_D$-$V_D$ appears linear. Above room temperature the TAT is large enough to result in linear low-field $I_D$-$V_D$ behavior and Ohmic contact behavior. However, low-temperature measurements confirm the existence of a Schottky barrier for Au contacts to MoS$_2$, which is expected for n-type transport and high work function metals [178]. Also, it is appropriate to point out that when extracting mobility for Fig. 5.3, we use $V_D \leq 1$, i.e., sufficiently large $V_D$ for measurements below room temperature such that $I_D$-$V_D$ is in the
linear regime and the assumption of a constant contact resistance is more appropriate.

We note that although the TAT current increases with temperature, the resistance of the MoS$_2$ underneath the contact also increases with temperature due to a decreasing mobility. As the temperature increases, the former mechanism causes a decrease while the latter causes an increase in contact resistance, $R_C$. The simple transistor model used in this work assumes the temperature dependencies of these competing effects cancel out and lead to an approximately constant $R_C$, relatively independent of temperature which is in agreement with other recent observations [179]. Ongoing work in our group [180] is examining in more depth the different contributions to $R_C$ and their dependence on temperature and metal work function.

With respect to our high-field measurements, contacts are not playing a role in causing the observed NDC for several reasons. First, for all measured device channel lengths ($L = 0.4$-$7$ μm) the channel resistance at 80 K is two to more than 10 times larger than $R_C$ and dominates the

![Figure 5.8: (a) Low-field $I_D$ vs. $V_D$ ($V_{GT} \approx 20$ V) for a MoS$_2$ transistor ($L = 1.5$ μm, $W = 1.3$ μm, $t_{ch} \approx 4$ nm) at background temperatures $T_0 = 120$ (blue, solid), 300 (red, dashed), and 500 K (green, dotted). A Schottky barrier-like contact resistance is observed at low $V_D$ below room temperature. (b) Resistance at position of maximum drain current scaled with device width, $R_{peak}W$, vs. channel length $L$ for all devices measured in this work. The dependence of $R_{peak}W$ on $L$ indicates the device resistance is dominated by the MoS$_2$ channel, not the contacts, at high fields. Dashed line shows linear fit where the device with $L = 7$ μm has relatively low mobility and is treated as an outlier.](image)
total device resistance (see Fig. 5.7b). Second, as discussed above, we believe the resistance at the metal-MoS$_2$ interface to be determined by TAT current, and thus we expect more band bending at the contacts at higher fields to further decrease $R_C$. Third, $R_C$ has been found to decrease with increasing $V_{GT}$ [179, 180] (which renders the contacts more conductive) but our high-field $I_D$-$V_D$ measurements show NDC behavior (and thus a more resistive channel) only at high $V_{GT}$. Also, the electric field value where NDC starts (i.e., position of peak current) decreases with increasing $V_{GT}$ (see Fig. 5.4c). Lastly, a plot of device resistances (adjusted for width) at the maximum current position (i.e., current value at the onset of NDC) shows a clear length dependence in Fig. 5.8b. If contact resistance were dominant at high fields then we would expect little length dependence.

Figure 5.9 shows all devices measured at high fields and $T_0 = 80$ K ambient. Under these conditions, all electrical data showed repeatable NDC. As in Fig. 5.4, we show forward and reverse $I_D$-$V_D$ sweeps in order to highlight that hysteresis is negligible for most devices. Despite some sample-to-sample variation, current densities at high drain bias (and high $V_{GT}$) are comparable among our devices, with all FETs showing $I_D > 200 \mu$A/µm and a maximum measured value of $I_D = 291 \mu$A/µm (see Fig. 5.9d). The devices corresponding to Figs. 5.9h and 5.9i show relatively less pronounced NDC, which may be due to these samples having relatively larger channel areas ($LxW$). The larger area leads to improved heat dissipation to the substrate, which lowers the self-heating effect contribution to NDC.

We note that Fig. 5.9d is a monolayer MoS$_2$ device with Ni contacts, showing high-field NDC similar to that of the few-layer MoS$_2$ devices with Au contacts. Observing comparable NDC behavior for different contact metals provides additional support to our claim above that contacts do not play a role in causing NDC. A monolayer sample showing NDC could indicate
that the dominant mechanism causing NDC may be self-heating, which has little dependence on channel thickness here. Another possibility is the structure of the conduction band for monolayer MoS$_2$ being fairly similar to that of few-layer MoS$_2$. As stated above, more theoretical work may be needed to settle the high-energy band structure of single- to few-layer MoS$_2$.

Figure 5.9: (a-i) Measured current vs. drain voltage $V_D$ at $T_0 = 80$ K for nine different MoS$_2$ devices, ordered by increasing channel length, $L$ from 0.4 to 7 μm. All plots correspond to few-layer samples with Au contacts except for (d), which corresponds to a monolayer sample with Ni contacts. The gate overdrive voltages $V_{GT}$ correspond to the measurements from top to bottom, respectively. Both forward and reverse $I_D$-$V_D$ sweeps are plotted (arrows indicate sweep direction) but most devices show little to no hysteresis. We observe NDC in all devices, especially for large $V_{GT}$.
5.7 Conclusions

In conclusion, we experimentally and theoretically analyzed transport in MoS$_2$ over a wide range of temperatures (80-500 K) and up to high electric fields (6 V/μm). Low-field mobility shows a strong temperature dependence above room temperature due to scattering with OPs. High-field measurements reveal NDC below room temperature and usual velocity saturation at higher temperatures. We uncover that the NDC is due to a combination of self-heating and high-energy band structure effects in 2D MoS$_2$. Importantly, our results suggest that both the lower ($K$) and upper ($Q$) valleys play important roles in all common transport regimes, and must be carefully considered in MoS$_2$ transport problems. While our two-valley model is sufficient to explain the experimental transport data in MoS$_2$, future work remains needed in order to understand the high-energy band structure of other similar 2D materials.
CHAPTER 6: CONCLUSIONS AND FUTURE WORK

We have provided detailed studies of high-field transport in two-dimensional graphene and MoS$_2$ and investigated the energy dissipation mechanisms that limit transport, and ultimately, the current carrying ability of these materials. Substrate effects play a role in limiting transport in supported-graphene devices, and thus, choosing optimal substrates for ideal interfaces is an essential task for the future development of 2D nanoelectronics. Our study of suspended graphene allowed us to glimpse the intrinsic properties of graphene, but sample-to-sample variability associated with the challenging fabrication process complicated our analysis. Nevertheless, the “extreme” case of suspended graphene allowed us to observe coupled electrical and thermal transport at high-fields up to device breakdown.

The challenge posed by the absence of a band gap in graphene for future use in nanoelectronics, especially digital electronics, is great. Although it was not discussed here, we briefly comment on it now given that much of the motivation for studying MoS$_2$ relative to graphene is because MoS$_2$ has a band gap. Small band gaps can appear in graphene nanoribbons (GNRs) due to quantization of the width direction, but transport properties degrade due to edge roughness [181]. Analogously, Si bodies with thicknesses down to 2 nm have been reported [182] but rough interfaces cause their mobility to deteriorate and thickness fluctuations lead to unacceptable threshold-voltage variations.

Moving on to our study of electrical transport in 2D MoS$_2$ transistors, we find that few-layer MoS$_2$ has a mobility two orders of magnitude lower than that of graphene and its saturation velocity is almost an order of magnitude less than that of bulk Si. With respect to ultrathin Si, the transport properties of MoS$_2$ may be more comparable, but we emphasize that if future development of large-area growth techniques does not produce atomically-thin MoS$_2$ (or other TMD)
films with electronic properties better than those (at the present time) of exfoliated MoS$_2$ flakes, then TMDs like MoS$_2$ may only prove suitable for applications where device performance is not the top priority. One example of this is flexible electronics, where functionality may be sacrificed to achieve arbitrary form factors and make electronic devices available to a wider range of environments.

The observed phenomena of high-field negative differential conductance in few-layer MoS$_2$ may not be directly practical, considering the NDC is slight and only seen below room temperature. However, the analysis of our high-field electrical data allowed us to probe the high-energy band structure, revealing discrepancies among reported works and an unsettled picture of the MoS$_2$ band structure. A firm understanding of a material’s band structure is fundamental to semiconductor technology research, and as such, we hope our work motivates other researchers to investigate this matter further.

The issue of high-energy band structure becomes more important when we look into ultra-short channel devices and the possibility of quasi-ballistic transport, where detailed knowledge of the band structure is essential to properly understand device operation. If we take the time to further consider ultimate-scaled transistors and fundamental limits to device performance, research into 2D nanoelectronics must address the issue of large contact resistances. Although contact resistance was accounted for in all of our analysis here, we did not go into detail about the challenges of contacting a three-dimensional (3D) metal to a 2D transistor body. This may prove to be the most challenging problem when trying to scale down 2D transistors, and be the limiting factor in terms of current drive. Similar problems exist for designing contacts to ultrathin silicon [183].

To provide one last point, any near-future successful applications taking advantage of
graphene or MoS\(_2\) (or any other 2D material) will most likely exist because the application is novel, not just the material. Most of the work here (and in the 2D community in general) has been conducted with respect to how we traditionally study and investigate semiconductor technology. Replacing entrenched technology is difficult, and at times, not plausible. However, we hope that our specific work of improving the understanding of transport properties in these materials will not only advance us along the path to applicable traditional devices, but facilitate the development of unforeseen 2D-based structures. Scaling down the transistor has propelled semiconductor technology for decades, and as the continuation of scaling becomes increasingly more challenging and uncertain, many look to find new ways to achieve the same performance benefits offered by scaling (either by using a new material or a new device structure). However, finding innovative and original uses for IC technology, not just ways to improve existing IC technology, may prove equally necessary for the continued growth of the semiconductor industry.
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