NON-LITHOGRAPHIC MANUFACTURING OF 1-D SILICON NANOSTRUCTURES WITH TUNABLE SURFACE MORPHOLOGY VIA THERMAL DEWETTING AND METAL-ASSISTED CHEMICAL ETCHING

BY

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THESIS

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Abstract

This thesis presents a non-lithographic approach to generate wafer-scale single crystal silicon nanowires (SiNWs) with controlled side-wall profile and surface morphology. The approach begins with silver (Ag) thin-film thermal dewetting, gold (Au) deposition and lift-off to generate a large-scale Au mesh on Si substrates. Followed by metal-assisted chemical etching (MacEtch), where the Au mesh serves as catalyst, arrays of smooth Si nanowires with tunable taper are produced. By using the Le Chatelier Principle, the rate of reduction relative to that of oxidation is increased by adding increasing amounts of ethanol to the etchant. Consequently, excess electron holes migrate and diffuse away from the catalyst-silicon interface and towards the wire surface, making the wire surface susceptible to lateral etching as well. The ratio between the vertical and lateral etch rates can be tuned to produce wires with taper angle up to 13 degrees. The mean diameter of so fabricated SiNWs can be controlled to range from 62 nm to 300 nm with standard deviations as small as 13.6 nm, and the areal coverage of the wire arrays can be up to 46%. Control of the mean wire diameter is achieved by controlling the pore diameter of the metallic mesh which is, in turn, controlled by adjusting the initial thin-film thickness and deposition rate. To control wire surface morphology, a post-fabrication roughening step is added to the approach. This step uses Au nanoparticles and slow-rate MacEtch to produce rms surface roughness up to 3.6 nm. Additionally, 1-D nanostructures with complex cross-section shapes – such as I-beams, tubes, multiwalled concentric tubes – are demonstrated by replacing the self-assembled thermally dewetted patterns in the manufacturing approach described above. Instead, silver patterns are created by Solid-State Superionic Stamping (S4), a non-lithographic and ambient method for patterning silver thin-films, and combined with the lift-off and MacEtch processes to
produce such complex nanostructures. Sub-160 nm nanostructures were produced by this approach with high pattern fidelity over millimeter scale silicon substrates.
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1 Introduction

Today, nanomanufacturing research and development address the challenge of accurately and precisely shaping, tailoring, integrating and functionalizing 3-D nanomaterials at large-scales to deliver solutions for the pharmaceutical, space, defense, computing and related industries. Since the inception of the Silicon Valley, applications of nanotechnology expanded beyond transistor physics and away from traditional materials. To enable the industrial application of novel nanomaterials - such as quantum dots (QD), carbon nanotubes, graphene, silicon nanowires, and etc - novel manufacturing processes have been developed with the aim of economically fabricating large volumes of bulk material. To integrate such nanomaterials together with existing technologies, the concept of heterogeneous integration was then developed and implemented to combine a large variety of material classes such polymers, biomaterials, semiconductors, metals, and ceramics into functional devices. Transfer-printing, ink-jetting, and contact transfer printing are some of the recently developed manufacturing technologies that enable heterogeneous integration of nanomaterials.

A successful example of heterogeneous integration appears in the fabrication of quantum dots and its assembly in foreign substrates such as biological and inorganic materials. QD can be manufactured in a variety of ways such as colloidal chemical synthesis, lithographical methods, and molecular seeding. While lithographical methods can fabricate quantum dots embedded into
semiconducting devices, the sub 50 nm resolution needed to make QD requires the use of expensive lithographical tools not scalable to the demands and low-costs imposed by the display and electronics industry. Large scale synthesis in colloidal form provides a non-lithographic and self-assembly route for economically manufacturing large volumes of QD. Additionally, the assembly and dispensing of QD from colloidal suspensions into thin-films is a fundamental step in its integration to foreign substrates. Recent commercial use of QD appear in QD solar cells for photovoltaic applications, QD light emitting diodes for display technologies (see Figure 1a) [1], and QD photodetectors for bioimaging applications. QD are also proposed as qubits for quantum information processing and manufacturing and operation of such technology remains a topic open for research. Other examples of nanomaterials suitable for scalable integration with foreign substrates are carbon nanotubes (CNTs). CNTs benefit from high current carrying capabilities, high strength, high thermal conductivities and semiconducting properties. CNTs are primarily manufactured by chemical vapour deposition (CVD) and dispensed or spun onto foreign substrates from a solution made of suspended CNTs. Alternative methods for yarn and sheet production have shown great promise for finding use in scaled-up applications [2]. Currently, CNTs find a growing range of commercial applications such as light-weight structural composites, anti-fouling painting products, electrical interconnects, flexible transistors (see Figure 1b), and spacecraft shielding.
Figure 1: Examples of heterogeneous integration. (a) Display image of a 46 inch LCD TV panel and a quarter of the white QD-LED backlights (inset), adapted with permission from literature [1]. Copyright (2010) Advanced Materials. (b) Flexible TFTs using CNT networks deposited by aerosol CVD, adapted with permission from literature [2]. Copyright (2013) Science. (c) Passive matrix, stretchable ILED display that uses a noncoplanar mesh configuration, on a rubber substrate. Here, interconnect lines between adjacent devices are supported by arc-shaped bridge structures that can deform in response to applied strain. Both the main panel and the inset images were collected with an automated camera system that combines pictures captured at different focal depths to provide a sharp, composite image, adapted with permission from literature [3]. Copyright (2009) Science.
1.1 Background and Motivation

Like QD and CNTs, silicon nanowires have many unique benefits and they find strong applications in solar cells, biosensors, high-emissivity surfaces and, more recently, thermoelectric devices. In particular, this thesis is motivated by the two latter applications discussed below.

In one case, a thermoelectric π-junction (Figure 2a) uses thermal gradients to move electrons and electron-holes in a p-type and n-type semiconductor material, respectively and can create electricity for energy applications. The efficiency of such processes is dictated by the thermoelectric figure of merit (ZT) and tellurium compounds - which are scarce in nature and often forms toxic compounds – have unit ZT value at room temperature. The price of Tellurium (Te) in 2000 was 3.28 USD per pound and, in 2011, its price peaked at around 150 USD per pound [4] due to increasing use of Te in the photovoltaic and semiconductor industry. At room temperature, bulk electronic grade silicon – whose price is approximately 5 USD per pound - has a ZT value in the order of 0.01. However, in 2008, researchers found that silicon nanostructures exhibit two orders of magnitude lower thermal conductivity [5] which would imply that the ZT value is much improved. This result sparked a plethora of studies to understand the mechanisms behind such phenomena and to ultimately attempt to create a nanostructured thermoelectric material with unity-ZT coefficient [6, 7, 8]. In fact, it was found that, as the diameter of SiNWs decreases and its surface roughness increases, lower thermal conductivity is achieved at room temperature. This is due to the confinement and boundary scattering of phonons traveling in the
SiNWs (Figure 2b) [5]. Thus, the possibility of replacing tellurium-based thermoelectric devices with nanostructured silicon represents an opportunity to economically harvest waste-heat at large scales. On Figure 2c, a conceptual design of a flexible nanostructured silicon thermoelectric device is depicted whose heterogeneous integration onto flexible substrates is proposed via transfer-printing technologies. Such assembly could be wrapped around a heat source, such as a car exhaust (hot side) and air (cold side) to generate electricity.

\[ n = n_{\text{carnot}} \times \frac{\sqrt{1 + ZT} - 1}{\sqrt{1 + ZT} + \frac{T_C}{T_H}} \]

Figure 2: Realizing cheap flexible thermoelectric devices based on SiNWs. (a) diagram of \( \pi \)-junction and equation of theoretical thermoelectric device efficiency based on Carnot efficiency and the thermoelectric figure of merit (ZT), (b) illustration of phonon nanoscale interactions with rough boundaries (courtesy of Dr. Sanjiv Sinha) and (c) conceptual design of a SiNW thermoelectric \( \pi \)-junction constructed onto a flexible heterogeneous plastic substrate with integrated top and bottom electrical contacts (courtesy of Dr. Sanjiv Sinha).
Aside from nanostructured SiNWs thermoelectric devices [9], the optical properties of a SiNW forest are also remarkable. High-aspect ratio, tapered SiNWs [10] allow for near broadband black-body behavior due to the smooth transition in the refractive index between air and silicon and photon trapping, biomimicking the anti-reflective texturing of a moth’s eye. Best reported metrics for the reflectivity of SiNW forests are sub-0.8% in the visible (300-1 µm), sub-1% in the near infrared (1-20 µm) and sub-30% in the far infra-red range (20-200 µm) [10]. Such surfaces find strong applications in the baffles of space telescope, significantly reducing the negative effects of stray light. The reported metrics over the entire electromagnetic range beats most, if not all, state-of-the-art high-emissivity coatings for space telescopes, justifying the pursuit of such nanomaterial.

The use of conventional semiconductor manufacturing methods represents one possible route to produce SiNWs, using tools such as high-resolution e-beam lithography, selective ion-implantation, and deep-reactive ion etching. These tools produce silicon nanowires (SiNWs) on a SOI wafer, selectively dope them, and make top and bottom electrical contacts of the π-junction (Figure 2a) [11]. However, this route hinders the applicability of silicon-based thermoelectrics to large-scale devices due to its large cost. Alternatively, self-assembled patterning, and catalyst-based semiconductor growth or wet etching have been proposed as a manufacturing route due to its high-resolution, high aspect ratio and avoidance of expensive lithographic processes. Substantial work has gone into improving the resolution [12] and aspect ratio [13], and to controlling geometry [14] and morphology [15] of these 1-D semiconductor nanostructures.
1.2 Scope of Research

This thesis highlights the progress made to develop a large scale, self-assembled, non-lithographic manufacturing process for silicon-based thermoelectric devices and anti-reflective surfaces that are environmentally benign, cost-effective, scalable and meet or beat the efficiency of state-of-art devices. Here are some of the requirements of the manufacturing process:

• Create a process flow that is capable of large-area fabrication of SiNWs. The approach is to be free of photolithography and must not require a cleanroom environment

• As a general requirement, the process must be scalable, reproducible in large-areas (greater than 3 inches in sample size)

• Production of SiNWs arrays with sub-100 nm diameter for thermoelectric devices and sub-300 nm diameter for high-emissivity surfaces

• Rough SiNWs surfaces with controllable RMS roughness in the range of 1-4 nm

• Areal coverage of active material (SiNWs) greater than 40%

• Aspect ratio of active material greater than 10

• Defect-free SiNWs (e.g. no twinning, porosity, or other crystallographic defects)

• Tunable taper angle (smaller than 15°) with diameter in the range of 200-300 nm and high areal coverage (greater than 30%)
In light of such requirements, the primary goal of this research is to devise a manufacturing strategy that could deliver all desirable metrics. The first proposed process flow is called “SiNW production via thermal dewetting and Metal-assisted chemical etching”. This approach is described as follows. It begins with silver (Ag) thin-film thermal dewetting in which a sub-15nm layer of evaporated silver film is heated to induce dewetting of silver onto a silicon substrate. Then, gold (Au) is deposited over the silver nanoparticles and the particles are removed by a metal lift-off technique to generate a large-scale Au mesh on Si substrates. Followed by metal-assisted chemical etching (MacEtch), where the Au mesh serves as catalyst, arrays of smooth Si nanowires are produced. The subsequent task was to show that this process combination can controllably deliver the wire diameter, areal coverage, roughness, taper, aspect ratio and defect level required by the applications.

1.3 Thesis Outline

This thesis shows the integration of two unique manufacturing processes that together may be applied to fabricate near end-use devices for two specific applications: SiNW-based thermoelectric energy harvesterst and high-emissivity surfaces for anti-reflection. Firstly, the literature review (Chapter 2) is organized to present a formal and detailed review of existing manufacturing methods for silicon nanowire production, including planar self-assembly methods, and top-down and bottom-up approaches.
Secondly, Chapter 3 presents the details of the integration of thin-film metal dewetting and metal-assisted chemical etching used to obtain silicon nanowires with prescribed metrics within the target values. Further, it discusses how to utilize metal-assisted chemical etching to modulate the roughness and taper angle of SiNWs and provides the characterization of the average root-mean-square height variations along the rough wire surface via image analysis of transmission electron microscopy data and the anti-reflective properties of tapered structures. Much work has gone into process improvement to achieve smaller wires with higher areal coverage. Graph 1 depicts the time-evolution of key process targets – diameter and areal coverage - that resulted in the achievement of sub-70 nm nanoparticles with areal-coverage greater than 45 % during this project.

Graph 1: Time-evolution of process target parameters: diameter and areal coverage. The graph highlights the difficulty in translating the self-assembled patterns ever smaller in diameter into silicon nanowires due to limitations on the process and its conditions. Time is plotted on the x-axis as a function of the quarters of a year. The blue curve shows the minimal silver nanoparticle size that could be obtained with the dewetting approach while the red curve shows the minimal wire diameter produced after improved lift-off strategies were implemented.
Finally, in chapter 4, a similar and alternative approach for patterning silicon nanowires, nanobeams, and nanotubes with prescribed dimensions is introduced. Instead of using Ag dewetting patterns, this approach uses a non-lithographical approach, called the Solid-State Superionic Stamping (S4), to pattern silver domains on a silicon wafer. It provides greater versatility to create 1-D structures with complex cross-section shapes. Since the S4 method is most suitable for patterning Ag films, it is integrated with the lift-off method to produce an Au pattern on a silicon substrate and etched in MacEtch. This approach represents an advance of the integration of S4 and MacEtch, since gold is a better and more reliable catalyst than silver for the MacEtch process.
2 Literature Review

In every silicon nanowire production process flow, three building blocks are present (see Diagram 1). Firstly, a 2-D template is created to define the location, spacing and dimension of SiNWs. Subsequently, the template assists or participates in an out-of-plane growth or etching process, giving SiNWs a prescribed height or depth, respectively. Finally, the last step is to functionalize its surface according to the desired application. This chapter is structured to provide an overview of the etching and growth methods for SiNWs and the techniques for creating 2-D templates. The functionalization approaches (most of which are chemical treatments used in biosensing applications) abound in the literature and are irrelevant for the discussion presented in this thesis and will not be reviewed.
2.1 Unconventional Bottom-up and Top-down Approaches

The most common etching and growth techniques that have been used to produce 1-D silicon nanostructures includes: deep reactive ion etch (DRIE), vapor-liquid-solid (VLS) growth [16, 17], and metal-assisted chemical etching (MacEtch) [18] in order of decreasing maturity. DRIE was developed in the 1990’s to serve the microelectronics industry’s need for high-aspect ratio structures with fast etching rates and has remained the industry standard since then. VLS growth was invented in the 1960’s and it did not receive much attention at the time. It reemerged in 1990’s as a method for making silicon nanowires [19]. Today, VLS is still not commercially used.
due to slow and size-dependent growth rates, and little control over growth direction. In 2000, MacEtch emerged out of a ground-breaking work of Professors Xiuling Li and Paul Bohn. It has received much attention due to its ability to create silicon features with sub-5 nm resolution [20], and aspect-ratios greater than 100. Over the last decade, MacEtch literature has matured but it has yet to see a commercial application. The following section discusses the advancements made in the last decade on this later technique.

2.1.1 Metal-Assisted Chemical Etching

Metal-assisted chemical etching (MacEtch) is a process in which a mixture of HF and an oxidant (typically H$_2$O$_2$) is used to etch a semiconductor such as Si in the presence of metal [21]. The process works by injecting a hole into the semiconductor from the reduction of an oxidant at the metal-solution interface. Then, the availability of holes in the vicinity of the semiconductor-metal interface triggers a reaction between surface silicon atoms and hydrofluoric acid through one of the proposed mechanisms in literature [22]. In the case of hydrogen peroxide as oxidant, the most accepted mechanism in literature is the reduction of hydrogen peroxide into water and an electron-hole followed by its injection into the valance band of silicon. Subsequently, electron-holes are consumed in the dissolution of silicon by hydrofluoric acid transforming silicon into a water-soluble product called hexafluorosilic acid ($\text{H}_2\text{SiF}_6$). The reactions steps are shown below:
\[ H_2O_2 + 2H^+ \rightarrow 2H_2O + 2h^+ \]

\[ Si + 4h^+ + 4HF \rightarrow SiF_4 + 4H^+ \]

\[ SiF_4 + 2HF \rightarrow H_2SiF_6 \]

The balance between hole injection and consumption maintains holes localized at the metal-substrate interface and, consequently, directional etching is achieved with non-porous single crystalline features being generated. When deployed in SiNW fabrication, MacEtch produces nanowires with aspect ratios greater than 100 [13], provided the diffusion of reactants and products to and from the reaction zone is abundant. For this reason, MacEtch has been widely used for generating dense and vertically aligned nanowires for integration with planar manufacturing processes [23].

In regards to porosity control of SiNWs, MacEtch has been demonstrated to produce solid or porous features by controlling the ratio of the oxidizer concentration to that of HF [15] and by changing the catalyst metal [24]. Previous work [25], reproduced on Figure 3a, demonstrates that the etch rate peaks when the value of a parameter \( \rho \), defined as a molar ratio, is in the range 70-80\%, where:

\[ \rho = \frac{[HF]}{[HF]+[oxidizer]} \]
In this range, the rate of reduction of hydrogen peroxide is stoichiometrically balanced to the rate of oxidation of silicon underneath the catalyst. Increased oxidizing activity produces excess holes which are injected into Si and transported to the SiNW boundary. The presence of holes at the SiNW surface as it is formed makes it susceptible to chemical dissolution by HF and causes roughening of the surface of the nanowire followed by the growth of a porous layer on the shell of the nanowire that progresses toward its core as the etches progresses in time (see Figure 2b and 2c).

The rate-limiting mechanism for the dissolution of silicon is the diffusion of either reactants or products towards or away from the metal-semiconductor interface, respectively. Dr. Nadine Geyer and collaborators working at the Max Plank Institute proposed and verified a diffusion model in which the pathway for reactants and products takes place around the edges of the catalyst layer (Model II in Figure 3) and not through it as previously proposed in literature (Model I in Figure 3). Furthermore, it was verified that MacEtch works by first creating a thin Si porous layer under the catalyst until it reaches a uniform and stable porous thickness that allows for the diffusion of reactants and products as the etching progresses in time. When the feature size of the catalyst layer is in the order of sub-500 nm, the diffusion lengths are small and the thickness of this porous layer is thin to the point that it is hard to observe it in the silicon nanowire samples produced in this thesis. However, in theory, it exists and is fundamental for the progress of the etching. Another consequence of this model is that the rate of oxidation of silicon at the vicinity of the metal-semiconductor junction is dependent on the length that ions have to diffuse through
and, consequently, dependent upon the feature size. Thus, when implementing metal-assisted chemical etching, one should never take the solution parameter $\rho$ reported elsewhere and assume it is universal and will yield equal morphological results for all catalyst geometries. Instead, one should choose a parameter near and above the value corresponding to the peak in etch rate. Porous layers under the catalyst may grow as large as several microns before it reaches a steady state thickness for the case of features sizes greater than one micron, approximately.

![Figure 3. Scheme of possible diffusion processes of the reactants and reaction products during metal-assisted chemical etching. (a) Model I: Diffusion of reactants and reaction products through a porous thin metal film. (b) Model II: The oxidation of the Si surface proceeds at the interface of the metal and the Si substrate by forming a porous silicon layer. Through the porous layer, the HF can diffuse to the bulk Si to facilitate the dissolution. The reactants and the byproducts diffuse as well through the porous layer. Adapted with permission from literature [22]. Copyright (2012) American Chemical Society.](image)

In regards to morphology control of SiNWs, MacEtch can achieve some roughness control of its sidewall profile by decreasing the parameter $\rho$ or, similarly, adding more hydrogen peroxide. Our previous work [15] shows that RMS roughness can be controlled only in the 0.5-2 nm range. Beyond 2 nm, the wire roughening becomes so aggressive that it results in the formation of
porous SiNWs, significantly reducing their electrical conductivity. The same mechanism for roughness generation can also be used for tuning the taper of its sidewall feature. For instance, further increasing the oxidizing activity accelerates the side-wall porous formation and its subsequent dissolution in HF, resulting in a tapered external profile [25] (see Figure 2d). This approach, unfortunately, also causes the core of the SiNW to be porous for most levels of useful roughening and tapering.

Figure 4: (a) the etch rate of Macetch is characterized as a function of the etch parameter ($\rho$) and as a function of water molarity for a catalyst mesh with areal coverage of 22% and average hole diameter of 120nm. These results are partially reproduced from literature [25]. In figures (b) and (c), the sidewall morphology of the tips of silicon nanowires portrayed by SEM images are smooth and rough according to the etch parameter chosen: 75 and 65, respectively [15]. An evident taper (d) is observed at etch parameter typically in the range of 55 and below.
2.2 SiNW Production: Unconventional Non-Lithographical Methods (by process)

A template is first defined to mask or catalyze the growth or etching of silicon nanowires. This section discusses five non-lithographical methods to produce such templates and how they have been integrated with growth and etching methods to produce silicon nanowires.

2.2.1 Template-Free Direct Method Using Deep-reactive Ion Etch (DRIE)

A direct example of forming a forest of 1-D silicon nanotips was first investigated by Jansen et al., using reactive ion etching (RIE) on a Silicon wafer. The redeposition of polymer masks and adsorption of silicon dioxide particles during the etching step in RIE create micromasks that protect the substrate to form silicon tips (also known as micrograss). The taper profile of these structures was controlled by adjusting pressure, flow of reactive gases, and power of the RIE process [26]. In a single-step, this process can both (1) create the mask for nucleating the tips, and (2) etch the substrate, creating high-aspect ratio, tapered, and dense arrays of nanotips. More recently, other plasma etching techniques have been developed to yield more robust results for controlling the taper and creating self-masks with higher densities such as pulsed-mode DRIE [27] and electron cyclotron resonance plasma etching [10], respectively. While these approaches are economical and yield samples with low reflectivity in the visible and near-IR
range, little work has been done to independently adjust the taper and the density of self-masked patterns which may allow for further reduction in reflectivity.

### 2.2.2 Nanoparticle Dip Coating Assembly

A typical indirect example is dip coating with a monolayer of silica beads [28] uses the Langmuir-Blodgett assembly method [29, 30] to produce a close-packed layer of beads over large areas [31, 14]. This step is followed by an isotropic RIE step to separate and shrink the beads starting from a 200-600 nm diameter [14]. Used as a mask over which a thin metal film is deposited, a metallic mesh with monodispersed pores is produced by the removal or lift-off of the beads. This, in turn, is used as catalyst by the MacEtch process to produce SiNW arrays [30]. As-fabricated wires can be shrunk to 60-120 nm by a thermal oxide growth and removed by etching in hydrofluoric acid. However, this approach suffers from the drawback of producing SiNW forests with low areal coverage, detrimental for system-level efficiency of several of the applications previously discussed.

### 2.2.3 Anodized Aluminum Oxide

Porous anodized aluminum oxide (AAO) [32] with monodispersed pores has also been used for producing SiNWs with the advantage of having highly tunable diameter control in the sub-200nm
range. AAO is grown on a bulk aluminum foil [33, 34] or thin-film [35] by a two-step anodization with the pore depth and size controlled by the anodization time and the pore opening step. Multiple approaches [14, 35, 33] may be used to open up the bottoms of the pores so that the membrane can be used as a template. The AAO membrane is manually transferred to the silicon substrate with the use of a polymeric film as a handle after the Al substrate is etched away [33]. The polymer handle is then removed by dissolving in a solvent. Finally, the closed ends of the AAO pores are opened using an isotropic AAO etchant. AAO membranes – transferred via this method - are covered with an Au film and immersed in MacEtch solution to produce SiNWs. Even though this process integration has been shown to produce SiNWs arrays, the areal coverage of SiNWs produced by this method is limited by the template wall thickness and pore closure effects [33, 34]. Also, the process requires a number of delicate manual steps in the transfer of the template, thus limiting the size of the patterned surface and the yield.

2.2.4 Solid State Superionic Stamping and Metal-Assisted Chemical Etching

A more versatile approach to manufacturing a metal template with a non-photolithographic approach is to use Solid State Superionic Stamping (S4). Solid state superionic stamping (S4) is a non-photolithographic process that electrochemically dissolves silver thin films into silver ions in the contact areas between an ionic conductive stamp and a metal substrate (Figure 5). Metal ions are transported into the solid electrolyte stamp by an applied bias and reduce on the back of the
This stamp-based approach can produce sub-100 nm Ag features at high-throughput rates [36].

Figure 5: Schematic of solid state superionic stamping process. Left: A patterned stamp of superionic conductor—of M⁺ ions—is pressed against a film of metal M. Center: A small applied voltage anodically dissolves metal in contact with stamp; M⁺ ions are absorbed into the electrolyte. Right: Removal of metal continues eventually reproducing the relief patterns from the stamp in the remaining metal (courtesy of Kyle Jacobs) [36, 37].

Since, metal-assisted chemical etching widely uses silver as a catalyst, S4 can be easily integrated with this approach to produce silicon nanowires with sub-150 nm features. Silver features are produced by S4 on a silver thin film deposited onto a silicon wafer and, subsequently etched in metal-assisted chemical etching [24] (Figure 6). However, control over the etching direction and porosity during MacEtch with silver has been an issue due to silver dissolution into ionic form and its redeposition, and the absence of a method to predict or suppress this phenomena.
2.2.5 Metal Nanoparticle Formation: Thin-film Dewetting

Thin-film dewetting is a scalable and robust process for creating self-assembled monolayers of metal nanoparticles in the 10-500 nm size range on oxide surfaces [15, 38]. A metallic thin-film is first deposited on the substrate. This is followed by a thermal annealing step that activates thermal grooving in the thin film and results in the formation of individual nanoparticles. Unlike approaches that use AAO templates or dip-coating and are capable of producing monodispersed metal particles for MacEtch, this process inherently creates particles with a size distribution with standard deviations starting at 5 nm for sub-20 nm particles and growing up to 40 nm for 150 nm particles. The dewetting behavior has been shown to spontaneously occur for metals such as Ag.
[38], Co [39], Ni [40, 41], Cu [42], Au [43] and Pt [44]. The annealing temperature to cause
dewetting is usually less than a third of the metal’s bulk melting temperature. Accelerated
diffusion of impurities into semiconductors at elevated temperatures limits the use of high-
melting point metals. Low-temperature options include Ag, Au, Co, and Ni which typically exhibit
the dewetting behavior around 300 °C and below 600 °C.
3 Silicon Nanowire Production Via Thin-film Metal Dewetting and Metal-assisted Chemical Etching

In this chapter, a fabrication scheme for obtaining SiNW arrays with controlled sidewall morphology, size distribution and density is reported. Our approach combines the thermal dewetting process with MacEtch through image reversal by a lift-off process that converts Ag particle patterns into an Au mesh pattern. By fine control of the deposition rate and thickness of the evaporated Ag film that is dewetting into Ag nanoparticles, SiNW arrays with average diameter as small as 61nm with a standard deviation of 13 nm are produced. Further, it is shown that, by altering the chemical composition of the MacEtch solution, tapered wires are also produced with application to broadband anti-reflection surfaces. This chapter also develops an approach to produce SiNWs with surface roughness fine-tuned in the 0.5-3.5 nm range consistently across the wire length. To accomplish this, an additional post-roughening step is used. As-formed SiNWs are coated with Au nanoparticles via sputtering and etched by MacEtch again. Au nanoparticles etch toward the core of SiNWs. Roughness control is obtained by controlling the etching time. After roughening, the SiNW surface develops a native oxide and the Si/SiO₂ interface roughness is characterized by TEM. This work may enable a deeper understanding of the relationship between roughness and thermal conductivity of SiNWs, and can potentially be implemented in large-scale manufacturing of SiNW thermoelectric devices. It also provides an affordable and scalable pathway to manufacturing large-area, high-emissivity surfaces for stray light reduction in telescopes.
3.1 Experimental Method

Two sets of samples were manufactured for the purpose of investigating the roughness dependence on MacEtch parameters and the broadband anti-reflective properties of tapered SiNWs. The first set was comprised of smooth SiNWs with average diameter in the 110-140 nm range that were roughened to various levels and analyzed under TEM. The second set is comprised of as-doped and post-doped tapered SiNWs with average diameter around 300 nm.

3.1.1 Particle Size Control via Dewetting Parameters

The process begins by growing a 15nm oxide layer on degreased and RCA-1 cleaned (100) Si wafers (1-10 ohm.cm) in a Lindberg Hevi-Duty Lancer M-300 Tube Furnace at 1000 °C for 13 min with a 4 sccm pure oxygen flow rate. Subsequently, silver deposition was performed in a Temescal E-Beam Evaporation System with thickness and deposition rate monitored by a quartz crystal monitor (Figure 7a: step 1). Silver films are then annealed at 350 °C in rapid thermal annealing chamber that focuses an infrared light source on the sample (model SSA-P610C, manufactured by ULVAC-RIKO, Inc) for 4 hours at 3-8×10⁻⁷ torr (Figure 7a: step 2); at the end of this step, the Ag film is fully dewetted into isolated particles (Figure 7b). For sub-100 nm particles, we used scanning electron microscopy (SEM) to characterize the particle size distribution as a function of the deposition thickness at a deposition rate as low as 0.1 Å/s. The SEM data is analyzed with ImageJ (see supplementary figure 1) and results for the average particle diameter
and areal coverage are shown in Figure 9 as a function of the deposition parameters. Parameters for the 100-400 nm particle size range were reproduced from previous studies [38].
Figure 7: (a) Fabrication overview: silver films are evaporated onto a clean 15 nm thick thermally grown SiO$_2$ surface at controlled deposition rate and thickness (step 1) (b), thin-films are annealed in vacuum breaking into individual particles (step 2), sub-120 nm Ag particles are undercut with BOE to increase its height and facilitate lift-off (step 3) (c), thin Au catalyst layer is evaporated (step 4), Ag nanoparticles are etched away at room temperature with silver etchant solution (step 5), MacEtch at different ethanol concentrations produce straight and tapered SiNWs (step 6) (d), and Au nanoparticles are sputtered (step 7) and etched in diluted MacEtch solution to generate surface roughness (step 8) (e).
Samples are immersed in a buffered oxide etch (HF:NH₄F = 6:1; v:v) for 20 seconds in an ice bath with temperature kept at 0 °C with constant agitation (Figure 7a: step 3). This step undercuts the oxide film under the silver particles and facilitates the subsequent lift-off process (Figure 7c). As observed from cross-section SEM images, the undercut depth was controlled with etching time (Figure 8). Theoretically, 1% HF could also be used to achieve even slower undercut rate [45]. It is particularly important for sub-120nm particles and unnecessary otherwise (see supplemental figure 2).

Figure 8 – Tilted scanning electron micrographs of samples before (a) and after (b) lift-off step in ultrasonic bath. Also, to improve the lift-off of smaller particles, BOE undercut was performed. The cross-section of silicon substrates covered by thermally dewetted silver nanoparticles and undercut by buffered oxide etch at 0 °C for 10s (c), 20s (d), and 30s (e) are shown.
Next, all samples are evaporated with 10 nm Au at 0.5 Å/s in the same e-beam evaporation system (Figure 7a: step 4), immersed in a RCA-1 solution (NH$_4$OH:H$_2$O$_2$:Methanol = 1:1:2; v:v:v) at room temperature and sonicated four times for 10min in each round. After sonication in RCA-1, most silver nanoparticles covered with Au have been etched (Figure 7a: step 5), leaving behind a gold mesh pattern on the substrate. The gold mesh is now used as the catalyst template for MacEtch (Figure 7a: step 6).

3.1.2 MacEtch: Straight vs. Tapered Wires

The Si substrates with the patterned Au mesh are etched in MacEtch to produce straight (HF(49%):H$_2$O$_2$(30%):Ethanol = 13:2:19; v:v:v) and tapered (HF(49%):H$_2$O$_2$(30%):Ethanol = 13:2:X; v:v:v) SiNWs (Figure 7d), in which “X” represents the volume ratio of added 99.9% Ethanol to the mixture. For this work, solutions are always made fresh before each experiment and used immediately within 10min. To understand the effect of ethanol concentration on taper formation, the volume ratio of ethanol (X) was varied from 56 to 110 at a fixed 13:2 volumetric ratio of HF(49%) and H$_2$O$_2$(30%). Samples were cleaved and we studied their cross-sections in a SEM, measuring the taper of the wires produced. The taper of the wires is constant throughout its height for all cases which indicates that the local rates of hole injection and consumption are constant. This observation leads to the conclusion that the reactants’ concentration do not decay during the etching. Additionally, MacEtch etch rates are reported constant for several hours in other papers [21]. From the analysis of the SEM data, we found that the external taper angle of
SiNWs increases for solutions with higher ethanol concentration and detailed information is shown in Figure 7 (see supplementary figure 3).

3.1.3 SiNW Roughening

The next step to roughen the wire surface was to deposit Au nanoparticles on a set of straight SiNWs samples - 1 µm long with average diameter between 110-140 nm by sputtering on a Denton Desk II TSC (power was set at 20% for 15 seconds). All-angle rotation was activated to uniformly coat the nanowire surfaces (Figure 7a: step 7). At that point, samples were cleaved into 1 cm² pieces and SiNWs were roughened (Figure 7a: step 8) by a second etch step that involved immersing the samples in dilute MacEtch solution (HF(49%):H₂O₂(30%):H₂O = 1:1:24; v:v:v) for different durations of time, ranging from 5 to 25 seconds. Subsequently, samples were immersed in aqua regia (HNO₃(68%):HCl(37%) = 1:3; v:v) for 3 min to remove the Au mesh.

The sidewall roughness of the samples was characterized by high-resolution transmission electron microscopy (HRTEM) (Figure. 7e) and the RMS roughness is plotted as a function of the duration of the roughening etch step shown on step 8 in Figure 7a. High resolution images of the Si/SiO₂ boundary are obtained by tilting the nanowire to [110] zone-axis angstrom level resolution. Several HRTEM images recorded continuously along the length of a nanowire are seamlessly stitched together to generate the roughness profile of the nanowire over a length of
~500 nm. This procedure was conducted for three nanowires from each array to obtain an average RMS roughness for each sample.

3.1.4 Tapered SiNW for Anti-reflection Measurements

For investigating light reflection, two sets of straight and tapered SiNWs samples with a 300 nm average diameter were fabricated using MacEtch. Tapered samples were made with 13.4 Mol/L ethanol concentration. The first set contained wires that were straight and tapered with lengths of 2 µm and 1.5 µm, respectively. For the second set, tapered wires with lengths set at 11 µm were boron doped in a diffusion chamber with a boron diffusion source (BN-975, Saint-Gobain Ceramics) for 40 min at temperatures of 900 °C and 1000 °C. The reflectivity in the visible and near-IR range of the first (Figure 14a) and second (Figure 14b) sets was obtained in a Cary 5000 spectrophotometer.

3.2 Characterization of Silicon Nanowires

In this section, the results for particle size control of dewetted silver patterns, sidewall taper control of SiNWs, post-roughness generation, and reflection measurements are presented and discussed in the context of the applications and existing literature.
3.2.1 SiNW Fabrication and Taper Control

It has been shown that dewetting of an Ag thin-film can result in nanoparticles with diameters in the size range of 10-80 nm and with area coverage in the 32-42% range. This is related to the changes in thin-film nucleation and growth kinetics as a result of selecting a deposition rate as well film thickness [38]. The nucleation process during evaporation produces peaks and valleys on the thin-film top surface, centered at the nucleation site and the mid-point between them, respectively. These peaks and valleys on the film surface serve as the initial condition for dewetting upon exposure of the film to elevated temperatures. The initial shape favors thermal grooving at the valley region (grain boundary), resulting in the formation of particles centered at their nucleation sites. For a given temperature cycle, the nucleation density for silver island formation on a substrate during dewetting remains the same as that of silver grain formation during deposition. This is shown to be inversely proportional to the incoming flux of atoms during deposition [38]. This allows us to obtain high area coverage (particle density) at low evaporation rates (Figure 9). In the same figure, the average diameter increases with thickness and we observe a peak in the area coverage. This slight decrease in area coverage as the deposition thickness increases is due to merged grains during dewetting. This is possible because the thermal grooving process becomes less efficient at completely separating nucleation sites as the film thickness increases. This also causes the resulting particles to lose their circular shape, and the resulting particle density to decrease.
Figure 9: Characterization of sub-100 nm average Ag particle size: (black) average diameter (error bars represent one standard deviation of the wire diameter distribution) and area coverage (red) as a function of film thickness at constant 0.1 Å/s. The SEM images on the top represent each data point at the same magnification.

In the fabrication process, the limiting step for producing SiNWs from the dewetted sub-100 nm Ag particles via MacEtch is the metal lift-off technique described in section 4.1. For this regime, the particle’s height is small and less than twice the Au film thickness (see supplementary figure 2). Therefore, many particles are coated by Au resulting in a low lift-off yield. To address this issue, we use a BOE (Buffered Oxide Etch) step to etch the oxide layer that was deposited before the Ag film. This increases the height of the particles by an additional 10-15 nm and also undercuts the oxide under the silver particles to produce pedestal-like structures that greatly facilitate the lift-off process. The smallest reproducible average diameters over 1 cm² samples were 61 nm at 22% area coverage and 67 nm at 46 % area coverage (see supplementary table 1).
Further improvements such as decreasing the Au grain size and its thickness are being investigated to fine tune the lift-off yield for even smaller diameters.

Silicon wire tapering is possible by adding ethanol and changing its concentration in the MacEtch solution. The flux of holes injected into the band structure of Si is generated from the H₂O₂ reduction at the Au-MacEtch solution interface (cathode). When excess holes— not consumed by the anodic Si dissolution reaction at the Si-Au interface — become available, they diffuse and migrate away from the Si-Au interface, toward the rest of the Si surface exposed to the etchant. The presence of excess holes in Si near the wires’ surfaces increases the rate of SiO₂ formation at the surface. This is subsequently etched by HF [25] to create a porous Si layer. Continuation of this process results in growth of the pores, the loss of the outer surfaces layer, and the extension of the porous layer towards the center of the wires. The tips of the wires, having been created first, are subjected to this process for the longest time and hence the wires develop a taper. The thickness of the porous Si layer on the already formed wires increases monotonically with time. As a result of this, the tips of the nanowires have the thickest porous layer as compared to the bottom of the wire (Figures 10a and 10b). A similar observation has been made by Chartier et al. [25]. In their study of Si MacEtch with Au nanoparticles as catalysts, they found that decreasing the molar concentration of HF relative to H₂O₂ produces a porous tapered sidewall. The characterization of the external taper angle versus ethanol concentration is shown in Figure 10c. While the addition of ethanol can create controllable wire tapering, this effect was not observed when water was used instead of ethanol to dilute the solution.
Figure 10: Taper Control: (a) schematics of hole diffusion and migration towards SiNW shell surface, showing external angle, $\theta$, (b) TEM images of the tip through base (from left to right, respectively) of a SiNW etched in MacEtch in [EtOH]=13.4 M, (c) dependence of taper angle on ethanol molarity on solution. Scale bars are 100nm in length.
As described earlier when excess holes become available, the process described above can result in tapered SiNWs. From the overall reaction’s perspective [21], excess holes can become available by two means: an increase in hole generation on the cathode (Au-etchant interface), or a decrease in the rate at which holes are consumed on the anode (Au-Si interface). Our observations indicate that while the water addition reduces the kinetic rates of the cathode and anode reactions equally, the addition of ethanol reduces preferentially the hole consumption rate on the anode. As a result of this, excess amount of holes can migrate from the anode (Au-Si interface).

3.3 TEM characterization of roughness dependence on etching time

In the roughening approach, the catalyst is composed of Au nanoparticles that penetrate a few nanometers into the core direction of the nanowires etching a variety of crystallographic planes towards the SiNW core, causing the reformation of the Si and SiO$_2$ surfaces (Figure 11). Since the penetration path is small, we do not observe any coherence or preferred crystallographic direction in the etching done by the nanoparticles. TEM imaging followed by image analysis reveals the longitudinal topography and surface roughness of the nanowires and the Si and SiO$_2$ interface. Control over RMS roughness height is attained in the 0.5-3.5 nm range by controlling the etch time (Figure 11a). Successful control of the roughness levels by timed etches is a result of using diluted MacEtch solutions as elaborated in section 3.4.
Figure 11: Post-roughening characterization: (a) RMS height as a function of roughening time in diluted MacEtch solution, and low-magnification TEM images of SiNWs: (b) as-prepared, and after (c) 5 s, (d) 10 s, and (e) 20 s of roughening.
3.4 Discussion on Porosity Generated by MacEtch

We compared the etch chemistry (Figure 12a, $\rho = 35\%$) employed in a recent study to roughen SiNWs [6] and study its effect on thermal conductivity, and found the tips of nanowires to be relatively smoother and well-defined under high-magnification SEM regardless of the water molarity at $\rho = 75\%$ (Figure 12b-c) [7]. Since porosity has adverse effect on thermal conductivity, it is important to use the correct ratio.

![Figure 12: The morphology of the tip of the silicon nanowires is depicted under SEM as a function of etch parameter used to make silicon nanowires. From left to right, the images depict samples etched for 40 s, 40 s and 80 s. The scale bars are 250 nm.](image)

Additionally, it is fundamental to increase surface roughness of nanowires in a controllable manner to further decrease its thermal conductivity below the Casimir limit. Particularly, it was necessary to investigate diluted Macetch chemistries to reduce the etch rate while not creating porosity on the wires. Thus, a separate set of silicon substrates patterned with the Au mesh were immersed in solutions with $\rho = 75\%$ while varying the water molarity from 38.1 M to 54.9 M.
The etch rates were measured from SEM cross-section data. The wires are straight for all cases and the tip of the wires produced with diluted solutions remains sharp and seems to not be attacked by the slow Macetch process (see Figure 13). This finding is evidence that the ratio between the rates of the cathodic and anodic reactions remains constant and that the $\rho$ parameter accurately predicts the porosity of diluted macetch solutions for this given geometry of the catalyst. Also, this finding permitted the development of the roughening MacEtch recipe used with the samples shown in Figure 11.
Figure 13: Slow etching in MacEtch. Pre-patterned silicon substrates etched in solutions with $\rho = 75\%$ while varying the water molarity from 38.1 M to 54.9 M show no indication of porosity at the sidewalls or tips. By changing the molarity from $M_{H_2O} = 38.1 \text{ M}$ to $M_{H_2O} = 54.2 \text{ M}$, we further reduced the etch rate from 108 nm/s to 0.5 nm/s, respectively (see Appendix C).

3.5 Anti-reflective properties of tapered and doped SiNWs

Firstly, it is necessary to compare the reflectivity characteristics of straight and tapered structures in the visible and near-IR range. The effect of a slightly tapered SiNWs is captured in Figure 14a. A smooth transition in the refractive index derived from tapered nanowires reduces the reflectivity in the visible range by 77% (particularly around wavelength of 700 nm) relative to straight nanowires for samples with similar lengths. This is possible due to the subwavelength
scale of the SiNWs. In the visible range, the reflectivity spectrum for tapered SiNW agrees well with studies on anti-reflection of silicon nanotips of equivalent length [10]. Beyond the band gap wavelength, light travels into the sample and it is not well absorbed due to the low absorption coefficient of low-doped Si. As a result, light reflects from the back of the wafer and, thus, we observe a jump in reflectivity.

Increasing absorption in the near-IR becomes fundamental to reduce reflectivity in this range. One approach is to increase doping level. Higher doping concentrations facilitate phonon-assisted absorption around the band gap wavelength [46, 47] and increase free carrier density [48]. Both of these effects contribute to lower the reflectivity in our measurements. Figure 14b shows the effect of doping on anti-reflection of tapered SiNWs as a function of the temperature in which the boron doping was carried on.
Figure 14: Reflectivity of (a) straight 2 µm long (black) and tapered 1.5 µm long (red) SiNW and (b) of tapered 11 µm long SiNWs with different doping conditions: 1-10 ohm p-type (reference, blue), post-doped at 900 °C for 35 min (red), post-doped at 1000 °C for 35 min: instrumental noise was significant at 800-900 nm and 2000-2500 nm but does not obscure data trend; (c) SEM of post-doped SiNWs post-doped at 1000 °C; (d) photograph of sample fabricated on a 2 in wafer.
4 Beyond Silicon Nanowires: Combining Solid State Superionic Stamping and MacEtch to Fabricate Nanotubes, I-Beams and Complex 1-D Structures

In this chapter, the S4 process was reproduced from literature [49, 36, 50, 51, 52, 53] using Ag$_2$S stamps and focus-ion beam (FIB) lithography to define nanoscale features. These features were reproduced onto silver films (Figure 15a-b) which were deposited onto silicon substrates. The Ag features were coated in a sub-10 nm thick layer of gold and submitted to the lift-off procedure in sonication as described in section 3, resulting in a patterned mesh of gold. For the first set of samples, 15 arrays of 50 x 50 µm were produced with varying dot size from 180 nm to 1 µm and etched in MacEtch to produce wires (Figure 15b-f). The etch depth was around 25-30 µm.

For the purpose of demonstrating the capability to pattern complex features, a second set of samples was produced with the following silver patterns such as: rings, concentric rings, concentric ring-shaped holes, dots, and i-beams. After lift-off and MacEtch, the corresponding reversal image of these patterns etched onto silicon, producing tubes (Figure 16a), concentric circular walls (Figure 16b), concentric circular holes (Figure 16c), posts (Figure 16d), and i-beams (Figure 16e), respectively.
As discussed earlier, the most accepted diffusion model for MacEtch suggests that etching begins on the edge of an Au feature and progresses laterally and underneath the Au layer as opposed to going through the Au layer [22]. A rather non-intuitive result obtained and shown in Figure 16 is that the areas of continuous gold catalyst (without patterns) etched uniformly onto silicon without catalyst folding or slower etch rates. Our main hypothesis to explain the occurrence of uniform etching on continuous areas of Au film is the existence of sub-5nm cracks in itself. These cracks are created when the evaporated Au layer is thinner than 10 nm. The evidence to sustain this hypothesis is depicted in Figure 16c-e where one can observe sub-5 nm thins of silicon emerging from the cracks and collapsed onto the substrate as a result of surface tension forces acting during the drying step in which samples underwent.

It is observable that the catalyst in the center of the tubes in Figure 16a as well as the catalyst rings in Figure 16b and 16c did not etch uniformly onto silicon. This phenomena is called catalyst folding and was studied extensively by Dr. Owen Hildreth and collaborators at Georgia Institute of Technology [54, 55] and, more recently, by Dr. Carl V. Thompson at the Massachusetts Institute of Technology [56]. The origin of catalyst folding arises from different forces exerted in the Au layer as it is being etched. Dr. Hildreth argued that electrophoresis forces is one of the possible mechanisms for catalyst folding. While this understanding does not provide a solution, it helps to understand the limitations of the results obtained with the S4-MacEtch integration as it has failed to produce high-aspect ratio holes patterns or suppress catalyst folding.
Figure 15: SEM images of arrays of silver dots made by S4 process (a-b) followed by its corresponding nanostructures after MacEtch (c-f). The etching throughout the entire sample was uniform even though the regions separating the arrays of dots was larger than 50 µm in some locations of the sample. The hypothesis is that small sub-5 nm cracks are present in the catalyst layer which facilitate diffusion through the cracks.
Figure 16: SEM images of nanostructures after S4 and MacEtch (a-e), demonstrating the versatility of producing complex patterns on silicon. In regions where the catalyst was thin and disconnected from the mesh, the catalyst folded onto itself producing features whose bottom was not uniform as was the case on (a-c). This is in agreement with MacEtch literature on catalyst folding [54, 55].
5 References


[12] C. Wang, P. Murchpy, N. Yao, K. McIlwrath, and S. Chou, "Growth of straight silicon nanowires on amorphous substrates with uniform diameter, length, orientation, and


Appendix A: Image Analysis

A1 Using Image J for analyzing particle size

As shown on Figure A1, all samples were analyzed under SEM with the samples mounted horizontally. Scanning Electron Microscopy data was adjusted for threshold using Image J and particle area for each particle was measured. Assuming perfectly rounded particles, the diameter was derived and results have been summarized and reported in this document. Each row in the figure below represents a stage of the image analysis. Samples were obtained by loading each for an individual evaporation round with the thickness and evaporation rate being monitored directly by the crystal quartz monitor for all samples.
Figure A1 – Image analysis step-by-step. The first and last row display the evaporation parameters for thickness and deposition rate of the silver film, respectively. And, the second, third and fourth rows display the corresponding raw scanning electron micrograph image of dewetted silver particles, the black and white image generated after applying a contracts threshold, and the highlighted particle contour of the data analyzed via image J.
Appendix B: Taper angle characterization and image analysis

The taper characterization used high-magnification SEM images of SiNW cross-section as shown in Figure B1 below (left, [EtOH]=13.7 and right, [EtOH]=14.61). Images were loaded into free-software GIMP for manual measurement of the taper at the base of the wires.

Figure B1 - Details on taper angle dependence on ethanol concentration
Appendix C: Roughness: generation and characterization

C1 Reducing The Etch Rate of Metal-Assisted Chemical Etching

In the selection of MacEtch solution for roughening of SiNWs, we sought a solution with reduced etch rate and no excess holes being produced as to avoid porous formation. Silicon chips patterned with a gold mesh were immersed in MacEtch at a $\rho=75$ and for varying degrees of water content. Note that this parameter is defined in literature [25] as the molar concentration of HF divided by the sum of the molar concentration of HF and $\text{H}_2\text{O}_2$. No pores were observed in the SiNWs for the entire water molarity range studied. The etch rate was reduced by almost 3 orders of magnitude as shown in Figure C1.
For roughness characterization of the nanowires, we disperse the nanowires on holey carbon grid. A double-tilt holder is used to align the nanowire with [110] zone axis to obtain atomic resolution images. The diffraction pattern of the roughened nanowires reveals the single-crystallinity on Figure C2.
In order to construct the roughness profile of the sidewall, we take several continuous images along the boundary of the wire. The Si/SiO$_2$ atomic boundary is traced out in every image using ImageJ and the resulting profiles are stitched into a continuous surface. The mean surface of the boundary is obtained by a linear fit to the stitched profile. The roughness height ($\zeta(x)$ where x-axis is along the length of the wire) is defined about this mean surface and the standard deviation of $\zeta(x)$ yields the root-mean square (RMS) roughness height. We conduct this procedure with at least three nanowires from the same sample to obtain a statistical mean RMS height as shown on Figure C3.
Figure C3: Details on TEM analysis. The surface roughness profile analysis of Si/SiO₂ boundary for different etch times imaged using HRTEM.
Appendix D: Sample Records

The following samples were reproduced on 2-4 cm$^2$ Si chips. Table D1 summarizes the results obtained, showing the particle distribution, areal coverage, the lift-off yield and the as-fabricated SiNW sample. The results reported here have been repeated and are consistent.
<table>
<thead>
<tr>
<th>Sample Code</th>
<th>SEM of Wires</th>
<th>Lift-off Yield</th>
<th>Histograms</th>
</tr>
</thead>
<tbody>
<tr>
<td>A-05/26/11</td>
<td><img src="image1" alt="Image" /></td>
<td>61nm Ave. Dia. 32% A.C.</td>
<td><img src="image2" alt="Histogram" /></td>
</tr>
<tr>
<td>B-06/01/11</td>
<td><img src="image3" alt="Image" /></td>
<td>78nm Ave. Dia. 32% A.C.</td>
<td><img src="image4" alt="Histogram" /></td>
</tr>
<tr>
<td>C-07/06/11</td>
<td><img src="image5" alt="Image" /></td>
<td>77.5nm Ave. Dia. 29.2% A.C.</td>
<td><img src="image6" alt="Histogram" /></td>
</tr>
<tr>
<td>D-08/17/11</td>
<td><img src="image7" alt="Image" /></td>
<td>&gt;95%</td>
<td><img src="image8" alt="Histogram" /></td>
</tr>
<tr>
<td>E-09/28/11</td>
<td><img src="image9" alt="Image" /></td>
<td>&gt;95%</td>
<td><img src="image10" alt="Histogram" /></td>
</tr>
<tr>
<td>F-09/28/11</td>
<td><img src="image11" alt="Image" /></td>
<td>&gt;95%</td>
<td><img src="image12" alt="Histogram" /></td>
</tr>
</tbody>
</table>

Table D1: Sample records show the minimum particle size and maximum areal coverage obtained consistently.