DIRECTED LITHIUM TRANSPORT IN HIGH CAPACITY LITHIUM-ION BATTERY ELECTRODES

BY

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DISSERTATION

Submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Materials Science and Engineering in the Graduate College of the University of Illinois at Urbana-Champaign, 2014

Urbana, Illinois

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Lithium-ion batteries enable a modern, mobile society and are a widely used source of portable energy storage. Chapter 1 provides background and motivation for improving lithium-ion battery performance. Specifically these batteries still need improvements in terms of specific energy, specific power, cycle life, and safety. The rest of this document describes experiments utilizing model semiconductor electrodes to investigate fundamental phenomenon occurring during the operation of lithium-ion batteries in order to improve battery performance.

Chapter 2 examines the crystallographic anisotropy of strain evolution in model, single-crystalline silicon anode microstructures on electrochemical intercalation of lithium atoms. We highlight model strain-limiting silicon anode architectures that mitigate these impacts. By selecting a specific design for the silicon anode microstructure, and exploiting the crystallographic anisotropy of strain evolution upon lithium intercalation to control the direction of volumetric expansion, the volume available for expansion and thus the charging capacity of these structures can be broadly varied.

Chapter 3 examines the properties of microstructured Ge electrodes for Li-ion battery applications. Unlike Si electrodes, Ge electrodes do not exhibit the same anisotropic electrochemical lithium insertion. Model microfabricated single-crystalline Ge electrode structures are used to investigate the effect of microstructure design, coatings, and partial discharging on cycle life. These results provide an understanding of
the effects of electrochemical processes on model microstructured Ge electrodes which may ultimately aid in the development of high capacity anodes for Li-ion batteries.

In-situ characterization of lithium-ion batteries utilizing x-ray microscopy, nuclear magnetic resonance, transmission electron microscopy, and scanning probe microscopy have recently been utilized to understand fundamental phenomena occurring during (dis)charge cycling. X-ray Reflection Interface Microscopy (XRIM) was recently demonstrated by Fenter et al. utilizing the Advanced Photon Source at Argonne National Lab. In Chapter 4 we used full-field x-ray reflection interfacial microscopy in order to image the extent of the lithiation and the degree of residual crystallinity in individual silicon micro-posts directly. Images of the silicon posts are interpreted using a novel, but straightforward, model relevant for XRIM images obtained from large scale topological features. This approach should be widely applicable to a broad range of battery materials and for probing the liquid/solid interfaces of complex heterostructures during lithiation reactions.

In chapter 5 we examine encapsulated micropore-modified silicon anodes that define lithium mass-transfer dynamics to constrain strain evolution and improve capacity retention during (dis)charge cycling. Fully integrated cells incorporating this silicon anode and a commercial grade LiCoO₂ cathode maintain their capacity for 110 cycles with >99% average coulombic efficiency from cycles 5 to 100. Anodes with thicknesses up to 50 µm resulted in area-normalized capacities of up to 12.7 mAhcm⁻². When the silicon anode microstructure pitch is varied, a direct relationship is found to exist between the rate capability and volumetric capacity of the anode. Helium-ion
Microscopy, Secondary Ion Mass Spectrometry, and Scanning Electron Microscopy, used as \textit{ex-situ} characterization methods for the evolution of the electrode’s structure on cycling, reveal significant changes in nanoscale morphology that otherwise retain the essential laminate micropore motif of the initial Si anode.

The first appendix chapter uses recent advancements in terms of electrode coating and fabrication in order to demonstrate a solid-state battery using an inorganic solid-state electrolyte. We investigate whether cathode materials printed into channels could be utilized as a demonstration of a printed battery. Also the ability of conformal, thin ALD coatings of Al$_2$O$_3$ or LiAlO$_x$ to act as both separator and electrolyte was also tested. Neither ALD coating had the performance metrics required to serve as both separator and electrolyte. The second appendix chapter details our investigation of the impact of tetraethoxysilane (TEOS) as an electrolyte additive.
ACKNOWLEDGEMENTS

I want to thank my thesis advisor, Ralph Nuzzo, who made this work possible. The guidance and mentorship he has provided has been invaluable. He has provided not only funding, but also opportunities for both personal and professional development that have made me a stronger, better person. I will apply the lessons I have learned into all my future endeavors.

I want to thank my committee members, Andrew Gewirth, Shen Dillon, Jennifer Lewis, Paul Braun, and John Rogers. I want to especially thank Andrew Gewirth for the time he has spent to have great discussions as a collaborator on the work described within.

I am grateful beyond words for the support of my family—without their help over the years this achievement would not be possible. They have provided guidance and acted as an invaluable sounding board through the rough and the good times. In my own way I strive to achieve as much as they have.

I would also like to thank my research group members and collaborators that have given me so much help and mentoring throughout graduate school. I especially want to thank my friends, Brandon, Evan, and Ben, whose guidance and advice helped me get through graduate school. The great mentorship of older students has made it possible for me to successfully complete the rigorous process that is graduate school. Evan was my mentor for electrochemistry in the Nuzzo group. My ability to get the project off the ground owes to his patience and willingness to help. I want to thank the
other members of the energy frontier research centers that have provided feedback throughout my graduate career. I want to thank the staff at MRL and MNTL who trained me on instruments that made the work conducted in this thesis possible.

I very much want to thank my undergraduate advisor at Rice who showed me how to conduct research. I owe huge debt to my first real boss, Prof. Cytron at WUSTL, who took a chance on me and taught me creative problem solving that has been absolutely indispensable.

UIUC creates an amazing environment for learning and growth. I want to especially thank the technology entrepreneurship center for the events that they have hosted. The events in San Francisco and Chicago were especially important to me and have changed my perspective. I want to also thank Ron Watkins at Illinois Business Consulting for his mentorship and help throughout my graduate career.

This research was supported as a part of the Center for Electrical Energy Storage – Tailored Interfaces, an Energy Frontier Research Center funded by the US Department of Energy, Office of Science, Office of Basic Energy Sciences under award number DE-AC02-06CH11 (subcontract no. 9F-31921). This work was carried out in part in the Frederick Seitz Materials Research Laboratory Central Facilities, University of Illinois.

Any opinions, findings, and conclusions or recommendations expressed in this material are those of the author and do not necessarily reflect the views of the Department of Energy or other sponsors.
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CHAPTER 1

INTRODUCTION

1.1 Batteries

Batteries can be classified into two categories, non-rechargeable (primary) batteries and rechargeable (secondary) batteries. Secondary batteries reversibly convert between chemical energy and electrical energy via oxidation and reduction of two different electrodes in order to store / release energy. In electrochemistry, oxidation is when a species loses an electron, and reduction is when a species gains an electron. By convention, the anode is the electrode that is oxidized, and the cathode is the electrode that is reduced when the battery is discharging. These two electrodes are physically separated but maintain ion transfer through both electrodes being immersed in an ion-containing solvent called the electrolyte.

1.1.1 Common Battery Experimental Setups

Electrochemical testing can consist of two electrode or three electrode experimental setups. Two electrode testing has the working electrode coupled with a counter electrode across which the potentials and current are monitored. Three electrode testing passes current between the working electrode and a counter electrode where a third (reference) electrode measures the potential between the working and reference electrode. Since no current is passed through the reference electrode, it should not undergo significant changes during electrochemical testing and
therefore is a more accurate reference for measuring potential changes at the working electrode.

Commonly used cells for electrochemical testing include beaker cells, coin cells, pouch cells, cylindrical cells, and prismatic cells. Beaker cells—as the name implies—consist of a beaker filled with electrolyte that the electrodes are dipped into. These cells are tested in an inert environment such a glove box with argon. Coin cells—such as standard 2032 cells—utilize an o-ring pressed between two metal casing by a crimper in order to seal the cell and maintain an inert atmosphere inside the cell when the cell is being tested outside of an argon-filled glove box. The close proximity of the two electrodes requires the usage of a permeable polymer film (known as a separator) to physically buffer the electrodes and prevent shorting. The separator is soaked in electrolyte in order to facilitate lithium ion transport between the electrodes.

1.1.2 Common Electrochemical Testing Techniques for Batteries

These two or three electrode cells are electrochemically tested using methods including cyclic voltammetry, galvanostatic charge/discharge cycling, open circuit potential testing, and electrochemical impedance spectroscopy.

Voltammetry measures current as a function of potential. This current corresponds to electrochemical reactions occurring between the electrodes and the solution at the measured potential. Normalizing the current per active surface area allows the amount of electrochemical reactions occurring to be compared between samples. Cyclic voltammetry, abbreviated CV and also known as double potential sweep
chronoamperometry, measures current while sweeping back and forth across a set voltage range at a given rate (mV/s) [Figure 1.1].

Galvanostatic charge/discharge cycling (also known as chronopotentiometry) holds current fixed for a set amount of time and measures changes in potential required to provide the required current. Charge/discharge cycling of batteries consists of switching between positive and negative current in charging and discharging steps (cyclic chronopotentiometry) [Figure 1.2]. For example, for a lithium-ion battery, by convention lithium ions flowing from the cathode to the anode is referred to as the charging step. The reverse—lithium ions flowing from the anode to the cathode—is called the discharging step.

1.1.3 Metrics for Battery Testing

For these electrochemical experiments many common metrics are used to evaluate battery performance. The capacity (mAh) of a battery is the amount of time it can supply a given current (mA). For a given cycle, the ratio of the capacity that is released by the battery during the discharge step to the capacity stored in the battery during the charging step is known as that cycle’s coulombic efficiency.

The power (W) of an energy storage system is the current, mA, the battery can provide at a given voltage (V). Energy (Wh) is how long that battery can supply that power. It should be noted that for batteries power and energy are inversely related—higher currents result in lower total Wh for that charge/discharge step. Typical metrics for energy storage system are gravimetric capacity (mAh / g), volumetric capacity (mAh / cm³), gravimetric specific energy (Wh / g) & power (W / g), volumetric specific energy
(Wh / cm³) and power (W/ cm³), coulombic efficiency (energy in to energy out per cycle), and cost ($ / kWh). Portable applications can require a lightweight—high gravimetric capacity—and small—high volumetric capacity—energy storage system. Cost cannot only be reduced by utilizing lower cost materials but also by increasing the capacity (kWh) or capacity retention of the energy storage system.

1.1.4 Applications for Batteries

Batteries are a widely used component for portable energy storage because of their high specific energy relative to other forms of energy storage—recent advances in secondary battery performance facilitated the development of a mobile, interconnected society. The worldwide market for rechargeable batteries was approximately $ 48 billion in 2009.[1.1] A particular high performance subset of secondary batteries, lithium-ion batteries, are utilized as system level components in modern technologies of diverse form, with applications that include smart electric grid infrastructure, transportation systems, medical devices, military equipment, and portable electronics.[1.2-1.10] With such widespread applicability, there were 3,163 billion lithium-ion cells produced in 2008.[1.1] The market for lithium-ion batteries is predicted to triple (from $10 billion to >$30 billion) between 2009 and 2016.[1.11]

The most widespread usage of lithium-ion batteries is in consumer electronics. Consumer electronics—especially high-end devices—require high gravimetric and volumetric specific energies for portability and ease of use. [1.1] Lithium-ion batteries have also been used in a similar manner in high-end power tools.[1.12]
Transportation systems have long utilized batteries in systems such as starting, lighting, and ignition (SLI) automotive systems and industrial truck materials-handling equipment.[1.1, 1.13] More recently lithium-based energy storage systems have been proposed for hybrid-electric vehicles, fully-electric vehicles, and planes.[1.3, 1.14] These transportation systems have the potential to reduce US dependence on foreign oil, reduce carbon dioxide emissions, and reduce exhaust emission within dense urban areas.[1.15, 1.16] The performance of these transportation systems is strongly tied to their energy storage systems resulting in high performance lithium-ion batteries generally being used.

Numerous biomedical devices from pacemakers to artificial limbs rely on energy storage to operate.[1.4, 1.17-1.21] These devices can treat many conditions including brady cardia (cardiac pacemaker), tachy cardia (cardioverter defibrillator), syncope (implantable cardiac monitor), congestive heart failure (cardiac resynchronization therapy defibrillator), and chronic pain / epilepsy / hearing loss (neurological stimulator).[1.1, 1.17] These batteries can be classified in terms of required current.[1.1, 1.17, 1.18] Biomedical devices with high energy/power requirements, such as in ventricular assist and total artificial heart devices or when wireless telemetry is included with the device, commonly use rechargeable lithium-ion batteries.[1.18, 1.21]

Grid-level energy storage has numerous beneficial applications—currently electric infrastructure is the largest just-in-time (JIT) supply chain.[1.1] Energy storage systems attached to the grid could buffer energy generation by baseload power plants enough to reduce the need for load-following, non-optimal energy generation.[1.12,
Energy storage can also provide ancillary services to the electric grid such as backup, reducing requirements for regulation and contingency electricity generation reserves, frequency regulation, and ramping. The main barrier to the adoption of lithium-ion batteries for grid-level energy storage is the cost per kW, except in systems that also require portability. Another concern for widespread adoption of large lithium-ion batteries is the prevalence of cheaply accessible lithium.

Further implementation of batteries requires significant research in order to increase the rate of performance improvement that—over the past couple of decades—has been sluggish relative to performance improvements in other components of electronics [Figure 1.3].

1.1.5 Battery Chemistries

Many different battery chemistries exist—including Pb-acid, Zn-air, Na-S, Ni-Cd, Li-air, Li-S, Na-ion, and Li-ion—each having unique performance characteristics [Figure 1.4]. Na-S batteries have significantly lower costs—in terms of $/kWh—relative to lithium-ion batteries and thus Na-S batteries have greater prospect for usage in grid-level energy storage. Li-S and Li-air batteries have potential for higher performance than lithium-ion batteries, but Li-S and Li-air batteries are still inhibited by fundamental phenomena that limit practical application. Li-ion batteries are currently the highest performance secondary batteries on the market. Significant research focused on high performance lithium-based batteries because lithium is the most electronegative metal (~3 V vs. standard hydrogen electrode) and is one of the lightest metals (.534 g / cm³). Lithium metal electrodes were originally the focus of
research, however, severe safety issues related to lithium metal dendrites that form
during operation causing battery fires have caused them to be recalled from use.

1.1.6 Lithium-ion Batteries

After commercialization of “rocking-chair” lithium-ion batteries by Sony in 1991[1.1],
these batteries saw widespread usage for consumer electronics and transportation
because they have the highest specific energy and power of currently available
secondary battery chemistries. Typical commercial lithium-ion batteries are comprised
of graphite and a lithium ion inserting oxide such as LiMO_2 (where M = Co, Mn, Ni,
Ni_xCo_yAl_z [NCA], and Ni_xCo_yMn_z [NCM]) [Figure 1.5] [1.6, 1.30]. Most commercial
lithium-ion cells consist of anode and cathode films that are tens to hundreds of
microns.[1.1] These electrode films are made from a slurry of active material,
conductive additives, and binders on a metallic current collector.

A majority of research on lithium-ion batteries is conducted in half-cells—with
lithium metal as the reference electrode. The reversible half-cell reaction that occurs at
the graphite electrode is shown below, with the forward reaction corresponding to
charging and the reverse reaction corresponding to the discharge process.

\[ C_6 + xLi^+ + xe^- \rightleftharpoons Li_xC_6 \]

The maximum electrochemical lithium insertion (lithiation) is one lithium atom per 6
carbon atoms, corresponding to a theoretical gravimetric capacity for carbon of 372
mAh/g. The reversible half-cell reaction that occurs at the lithium cobalt oxide is shown
below, with the forward reaction corresponding to charging and the reverse reaction
corresponding to the discharge process.
\[ LiCoO_2 \rightleftharpoons xLi^+ + Li_{1-x}CoO_2 + xe^- \]

For this system limiting \( x \leq 0.5 \) is required for stable cycling of the electrode.\[1.31-1.34\]

The electrochemical reaction occurring in the full-cell—a cell not utilizing a lithium metal electrode—shows the so-called “rocking chair” mechanism behind energy storage in common lithium-ion batteries.

\[ LiCoO_2 + C_6 \rightleftharpoons Li_xC_6 + Li_{1-x}CoO_2 \]

For half-cell experiments coulombic efficiency is not crucial because the lithium metal counter electrode provides a massive surplus of lithium in the cell. In full-cells (the setup used in commercial lithium-ion batteries), however, the coulombic efficiency will dramatically lower the capacity retention of the cell as lithium ions are lost on each cycle. Additionally for half-cells experiments with the anode the capacity of the anode is commonly reported while for full-cells the specific power /energy is commonly reported.

1.1.6.1 Lithium-ion Battery Electrolytes

For lithium-ion batteries, the electrolyte—a lithium salt dissolved in non-aqueous solvents—facilitates ion transport between electrodes. The choice of electrolyte components is crucial because during operation of the battery, these electrolytes decompose on the surface of the electrodes to form a passive film, known as the solid-electrolyte interfaces/interphases (SEI) that dramatically impact battery performance [Figure 1.6].\[1.35-1.38\] Typical lithium salts used in electrolytes include LiPF\(_6\), LiClO\(_4\), LiBF\(_4\), or LiAsF\(_6\).\[1.38\] These salts are chosen for their stability and high mobility in the non-aqueous solvents in the battery. LiPF\(_6\) has been widely used in
batteries because it has a good balance of properties—it is not as stable as LiClO$_4$ and doesn't have the high ionic mobility of LiBF$_4$.[1.38] The solvents are typically a mixture of cyclic and linear alkyl carbonates such as ethylene carbonate (EC), diethyl carbonate (DEC), dimethyl carbonate (DMC), and propylene carbonate (PC). Solvent selection is critical for stable battery operation; when EC is used as a co-solvent with another alkyl carbonate, a stable SEI is formed that prevents exfoliation of the graphite electrode and dramatically improves capacity retention of the battery.[1.38]

The composition of the SEI is dictated by the electrolyte used in the battery. Possible components of the SEI include LiF, LiC$_2$O$_3$, LiOH, semi-carbonates, and polyolefins.[1.39-1.42] Certain components of the SEI such as LiF negatively impact performance—LiF consumes some of the limited lithium in the cell and forms a highly resistive, insoluble (in the electrolyte) film on the surface of the electrode.[1.43]

Recently, additives such as fluoroethylene carbonate (FEC) or vinylene carbonate (VC) have been added as lower weight percentage components to electrolytes in order to alter the composition of the SEI and improve battery performance.[1.44-1.48]

It should be noted that these non-aqueous electrolytes used in lithium-ion batteries are a serious point of concern for safety as they are flammable.[1.49-1.53] Thermal runaway in lithium-ion batteries leads to significant damage to the battery and surrounding environment.

1.1.6.2  Required Improvements to Lithium-ion Batteries

Improvements to lithium-ion batteries are needed in terms of specific energy, specific power, multi-cycle lifetime, and safety. These required improvements can not
only be achieved by higher energy/power density electrode materials (than conventionally used carbon anodes and LiCoO₂ cathodes), but also advancements in other areas such as battery packaging.[1.6, 1.36, 1.55, 1.56] Inactive materials can be 50% of the weight of a lithium-ion battery.[1.54] Advances in multiple areas are required to improve battery performance—increasing the capacity of the anode by an order of magnitude (from that of carbon) for a battery with a 200 mAh/g cathode only results in a capacity improvement of the battery by ~20% [Figure 1.7].[1.63]

Silicon, germanium, and tin can have higher gravimetric and volumetric capacities than a carbon electrode [Figure 1.8].[1.57] Germanium has a much larger theoretical gravimetric capacity (1623 mAh/g) than carbon (372 mAh/g). The power density of germanium batteries is significantly higher than that of carbon and silicon due to the high mobility of lithium-ions in Ge.[1.58] A downside is that Ge is not as widely used in research as other semiconducting materials, such as silicon, due to its higher cost.

1.1.6.3 High Capacity Silicon Electrodes for Lithium-ion Batteries

Silicon anodes for lithium-ion batteries have garnered attention because the material has the highest theoretical gravimetric capacity (3579 mAh/g). During battery charging the lithium ions are inserted into the silicon, and during discharging the lithium ions are removed from the electrode.

\[ \text{Si} + x\text{Li}^+ + xe^- \rightleftharpoons \text{Li}_x\text{Si} \]

Significantly more lithium ions can be inserted into a silicon electrode relative to a carbon electrode; lithiation of silicon up to Li₃.₇₅Si is not only accompanied by the loss of crystallinity of the silicon[1.59-1.62] but also a 300% volumetric expansion[1.63, 1.64]
[Figure 1.9]. This strain on thick films of silicon during lithiation results in fracture of the electrode and the loss of electrical contact after only a few cycles.[1.63, 1.65]

1.1.6.4 Previous Research on Silicon Lithium-ion Battery Electrodes

Numerous approaches have been tried to mitigate the impact of these massive strains in order to improve the capacity retention of silicon-based batteries. Thin films of silicon,[1.66-1.71] porous silicon electrodes,[1.72-1.79] composites that mix silicon with (in)active materials,[1.63,1.80-1.86] tailored silicon micro-/nanostructures,[1.65, 1.80, 1.87-1.96] and inclusion of binders such as carboxymethyl cellulose[1.97] and sodium alginate[1.98] have demonstrated improved performance relative to a bulk silicon electrode.

1.2 Research Summary

The research within this document has focused on investigating—and then directing—mass transport in lithium-ion battery electrodes (especially silicon) to improve lithium-ion battery performance. After demonstrating crystallographic-dependent anisotropic lithium transport in silicon, we utilized materials selection and geometric design to cause non-crystallographic-based anisotropic lithium transport. We then investigated characterization techniques and materials for improvement of electrode performance and safety.
1.3 References


1.4 Figures

Figure 1.1: a) Potential versus time and the b) resulting current versus potential graph.

Cyclic voltammetry can be used to determine the potential of electrochemical reactions occurring in a lithium-ion battery system.[1.99]

Figure 1.2: a) Current versus time and the b) corresponding potential versus time graph.

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CHAPTER 2

STRAIN ANISOTROPIES AND SELF-LIMITING CAPACITIES IN SINGLE-CRYSTALLINE 3D SILICON MICROSTRUCTURES: MODELS FOR HIGH ENERGY DENSITY LITHIUM-ION BATTERY ANODES


2.1 Introduction

Lithium-ion batteries are extensively utilized in technology, with notable growth coming from applications in portable electronics, medical devices, and hybrid/electric vehicles.[2.1-2.7] Improvements in lithium-ion battery technology—specifically in terms of energy density, operating multi-cycle lifetimes, and safety—are of particular interest for the roles they might play in providing storage capacity for intermittent renewable energy sources,[2.3, 2.8-2.10] system level components in a smart/modern electric grid,[2.11] actuatable prosthetic limbs,[2.12, 2.13] batteries for fully electrical vehicles [2.14], and microelectromechanical systems.[2.15] Fundamental limitations inherent to materials currently used in lithium-ion batteries have notably impeded progress in
achieving higher energy densities as well as limited the attainable charge-discharge cycles. The emerging consensus in the field suggests that the basic mechanism of energy storage in the current commercial lithium-ion batteries, an electrochemical reaction of lithium ions with a carbon-based anode and LiCoO$_2$ cathode, likely needs to be modified in order to achieve significantly higher energy storage densities.[2.16] It is largely for this reason that silicon, a material that has an energy storage capacity of 4200 mAhg$^{-1}$ [2.17, 2.18] or approximately ten times greater than carbon, has attracted considerable attention as an anode material in lithium-ion battery research. [2.19, 2.20] Poor capacity retention with cycling, a result of a nearly 400% volumetric expansion during operation, has prevented the adoption of silicon anodes.

Research on improving the capacity retention of silicon anodes on cycling has focused recently on the properties of anodes of silicon intermetallics/composites [2.21] as well as various forms of micro/nanostructured silicon.[2.22, 2.23] Anodes of silicon in composite matrices that experience less volumetric expansion during charging, for example, demonstrated increases in the number of attainable charge-discharge cycles.[2.21] During charging, the non-silicon additives helped to mediate the expansion as well as maintain electrical contact between silicon particles. Silicon also has been combined with conductive binders as well as metals that include: (a) lithium active Ag, Sb, Al, Sn, C, and Mg; and (b) lithium inactive Fe, Co, Cu, and Ni.[2.21] These more complex anode compositions have provided some improvements in performance. A recent approach suspended the silicon anode material in an elastic matrix. Anodes fabricated by this method in one report achieved twice the capacity of carbon anodes
over hundreds of cycles and in another report achieved four times the capacity of carbon anodes over 50 cycles.[2.21] Despite these promising results, none of these systems has approached the theoretical capacity of silicon without significant capacity fading upon cycling.

It has recently been shown that the modification of the mesoscopic architecture of a silicon anode can increase the number of achievable charge-discharge cycles.[2.21] The properties of thin film silicon anodes fabricated using chemical vapor deposition, thermal vapor deposition, sputtering, and milling illustrate this effect;[2.21, 2.22, 2.24-2.26] at film thicknesses of less than one micron, the anodes sustain capacities near the theoretical limit for silicon for hundreds of cycles. Reducing the anode feature sizes to the micron scale was also found to enhance lithiation kinetics by decreasing the diffusion lengths for lithium ions.[2.23] Thin anodes are also compliant with significant amounts of mechanical flexure,[2.27] but also as a consequence limit the total amount of energy that can be stored.

The latter limitation is one that recent work suggests can be addressed via the use of 3D silicon microstructures for lithium-ion battery anodes.[2.28-2.30] For example, thin film silicon anodes with increased total active material can be fabricated by low pressure chemical vapor deposition of a 50nm thin silicon film on a mandrel comprised of arrays of high aspect ratio trenches.[2.31] A recently reported 3D architecture consisted of silicon nanowires (NW) grown on a steel substrate by a vapor-liquid-solid process using a gold catalyst.[2.17, 2.32-2.35] Another recent study utilized hollow silicon nanotubes (NT) to demonstrate that the number of attainable cycles can
be increased by designing structures that experience less stress upon lithium intercalation.[2.18] These nanostructures were fabricated by chemical vapor deposition of silicon on a sacrificial ZnO nanowire (NW) template, followed by subsequent removal of the oxide template. Modeling of the theoretical stresses on both the hollow Si NTs and Si NWs demonstrated that the higher free surface area of the NTs results in lower stresses during lithium intercalation. This reduction in stress enabled the NTs to sustain a higher performance over more charge-discharge cycles as compared to the Si NWs. Even so, the silicon NTs still experienced appreciable capacity losses with cycling. The high cost of silicon NW/NT, their susceptibility to failure at the substrate, as well as the risk of broken NW/NT shorting the battery remain as serious concerns for this class of material.

The current work addresses questions related to atomic dynamics of strain evolution in model silicon anodes, examining a variety of 2D and 3D mesoscopic constructs fabricated using electronic grade single-crystalline silicon. We describe the significant anisotropies that characterize the charging/discharging strain evolution that occurs in this system and highlight strategies that can provide mechanisms through which to control its attributes. Toward this end, we describe a set of design strategies that provide passive mechanisms—that is, self-generated ones—for controlling strain evolution in silicon anodes. We show that, through an interplay of the 3D design rules of the silicon microstructures and the crystallographic anisotropy of the strain evolution upon lithium intercalation, both the form of the volumetric expansions, and limiting capacities of the anodes can be broadly varied. We illustrate these ideas in the
threshold values for volumetric expansion and strain above which further lithium intercalation cannot occur—a structurally mediated self-limiting capacity. We suggest approaches for further work that might provide robust designs to limit the strain on the structures, while still enabling higher capacities than carbon anodes.

2.2 Experimental

2.2.1 Sample Fabrication

Arrays of structures were fabricated using (111) N-type single-crystalline silicon wafers (Virginia Semiconductor) with a resistivity of .1-1ohm-cm. Intrinsic (100) and (111) silicon wafers (Sigma Aldrich) and (110) wafers (Nova Electronics) with a resistivity of 5,000-10,000 ohm-cm were used for the Raman characterization. Before photolithography samples were cleaned with Nanostrip (Cyantek). AZ 5214 (Clariant) was spun onto wafers, exposed, developed in AZ 327MIF (Clariant) and postbaked at 110°C for 7 minute in order to provide a resilient mask to etching. Masked samples then underwent anisotropic vertical etching using the Bosch process by Inductively-Coupled-Plasma Reactive Ion Etching (ICPRIE) using a STS Mesc Multiplex Advanced Silicon Etcher. 26 second etch steps and 10 second passivation steps resulted in sidewalls with deeper, longer waves while relatively smooth sidewalls were achieved through 7 second etch steps and 5 second passivation steps. In order to clean the samples after ICPRIE the samples were sonicated in acetone for 10 minutes and then IPA for 10 minutes before using RCA1 (1:1:5 H₂O₂:NH₄OH:H₂O) at 100 °C to remove the flouronated polymer. In order to create 3D structures of controlled spacing an additional angled
metal deposition of 13 nm Cr and 25 nm Au (Temescal E-Beam Evaporation Systems) and then etching of the samples for 2 minutes in PSE-200 (Transene) at 100°C was used to form the “tiered” structures. The Au and Cr were then removed by their respective preferential etchants (Transene). In order to create an electrical contact and current collector all samples had Ti (15 nm) and Au (100 nm) deposited on the backside as a current collector by electron-beam evaporation. The titanium acts as an adhesion layer for the electrically conducting gold layer. All but the active area and top electrical contact were covered in epoxy (Devcon) in order to control the amount of silicon exposed to the electrolyte.

2.2.2 Characterization

Samples were imaged using two scanning electron microscopes (JEOL JSM-6060LV Low Vacuum Scanning Electron Microscope and Hitachi S-4800 High Resolution SEM). For each sample a small section of the wafer was broken off and investigated under cross-sectional SEM to determine the surface area of that particular sample before galvanostatic charge/discharge cycling. Imaging each sample eliminated the possibility of small variations in the fabrication process causing error in the current density calculations. These cross-sectional images in conjunction with top-down images by camera were used to determine the total active surface area of the sample. Compositional analysis of the samples was determined using an Oxford Instruments ISIS EDS System attached to the JEOL 6060 SEM. Each sample was charged, washed in diethyl carbonate, and then immediately taken to the SEM. Raman experiments were carried out using instrumentation previously described.[2.46] An in-situ
spectroelectrochemical cell was used to acquire Raman spectra while potentiostatically cycling the silicon. The spectroelectrochemical cell was assembled and sealed in an argon filled glove box (Vacuum Atmospheres). A He-Ne laser (632.8 nm) was used as the excitation source. Electrochemistry during Raman experiments was conducted using a CHI760D in a three electrode configuration with a lithium ribbon counter electrode and reference electrode. Spectra were continuously obtained with an acquisition rate of 0.05 spectra per second, during a scan rate of 200 μVs⁻¹ so that acquisition times were 10 seconds. Peak heights were determined using peak analysis software (OriginPro 8.1).

2.2.3 Galvanostatic Experiments

All electrochemical experiments were conducted in an argon filled glove box (Innovation Technologies) that was kept at <10 ppm oxygen. Galvanostatic experiments were conducted using a galvanostat (CHI660D) in a three electrode cell with a lithium foil counter electrode and reference electrode and were run from 2 V to .01 V (vs. Li/Li⁺). The lithium foils (Alfa Aesar) were cleaned under argon by washing with pentane and then diethycarbonate (Sigma Aldrich) in order to minimize the addition of impurities into the system. The electrolyte was prepared under argon and consisted of 1.3 M LiPF₆ (Strem Chemicals) in 1:1 (w/w) DEC:EC (Sigma Aldrich). Raman experiments were carried out using 1 M LiClO₄ (Sigma Aldrich) in propylene carbonate (Sigma Aldrich) to avoid interference from vibrational modes from the solution near the silicon phonon mode (520 cm⁻¹). Glassware used in the experiment was cleaned with NOCHROMIX (Godax laboratories, Inc.), washed, and dried in an oven to remove moisture.
2.3 Results and Discussion

2.3.1 Fabrication of Ordered Microstructural Arrays in Single-Crystalline Silicon

Embedding 1, 2, and 3D Design Rules

The most basic silicon microstructure examined in this work, one with a quasi 1D design rule, consisted of a line pattern of micron scale silicon bars. An example consisting of 10 µm cross-sectional bars spaced 10 µm apart is shown in Figure 2.1a. This architecture can be used to directly demonstrate the significant anisotropies of the structural changes that occur during lithium intercalation. The second model design we explored comprised discrete arrays of rectangular pillars, herein referred to as microposts, fabricated with a quasi 2D lateral design rule for the spacing between individual posts [Fig. 2.1b]. For a specific orientation of the single-crystalline silicon substrate, the microposts provide a means to characterize the crystallographic anisotropies of the lithiation/delithiation process as two different crystallographic orientations are exposed upon vertical etching. Structures embedding quasi 3D design rules were also fabricated and tested. In this case, the lateral spacing between structures in the x and y directions was controlled as in the microposts, however, the structure was also broken into discrete platelets supported by a central silicon bus bar and spaced in the z direction. Examples of these “tiered” structures—ones formed through a combination of anisotropic vertical etching, angled metal deposition, and anisotropic wet chemical etching—are show in in Figure 2.1c.[2.36] Modifications of individual processes enable facile tailoring of the design rule in any of the three
dimensions, providing a means to generate structures with different spacings and feature sizes with further hierarchical control over the array pitch [Fig. 2.2].

The model anodes examined in this work were fabricated using combined lithographic and wet-chemical/ion-based etching protocols that have been described in depth in earlier publications,[2.36, 2.37] being adapted here to allow examinations of the sensitivities following from crystallographic anisotropy. The fabrication processes were carried out on both (111) and (110) oriented wafers, aligning the silicon structures along specific crystallographic directions to provide visualizations of the structural anisotropies that characterize the lithium intercalation dynamics. The typical process flow for the structures shown in Figure 2.1—the sequence of photolithographic patterning and etching steps—is depicted schematically in Figure 2.3. The Figure 2.3a shows a model process flow for constructing regular arrays of micron sized silicon bars. A model process for constructing post arrays is illustrated in the Figure 2.3b. In each case, the feature can be (and in this work are) aligned to orient the various sidewalls along specific desired crystallographic planes. This latter aspect of the chemistry and fabrication process is described in more detail below. Finally, as illustrated in the Figure 2.3c, the details of the patterning can be modified to generate a more complex, fully 3D set of design rules. The example shown in the scheme follows but modifies methods reported by Rogers et al. that exploit highly anisotropic wet chemical etching to amplify and deepen side wall modulations developed during deep reactive ion etching (RIE) processing.[2.36] This fabrication scheme is easily scalable to large areas, given the requirements for relatively low-resolution, single level photolithography and simple
forms of substrate alignment. In this work we typically fabricated ordered test microstructures over 2 cm x 2 cm areas with minimal defects [Fig. 2.3d].

2.3.2 Exploration of Structural Dynamics in Single-Crystalline Silicon Microstructural Arrays during Lithium Intercalation by SEM and EDS

Scanning electron microscopy (SEM) was used to investigate the gross structural changes that occur during lithium intercalation in silicon. The data from correlated measurements (acquired by energy dispersive X-ray spectroscopy (EDS)) provided information on the compositional evolution of the silicon at varying degrees of lithium intercalation. In a specific study of lithium intercalation, silicon bars 10 µm wide, 20 µm tall, and spaced 10 µm apart were examined [Figure 2.4a]. These bar motifs were fabricated using a (111) orientation of silicon, aligning their long axis along its <111> direction. After one hour of galvanostatic charging at 123.1 µAcm⁻², cross-sectional SEM and EDS data revealed areas of lithium intercalation residing predominantly along the edges of the bars, as revealed by both the secondary electron emission contrasts and X-ray counts [Fig. 2.4b]. After 10 hours of lithium intercalation at 109.9 µAcm⁻², larger areas of volumetric expansion, and thus silicide growth, are apparent [Fig. 2.4c]. The step-profile in the silicon-counts shown by the cross-sectional trace suggests a progressive growth that consumes a pristine single-crystalline silicon core. The composition of the lithiated areas was identified as likely being that of a lithium-silicide (see below) and not part of a thickening solid-electrolyte interface/interphases (SEI) because of the minimal counts of carbon and oxygen detected by EDS [Figure 2.5]. The
SEI phase that is present is thin at the scale of the magnification used in these measurements.[2.38] To determine the stoichiometry of the observed lithium-silicide, the EDS data was compared to a Monte Carlo model (Win X-Ray) that predicts the silicon counts that EDS will detect for samples of varying atomic composition of silicon and lithium. By comparing the predicted silicon counts for pure silicon to specific compositions of lithium-silicides, two possible phases were identified. The model predicts a reduction in silicon counts from pure silicon of 46% and 49% respectively for Li-Si phases of 19% atomic silicon / 81% atomic lithium and 21% atomic silicon / 79% atomic lithium. This correspondence with the observed reduction in silicon counts suggests that the silicide phase formed is most likely either Li$_{22}$Si$_5$ or Li$_{15}$Si$_4$. The theoretical capacity for Li$_{22}$Si$_5$ is 4200 mAh$^{-1}$ and the theoretical capacity for Li$_{15}$Si$_4$ is 3600 mAh$^{-1}$. Based upon literature guidance, the Li$_{15}$Si$_4$ phase is likely that formed here.[2.19]

It is important to note one additional feature of the structural evolution evidenced in the micrographs shown in Figure 2.4, namely the biconvex sidewalls of the central silicon pillars. We believe this structural feature could result from several different competing mechanisms. In the first, electrical resistance in the silicon is assumed to drive a preference for lithium intercalation at the bottom of the structure. The transport limitations that develop as lithium intercalated into the silicon from the solution (where the depletion of lithium ions at the bottom of the structures should be highest) would in turn cause a preference for lithium intercalation at the top of the structure. If these effects are of the same magnitude, the largest volumetric expansion
might then occur in the middle of the structure, as is observed experimentally. Even so, the high symmetry of the biconvex silicon shape seems hard to rationalize on the basis of such a fortuitous compensation. Alternatively, strain attributes (i.e. its relaxation being greatest away from sharp corners) might also play a contributing role. The role resistance plays in causing the biconvex sidewall after galvanostatic charging was explored by charging a structure with the same width and crystallographic orientation as the previously discussed structures, but with half the height (10 µm wide x 10 µm tall cross-section) [Figure 2.6]. For these shorter structures the largest expansion occurred at the top of the structures. This change in the sidewall profile when the structure height was reduced implies, at a minimum, that the electrical resistance plays some role in the observed bowing.

2.3.3 Crystallographic Anisotropy of Strain upon Lithium Intercalation

The previous data showed that an anisotropy exists in the diffusion rates of lithium in single-crystalline silicon, one that is approximately an order of magnitude larger for lithium motion along the <110> direction. This crystallographic anisotropy of the lithium intercalation process is demonstrated by the data given in Figure 2.7, which examines the strain evolution in microbar structures fabricated with comparable dimensions on samples exposing both {111} and {110} planes to the electrolyte. As is clearly seen in Figure 2.7, the lattice expansion that follows from lithium insertion occurs preferentially in the <110> direction. On a (111) wafer, the bar structures were patterned perpendicular to the (111) crystal plane, such that sidewalls of {110} planes
were exposed after anisotropic vertical etching [Fig. 2.7a],[2.36, 2.37, 2.39, 2.40] During the galvanostatic charging of the silicon, volumetric expansion predominately occurred laterally between the structures along the <110> direction [Fig. 2.7a]. Using a (110) wafer with lines patterned perpendicular to the (110) crystal plane, the same anisotropic etching (with proper in-plane alignment) exposed sidewalls of {111} planes [Fig. 2.7b].[2.37] Galvanostatic charging in this case led to volumetric expansion again along the <110> direction, resulting in a marked vertical extension of the bars. Exploiting this crystallographic anisotropy of the strain developed upon lithium intercalation enables a means to control both the direction and degree of the volumetric expansion. This prospect is in fact demonstrated in the bottom left panel of Fig. 2.7a, where a bar microstructure properly aligned and fabricated on a (111) wafer reaches a self-limiting volumetric expansion in the <110> direction that limits further lithium intercalation [Fig. 2.7a]. The specific example shown in Figure 2.7a suggests that the galvanic charging capacities of single-crystalline silicon microstructures can be manipulated, via the agency of the strain anisotropy, by mass transfer limitations. In the system shown, the expansion occurring along the <110> direction eventually leads to contacts that pinch off the trenches. In this way electrolyte access is impeded and the charging rate drops markedly as a result. This implicitly suggests that other design rules would evolve differently and for this reason would lead to different outcomes/limits on capacity.

The data presented above in Figures 2.4 and 2.7 demonstrate that the volumetric expansion of the silicon lattice that occurs as a consequence of lithium
intercalation is strongly anisotropic, evolving in a manner that is dependent on the specific crystallographic planes that are exposed to the electrolyte. It is interesting to note that crystallographic anisotropies are well established in the wet etching chemistries of silicon.[2.37-2.39, 2.41, 2.42] For example, it is well known that the wet etching of silicon in KOH solutions proceeds much more rapidly along the <110> direction, with a rate that is significantly faster ($\sim 10^3-10^4$) than that along the <111> direction.[2.37-2.39, 2.41, 2.42] The data in Figure 2.8 provides additional insight into the anisotropy of the electrochemically-driven diffusion of Li into {100}, {110}, and {111} crystal planes, one which is similar to the anisotropy that has been previously demonstrated in exemplary wet chemical etching processes as well as in Figures 2.4 and 2.7. These measurements were made using in-situ Raman spectroscopy in conjunction with single-crystalline silicon wafer substrates with different crystallographic orientations. It has previously been demonstrated that the transition from crystalline silicon to a possibly amorphous lithium-silicide phase can be monitored during lithiation through the intensity of the $T_{2g}$ first order optical phonon mode located at 520 cm$^{-1}$.[2.43] The potential dependent decay of this phonon mode intensity directly tracks the progressive transition of crystalline silicon to the amorphous silicide on Li$^+$ insertion.[2.44] For excitation at the wavelength used in these experiments (632.8 nm), the relatively lightly doped wafers have a optical penetration depth on the order of $\sim 3$ µm.[2.45] The onset potential for lithium insertion is modestly responsive to the doping levels and type of the wafer used. In the present case, we used undoped commercial (111) and (100) wafers and a low-doped N type (110) wafer (the only commercial grade
available) to carry out these measurements. To account for the small shifts in the lithium insertion potentials this elicits, the potential scale for each graph is standardized to the onset of the phonon decay (as denoted by a solid line) and plotted as a potential difference in order to illustrate the differences in the electrochemically driven decay profiles of the phonon mode intensity for each of the different crystal types. Interestingly for constant potential sweep velocities of 200 µVsec⁻¹, the decay of the phonon mode intensity for the (110) oriented sample occurred at the fastest rate as illustrated by the data given in Figure 2.8a. The decay of the phonon mode intensity for the (100) sample orientation is also relatively fast [Fig. 2.8b], but somewhat slower than found for the (110) orientation. The decay profile of the phonon mode intensity for the (111) sample orientation is markedly slower than for either of the other two low index orientations [Fig. 2.8c]. These trends strongly suggest that lithium inserts into and disrupts the crystallinity of both the (100) and {110} planes more easily than the {111} planes. This is corroborated by the cyclic voltammetry of the previously described samples under in-situ Raman spectroscopy [Fig. 2.9]. The voltammograms for the different silicon crystal planes show markedly different current densities and amounts of lithium intercalation during electrochemical lithium insertion. The relative magnitude of charged transfer to the samples with different crystallographic orientation was (111) < (100) < (110). The total charge transferred into the (111) oriented sample was an order of magnitude less (0.98 x 10⁻³ C) than the charge transferred into the (110) oriented sample (20.0 x 10⁻³ C). 3.83 x 10⁻³ C were transferred into the (100) sample.
2.3.4 Strain Anisotropy, Self-Limiting Volumetric Expansion, and Strain-limited Capacity of Model Single-Crystalline Silicon Anodes

Figures 2.10a and 2.10c shows images of a series of micropost arrays similar to those presented in Figure 2.1b but with varied spacing. These structures were spaced at factors of 2x and 5x the size of the latter structure before charging. As before the arrays were fabricated on a (111) wafer, aligning them such that on the two longer sides of the rectangle (110) sidewalls were exposed, while on the two shorter sides (111) sidewalls were exposed. Due to the anisotropy of volumetric expansion, these architectures are expected to predominately expand and fill the volume lying between the (110) sidewalls. The anisotropic strains so engendered can be quite large. For example, galvanostatic charging resulted in the fracture/delamination of a majority of the structures spaced at a factor of 5x, while significantly less delamination occurred for structures spaced at a factor of ¼x, ½x, and 2x [Figures 2.10b,d and 2.11]. In this way, limiting strain by blocking the intercalation of lithium at a fractional charging capacity might provide a possible mechanism to prevent degradation of the anode.

Figure 12 demonstrates the threshold for self-limiting volumetric expansion and the corresponding maximum strain-limited charge capacities for an array that consisted of 10µm wide bars spaced 10 µm apart [Figure 2.12a]. In order to demonstrate the maximum level of volumetric expansion this design can sustain, samples were galvanostatically charged between 2V and .01 V (vs. Li/Li⁺) at different current densities for up to 10 hours [Fig. 2.12a-e]. For a sample charged for 10 hours at a current density
of 36.8 µAcm\(^{-2}\), an effective charge level of 304 mAhg\(^{-1}\) was obtained. The volumetric expansion within 10 hours observed was below the threshold value for expansion-based pinching to limit lithium intercalation [Figure 2.12b,f]. Doubling the charging current density to 73.9 µAcm\(^{-2}\) caused a greater volumetric expansion, reaching a limiting charge storage capacity of 611 mAhg\(^{-1}\) after 10 hours of charging, but as before the expansion of the structures did not block the \{110\} planes’ access to the electrolyte [Figure 2.12c,f]. At a charging current density of 147 µAcm\(^{-2}\), however, a threshold value for volumetric expansion was reached in 9 hours [Fig. 2.12d,f]. Here, as demonstrated by both the filling of the space in between the bars [Fig. 2.12d] as well as the mass transport preclusion of electrochemical lithium insertion along the preferred <110> direction (as noted by the drop in the potential for this current density, Figure 2.12f), a design-limited charging capacity is reached. The strain-limiting charge capacity for this sample was 1135 mAhg\(^{-1}\). Increasing the current density to 289 µAcm\(^{-2}\) leads to the volumetric expansion threshold value being reached in 3 hours (with a corresponding strain-limited charge capacity in this case of 775 mAhg\(^{-1}\)). As evidenced by the SEM images [Figure 2.12e] and electrochemical data [Fig. 2.12f], the volumetric expansion of the silicide along the <110> was sufficient to generally impede access of the electrolyte and lithium ions to this growth interface. An interesting, and as yet incompletely understood, point to note is that similar amounts of expansion were seen in the samples charged at 147 µAcm\(^{-2}\) and 289 µAcm\(^{-2}\) but the amount of lithium taken up for the sample charged at 289 µAcm\(^{-2}\) was less. This suggests that different, and possibly graded, lithium-silicides stoichiometries might be formed at the different
charging current densities. Alternatively, and more likely in our view, is that structural
damage to the anode might be acting to limit the capacity reached at the charging
current density (see below).

Charging experiments also were performed using arrays of micron-sized silicon
bars, ones fabricated with the same cross sectional dimensions and crystallographic
orientations as those shown in Fig. 2.12, but here arraying them with different spacings
(5 and 20 µm were adopted, Figure 2.12g-i). These data confirm expected trends.
Doubling the spacing between the structures to 20 µm approximately doubled the
maximum strain-limited charge capacity when charging at 363 µAcm⁻², in this case to
2833 mAhg⁻¹, while reducing the spacing to 5 µm lowered it to 677 mAhg⁻¹ when
charging at at 125 µAcm⁻². These data strongly support a model in which anisotropic
volumetric expansions serve to mediate what are essentially mass transfer imposed
constraints on first cycle anode capacity.

2.3.5 Capacity Retention of Model Single-Crystalline Silicon Anodes after Multiple
Charge/Discharge Cycles

Limiting the strain based on the design of the structures adopted in Figure 2.12a
did not ensure capacity retention with cycling as might be expected given the
amorphization that accompanies lithium insertion in silicon.[2.17, 2.20, 2.44] Indeed
after three charge/discharge cycles the discharge capacity dropped to approximately
1/10th the discharge capacity found for the first cycle [Fig. 2.13a]. This marked loss in
capacity after the second cycle was further correlated with very high discharge
coulombic efficiencies. The data suggests changes to the anodes have occurred which lead to low charging capacities that, all the same, are capable of operating stably. The mechanisms involved in the changing performance were probed by SEM. The data in Fig. 2.13b show a representative anode after one charge/discharge cycle. The sidewalls of these structures (the areas where lithium intercalation had occurred) were found to have delaminated (or fractured) from the rest of the structure, leaving silicon debris filling the trenches. This reduction in the volume available for expansion of the still electrically active area of the anode appears to limit the subsequent charge and discharge capacities. Cross-sectional SEM of the structures clearly reveals a considerable and highly anisotropic fracture occurs, one running predominately along the \{110\} planes of the silicon at or near the interface with the lithium-silicide [Fig. 2.13d]. A differing anisotropic fracture also occurs after discharging for similar microstructures fabricated on (110) wafers. As previously noted, galvanostatic charging of (110) oriented bars results in significant anisotropic vertical extensions of the silicide phase [Figure 2.7b]. These strains lead to a shedding of the lithiated material via fracture localized along \{110\} (and possibly \{100\}) planes [Fig 2.14]. A possible mechanism driving this failure is critical strains due to the lattice mismatch that likely exists between the (de)lithiated and pristine silicon.

To explore a method to redress the limitations in capacity retention revealed in the data of Figure 2.13, we examined a model for a 3D design that could frustrate their failure modes while still providing large capacities. The capacity retention seen after multiple charge/discharge cycles for arrays of the “tiered” structures fabricated with
quasi 3D design rules [Fig. 2.1c] showed towards this end a marked improvement as compared to the arrays of micron sized bars discussed above. As shown in Figure 2.15, we examined two exemplary designs in which thin platelets were appended to a central bus bar. The specific crystallographic orientation used orients these platelets along the same (111) axis as the bus line. To illustrate general scaling trends, thin (.2 μm, Fig. 2.15a) and thick (.8 μm Fig. 15b) platelets each spaced at 1 μm were examined. The initial, first charging capacity (at a charging current density of 153 μAcm\(^{-2}\) for 10 hours) was largest [Fig. 2.15c] for the thin platelets sample (1770 mAhg\(^{-1}\) vs. 862 mAhg\(^{-1}\), respectively). It is interesting to note that both of these quasi 3D motifs exhibited significantly greater capacity retention after a modest number of cycles as compared to the simple bar samples discussed in Figure 2.13. Further work will investigate the mechanism responsible for the frustration of this anisotropic failure. While these “tiered” structures have better capacity retention than the bar structures, by the third charge/discharge cycle, delamination of some of the central silicon bus bars from the substrate still occurred. Interestingly, the structures with thinner platelets not only experience significantly more deformation of the platelets but also had significantly more bus bars delaminate from the substrate [Fig. 2.15d,e and 2.16]. We postulate that the additional deformation of the thinner, less constrained platelets causes more torque on the bus bar which when amplified by the stress concentration at the substrate induces delamination of a higher portion of the bus bars from the substrate. These suggest structural designs that account for the noted strain anisotropy, and more
importantly remove the silicon from the supporting crystal, might provide a means to construct more durable versions of anodes of this type.

2.4 Conclusions

This paper highlights studies of model single-crystalline silicon microstructures that demonstrate the crystallographic anisotropy of strain evolution, and establish quasi 1D, 2D, and 3D design rules that result in strain-limited performance in model silicon anodes for lithium-ion batteries. The studies described here establish that strain evolution in these materials on charging/discharging is highly anisotropic and drives gradient strain fields which can both degrade and/or be exploited to progress important aspects of materials performance. We illustrate fabrication techniques that can be utilized to create advanced 3D structures with different thresholds that enable capacity retention while still maintaining high capacities. The mechanistic lessons developed in this work are ones we hope to apply in future work that seeks to optimize polycrystalline anode materials with quasi 3D design rules in order to create high-energy density anodes (of silicon and other materials) with long cycle lifetimes.
2.5  References


2.6 Figures

Figure 2.1: Arrays of micron sized single-crystalline silicon a) bars with quasi 1D design rules, b) posts with quasi 2D design rules, and c) "tiered" (platelets connected to a central bus bar) structures with quasi 3D design rules.
Changing individual processes of the protocols enables tailoring of the spacings in all three dimensions. For instance, through changing the mask a design rule can be changed from a) 17 µm x 17 µm spacing between structures and 1 µm spacing between platelets to 8 µm x 8 µm spacing between structures x 1 µm spacing between platelets.

Figure 2.2: SEM images of two different 3D design rules.
Figure 2.3: Fabrication protocols for single-crystalline silicon architectures with quasi 1D, 2D, and 3D design rules.  

a) Arrays of micron sized bars with quasi 1D design rules were fabricated by using photolithography to pattern lines of photoresist (PR) on a single-crystalline silicon substrate and then anisotropic vertical etch areas not masked by PR. 

b) Posts are formed by following a similar protocol as in a) except patterning rectangles of PR instead of lines. 

c) “Tiered” structures with quasi 3D design rules were fabricated by patterning rectangles of PR and then anisotropic vertical etching unmasked areas. Longer etch steps (relative to etching for the posts) during anisotropic vertical etching are used to control the segment of the sidewall that is masked during directional metal deposition. Subsequent anisotropic wet chemical etching undercuts the structures which after metal mask removal results in a central silicon bus bar with platelets. 

d) Demonstration of a large area array of structures fabricated with minimal defects.
**Figure 2.4:** Exploration of lithium intercalation in a single-crystalline (111) silicon wafer using a microstructure of known dimension.  
a) Cross-sectional SEM image of a single-crystalline silicon bar fabricated on a (111) wafer before charging.  
b) Single bar of silicon galvanostatically charged for 1 hour at 123.1 µAcm$^{-2}$ and a plot of normalized silicon counts of the line scan detected by EDS. EDS detected areas of reduced silicon density on the edges of the structures.  
c) A sample with the same cross-section galvanostatically charged for 10 hours at 109.9 µAcm$^{-2}$ and a plot of normalized silicon counts of the line scan detected by EDS. Significant areas of reduced silicon density were observed in the areas of volumetric expansion.
Figure 2.5: Cross-sectional SEM image of (111) single-crystalline micron sized silicon bars a) after 1 hour of galvanostatic charging at 123.1 μAcm⁻² and b) the corresponding EDS data derived from the line scan in a). Cross-sectional SEM image shows the results c) after 10 hours of charging at 109.9 μAcm⁻² as well as d) the associated EDS data from the line scan in c).
Figure 2.6: Cross-sectional SEM images of (111) single-crystalline micron sized bars a) which are 10 µm tall before galvanostatic charging. The height of the bars were roughly reduced by half by adjusting the ICPRIE etching time. b) Charging for 10 hours at 147 µAcm$^{-2}$ resulted in a similar expansion along the (110) direction but with a different concavity (maximum expansion occurs at the top of the 10 µm tall bars) than previously seen in the c) 20 µm tall structure.
Figure 2.7: a) Cross-sectional SEM image of a (111) single-crystalline silicon wafer with {110} (red) and {111} (blue) crystal planes exposed to the electrolyte before and after galvanostatic charging. Galvanostatic charging at 289 µAcm$^{-2}$ for 10 hours caused lateral expansion of the initial silicon structure in the <110> direction. Expansion of the structures in the <111> direction was negligible. b) (110) single-crystalline silicon wafer with {110} and {111} crystal planes exposed to the electrolyte before and after galvanostatic charging. Galvanostatic charging at 334 µAcm$^{-2}$ for 10 hours caused significant vertical expansion of the structures in the <110> direction but minimal lateral expansion in the <111> direction.
Figure 2.8: Plots of c-Si phonon mode peak height vs. potential measured by *in-situ* Raman spectroscopy during electrochemical insertion of lithium ions for a) (110), b) (100), and c) (111) single-crystalline silicon wafers. Each plot is standardized to the onset of phonon decay (solid line). The dashed lines indicate the complete disruption of the crystalline phonon mode. The decay of the phonon mode for (111) crystal plane was significantly slower than the decay of the phonon mode for (110) crystal plane.
Figure 2.9: Cyclic voltammograms of a) (110), b) (100), and c) (111) single-crystalline silicon wafers from Figure 2.8 at a scan rate of 200 μVs^{-1}. Charge transfer was most observed in the (110) oriented samples (20.0 x 10^{-3} C), followed by the (100) oriented sample (3.83 x 10^{-3} C), and least in the (111) sample, .98 x 10^{-3} C.
**Figure 2.10:** Design rules can limit degradation of the electrode. Top-down SEM images of a (111) single-crystalline silicon wafer with an array of microposts spaced at 5x their size a) before galvanostatic charging. b) The microstructure in a) after galvanostatic charging for 10 hours at 73.4 μAcm⁻². A large proportion of the silicon structures delaminated from the substrate. Top-down SEM images of a (111) single-crystalline silicon wafer with an array of microposts spaced at 2x their size c) before galvanostatic charging. d) The same microstructure after galvanostatic charging for 10 hours at the same current density.
**Figure 2.11:** Top-down SEM images of a (111) single-crystalline silicon wafer with an array of microposts laterally spaced at ½x their size. a) before galvanostatic charging. b) After galvanostatic charging for 10 hours at 73.4 µAcm\(^{-2}\). Top-down SEM images of an array of microposts laterally spaced at ¼x their size c) before galvanostatic charging. d) After charging for 10 hours at the same current density.
Figure 2.12: Single-crystalline (111) silicon wafer with an array of 10 µm wide bars spaced 10 µm apart galvanostatically charged at current densities of b) 36.8 µAcm⁻² c) 73.9 µAcm⁻² d) 147 µAcm⁻² e) 289 µAcm⁻² for up to 10 hours. f) Within 10 hours of galvanostatic charging at current densities greater than 73.9 µAcm⁻², the threshold value for volumetric expansion which limits lithium intercalation is reached. Data for galvanostatic charging at various current densities for up to 10 hours of arrays of micron sized single-crystalline silicon bars spaced g) 5 µm and h) 20 microns apart. i) Modulating the spacing between the structures alters the maximum obtainable strain-limited charge capacity.
Figure 2.13: a) Discharge capacity and coulombic efficiency for galvanostatic charge/discharge cycling at 273 μAcm⁻² for 10 hours per half cycle (C/10) of the same architecture in Figure 2.12a. b) An array of micron sized bars fabricated on a (111) silicon wafer after one charge/discharge cycle at C/10. Cross-sectional SEM image of silicon bar after galvanostatic c) charging and then d) discharging at C/10. These images illustrate the anisotropy of not only electrochemical lithium intercalation but also the anisotropy of the failure mechanism.
Figure 2.14: Cross-sectional SEM images of the single-crystalline (110) wafers a) after galvanostatic charging at 334 µAcm⁻² as well as b) charging and discharging at 364 µAcm⁻². The white line denotes that the height of the structure after one cycle is similar to the height of the predominately silicon area after charging.
Figure 2.15: Cross-sectional SEM images of a “tiered” structure with quasi 3D design rules which consists of a) thinner (.2 micron) platelets and b) thicker (.8 micron) connected to a central bus bar. c) Discharge capacities of the “tiered” structures with thin platelets and thick platelets galvanostatic charge/discharge cycled at 153 µAcm⁻² and 172 µAcm⁻² respectively demonstrates better capacity retention than the anodes with quasi 1D design rules. Top-down SEM images of “tiered” structures with d) thinner platelets and e) thicker platelets after the three galvanostatic charge/discharge cycles shown previously. The sample with thinner platelets experienced significantly more deformation and a higher percentage of the central bus bars delaminated from the substrate.
Figure 2.16: SEM images of “tiered” structures with a) thin and b) thicker platelets after 3 galvanostatic charge/discharge cycles at 153 μAcm$^{-2}$ and 172 μAcm$^{-2}$ respectively. The thinner platelets deformed significantly more than the thicker platelets.
CHAPTER 3

MODEL GE MICROSTRUCTURES AS ANODES FOR LI-ION BATTERIES

The results presented in this chapter have been previously published with minor modifications in Brandon R. Long & Jason L. Goldman & Ralph G. Nuzzo & Andrew A. Gewirth, "Model Ge Microstructures as Anodes for Li-ion Batteries", The Journal of Solid State Electrochemistry, 17, 2013, 3015. Used with kind permission from Springer Science and Business Media.

Sample fabrication and electrochemical testing was done by both Jason L. Goldman (UIUC) and Brandon Long (UIUC).

3.1 Introduction

Lithium-ion based energy storage devices are ubiquitous in applications such as consumer electronics.[3.1] Applications in the transportation sector are of extreme interest as well.[3.2] For Li-ion batteries to be more applicable for uses in transportation, improvements in specific energy and power densities, as well as in safety of operation, are desirable.[3.3] Alternatives to the typically used electrode materials are required to achieve the challenging improvements in performance that are necessary.[3.4] Semiconductor electrodes, such as Ge and Si, are able to achieve higher specific and volumetric energy densities than traditional carbonaceous anodes.[3.3,3.5] Both Ge and Si are theoretically able to accommodate 4.4 Li atoms for every one
semiconductor atom; giving theoretical specific capacities of 1623 and 4200 mAhg\(^{-1}\) respectively. These theoretical specific capacities are over 4 and 10 times the theoretical specific capacity of graphitic anodes (372 mAhg\(^{-1}\)). The two materials are comparable in terms of volumetric capacities in which Ge and Si have theoretical volumetric capacities of 8642 and 9783 mAhcm\(^{-3}\) respectively.

The aforementioned beneficial attributes not withstanding, battery designs based on Si or Ge electrodes have found limited practical use owing in part to the large volumetric expansion that occurs in these materials upon lithiation—strains that lead to both poor efficiencies and limited cycle lifetimes.[3.6] Various methods of structuring and morphological control have been implemented as means to improve the cycle life of Ge electrodes, such as carbon composites,[3.7-3.11] thin films,[3.12-3.14] nanowires and nanotubes,[3.15-3.17] and metal substrates.[3.18] Graetz et. al. reported that Ge is a promising high-rate material for Li-ion applications.[3.14] A 250 nm thick nanofilm was capable of retaining 75% of its 1C capacity at a delithiation rate of 1000C. The diffusivity at room temperature of Li in Ge was estimated to be 400 times higher than in Si. The results of X-ray diffraction studies show the final lithiation product formed at room temperature is Li\(_{3.75}\)M (where M = Si or Ge).[3.19,3.20] This reveals that the experimentally realized specific (volumetric) capacities at room temperature are in fact lower than those predicted by theory, being 1384 mAhg\(^{-1}\) (7365 mAhcm\(^{-3}\)) and 3579 mAhg\(^{-1}\) (8338 mAhcm\(^{-3}\)) for Ge and Si respectively.

We recently showed that single-crystalline Si exhibits strongly anisotropic lithiation, showing markedly enhanced Li-insertion along directions transverse to \{110\}
planes. The Si can be microstructured to exploit this strain anisotropy as a means to tailor its capacity and cycle life.[3.21] Although Ge has the same diamond unit cell and the same theoretical lithiation stoichiometry of 4.4 Li atoms, it does not exhibit the same anisotropy and dopant effects upon lithiation that Si does.[3.22] As a result, strains developed in microstructures of Ge are not expected to perform in the same manner as is found in Si. The work in this paper is aimed at exploring design rules that might be used to exploit transport related effects in the charging of Ge microstructures, doing so to mitigate strains in ways that can enhance capacity retention after multiple charge/discharge cycles. We present data on the fabrication and electrochemistry of single-crystalline Ge microstructured electrodes, examining the effect of Cu coating on lithiation. We show that the Cu coating combined with a microbar geometry can enhance the cycle life of Ge when coupled with limited volumetric expansion below the full theoretical capacity of the semiconductor.

3.2 Experimental

Ge single crystal wafers were purchased from MTI Corporation and had a resistivity of ≈ 0.008 Ωcm. The fabrication process used followed with slight modifications a method previously reported.[3.23] Before processing, the Ge wafers were rinsed with water, isopropanol, and then dried at 110°C for 5 minutes. An AZ 5214 (Clariant) photoresist was spun onto wafers at 3000 rpm for 30 seconds. The wafer was baked at 110°C for 1 minute before UV exposure. The photoresist was exposed using a Cr mask with the desired exposure pattern using a standard mask aligner. The total exposure was typically 75 mJcm⁻². The photoresist was developed in AZ 327MIF
(Clariant) for 1.5 minutes and then dried with N₂ gas. Finally, the electrode was baked at 110°C for 7 minutes in order to provide resilient resist structures for etching.

Masked samples were vertically etched anisotropically using a Bosch process—an Inductively-Coupled-Plasma Reactive Ion Etching (ICPRIE) using a STS Mesc Multiplex Advanced Silicon Etcher. Relatively smooth sidewalls were achieved by using 7 second etch and 5 second passivation steps, respectively. After etching, the samples were sonicated for 5 minutes in an acetone bath and then an isopropanol bath to remove residual photoresist.

After microfabrication, a 10 nm Ti adhesion layer and then a 100 nm Au layer were deposited on the backside of the electrode to act as a current collector using e-beam evaporation (Temescal). For the Cu coated samples, 50 nm of the metal were deposited on the top surfaces using e-beam evaporation. Microstructure dimensions were verified using scanning electron microscopy (SEM).

Electrochemistry was performed using a one compartment air-tight cell in an Ar filled glovebox. A two electrode configuration was used, with Li metal acting as a counter/reference electrode. The solvent used was 1 M LiClO₄ in 1:1 (v) EC:DMC (Sigma-Aldrich). An Arbin cycler was used for the cycling studies, while a CH Instruments electrochemical workstation was used for the microscopy characterization experiments. The C rates were calculated from the practical capacities discussed in the introduction section.
3.3 Results and Discussion

3.3.1 Microbar Fabrication

Ge microbars were fabricated using traditional photolithographic processes. Figure 3.1 shows electron micrographs of representative microstructures, microbars etched into a single-crystalline Ge (111) wafer, prior to Cu deposition. The microbars examined in this work were 13 µm wide with a 17 µm void space between adjacent features (i.e. 13 × 17 µm). The microbar depth was held in the range 40 ± 5 µm. Large areas of the pattern can be made on Ge wafers as shown in Figure 3.1a. The area patterned for this study was 1 × 1.5 cm. Figure 3.1b illustrates the uniformity and relatively smooth sidewalls of the resultant Ge microbars at a higher magnification. As a result of the Bosch process and cleaving of the wafers, the top surface of the microbars is the (111) crystallographic face while the sidewalls are the (110) face, as shown in Fig. 3.1 by red and blue respectively. Cu deposition resulted in a Cu coat on the top of the Ge microbars and at the bottom of the trenches with minimal sidewall deposition as measured by energy dispersive X-ray spectroscopy (EDX). As we show below, this non-conformal deposition exerts a strong impact on the character of the Li insertion seen.

3.3.2 Electrochemical Characterization

Electrochemical measurements were used to examine whether the microbar Ge electrode impacts stability during lithiation in a way differing from that found for planar Ge electrodes. The literature has yet to definitively show microstructuring dramatically improves the charging dynamics of this material. For example, prior work has shown
that small (albeit commensurately sized) Ge particles (ca. 40 µm) are only capable of ca. 5-6 cycles before complete loss of capacity.[3.14]

Figure 3.2 shows lithiation and delithiation capacities and SEM micrographs for exemplary microstructured Ge of the type shown in Fig. 3.1 when cycled both with and without a Cu coating. The micrographs show that the lithiation in this case is largely confined to the near surface region of the wafer (i.e. of the textured bars). For this reason, the specific capacities cited below were determined considering only the material present in the microstructured region of the Ge electrode. Figure 3.2a shows that lithiation capacities as high as 1384 mAhg⁻¹—close to the capacity limit[3.20]—were obtained for as many as 3 cycles. The coulombic efficiency of the delithiation cycle, however, was always less than unity. This irreversible capacity loss increased markedly as the electrode was cycled until little lithiation capacity was left at cycle number 4. Figure 3.2a also shows the cycle performance of a bulk Ge wafer without microstructuring. The bulk wafer is capable of 1 cycle before a complete loss of capacity. After 1 cycle, the several 100-mu-thick wafers fractured and the bulk of the active area became electrically isolated. This effect is likely due to the strain developed in the bulk wafer upon lithiation.

The steady decay in the coulombic efficiency shown in Fig. 3.2a is similar to that found in other studies using Ge electrodes.[3.24] The origin of the capacity loss originates from mechanical instabilities due to volume changes occurring during the lithiation/delithiation process.[3.25,3.26] Figure 3.2c shows the corresponding electron micrograph of the bare Ge microstructure after the first cycle lithiation to 85% of its
practical specific capacity. As can be seen the microbars have expanded into contact with each other. Also there is noticeable disruption of the bulk Ge substrate due to lithiation at the bottom of the trench. The disruption and expansion likely result from substantial stresses arising during the lithiation process.

Figure 3.2b shows the effects of a 50 nm Cu layer on the cycling properties of the Ge microstructure. The Cu layer is inert towards Li insertion and must, as a result inhibit lithiation of the bulk part of the Ge crystal to some degree. Figure 3.2b shows that the Cu layer in fact acts to decrease irreversible capacity losses and improves the coulombic efficiency for the first 3 cycles, extending the life of the Ge microstructure by 2 cycles. Figure 3.2d shows the corresponding electron micrograph for the Cu coated Ge microstructure lithiated to 85% of its practical specific capacity. The volumetric expansion encountered by the microbars is again sufficient to cause contact between neighboring microbars. There is also noticeable delamination of the microbars from the bulk Ge substrate. Thus, lithiation of the Ge microstructure to 85% capacity leads quickly to its destruction.

The lithiation seen here is more isotropic in that expansion along the <111> direction (13 μm for bare and 8 μm for structures with a Cu coat) and is similar to that found along the <110> (10 μm for both of these samples). Comparable structures in single-crystalline Si exhibit minimal vertical expansion for structures with this crystallographic orientation.[3.21] A more isotropic expansion of Ge relative to Si is expected and results from the lower band gap of Ge compared with Si,[3.22] leading to a little difference in the potential to lithiate the (110) and (111) faces of Ge. This lower
overpotential to lithiate the (111) face of Ge relative to Si prevents Ge from reaching a self-limiting charging state as seen in Si microbars.[3.21]

The poor behavior of the Ge electrode upon lithiation is related to the more isotropic volumetric expansion of the material. There is no thermodynamic difference for Li insertion into different Ge crystal faces, in contrast to that found for Si.[3.22] A horizontal expansion of 130 % would lead to the Ge structures coming into contact with each other, however, a volumetric expansion of 370 % is expected for full theoretical lithiation.[3.7, 3.27]

Limiting the amount of charge that is stored in the electrode material and, therefore, its volumetric expansion can increase the cycle life.[3.28–3.30] In order to evaluate this effect on cycle life, partial lithiation was performed on Ge electrodes, supporting the microbar structural motif.

Figure 3.3 shows the cycle performance and SEM micrographs for Ge microbars which are partially lithiated to 40% of their practical capacity. The bare Ge microbar electrode [Figure 3.3a] is capable of much longer-term cycling relative to the fully lithiated bare Ge electrode [Figure 3.2a]. The first four cycles show irreversible capacity loss, most likely associated with the formation of the SEI. After the first four cycles the electrode exhibits high coulombic efficiency for approximately 20 cycles, at which time the delithiation capacity begins to slowly decay. This decay is similar to that found with other Ge electrodes.[3.18] The inset in Figure 3.3a shows the voltage profile for the lithiation and delithiation curves for cycles 1, 3 and 20. The 1st cycle lithiation curve shows a sharp onset to the crystalline Ge lithiation at lower potentials. The 3rd and 20th
lithiation curves are similar, indicating the Ge microstructure has undergone a crystalline to amorphous structural transition that yields a state for the Ge that is more electrochemically stable. The delithiation curves for all three exhibit similar voltage plateaus and only differ by the amount of charge removed from the electrode.

Figure 3.3b shows the effect of a 50 nm Cu coating on the partial lithiation of Ge microbars. As was the case for the data for electrodes without Cu [Figure 3.3a], there is an irreversible capacity loss seen for the metal-overcoated sample during the first several cycles, but its magnitude is markedly decreased as evidenced by the higher delithiation capacities. After 20 cycles the delithiation capacities begin to decrease, but the Cu coated electrode stabilizes and retains a higher delithiation capacity at higher cycles relative to the uncoated electrode. The Cu coated Ge microbar has a coulombic efficiency of 95% at cycle 43. The use of Cu coating is expected to block lithiation on certain faces of the Ge microbar and results in selective lithiation that should more closely mimic anisotropic lithiation in directions transverse to the sides of the bars.

Figures 3.3c and 3.3d shows the SEM micrographs for bare and Cu coated Ge electrodes that were partially lithiated to 40% and cycled. The micrographs were taken after 3 full cycles and then after the lithiation on the fourth cycle. The bare Ge microbar electrode in Figure 3.3c shows volumetric expansion and significant bulk Ge substrate lithiation; whereas the Cu coating combined with the charge limiting shows improved mechanical stability [Figure 3.3d]. The Cu coating at the bottom of the trench significantly blocks lithiation of the bulk Ge substrate which leads to the increased stability at high cycle numbers [Figure 3.3b].
Since the diffusivity of Li is 400 times higher in Ge than in Si electrodes,[3.14] we investigated whether the Ge microbars might delithiate faster than those made from Si, to determine whether either might perform better at increased rates. Figure 3.4 shows the effect of increasing C-rate on delithiation capacities for 13 × 17 μm uncoated structures made from both Ge and Si. The microstructured electrodes were lithiated to 40% capacity at a rate of C/20 for each cycle. The delithiation capacities shown are normalized to the lithiation capacity on the first cycle for both materials. The Ge and Si microbar electrodes both show complete delithiation at C/10 and C/5 rates. At a delithiation rate of C the Ge microbar electrode shows zero delithiation capacity, while the Si retains full delithiation capacity. Both materials fail at a delithiation rate of 2C, as Ge and Si microbar electrodes both show zero delithiation capacity at this cycle rate.

The results presented in Figure 3.4 show that the high diffusivity of Li in Ge is not the only property necessary for a high-rate microstructured electrode. Design rules, and their impacts on mass transfer dynamics, must also be taken into account for high-rate microstructures. We believe the poor performance of the Ge microbars, relative to Si, is due to the more isotropic expansion seen in Ge, as revealed in the images shown in Figure 3.2.

It is now well established experimentally [3.21] and theoretically [3.31] that Si microstructures featuring (110) sidewalls lithiate with a much higher strain-limiting anisotropy. Chan et al. attributed this characteristic expansion to the thermodynamic favorability of Li insertion in the (110) sidewalls relative to the (111) top and trench surfaces.[3.31]
In contrast to the Si case there is no thermodynamically favored surface for lithiation in the case of Ge. There is, consequently, no curvature of the Ge microbars upon lithiation. In the particular form factor used here, the sidewalls expand during lithiation and run into each other. This leads to blockage and a decrease in exposed area for lithiation and delithiation. In the pristine microstructures examined the sidewalls account for 86% of the exposed microbar surface area. During delithiation, this surface area is inaccessible. Consequently, we expect that the rate performance of the Ge microbars is limited by the Li removal through the top surface, as is in fact observed. Microstructures for high-rate applications would need to take this into account when being designed.

3.4 Conclusions

In this paper, we have shown the effects of microstructures and Cu coating on the lithiation of model crystalline Ge microbar electrodes. We found that Ge microbar electrodes exhibit improved cycle life relative to bulk Ge wafers with a lithiation that is more isotropic than is seen for comparable Si microbars. Full lithiation of Ge microbars resulted in limited cycle life resulting from mechanical degradation. Limiting the charge significantly improved the cycle life of microstructured Ge electrodes by decreasing the mechanical degradation. Cu coating further improved the cycle life and capacity retention by selective lithiation of microbar sidewalls and limiting lithiation of the bulk Ge wafer substrate. Delithiation rate studies were performed to compare Ge and Si microbars, and it was found that—even though the Li diffusivity in Ge is significantly higher than Si—these Ge microstructures exhibit poor performance at high delithiation
rates. The likely origin of this is blockage of the sidewalls which run into each other in the form factor used here due to the isotropic lithiation found with Ge. The results presented here may provide guidance on design rules for advanced high-rate battery anodes using structured electrodes.
3.5 References


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Sources 119–121:64–68

3.6 Figures

**Fig. 3.1:** a) SEM image of Ge microbars after microfabrication process showing the large area of structures. b) Higher magnification SEM image showing the smooth sidewalls and uniformity of the microbars. Red top surface indicates (111) while blue sidewall surface represents (110).
**Fig. 3.2:** Specific and volumetric capacities as a function of cycle number for a bare Ge microbar (circles) and bulk Ge (squares) a) and 50 nm Cu coated Ge microbar b). Lithiation (solid features) and delithiation (hollow features) capacities are shown for the structures at a C/20 rate. Electron micrographs from bare c) and Cu coated d) Ge microstructure after first cycle lithiation.
Fig. 3.3: Specific and volumetric capacities for a) bare Ge and b) 50 nm Cu coated Ge. Lithiation (filled circle) and delithiation (empty circle) points are shown for 40% partial lithiation at C/20. Inset in (a) shows the lithiation and delithiation voltage profiles for the 1st (solid black), 3rd (dotted blue), and 20th (dashed red) cycles. Electron micrographs after 4th partial lithiation for bare c) and Cu coated d) Ge microstructures.
**Fig. 3.4:** Delithiation capacities of Ge microbars (filled circle) and Si microbars (empty square) of the same dimensions at varying rates. Lithiation for each cycle was to 40% capacity at C/20.
CHAPTER 4

IN-SITU X-RAY REFLECTION INTERFACE MICROSCOPY (XRIM) ON SINGLE-CRYSTALLINE SILICON DURING ELECTROCHEMICAL LITHIUM INSERTION

The results presented in this chapter have previously been published with minor modifications. Reprinted with permission from Tim T. Fister, Jason L. Goldman, Brandon R. Long, Ralph G. Nuzzo, Andrew A. Gewirth, and Paul A. Fenter, “X-ray diffraction microscopy of lithiated silicon microstructures”, Appl. Phys. Lett. 102, 131903 (2013). Copyright 2013, AIP Publishing LLC.

X-ray experiments and modeling were done by Tim Fister (Argonne), Brandon Long (UIUC), and Paul Fenter (Argonne)

4.1 Introduction

Enthusiasm for silicon’s unrivaled gravimetric capacity for lithium (up to Li_{4.2}Si) is often tempered by its rapid performance loss over repeated cycles.[4.1] This poor cycling behavior originates from the large volume expansion of silicon (up to 400%) during its first discharge,[4.2] which, at room temperature, destroys its crystal structure[4.3] and can lead to pulverization or delamination from its current collector over repeated cycles.[4.4] Several groups have found that controlling silicon’s morphology—using etched microstructures,[4.5] nanowires,[4.6] patterned thin films,[4.7] or even ‘nanoscoops,’[4.8] for example—can improve the reversibility of the
lithiation. Electron microscopy has revealed the extent of silicon’s expansion in post-mortem electrodes,[4.4-4.6] but this approach is challenging to implement in situ, e.g. in the organic liquid environment of a lithium ion battery.[4.9] Furthermore, internal strain analysis often requires use of a focused ion beam, which can further damage such structures.[4.10] Using an alternative approach, we have applied x-ray reflection interfacial microscopy (XRIM)[4.11] to explore changes in the crystal structure of silicon microposts before and after lithiation. We find high diffraction contrast from the posts themselves, which allows for real-time, in-situ measurements from a wide range of patterned heterostructures in the future. In this study, XRIM is found to be sensitive to the size and internal crystallinity of the posts, in agreement with scanning electron microscopy measurements.

4.2 Experimental

A schematic of the XRIM experiment is shown in Figure 4.1. Working at 10 keV (λ = 1.24 Å), the sample is oriented in a symmetric “θ/2θ” geometry, such that the x-ray’s momentum transfer (q) is oriented vertically from the sample. Much like an optical microscope, Fresnel zone plates (FZPs) act as the condenser and objective focusing optics. An order sorting aperture (OSA) and slits are used to isolate the image with respect to unfocused x-rays due to the low efficiency of x-ray optics. At an incident angle of 11.06°, the size of the beam on the sample is 1x5 μm². This instrument has a 400× magnification (20× X-ray magnification from the objective FZP, illuminating the X-ray phosphor, followed by a further 20× optical magnification) and a CCD camera with an array of 1024x1024 13 mm pixels. Therefore each pixel of the detector images an
equivalent 33x170 nm² region on the sample. The resolution of this XRIM experiment is
170 nm (obtained from images of sub-nm high steps on an orthoclase crystal), well
below the size of the silicon microposts. Further details on the experiment and
interpretation of the images have previously been discussed.[4.11,4.12]

The silicon microstructures were patterned on (111) N-type (phosphorous-doped
doping) silicon wafers. The wafers were cleaned with NoChromix prior to
photolithography. The wafers were then patterned with positive AZ 5214 photoresist by
exposing wafers spin-coated with photoresist through chrome masks and then
developing in AZ327 MIF. Subsequent etching and passivation steps (Bosch process),
using inductively coupled plasma reactive ion, removed silicon from areas not coated by
photoresist. Residual photoresist and fluoropolymer were removed by cleaning with
acetone, IPA, and RCA1. The scalloping of the sidewalls produced by the repeated
isotropic etching and passivation of the Bosch process were removed via an immersing
in a KOH-based solution at 100°C. A current collector (15/100 nm of Ti/Au) was
deposited on the backside of the wafers by physical vapor deposition. Epoxy was used
to define the electrochemical active area of the sample.

Electrochemical experiments were conducted inside an argon filled glovebox
(<1ppm O₂). The setup consisted of a three electrode cell with lithium metal as the
counter and working electrodes fully immersed in 1.0 M LiPF₆ in a 1:1 mass ratio of
ethylene carbonate/dimethyl carbonate (Novolyte). Figure 4.2 shows the
electrochemical behavior of the samples. To ensure good electrochemical behavior,
cyclic voltammetry (CV) was run on duplicate samples between 2.0 and 0.01 V (vs.
Li/Li+) at 0.001 V/sec. The reductive feature at 0.1 V on the cathodic scan of the CV [Fig. 4.2b] corresponds to the lithiation of Si resulting in an amorphous Li\textsubscript{x}Si composition. For the samples examined using XRIM, galvanostatic discharging was run at 3579 mA/g corresponding to a rate of C/21 (21 hours to charge or discharge). Figure 4.2a shows the samples that were lithiated for 12 hours, which corresponds to 56% of the theoretical specific capacity of Si posts.

4.3 Results and Discussion

An XRIM image taken after partial lithiation of the posts is shown in Fig. 4.3. In the raw image [Fig. 4.3a] the lateral field of view is defined by the vertical detector slits. The images were measured at $q = 1.94 \text{ Å}^{-1}$, near the Si(111)-diffraction peak, which is located at 22° at 10 keV. With an incident angle of 11°, the image is effectively compressed along the vertical ($2\theta$) direction by a factor of 5.2. While the entire substrate is expected to diffract strongly at this condition, the image clearly shows the expected post structures with positive and negative contrast of up to 40%. The background signal from the unfocused beam and the slits were eliminated by extrapolating the background using a two-dimensional interpolation, combined with a Gaussian filter having a width matching the natural resolution of the XRIM optics. The intensity is offset so the minimum reflectivity (corresponding to the missing posts) in the image is zero and then scaled so that the basal plane reflectivity is one. The resulting images, now plotted as $R/R\text{base}$, are shown in Fig. 4.3b–4.3d with corresponding vertical and horizontal cross-sectional cuts.
Several factors can contribute to diffraction contrast in an XRIM experiment including: (i) topography, such as unit cell edge steps;[4.12] (ii) changes in \(d\)-spacing and film thickness, and overall crystallinity;[4.13] (iv) surface and interfacial roughness; and (v) x-ray absorption and resonant scattering;[4.14] These factors largely depend on nanoscale topological changes. In this case, XRIM is sensitive to surface reflections from the top of the posts \((R_{\text{top}})\) and the basal plane \((R_{\text{base}})\). The strong observed contrast, observed at \((h,k,l) = (0.99,0.99,0.99)\), is largely due to the physical offset of the X-ray beam when it is reflected from the top of the post with respect to that from the wafer surface, and the associated dark region due to the lack of a surface below the posts. This leads to bright and direct regions in the CCD image. As shown in Fig. 4, the reflectivity from the top of a post is offset by a factor \(h \cos \theta\). This shift appears offset by \(h \cot \theta\) on the CCD image since images are compressed by a factor of \(1/\sin \theta\) in the \(2\theta\)-direction of of the CCD \((y_{\text{CCD}})\). This results in an image of the post with postive net diffraction contrast \((R_{\text{top}} + R_{\text{base}})/R_{\text{base}}\). because the reflected image of the top of the post overlaps with the reflected signal from the basal plane, since there is no reflected signal from the basal plane underneath the post, a “shadow” with zero reflectivity appears at the original position of the post on the CCD, as outlined by the dashed lines in Fig. 4. Attenuation of the beam through the post makes the background near the shadow to appear sloped, as shown in Fig. 4. For the 6x6 \(\mu\text{m}^2\) silicon features in this experiment, this is less than a 5% effect in the CCD image. This description for a single post can be
generalized for an array of posts by simply adding their reflections and shadows. Similarly, more complicated features can be described by treating this process in the continuum limit, e.g.

\[ R(x_{\text{ CCD}}, y_{\text{ CCD}} \sin \theta ; z, \theta) = \int R(x, y + z \tan \theta , z) \, dz. \]

For the structures shown in Fig. 4.3, we designed 10 µm tall 6x6 µm² blocks that repeat with 10 and 17 µm spacing in the horizontal and vertical directions respectively. Using the process described above, the reflected image of enhanced and dark regions due to the posts are separated by \( h \cot \theta = 51 \) µm vertically, which leads to an overlap between a reflected image of a post with the dark region from its third neighbor. In general, we found posts with contrast higher than the reflectivity from the basal plane. This indicates that \( R_{\text{top}} > R_{\text{base}} \), likely due to roughening of the Si basal plane from the photolithographic etching procedure. Assuming nearly perfect reflectivity at the top of the posts, the reflectivity enhancement of \( R/R_{\text{base}}=3 \) [Fig. 4.3] would indicate 7.0 nm rms roughness in the etched basal plane.[4.15] The transition from “light” to “dark” posts in Fig. 4.3b is likely due to several missing posts that were removed during the liftoff procedure or during lithiation.

Having developed a formalism for understanding the XRIM diffraction contrast of the silicon micropost array, we now compare images of a single post measured before and after partial lithiation. As seen in Fig. 4.5, the lateral size of the post’s x-ray reflection associated with its crystalline core is reduced after lithiation, as expected.
There is no shift vertically between reflection and shadows of each post, indicating that the post height stays is minimally changed during lithiation. SEM images taken after the XRIM experiment [Fig. 4.5e and 4.5f] confirm that the microposts expanded laterally, indicating that the lithiation occurs preferentially on the sidewalls, reducing the crystalline portion of the posts in this direction. The posts appear to lithiate more greatly in the direction normal to the (110)-planes, in agreement with the a larger change seen in the XRIM images. However, the posts appear to expand nearly twofold in this direction, which is significantly greater than the 13% reduction found in the XRIM images. This indicates that the perimeter of the posts is significantly lithiated (up to Li$_{4.4}$Si) and possibly contains some solid electrolyte interphase (SEI) compounds, as indicated by the irreversible portion of the cyclic voltammetry taken on a duplicate sample [Fig. 4.2b].

4.4 Conclusions

The XRIM results are in close agreement with the original study by Goldman et al., who found that similar (111)-oriented posts lithiate preferentially at their (110)-sidewalls.[4.5] The thermodynamic origin of this behavior in crystalline silicon has also been discussed recently from a theoretical standpoint.[4.16] With planned improvements in resolution (ideally, ~50 nm), field-of-view, and throughput, the XRIM system will be able to resolve temporal changes in a large number of posts over repeated cycles in a working battery. The ability to resolve lateral heterogeneity opens the possibility of using XRIM to simultaneously image a wide range of controlled architectures. The high penetrating power of x-ray through liquid environment will
enable *in-situ* observations of the lithiation process which will be extremely valuable toward understanding structural changes in a variety of electrochemical systems.

Additional work was done to fabricate samples for *in-situ* measurements. Samples were prepared with an array of silicon microstructures surrounded by Ni fiduciaries [Figure 4.6]. These Ni structures would be detectable in XRIM and SEM and would enable investigation of the same spot on the microstructure before and after electrochemical lithium insertion / removal by both techniques. Additional work would need to be done to minimize decomposition of the electrolyte due to the X-ray beam, possibly by replacing the conventional electrolyte used in the previous experiments with an ionic liquid-based electrolyte.
4.5 References


4.6 Figures

**Figure 4.1:** Schematic of the XRIM setup including the major optical components, including the Fresnel zone plates (FZPs), order sorting aperture (OSA), sample, and CCD detector. The crystallographic directions that are indicated corresponding to the low-index silicon lattice planes are shown for reference. The circular inset illustrates the footprint of the beam on the micropost array.
Figure 4.2: a) Galvanostatic discharge data at 15 µA was used to partially lithiate the micropost sample. b) Cyclic voltammetry was measured for a duplicate sample to confirm typical silicon lithiation behavior (ΔE/Δt = 1 mV/s). The irreversible feature at 1.4 V during the first discharge is likely due to solid electrolyte interphase formation.
**Figure 4.3:** a) A CCD image before and after background subtraction of the partially lithiated posts. The dashed white lines surrounding each post indicate regions excluded from the interpolated background. b) In the background-subtracted ("residual") images, zero intensity is equivalent to the average reflectivity from the basal plane of the micropost array. The edges of the slits are faintly visible after background subtraction. The color bars for parts a) and c) are given in units of cts/sec/pixel. d) A vertical profile of the posts was taken from the projection of the tall box in part b. c) Similarly, horizontal cross-sections from the wide boxes labeled “1”-“4” are shown.
Figure 4.4: a) Schematic mechanism for scattering from a single micropost and its corresponding CCD image. The reflected intensity at the CCD is given by the red profile, with a dashed profile shown to illustrate the effect of attenuation through the post. Changes from the basal plane reflectivity ($R = R_{\text{base}}$) are found from scattering from the top of the post ($R = R_{\text{base}} + R_{\text{top}}$) and shadowing from the post itself ($R = 0$). The scattering conditions for these two scenarios are shown by the darker and dashed red lines respectively. b) Using the relative spacing of the posts along the $y_{\text{CCD}}$ direction, the total reflectivity is shown for one, two, and three posts.
Figure 4.5: XRIM images from a single post are shown before a) and after b) partial lithiation. The left and right sides of the post correspond to the (110) planes and the top and bottom correspond to the (112) planes. Cross sectional cuts of the XRIM images taken vertically c) and horizontally d) reveal that the crystalline part of the post has shrunk by 5% and 13% respectively (as measured by their FWHM). The regions used for the cross-sectional images are shown by the white outlines in a) and b). Comparison with cross-section e) and plan-view f) SEM taken after the XRIM measurement confirms that the posts have lithiated in the lateral direction, with increased lithiation in the horizontal direction along the (110) planes of each post. The SEM image in f) is oriented in the same direction as the XRIM images in a)-d) and in Fig. 3.
Figure 4.6: SEM image of Si microstructure array with Ni fiduciaries.
CHAPTER 5

DIRECTED TRANSPORT AS A ROUTE TO IMPROVED PERFORMANCE IN MICROPORE-MODIFIED ENCAPSULATED MULTILAYER SILICON ELECTRODES

The results presented in this chapter have been previously published with minor modifications. © The Electrochemical Society, Inc. 2013. All rights reserved. Except as provided under U.S. copyright law, this work may not be reproduced, resold, distributed, or modified without the express permission of The Electrochemical Society (ECS). The archival version of this work was published in Jason L. Goldman, Michael W. Cason, David J. Wetzel, Henning Vieker, André Beyer, Armin Gölzhäuser, Andrew A. Gewirth, and Ralph G. Nuzzo, “Directed Transport as a Route to Improved Performance in Micropore-modified Encapsulated Multilayer Silicon Electrodes“, J. Electrochem. Soc. 2013 160(10): A1746-A1752.

5.1 Introduction

Lithium-ion batteries are utilized as system level components in modern technologies of diverse form, with applications that include the smart electric grid infrastructure, transportation systems, medical devices, military equipment, and portable electronics.[5.1-5.9] Improvements in these batteries—in terms of energy density (Whkg⁻¹), power density (Wkg⁻¹), current density (Ag⁻¹), coulombic efficiency (fraction of recovered charge per cycle), multi-cycle lifetime, and safety—while maintaining low costs are particularly critical for improving the range and cost of
electric/hybrid-electric vehicles and smoothing intermittent renewable energy generation.[5.2, 5.5, 5.6, 5.8]

In lithium-ion batteries, energy is stored and released through electrochemical reactions of lithium ions with two different electrodes, the anode and cathode, which presently are comprised most commonly of graphitic carbon and a lithium ion inserting oxide such as LiCoO₂, respectively.[5.5] The electrolyte—a lithium salt dissolved in non-aqueous solvents—and a permeable polymer film (separator) facilitate ion transport between the electrodes while preventing short-circuiting due to their physical contact. The electrolyte also plays an additional role in mediating the stable operation of the batteries via reactions with the electrodes that form passive solid-electrolyte interfaces/interphases (SEI) within the range of the safe operating electrochemical potentials.[5.10-5.12]

Higher energy/power density electrode materials (than conventionally used carbon anodes and LiCoO₂ cathodes)—whilst maintaining safety—are required for the next generation of lithium-ion batteries.[5.5, 5.13] Silicon anodes for lithium-ion batteries have the highest achievable theoretical gravimetric capacity (4200 mAhg⁻¹ compared to 372 mAhg⁻¹ for a carbon anode). The lithiation of silicon to Li₄.₄Si, however, is accompanied by ~400% volumetric expansion. In simple, flat morphologies this large mechanical strain typically results in fracture of the electrode and the loss of electrical contact after only a few cycles.[5.13, 5.14]

Most form factors of commercial lithium-ion cells, such as cylindrical, pouch, and coin cells consist of thick anode and cathode films (tens to hundreds of microns).[5.5]
These films are a mixture of active material, conductive carbon (e.g. acetylene black), and a polymer binder cast in the form of a slurry and dried to a current collector such as copper foil, with carbon-based anodes typically using a polyvinylidene difluoride (PVdF) binder.[5.5] The substitution of Si for C in such cells has proven challenging and many approaches have been explored to mitigate the degradation of silicon during (dis)charge of the electrode to improve cycle lifetime. There has been some success using PVdF binders with silicon particles, but recent developments of binders such as carboxymethyl cellulose[5.15] and sodium alginate[5.16] have improved the long-term cycling efficiency of silicon. The use of inactive—or less active—additives to the silicon laminate matrix to form composites has also been explored as a means of buffering the expansion of active silicon and in some cases shown to improve the electrical conductivity of the film.[5.13, 5.17-5.20]

The size of the silicon particles, as well as the particle morphology, can have a considerable impact on the durability of the electrode. Silicon nanoparticles, as well as nanowires, nanotubes, and nanorods, have demonstrated near theoretical capacities over tens to hundreds of cycles with fast rate capability.[5.14, 5.18, 5.21-5.25] Recently, Cui et al. demonstrated electrodes consisting of yolk-shell[5.26] silicon-carbon nanoparticles and double-walled silicon nanotubes[5.27] that isolate the silicon surface from direct exposure to the electrolyte during cycling. This design is proposed to mitigate the continual formation of SEI during cycling and provide mechanical support to the silicon, allowing for thousands of (dis)charge cycles versus lithium metal.
Binderless thin films of silicon less that 500 nm thick, such as those deposited via sputtering, have been shown to withstand the stresses of volumetric expansion and contraction for a thousand (dis)charge cycles, but suffer from low area normalized capacity.[5.28-5.31] In an effort to increase the area normalized capacity, electrode concepts aimed at microbattery applications featuring thin silicon films deposited on three-dimensionally patterned substrates are being explored.[5.32, 5.33] Another binderless approach utilizes porous silicon electrodes that can have moderate capacities for hundreds of cycles and good rate capability.[5.34-5.36]

In an earlier paper we demonstrated a self-strain-limiting behavior in model single-crystalline silicon anodes exploiting the crystallographic-dependent anisotropy of the electrochemical lithium insertion reaction to do so.[5.37] Herein we demonstrate an approach to strain mediation, one that exhibits reduced capacity loss upon (dis)charge cycling via a new—non-crystallographic dependent—form of anisotropic lithium transport that exploits encapsulation of a micropore-modified silicon anode. Relatively thick (4 microns) binderless, free-standing silicon films of this form have been cycled in full cells versus commercial LiCoO₂ cathodes. This method utilizes the advantages of microlithography in order to fabricate well-defined microstructures, enabling the investigation of a geometric design rule relating rate capability and volumetric capacity.

5.2 Experimental
The process flow—the series of photolithography and etching steps—used to fabricate the Cu/Si/Cu anode is shown in Figure 5.1. The process scheme utilizes standard semiconductor fabrication methods to construct the prototypes needed to provide proof of concept design attributes for model anodes of this type. Previous data[5.37-5.40] affirm that the crystallinity of the silicon is lost during cycling, and for this reason, a single-crystalline source material is not required. We do so here, however, to facilitate the ease of fabrication using silicon-on-insulator (SOI) wafers obtained from Ultrasil Corporation as a source. The wafers consisted of a 4-50 micron silicon (device) layer; for the samples tested, the N-type (phosphorous-doped, resistivity of 1-10 ohm-cm) device layer had a (100) orientation. Before photolithography, silicon samples were cleaned using Nanostrip (Cyantek) and rinsed with DI water. Photolithographic patterning was performed using AZ 5214 (Clariant) photoresist and exposed to UV light using a patterned chrome mask and a mask aligner (MJB3 Mask Aligner, Suss Microtech), followed by development in AZ 327 MIF (Clariant). Bosch Process etching of the exposed regions of the silicon samples was performed using inductively coupled plasma reactive ion etching (ICP-RIE) on an STS Mesc Multiplex Advanced Silicon Etcher. The samples were then cleaned with acetone, isopropyl alcohol (IPA), and RCA1. The device layer (handle) was then released from the SOI wafer by etching the buried oxide layer with concentrated hydrofluoric acid (HF, 49%). Electrodes with varying arrays of channels (through altering channel geometry, size, or spacing) can be produced over large areas (mm by mm) with minimal defects [Figure 5.2].
Photoresist (AZ 5214) was spin coated onto a glass coverslip (same procedure as above) and baked for 10 minutes at 110 °C. The silicon was then transferred to the photoresist-coated slide. 100 nm of copper was directionally deposited (normal to the film) using an electron beam deposition instrument (Temescal). The samples were then removed from the glass slide, flipped over, and cleaned in IPA. A final 100 nm film of Cu was deposited on the silicon surface in the same manner as above.

Further experiments tested the performance after an additional layer of polyethylene was added to the anode. The polymer—in this case polyethylene (PE)—was dissolved in decalin under reflux and spun onto the top of the Cu-coated silicon film. PE (Filmgard) was dissolved in boiling (180 °C) decahydronaphthalene (decalin) at 8 wt% under reflux. The solution was spun on the sample at 500 rpm for 1 minute. In order to register the channels throughout the anode, the PE/Cu/Si layer stack is transferred (polymer side down) onto a polydimethylsiloxane (PDMS) block. Using the silicon as a mask during reactive ion etching (March) of the polymer, the resulting channels were registered through all three layers of the electrode [Figure 5.3]. The PE film was etched at 150 W, 150 mTorr, and 20 SCCM of O₂ for 4 hours. The PE coated samples were tested in a three electrode cell as described below.

Coin cell components (MTI) were assembled in an argon filled glove box (Innovation Technologies) with Cu/Si/Cu electrodes and sealed using a hydraulic crimper (MSK-110, MTI). The electrolyte was 1 M LiClO₄ in 1:3 (w/w) ethylene carbonate (EC) : dimethyl carbonate (DMC). Silicon active mass was determined by measuring the volume of each sample and multiplying by the known silicon density. The device areas
were measured optically, and the channel diameters and film thicknesses were
determined by scanning electron microscopy (SEM). Galvanostatic measurements of
coin cells were conducted using an 8 channel coin cell cycler (MTI). Coin cells cycled vs.
Li metal electrodes were galvanostatically (dis)charge cycled between 2.0 and 0.01 V (vs.
Li/Li\(^+\)) or to \(\sim 1400\) mAhg\(^{-1}\). Coin cells featuring commercial cathodes were
galvanostatically (dis)charge cycled between 3.0 and 4.2 V or to \(\sim 1400\) mAhg\(^{-1}\). Two
initial formation cycles were run at 90 mAg\(^{-1}\) (15 hours per complete (dis)charge) before
cycling at higher rates. Gravimetric capacities reported in this paper are based solely on
silicon mass. We were unable to stably charge/discharge cycle silicon anodes at near
theoretical capacities, likely due to this strategy’s inability to mitigate the drastic strains
obtained at near theoretical capacity for silicon.

Ex-situ analysis was performed on samples cycled in a three-electrode cell in
order to minimize sample damage during coin cell disassembly. Samples were prepared
as above and adhered to cover glass substrates using a spin-on-glass (SOG) adhesive
layer. Glass slides were cleaned and then spin-coated with SOG (Filmtronics 500F,
filtered with a 0.2 um pore size syringe filter) at 700 rpm for 6 seconds. The electrodes
were immediately transferred to the support where the SOG was allowed to dry at room
temperature before being cured in an oven at 130 °C for 12 hours. A copper wire was
fixed to the electrode with conductive silver epoxy (Epotek). An inert epoxy (5 Minute
Epoxy, Devcon) was then applied to define the active area of the electrode.

Three-electrode cell experiments were conducted in an argon filled glove box.
Galvanostatic (dis)charge cycling and cyclic voltammetry of Cu/Si/Cu electrodes was
conducted using a galvanostat/potentiostat (CHI660D) with Li metal counter and reference electrodes, operated between 2.0 V and 0.01 V (vs. Li/Li\(^+\)). Galvanostatic cycling of devices used for SIMS imaging were cycled at a rate of C/10. Cyclic voltammetry measurements used a scan rate of 10 mV/sec. The electrolyte was 1 M LiPF\(_6\) (Strem Chemicals) in 1:1 (w/w) diethyl carbonate (DEC) : ethylene carbonate (EC) (Sigma Aldrich). Additional experiments were performed with an additional polyethylene layer on top of the Cu/Si/Cu electrode. Channels were registered through all layers of the device. The details are described in the Supplementary Information. We had difficulties using the LiPF\(_6\) electrolyte in our coin cells for undetermined reasons, and therefore we shifted to using a LiClO\(_4\)-based electrolyte for coin cell experiments.

Samples tested in three-electrode cells were imaged after being washed with DEC and transported to the instruments in sealed vessels. Scanning electron microscopy (SEM) was performed using either a JEOL JSM-6060LV, Hitachi 4700, or Hitachi 4800. Depth profiling was performed using a Physical Electronics PHI Trift Time-of-Flight SIMS instrument in a dynamic/static mode, using O ions at 2 kV for material removal and Au\(^+\) at 22 kV as the analytical source ion. Helium ion microscopy (HIM) was performed with a Carl Zeiss Orion Plus. The helium ion beam was operated with an acceleration voltage of about 39.5 kV and a current of about 0.4 pA. We used a 10 µm aperture at spot control 5 and a sample distance of 11 mm. A dwell time per pixel of 1 µs at 32 lines averaging was used.
5.3 Results and Discussion

5.3.1 Capacity Retention of Silicon Electrodes in Full Cells

The multi-layered electrode consists of a 4-50 µm thick film of silicon and a 100 nm copper layer on the top and bottom silicon surfaces, with micron scale channels spaced in a hexagonal pattern registered through all layers of the anode [Figure 5.4a]. Based on the data presented below, we believe this encapsulated multilayer electrode design serves to direct the lithiation in ways that can enhance its (dis)charge stability. With the top and bottom surfaces blocked, electrochemical lithium insertion reactions are restricted to occur primarily transverse to the electric field, at the sidewall of the silicon in the channels [Figures 5.4b,c]. As shown by cyclic voltammetry in Figure 5.5, an evaporation deposited copper layer of 100 nm reduces the lithium transport to a silicon substrate by >90%.

These electrodes were tested in coin cells, shown schematically in Figure 5.6. This directed transport should result in a more cross-sectionally uniform lithiation of the multi-layered (Cu/Si/Cu) electrodes [Figure 5.7a]. Two types of non-encapsulated electrodes, one containing microchannels [Figure 5.7b, Cu/Si] and the other simply flat silicon [Figure 5.7c, Cu/FlatSi] were also fabricated as controls to investigate the benefits that result from the laminate, micropore structures. The Cu base layer is used in each case as a self-consistent current collector for the series of samples.

Anodes with 4 micron thick silicon layers were tested in coin cells versus LiCoO$_2$ cathode laminates. Cells were galvanostatically (dis)charge cycled between 3.0 and 4.2
V at 93 mAg\(^{-1}\) (15 hours per half-cycle) for the first two cycles and then at 280 mAg\(^{-1}\) (5 hours per half-cycle) for subsequent cycles. Figures 5.7d,e show a 4 µm thick Cu/Si/Cu device (blue circles) that maintained an average coulombic efficiency of >99.0% from cycles 5 to 100. This anode maintained capacity for 110 (dis)charge cycles.

Most controls performed very poorly (with failures after several cycles being common) and the highest performing examples of the controls are shown in the figure. The coulombic efficiencies exhibited by the controls were markedly lower on average than those of microstructured, encapsulated devices [Figure 5.7e]. Specifically, the average coulombic efficiency of cycles 2 through 65 was 98.2% for the non-encapsulated control, Cu/Si, and 98.0% for the flat silicon control, Cu/FlatSi (as compared to >99% for the Cu/Si/Cu device shown in blue). Of many control anodes tested, one maintained capacity for only ~70 (dis)charge cycles.

Figure 5.8 shows the voltage profiles for a coin cell with Cu/Si/Cu and a commercial cathode. A new plateau region near 4 V vs. silicon advances in the discharge curves, appearing after cycle 115. A rise in the charging voltage to above 3.9 V versus silicon [Figure 5.8c] coincides with the appearance of this plateau in the discharge region [Figure 5.8d]. A change in voltage profiles such as this implies a structural change of the LiCoO\(_2\) cathode material from a layered structure to a spinel structure, a feature that has been discussed in depth in prior literature.[5.42-5.44] Typically the formation of this phase is observed in Li\(_x\)CoO\(_2\) when x is at or below 0.5.[5.45-5.47] The spinel form of LiCoO\(_2\) has also been shown in a TEM study to form at higher lithium concentrations, specifically x = 0.72, and after extensive cycling (334
cycles) of the layered material the authors noted the spinel phase was dominant.\[5.48\] This phase is considered to be metastable and deteriorates rapidly upon cycling.\[5.43\] We associate the failure of the cell with the formation of this phase, although we believe that the evolution of the Cu/Si/Cu anodes could be partly responsible for the cell failure. It remains uncertain from the present data whether the irreversible losses of Li (e.g. to an SEI layer) or an inhomogeneity in the cathode developed on cycling contribute here. The high coulombic efficiencies seen prior to failure tend to implicate the latter mechanism in our view. The two types of controls shown in Figure 5.7 did not show the same advance in the voltage profile, but rather a decrease in capacity more indicative of a loss of active material.

5.3.2 Electrode Rate Capabilities and Thickness Variation in Half-Cells

Area normalized capacities of 1.06, 5.38, and 12.74 mAhcm\(^{-2}\) were achieved with silicon thicknesses of 4, 20, and 50 µm respectively at a charging rate of 5 hours per half-cycle [Figure 5.9]. Further optimization of the microstructure, e.g. tuning pore size/separation and encapsulation layer thicknesses, might lead to performance improvements.

The rate capability of the anode was explored by varying the channel array pitch (CAP). Electrodes were tested with CAPs of 0.21, 1.15 and 3.72 (corresponding to approximately 5.8 µm diameter channels and edge-to-edge spacings between the channels of 1.2, 6.7, and 22 µm respectively, Figure 5.10) in coin cells integrating a Li-metal counter electrode. The first two cycles of each Si electrode were charged and
discharged at 15 hours per half cycle. The anodes were then charged at increasing current densities—and for a fixed amount of anode material, faster rates—in order to determine the highest power density that an anode with a given CAP could sustain stably during continuous (dis)charging over multiple cycles. Under galvanostatic (dis)charge cycling conditions, CAPs of 3.72, 1.15, and 0.21 were able to (dis)charge to 1400 mAhg\(^{-1}\) (based on silicon mass) in 28.0 minutes (2.99 Ag\(^{-1}\)), 15.0 minutes (5.58 Ag\(^{-1}\)), and 10.0 minutes (8.37 Ag\(^{-1}\)) respectively [Figure 5.11].

An interesting trend evidenced in these data is the inverse relation between rate capability and volumetric capacity (mAHm\(^{-1}\)) for electrodes with this microstructure. Electrodes that were able to continuously (dis)charge at current densities of 2.99, 5.58, and 8.37 A\(^{-1}\), had maximum volumetric capacities of 3250, 2860, and 1340 mAHm\(^{-1}\) respectively. The rates do not scale in a simple geometric manner, as is illustrated by the data shown in Figures 5.10-5.14. Ideally the rates would scale according to the exposed silicon surface area as fabricated. We found, however, that higher rates are achieved than are predicted strictly geometrically, possibly due to an increase in the silicon surface area that occurs after the first two forming cycles are performed at low rate.

5.3.3 Capacity Retention of Polyethylene/Cu/Si/Cu Electrodes in Full Cells

Polyethylene was used as an additional means of surface passivation and to further stabilize the structural evolution of the Cu/Si/Cu electrode via a flexible transport blocking mechanical support. The PE was dissolved in decalin and spun onto
the surface of the electrode and subsequently etched to reveal channels in registration with the pores of the Cu/Si/Cu microstructure. This electrode is shown in Figure 5.15a. The PE-coated electrode was then electrochemically tested versus lithium metal, here using a three electrode cell in an argon glove box in order to facilitate *ex-situ* characterization of the electrode post-cycling (damage to thin Si foils always accompanies coin cell disassembly).

Figures 5.15b-d shows the (dis)charge cycling data and voltage profiles for a PE/Cu/Si electrode. The first cycle gravimetric discharge capacity was 1107 mAhg$^{-1}$, and the coulombic efficiency was 79%. By the 10$^{th}$ cycle the gravimetric discharge capacity was 1351 mAhg$^{-1}$, and the coulombic efficiency was 97%. This electrode maintained >98% capacity between the 10$^{th}$ and 125$^{th}$ cycles. The average coulombic efficiency for the 10$^{th}$ to 125$^{th}$ cycle was >98%. These performance metrics were of the same order as the simpler Cu/Si/Cu anodes. That the pore structure is retained is shown in Figure 5.15e, which presents an SEM of the test electrode recovered after 125 (dis)charge cycles. While retaining an intact pore structure, the cycling does lead to material deposition as well as impacts due to mechanical work. A cross-sectional image of the device after charge/discharge cycling is shown in Figure 5.16.

5.3.4  *Ex-situ* Characterization of Structural Evolution via HIM, SIMS, and SEM

Helium ion microscopy (HIM) was used to investigate the non-strictly geometric dependence of rate capability. HIM is an interesting technique due to its very high spatial resolution and large depth of field.[5.49] Figures 5.17a and 17b show
representative Cu/Si/Cu anodes before cycling. The ridges visible in the channel sidewalls of the silicon are a nanoscale corrugation that arises as a result of the ICP-RIE plasma etching process used to create a high aspect ratio channel with a predominately straight-sidewall through the silicon membrane. After a three (dis)charge cycles [Figure 5.17c], significant structural changes to the silicon surfaces of the channels result in increased surface area, possibly resulting in the non-geometric increased rate performance seen in Figure 5.4e. Higher resolution HIM images can be found in the Supplemental Information [Figures 5.18-5.22]. These data reveal that the cycling leads to a gross roughening of the exposed Si side walls. The changes in nanostructure seen reflect impacts of the large atomic strains that attend cycling.

SEM and secondary ion mass spectrometry (SIMS) were used to examine 4 μm thick Cu/Si/Cu devices before and after 0, 1, and 5 (dis)charge cycles. Samples for characterization were specifically (dis)charge cycled in a three electrode cell in order to minimize sample damage. The data of Figures 5.23a,b depict a typical Cu/Si/Cu device prior to cycling. Figures 5.23c,d and 5.23e,f show data for devices after 1 and 5 galvanostatic (dis)charge cycles, respectively, where lithium metal was used as the counter and reference electrodes and capacities for the silicon electrodes were limited to 1400 mAhg⁻¹ (based on silicon mass, the same limiting capacity used in the full coin-cell samples). The SEM images, while showing cracking as a result of the lithiation/delithiation process, demonstrate that the overall gross microstructure of the perforated silicon electrodes is retained. Data from SIMS provide a compositional depth profile for the samples shown in the SEM images and demonstrate that the Cu layer did
not delaminate from the silicon. The probe was focused on a non-channel area in order to sputter through the SEI and copper layers into the silicon. Some inter-diffusion at the copper/silicon interface was observed in all the samples analyzed—both before and after galvanostatic cycling, suggesting silicides may be important to the functioning of these electrodes. Quantitative interpretations of the SIMS data are complicated by the processing steps used to fabricate these glass mounted electrodes. The silicon membranes carry a thin oxide overlayer as initially fabricated, and it is on this layer that the Cu is deposited. Thermal curing of the SOG adhesive leads to interdiffusion of the Cu, generating a silicide and graded, oxide bearing interphase. Galvanostatic cycling appears to generate additional structure: (a) a lithium rich SEI layer forms atop the electrode and coarsens during the first and fifth cycles; and (b) some lithium accumulates at the copper/silicon interface as has been previously reported.[5.50]

5.4 Conclusions

In this paper we have demonstrated a new type of electrode that takes advantage of encapsulation of a micropore-modified, binderless silicon electrode in order to direct lithium mass transfer. Comparison of charge/discharge cycling data for encapsulated micropore-modified Cu/Si/Cu electrodes versus the control electrodes demonstrates that these strategies employed within this paper improve electrode performance. The Cu/Si/Cu electrode design has maintained capacity for 110 cycles and achieve >99% average coulombic efficiencies for 100 cycles versus a commercial LiCoO2 cathode. We were unable to stably charge/discharge cycle silicon anodes at near theoretical capacities. We also incorporated an additional polyethylene coating in order
to provide additional surface passivation and mechanical support. With this electrode design we were also able to obtain over 125 charge/discharge cycles in a three electrode cell, however with slightly lower coulombic efficiencies overall than were obtained in the Cu/Si/Cu samples.

The process flow for fabricating the anodes demonstrated in this paper was developed as an expedient means to provide a proof of concept, albeit one that also exploits relatively expensive materials and equipment when compared to possible alternative methods. In future work, we plan to explore techniques that can produce anodes with similar form factors as well as capabilities using less expensive polycrystalline silicon starting materials. Since the channel design and the materials chosen for the anode in this paper were a proof of concept, other methods of controlling mass transport (and strain) in high capacity/strain electrode materials or exploiting different form factors might achieve similar or even improved results in terms of higher capacities, rate capabilities, and coulombic efficiencies. Additional encapsulation schemes might improve safety attributes of similar devices. A detailed investigation of the transport-related inverse relationship between volumetric capacity and rate capability for silicon, and mechanisms to reduce coulombic losses (e.g. continual SEI formation) may be especially warranted.
5.5 References


5.6 Figures

Figure 5.1: a) Process flow for microporous silicon anodes encapsulated by copper (Cu/Si/Cu). b) Additional fabrication steps beyond a) to add an additional polymer layer (PE/Cu/Si/Cu). Channels are registered through all layers in b) by oxygen plasma etching of polymer using the silicon as a mask.
Figure 5.2: A high capacity multilayer Cu/Si/Cu electrode after anisotropic etching via ICPRIE. 6 um diameter channels can be patterned over large areas with minimal defects.
Figure 5.3: High angle SEM images of the polyethylene (PE) surface of a PE/Cu/Si anode after oxygen plasma etching. The channels are registered through all three layers of the electrode. Three different magnifications are shown.
Figure 5.4: a) Schematic of an encapsulated multilayer micropore-modified silicon anode stack (not to scale) consisting of a thin silicon layer (grey) coated with a copper (orange) and polymer layer (white) (PE/Cu/Si). Channels are registered through all layers. b) Cross-section of a) illustrating non-crystallographic dependent anisotropic electrochemical lithium transport primarily transverse to the electric field. c) Fixing the bottom of the PE/Cu/Si to a support results in expansion being primarily in the thickness (Z) direction upon electrochemical lithium insertion.
Figure 5.5: a) Cyclic voltammetry between 2.0 and 0.01 V (vs. Li/Li⁺) at a scanning rate of 10 mV/s of a (110) silicon wafer (black), (110) silicon wafer covered with Cu (red), and (110) silicon wafers covered with Cu and PE (green and blue). b) Gravimetric discharge capacity and voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V at 280 mAg⁻¹ (5 hours per half cycle) of a coin cell with a PE/Cu/Si/Cu electrode with channels registered through every layer but the PE. Voltage vs. time for the charge and discharge during cycle(s) 1, 5, 10, 20, 30, 40, & 50 are associated with red, dark green, black, cyan, magenta, brown and bright green respectively.
Figure 5.6: Optical image of a coin cell and the coin cell cycler. A diagram of the components of a coin cell are included to the right. All initial tests of the microstructured anodes using LiPF$_6$ as the electrolyte salt in coin cells would not cycle, therefore LiClO$_4$ was used as the electrolyte for all coin cell experiments. After completion of these experiments we found that coin cell components from Hoshen improved cell performance, possibly due to better sealing of the cell preventing the hydrolysis of LiPF$_6$. A cell with Hoshen coin cell components and the LiPF$_6$ salt was found to cycle for several cycles.
Figure 5.7: The schematic shown in a) depicts the encapsulated microporous device, Cu/Si/Cu, while b) and c) represent the non-encapsulated controls, Cu/Si and Cu/Si/Flat, respectively. d) Gravimetric capacity during delithiation and e) coulombic efficiency data for silicon anodes cycled in coin cells versus commercial LiCoO₂ cathodes. The Cu/Si/Cu anode with a channel array pitch of 1.15 and 4 µm thick silicon layer was galvanostatically charge/discharge cycled at 280 mAg⁻¹ between 3.0 V and 4.2.
Figure 5.8: Voltage vs. capacity profiles for the full cell shown in Figure 6. a) Cycles 1 through 80 are steady leading to voltage increases from b) 80 through 115. c) Charging and d) discharging curves are shown for cycles 116 through 126, wherein a new discharge plateau advances with cycle count corresponding with higher charging voltages. Not all cycles are shown in order to maintain clarity but are evenly spaced through each cycle range. Cycle count increases as the sequence: black, magenta, cyan, green, red, and blue; specifically, a) 1, 10, 20, 40, 60, and 80, and b) 80, 85, 95, 105, 110, and 115, and c,d) 116, 118, 120, 122, 124, and 126.
Figure 5.9: a) Area normalized capacity of Cu/Si/Cu anodes with silicon layers up to 50 µm thick. Gravimetric capacity during delithiation and corresponding coulombic efficiency data for Cu/Si/Cu electrodes b) 20 and c) 50 microns thick. The electrode with a channel array pitch of 1.15 and a silicon thickness of 4 µm was galvanostatically charge/discharge cycled between 2.0 V and 0.01 V in a 3 electrode cell.
Figure 5.10: SEM images of electrodes with CAPs of a) 3.72, b) 1.15, and c) 0.21 are shown. d) Volumetric capacity during delithiation silicon as a function of channel array pitch is shown in black. The blue dots indicate the maximum stable current density for a Cu/Si/Cu electrode having different channel array pitches under continuous (dis)charge cycling. Lines are drawn to guide the eye.
Figure 5.11: Gravimetric Capacity during lithiation of Cu/Si/Cu electrodes with channel array pitches of 0.21 (blue right-facing arrow), 1.15 (green diamond), and 3.72 (red left-facing arrow) at various times to charge or discharge (different Ag$^{-1}$g$^{-1}$ to a constant capacity of 1400 mAhg$^{-1}$) to 1400 mAhg$^{-1}$ in 28.0 minutes
**Figure 5.12:** a) Gravimetric charge capacity for a Cu/Si/Cu electrode with a channel array pitch of 1.15 and 4 µm thick silicon in a coin cell at 0.4 (upward point triangle), 0.57 (diamond), 1.0 (square), 2.5 (circles), and 5 (downward point triangle) hours per half cycle. The other electrode was lithium metal. b) Voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V for 24 minutes per half cycle at 3500 mA g⁻¹ in a). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), 30 (purple), and 40 (light green). c) Voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V for 34 minutes per half cycle at 2450 mA g⁻¹ in a). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), and 30 (magenta), and 40 (light
Figure 5.12 cont.: green). d) Voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V for 1 hour per half cycle at 1540 mAg⁻¹ in (a). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), and 30 (magenta), 40 (light green), and 50 (brown). e) Voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V for 2.5 hour per half cycle at 616 mAg⁻¹ in a). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), and 20 (cyan). f) Voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V for 5 hour per half cycle at 308 mAg⁻¹ in a). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), and 20 (cyan).

Figure 5.13: a) Gravimetric charge capacity for a Cu/Si/Cu electrode with a channel array pitch of 0.21 and 4 μm thick silicon (vs. lithium metal) in a coin cell at 4900 mAg⁻¹ (17
Figure 5.13 cont.: minutes per half cycle). b) Voltage (vs. Li/Li$^+$) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V in a). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), and 20 (cyan). c) Gravimetric charge capacity for a Cu/Si/Cu electrode with a channel array pitch of 0.21 and 4 μm thick silicon (vs. lithium metal) in a coin cell at 3500 mAg$^{-1}$ (24 minutes per half cycle). d) Voltage (vs. Li/Li$^+$) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V in c). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), 30 (magenta), and 40 (brown). e) Gravimetric charge capacity for a Cu/Si/Cu electrode with a channel array pitch of 0.21 and 4 μm thick silicon (vs. lithium metal) in a coin cell at 1540 mAg$^{-1}$ (60 minutes per half cycle). f) Voltage (vs. Li/Li$^+$) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V in (e). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), 30 (magenta), and 40 (brown).
Figure 5.14: a) Gravimetric charge capacity for a Cu/Si/Cu electrode with a channel array pitch of 0.21 and 4 \, \mu\text{m} thick silicon (vs. lithium metal) in a coin cell at 4900 mAg\(^{-1}\) (17 minutes per half cycle). b) Voltage (vs. Li/Li\(^+\)) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V in a). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 25 (cyan), 50 (magenta), 75 (brown), and 100 (bright green). c) Gravimetric charge capacity for a Cu/Si/Cu electrode with a channel array pitch of 0.21 and 4 \, \mu\text{m} thick silicon (vs. lithium metal) in a coin cell at 3500 mAg\(^{-1}\) (24 minutes per half cycle). d) Voltage (vs. Li/Li\(^+\)) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V in c). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), 30 (magenta), 40 (brown), and 50 (bright green). e) Gravimetric charge capacity for a Cu/Si/Cu electrode
Figure 5.14 cont.: with a channel array pitch of 0.21 and 4 µm thick silicon (vs. lithium metal) in a coin cell at 2450 mAg⁻¹ (34 minutes per half cycle). f) Voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V in e). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), 30 (magenta), 40 (brown), and 50 (bright green). g) Gravimetric charge capacity for a Cu/Si/Cu electrode with a channel array pitch of 0.21 and 4 µm thick silicon (vs. lithium metal) in a coin cell at 1540 mAg⁻¹ (60 minutes per half cycle). h) Voltage (vs. Li/Li⁺) vs. time for galvanostatic charge/discharge cycling between 2 V and 0.01 V in g). Charging and discharging curves are shown for cycles 1 (red), 5 (dark green), 10 (black), 20 (cyan), 30 (magenta), and 40 (brown)
Figure 5.15: a) Top-down SEM image of a PE/Cu/Si electrode before galvanostatic charge/discharge cycling. The insert is a magnified view of a channel. b,c) Gravimetric capacity during delithiation and corresponding coulombic efficiency data. The electrode was cycled between 2.0 V and 0.01 V in a 3 electrode cell. The dashed line denotes the theoretical gravimetric capacity for carbon. d) Voltage (vs. Li/Li⁺) vs. time for various cycles of the sample in b,c). Minimal changes in the voltage are observed with cycling. (Dis)charging curves are shown for cycles 25 (red), 50 (dark green), 75 (black), 100 (cyan), and 125 (magenta). e) Top-down SEM image of a PE/Cu/Si electrode after 125 charge/discharge cycles for 5 hours per half-cycle at 280 mAg⁻¹ with a magnified insert.
**Figure 5.16:** Cross-section SEM image of a PE/Cu/Si/Cu electrode after 5 galvanostatic charge/discharge cycles. A 1-3 micron layer of material can be seen on the top side of the Si.
Figure 5.17: HIM Images for Cu/Si/Cu electrodes a,b) before and c) after three (dis)charge cycles. The images were obtained at approximately a 30 degree tilt angle.
Figure 5.18: HIM Image of Cu/Si/Cu electrode before cycling.
Figure 5.19: HIM Image of Cu/Si/Cu electrode before cycling.
Figure 5.20: HIM Image of Cu/Si/Cu electrode before cycling.
Figure 5.21: HIM Image for Cu/Si/Cu electrode after three (dis)charge cycles.
Figure 5.22: HIM Image for Cu/Si/Cu electrode after three (dis)charge cycles.
Figure 5.23: SEM images and corresponding SIMS data for Cu/Si/Cu electrodes a,b) before galvanostatic cycling, c,d) after 1 (dis)charge cycle, and e,f) after 5 (dis)charge cycles. Red, black, and blue corresponds to counts of copper, silicon, and lithium, respectively.
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A.1 Introduction

Safety is an important metric for lithium-ion batteries. Adoption of lithium-ion batteries was driven by their better safety relative to lithium metal-based batteries. Further advances in battery safety are required as battery usage as well as energy density increases. Already the regularity and severity of safety incidents have risen. Lithium-ion battery fires forced many laptop batteries to be recalled in 2006. In 2013 Boeing had safety issues with batteries for the 787 Dreamliner planes, and Tesla has had a spate of lithium-ion battery fires in Tesla Model S cars.

Battery safety has become important enough to award a contract to the Bollré Group to supply electric cars to Paris because their vehicles use safer battery technology. The usage of flammable non-aqueous electrolytes in lithium-ion batteries represents a major safety concern especially considering thermal runaway.

Multiple approaches have been investigated to mitigate safety issues related to thermal runaway in lithium-ion batteries. Separators have been developed that melt during thermal runaway in order to shutdown the battery. Flame-retardants have been added to the electrolyte. Microcapsules have also been added to
the electrodes to improve the safety of the battery.\textsuperscript{[A.2]} Replacement of the liquid electrolyte and polymer separator with a lithium conducting film has the possibility to increase safety and battery performance. From a system level perspective 75% of a conventional battery pack is inactive material, 50% of each conventional battery is typically inactive material.\textsuperscript{[A.27]} One approach is to replace the liquid electrolyte and separator with a lithium-conducting polymer gel membrane (commonly PEO, PVDF, PAN, PMMA, and PVC).\textsuperscript{[A.17, A.28-A.33]} Another method utilizes inorganic solid-state electrolytes such as lithium phosphorous oxynitride (LiPON).\textsuperscript{[A.13, A.15, A.16, A.34-A.39]}

Development of a battery utilizing inorganic solid-state electrolytes requires numerous key challenges to be overcome in order for stable long-term operation. Methods must be developed for fabrication of non-planar electrodes in close proximity. In between these two electrodes a thin conformal coating that acts as both separator and electrolyte is required that allows stable battery operation and prevent self-discharge (and shorting) of the battery. The ability to fabricate thin coatings is crucial because of the lower transport rates for solid electrolytes relative to liquid electrolytes. A conformal coating is needed because any defects in the coating will cause shorting of the battery. These electrodes as well as the lithium-conducting layer must maintain contact for continued operation of the battery.

The work summarized in this chapter was a set of proof of concept experiments in order to determine the feasibility of using recent advances in electrode fabrication and coatings to develop a solid-state battery. The battery would consist of a multilayer...
copper/silicon/copper electrode (see figure 5.1) coated with a conformal electrolyte / separator film via atomic layer deposition (ALD) and a cathode deposited into the channels of the anode. ALD can be used to create self-limiting conformal coatings on complex 3D objects.[A.40-A.43] ALD coatings have been shown to be effective barrier coatings for batteries.[A.41] Recently lithium containing ALD coatings have been developed.[A.42] Demonstration of a thin (nm scale), conformal ALD-coating as both electrolyte and separator will enable more efficient integration of the battery—LiPON, a commonly used inorganic solid-state electrolyte, has to be fabricated microns thick to avoid pinhole defects causing battery shorting. This work was also meant as a demonstration of a printed battery. If both the deposition of the cathode into the channels and the ALD coating work well, then we will investigate mechanisms for stable operation of the electrodes during the deformation that accompanies galvanostatic charge/discharge cycling.

A.2 Experimental

Cyclic voltammetry was chosen as a method for rapidly testing the rate capability of samples for proof of concept experiments. Cyclic Voltammograms were obtained by testing devices in a three electrode cell in an Argon filled glove box at <10 ppm O₂. Electrolyte used in the experiments was EC:DEC 1:1 (w/w) with 1 M LiPF₆. The working electrode consisted of a (110) silicon wafer with a Ti/Au (15/100 nm) current collector deposited on the back surface. A CHInstruments 660D potentiostat/galvanostat was to conduct cyclic voltammetry. Cyclic voltammetry scans were conducted at 10 mVs⁻¹.
Current-voltage curves were measured using a Keithley current source scanning from 0 to 5 V. (110) silicon wafers were sandwiched between two coin cell stainless steel spacers (Hoshen). An external electrical connection was made with the samples via a wire that was epoxied to the metal spacers surface.

ALD is conducted by iteratively dosing precursors in an ABABAB... fashion, with each precursor forming a self-terminating monolayer. As a result, each AB cycle results in the deposition of a monolayer of material, which allows for the precise control of film thickness and composition. Furthermore, as the deposition is limited by surface reactions as opposed to precursor flux, ALD films tend to be highly conformal and pin-hole free. In this work, we deposited Al$_2$O$_3$ and LiAlO$_x$ by ALD. The Li doped Al$_2$O$_3$ was 1:1 Li to Al.[A.44] Depositions were conducted in a viscous flow reactor maintained at a temperature of 225 °C and a pressure of 1 Torr under a constant flow of 360 sccm UHP N$_2$ carrier gas. Al$_2$O$_3$ was deposited using iterative exposures of trimethylaluminum (TMA) and H$_2$O. Both TMA and H$_2$O were maintained at room temperature and introduced into the reactor at their respective vapor pressures. TMA was dosed for 1 sec followed by a 5 sec purge, and H$_2$O was dosed for 1 sec followed by a 5 sec purge. Al$_2$O$_3$ films exhibited a growth rate of ~.11 nm per cycle, and films of .5, 2, and 4 nm were deposited. LiAlO$_x$ was deposited by combining the Al$_2$O$_3$ ALD process with a LiOH ALD process at a 1:1 Al$_2$O$_3$:LiOH cycle ratio. LiOH was deposited using iterative exposures of lithium t-butoxide (LiOtBu) and H$_2$O. Due to its low vapor pressure, LiOtBu was maintained at 140 °C in a heated stainless steel bubbler and was dosed into the reactor by diverting 60 sccm of N$_2$ carrier gas through the bubbler. LiOtBu was dosed
for 5 sec followed by a 5 sec purge. H₂O was dosed for 1 sec followed by a 5 sec purge. LiAlOₓ films exhibited a growth rate of ~0.15 nm per cycle and films of thickness 2, 4, 8, 10, 20, and 40 nm were deposited.

Lithium Cobalt Oxide (LCO) ink was synthesized by first mixing LCO powder (Sigma Aldrich, 7 – 10 μm), Super-P carbon powder (Timcal Ltd., 50 nm), and graphite powder (Showa Denko America, INC., 5 μm) into Kynarflex-2080 (Arkema Inc.) binder solution in N-methyl-2-pyrrolidone (NMP), followed by homogenizing using a Thinky mixer at 2000 rpm for 30 min. The weight ratio of LCO:conductive filler:binder is 0.7:0.21:0.09, and the ink loading is 50 wt%.

Two prototype batteries were assembled. The first battery pressed the 20 nm LiAlOₓ-coated (110) silicon anode into contact with the LiCoO₂ cathode on an Al foil during curing. The second battery was assembled in an argon filled glove box. Six drops of 1 M LiPF₆ EC:DEC 1:1 (w/w) electrolyte was added to a separator. The 20 nm LiAlOₓ-coated (110) silicon anode and LiCoO₂ cathode were placed into contact, and a binder clip was used to apply pressure to the device in order to ensure good contact between the electrodes. Silver epoxy was used to make an electrical connection between the back of the (110) wafer and a wire. The LCO cathode was produced on top of an Al current collector.

A.3 Results and Discussion

A.3.1 Process Flow for Proposed Battery
A schematic of the fabrication scheme for the proposed solid-state battery is shown in Figure A.1. The process flow will utilize multilayer copper/silicon/copper (Cu/Si/Cu) electrodes as previously described in chapter 5 [Figure A.1a]. The multilayer electrodes would then be conformally coated with Al₂O₃ or LiAlOₓ, Figure A.1b. For safe battery operation this layer must act as both a separator and electrolyte—facilitate lithium ion transport while being resistive enough to prevent self-discharging of the electrode. After conformal coating, cathode material will be deposited in each channel [Figure A.1c]. Once the channels were in-filled, a current collector for the cathode would be formed on top of the cathode material and ALD-coated electrode surface via either physical vapor deposition of an Al layer or squeegeeing of an Al slurry [Figure A.1d].

A.3.2 Cathode Deposition in Channels

We started out by testing the ability to deposit cathode material into confined geometries of the channels of the Cu/Si/Cu electrodes [Figure A.2a]. Two possible methods we investigated for in-filling the channels with cathode material. One method was to create a slurry on top of the ALD-coated multilayer electrode and squeegee off the excess material [Figure A.2b]. This approach leaves residual traces of cathode material on the surface of the ALD-coated multilayer electrode. Another possible approach was ink-jet printing of a cathode material within 100 μm diameter channels [Figure A.2c]. This method would not have the extraneous cathode material on the
surface of the electrode but would require more advanced methods (e.g. multiple nozzle system) to fill in a large array of channels serially.

A.3.3 ALD-coatings as Separator and Electrolyte

Another crucial aspect was to determine for the proof of concept experiments was the ability of the conformal ALD coating to act as both a separator and electrolyte for this battery. These coatings were tested via cyclic voltammetry (measuring ionic conductivity) and current-voltage curves (measuring self-discharge current) [Figure A.3].

For determining if the ALD coating was resistive enough to prevent self-discharge we measured the current from 3.0 – 4.2 V (common operating voltage of commercial batteries with carbon and LCO); if the layer is acting as a separator we should measure minimal current. As a rule of thumb, typical devices of this size that we have fabricated in the past have been ~1 mAh. For this battery charging/discharging in 10 hours, a current below 1E-6 A is required to achieve a coulombic efficiency of 99%.

We started by investigating ALD coatings of Al₂O₃ (red curve) and recently developed ALD-coating containing LiAlOₓ (blue curve) [Figure A.3a]. A (110) wafer and a (110) wafer with an 8 nm LiAlOₓ coating measured a current of 9.0E-2 A and 3.3E-3 A respectively. The small reduction in measured current means that thicker coatings will have to be investigated for this coating to be used. For the Al₂O₃-coated (110) wafer the limited self-discharge current of 3.1E-5 A that was measured with a 2 nm coating drops two orders of magnitude to 1.9E-7 A for the (110) wafer with a 4 nm coating.
In order to determine if the ALD-coating acted as an effective electrolyte we measured the maximum current density during electrochemical lithium insertion (lithiation) via cyclic voltammetry. For good ionic conductivity we should measure minimal reduction in this current density during lithiation. When conducting cyclic voltammetry from 2.0 V to .01 V (vs. Li/Li$^+$), electrochemical lithiation of silicon starts around .1 mV (vs. Li/Li$^+$) and is a maximum at the lower limit of .01 V (vs. Li/Li$^+$). The lower limit was chosen to keep from plating lithium on the electrode surface.

Figure A.3b shows the current density for the two ALD coatings at .01 V (vs. Li/Li$^+$). The 2 nm Al$_2$O$_3$-coated (110) Si wafer had a current density of 2.9E-4 Acm$^{-2}$ and the current density dropped an additional order of magnitude for the 4 nm Al$_2$O$_3$-coated (110) Si wafer (6.1E-5 Acm$^{-2}$). This low current density during lithiation even with a few nm thick coating ruled out using the Al$_2$O$_3$ coating for a prototype device. For a (110) wafer and (110) wafer with an 8 nm LiAlO$_x$ layer the current density measured during lithation was 1.1E-3 Acm$^{-2}$ and 4.2E-4 Acm$^{-2}$ respectively.

For the 8 nm LiAlO$_x$-coated (110) Si wafer the reduction in the current at 3.0 V and small reduction in current density at lithiation suggested that a thicker coating might be able to provide the required high ionic transport but low self-discharge current required to act as separator and electrolyte. Further experiments with thicker LiAlO$_x$ coatings, however, showed a bigger than expected reduction in current density during lithiation as the coating thickness increases. When we tested LiAlO$_x$ coating from 10 nm up to 40 nm thick, a reduction in the current density of around 3 orders of magnitude was
observed, Figure A.4. These experiments suggested that neither ALD coating had the required properties to act as both a separator and electrolyte.

A.3.4 Fabrication of Prototype Device

To confirm the cyclic voltammetry measurements of the ALD coatings we tested a prototype device that consisted of a (110) wafer with a 20 nm thick LiAlO$_x$ coating pressed into contact with a cathode [Figure A.5a]. Contact was made between the anode and cathode by pressing into contact the electrodes during curing of the cathode slurry. For this sample near zero current was observed in the cyclic voltammogram between 3.0 and 4.2 V. This was possibly due to a lack of good contact between the ALD-coated anode and cathode that would enable lithium transport. We then tested if the zero current was a result of the electrodes not working or a lack of good contact between the electrodes. A device was fabricated with an electrolyte soaked separator between the two electrodes that were pressed together by a binder clip [Figure A.5b]. Cyclic voltammetry curves showing charging and discharging of the battery demonstrated that the issue was contact between the electrodes [Figure A.5c]. Attempts to perform cyclic voltammetry with liquid electrolyte but no polymer separator resulted in shorting of the battery. Current of a few A was measured, three orders of magnitude higher than the expected current. The experiment was immediately shut down. The 20nm thick LiAlO$_x$ coating did not have the desired performance metrics require to operate as both a separator and electrolyte.
A.4 Conclusions

The set of proof of concept experiments suggest new lithium conducting coatings will need to be developed for this system to be feasible. Currently tested thicknesses of the ALD coating that allow lithium ion transport also resulted in shorting of the battery. Additionally difficulties in terms of how to maintain contact between the cathode, anode, and ALD coating during battery operation were identified. Conformal contact during lithiation and delithiation may not be feasible for Si-based electrodes, but may be feasible for a lithium titanate electrode that undergoes less strain during galvanostatic charge/discharge cycling.[A.45]
A.5 References


Figure A.1: Process flow for proposed solid-state battery. a) The multilayer Cu/Si/Cu electrode is b) conformally coated with a layer that acts as both electrolyte and separator via atomic layer deposition (ALD). c) A cathode is then deposited within the ALD-coated channels. d) An aluminum current collector is deposited to connect the cathode pillars in the channels.
Figure A.2: a) 100 μm diameter channels were used as a test of the ability to deposit cathode into channels. We tried two methods b) ink-jet printing of the cathodes and c) depositing a layer of cathode material and then squeegeeing away the excess material.
Figure A.3: a) Current measured at 3.0 V for Al₂O₃ (red) and LiAlOₓ (blue) coated (110) wafers. b) Current density measured at the maximum electrochemical lithium insertion peak at .01 V (vs. Li/Li⁺) for Al₂O₃ (red) and LiAlOₓ (blue) coated (110) wafers.
Figure A.4: Current measured at the maximum electrochemical lithium insertion peak at .01 V (vs. Li/Li⁺) for samples with thicker LiAlOₓ coatings. Further testing of LiAlOₓ demonstrated a negative relationship between thickness and current density of lithiation. The line is meant as a guide to aid the reader.
Figure A.5: a) Images of the prototype device consisting of an LiAlO$_x$-coated (110) wafer and LCO cathode on an Al-foil current collector. b) Images of the modified device for usage with electrolyte and separator. The LiAlO$_x$ coated (110) silicon wafer is pressed into contact with the LiCoO$_2$ cathode by a binder clip. c) Cyclic voltammogram showing lithiation and delithiation of the electrode using a separator and electrolyte. Electrochemical testing without the separator—even with the ALD coating—resulted in shorting of the battery.
APPENDIX B

Investigation of tetraethoxysilane (TEOS) as an electrolyte additive

B.1 Supplemental Slides:
The slides may be found in a supplemental file named 140113_TEOS_Slides.pdf

B.2 Description of Slide 1:
All data for the experiments is available on the group storage drive.
Experiments conducted using the 3 electrode cell in the glove box are stored in /jason/data/CHI. Experiments conducted using the MTI coin cell cycler are stored in /jason/data/MTI. Data for the experiments on this slide can be found in 131101, 131105, and 131107 directories within the MTI folder.

For the first slide, coin cells were tested that contained a Li metal electrode and Si electrode (similar to the electrodes in Chapter 5 expect with channels but no copper layers) as shown by the diagram on the left. The coin cells were assembled and crimped in the large MBraun glove box. Hoshen coin cell parts were used in the construction of the cell—2 Hoshen coin cell spacers were used in the coin cell. 6 drops of 1 M LiClO₄ 1:1 (v/v) EC:DMC (Sigma Aldrich) electrolyte was used for the experiments. For the electrolytes with TEOS, TEOS was added to the solution such that the solution was 99 wt. % electrolyte, and 1 wt. % TEOS. The solution sat overnight before usage. Electrolyte was dropped three times after the Li metal was placed on the spacer. Three more drops of electrolyte were placed on the other side of the PE/PP/PE tri-layer separator before placing the Si electrode.

Coin cells were galvanostatically charge/discharge cycled between 3.0 to 4.2 V up to 1400 mAh/g (based on mass of Si) using the MTI coin cell cycler.

The sample with Li metal and Si electrode—but no TEOS additive—was able to stably charge to 1400 mAh/g for 7 cycles before subsequent cycles reached the potential limits with a capacity below 1400 mAh/g. Sample with 1.0 wt. % TEOS were able to cycle for 17 and 23 cycles before losing capacity. Typically coin cells with lithium metal electrodes and Cu/Si/Cu electrodes that we have tested in the past lasted 20-40 cycles before failure. The voltage profiles show dramatic variations in potential before complete loss in capacity of the electrodes.

The graph in the bottom right shows the difference in percent coulombic efficiency between the blue (coin cells with TEOS additive in electrolyte). A coulombic efficiency improvement is demonstrated for the first 7 cycles when TEOS additive was present in the coin cell electrolyte. Switching to Si electrode with channels instead of Cu/Si/Cu electrodes allows us to probe the improvement for a simple silicon electrode as well as cuts the fabrication time required to make electrodes in half.

B.3 Description of Slide 2:
Data can be found in 130920, 130922, and 130923 directories within the MTI folder. Long term cycling was also tested with coin cells containing a LiCoO₂ cathode and Cu/Si/Cu anode. The assembly and crimping of the cells was done the same way as the samples described above except 3 Hoshen coin cell spacers were
used in the coin cell due to the difference in thickness between the LiCoO$_2$ cathode and Li metal. Two coin cells—one with 1.0 wt. % TEOS additive and another with 5.0 wt. % TEOS additive—were tested. A beneficial impact of TEOS is shown for only 30-40 cycles before the coulombic efficiency of the coin cells with TEOS additive drops below the cells without TEOS. Additional coulombic losses occur due to the LiCoO$_2$ cathode. Electrochemical performance of coin cell characterizing these impacts can be found in the 131103 and 131110 directory in the MTI folder.

B.4 Description of Slide 3:

No long term viability is seen in cycling of coin cells with Cu/Si/Cu electrode and LiCoO$_2$ cathodes with 1.0 and 5.0 wt.% TEOS additive. After 50 cycles the coulombic efficiency of coin cells with TEOS is below that of the coin cells without TEOS—the coulombic efficiency in the cells with TEOS additive drops and the coulombic efficiency in the coin cell without TEOS additive rises. It should be noted that the coin cell with 5 wt. % TEOS additive lost capacity under the above electrochemical testing conditions before the coin cell with 1 wt. % TEOS additive.

B.5 Description of Slide 4:

Voltage profiles during galvanostatic charge/discharge cycling of Cu/Si/Cu electrodes versus LiCoO$_2$ at cycle 10 are shown on the left. Initial voltage profiles are very similar between all samples. By cycle 50, no significant change is seen in the voltage profile of the coin cells with TEOS additive, however, the coin cell without the TEOS additive have pronounced changed. For the non-TEOS coin cells the voltage profile during initial charging and final discharging (3.4 to 3.0 V) is much sharper—possibly due to the formation of a stable SEI. Also during discharging the voltage profile shifted upwards.

These coin cells were an experiment to determine the impacts of TEOS additive on cycling. The first batch of samples coin cells with TEOS additive on slide 3 started cycling late September and ended mid November to December. The initial concentrations of TEOS additive tested in the coin cell were high for an electrolyte additive in order to probe potential beneficial impacts on electrochemical performance of the coin cells. [B.1, B.2]

More investigation would be required to determine the cause of this coulombic loss during long term cycling. One possible explanation for the lack of change in the voltage profiles and the earlier failure of the higher concentration first is continual deposition of material on the electrodes. Another possible source of coulombic loss could be the conversion reaction of SiO$_x$ electrodes.[B.3, B.4]

B.6 References:


