ON-CHIP SELF-ROLLED-UP NANOMEMBRANE TUBE
INDUCTOR FOR RFIC PERFORMANCE ENHANCEMENT

BY

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THESIS
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Miniaturization of the commonly used on-chip lumped spiral inductor is highly desirable to reduce the fabrication cost and enhance the performance and functionality of radio frequency integrated circuits (RFICs). Numerous improvement methods have been demonstrated but all fail to fundamentally solve the intrinsic drawbacks of planar spiral structure, especially the most critical issue – substrate effects. A new design concept based on self-rolled-up nanomembrane nanotechnology that “processes like 2D and functions like 3D” is proposed and demonstrated. This thesis shows a global solution to obtain a lumped inductor with extremely small on-chip footprint and immunity to substrate effects. Experimental realization of self-rolled-up inductors shows a footprint two orders of magnitude smaller than that of the planar spiral inductors, with excellent quality factor (Q) and much higher operating frequency than the 2D counterparts in both capabilities.
To my father Shiyi Huang and my mother Huabi Ma

~ for always believing in me.
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CHAPTER 1: INTRODUCTION

1.1 Overview

On-chip passive lumped devices are very important circuit components in radio frequency integrated circuit (RFIC) design. Basic circuit elements among them include inductors, capacitors and resistors. Numerous types of advanced functional passive devices can be constructed by these circuit elements, like lumped filters, transformers and impedance matching networks etc. Nowadays, the development of RFICs is heading to a direction requiring higher integration level (reduce the size of on-chip devices), higher working frequency band and the ability to work on flexible substrates for wearable applications [1-3]. For the active devices on chip, the current record in the lab is reported achieving node size as small as 7 nm. However, for the passive components, they are unable to follow in the footsteps of active devices, and still occupy more than 90% chip area in most cases. Design and fabrication of current widely used on-chip passive components are based on two-dimensional (2D) processing, which is compatible with CMOS technology but limits the design of passive devices on 2D pattern. Among all the basic passive elements, the inductor is the one that suffers the most from the intrinsic problem of 2D design [4, 5].

The currently widely used on-chip inductor is based on planar spiral structures [4, 6-9]. They utilize the self-induction of metal wires and mutual inductance between wires to obtain desired inductance. However, as the self- and mutual induction are both weak, the planar spiral inductor has to be made as many turns as possible to reach desired performance, which inevitably leads to a large footprint. 2D structure cannot confine the radiated electromagnetic (EM) field very well, so half of the radiated EM field generated by planar inductor penetrates into the substrate and therefore introduces serious substrate parasitic parameters including
substrate capacitance and resistance, especially when the substrate is heavily doped. Substrate capacitance along with the inductance makes the inductor resonant at a lower frequency, which limits the maximum working frequency. Substrate resistance introduced by eddy current consumes input energy and therefore lowers the quality factor or Q factor. Those are intrinsic issues of 2D design, and are difficult to overcome at the same time although many methods have been proposed so far. To thoroughly solve the problems of planar spiral inductor, 2D design has to be abandoned.

In this thesis, a novel three-dimensional (3D) on-chip spiral inductor design is proposed and demonstrated based on self-rolled-up nanomembrane (RUN) nanotechnology. Electrical performance of RUN-inductor shows high frequency working ability into millimeter wave band with good Q factor and super compact on-chip footprint (10x ~ 100x smaller compares to planar spiral inductor with same inductance). Design methodology, physical modeling, fabrication process, characterization system and experimental results are illustrated in detail.

1.2 On-chip Inductors

Inductors, governed by Faraday’s electromagnetic induction law, resist the change in current passing through them. Inductors are characterized by their inductance, which is defined by the induced electromotive force to the rate of change of current. Inductance can be precisely designed in circuits for impedance matching, voltage / current transformation, frequency filtering, AC current blocking, etc. On-chip lumped inductors are very attractive in RFICs because of their considerable size reduction compared to distributed counterparts. The planar spiral inductor is the most commonly used on-chip lumped inductor due to its easy fabrication on Si and GaAs substrates.
1.2.1 Inductor Performance Characterization

Electrical performance of an on-chip inductor is characterized by inductance, $Q$ factor and self-resonant frequency. Inductance is defined as the ratio of the voltage to the rate of the change of current, which has units of henries (H). Physically, inductance describes the inductor’s ability to store temporary magnetic field energy. $Q$ factor is defined by the following equation (1.1) [6]:

$$Q = 2\pi \cdot \frac{\text{energy stored}}{\text{energy loss in one oscillation cycle}}$$

$$= 2\pi \cdot \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss in one oscillation cycle}}$$

(1.1)

The value of $Q$ factor is proportional to the net magnetic energy stored in the inductor, which can be calculated by the difference between the peak magnetic energy and the peak electric energy. Electric energy is stored in the parasitic capacitors and mainly introduced by crosstalk of EM fields between nearby metal parts of the inductor. The value of the peak electric energy is independent on operating frequency, but the value of the peak magnetic energy is dependent on it. Therefore, the value of $Q$ factor is dependent on frequency and vanishes at a certain frequency which is called the self-resonant frequency $f_0$. Above the self-resonant frequency $f_0$, an inductor is unable to output net magnetic energy to the external circuit.

1.2.2 Planar Spiral Inductor

Figure 1.1 shows a micro photo image of a planar rectangular spiral inductor fabricated on silicon substrate with 10 turns [4]. The planar spiral inductor is designed to utilize self- and mutual induction of long metal wires to achieve a desired inductance. Unfortunately, to obtain several nH inductance, spiral inductors generally require more than 10,000 $\mu\text{m}^2$ chip-area which
is huge compared to the footprints of other on-chip components (transistors, capacitors, resistors, etc.). Furthermore, when a spiral inductor is fabricated on low-resistivity substrate, capacitive and magnetic coupling between the spiral wires and the substrate stores electromagnetic energy which reduces the $Q$ factor. This parallel-connected parasitic capacitance also decreases the inductor resonant frequency point and prevents the application of spiral inductor in higher frequency band. When a planar inductor is fabricated on flexible substrate, as the working frequency is in the RF band, its electrical performance is sensitive to the substrate mechanical deformation, which is not acceptable in the application of wearable devices.

![Image](image.jpg)

**Figure 1.1** Top view of the micro photo image of a rectangular spiral inductor fabricated on silicon substrate with 10 turns [4].

Over the past several decades, significant progress has been made implementing advanced fabrication technologies to reduce the parasitic effects from the substrates and to scale down the dimension of planar spiral inductors. These improvement solutions can be classified into two categories: (1) isolation of the spiral wires and (2) constructing spiral wires in the vertical direction. In (1), the substrate can be etched under the spiral wires [10], the entire 2D spiral structure can be lifted above the substrate [11, 12], or the resistivity of the substrate can be selectively increased [13, 14]. Therefore, the electromagnetic coupling and the parasitic capacitance between the inductor and the substrate can be dramatically reduced. Available
fabrication techniques include bulk micromachining, surface micromachining, and electrochemical processes. In (2), multiple spiral wires can be stacked together vertically by the same 2D process technology and use metallic vias to connect adjacent layers [7, 15, 16]. All these solutions are able to substantially increase the resonant frequency \( (f_0) \) and \( Q \) factor (~2x \( f_0 \) and >20 \( Q \) factor) compared to conventional spiral inductors with the same inductance. Those solutions are still based on 2D design philosophy; although they are able to address some of the intrinsic issues of planar spiral inductors, the essential problems of 2D structure inevitably lead to the tradeoff of the on-chip footprint and overall inductor electrical performances.

1.3 Self-rolled-up Nanotechnology

Since the first report of strain-induced self-rolled-up microtubes in 2000 by Prinz et al. [17], self-rolled-up nanomembrane (RUN) tubes have attracted great attention in many academic laboratories. The first microtube was made by a strained InAs/GaAs epitaxial thin film bilayer, which is grown using molecular beam epitaxy (MBE). Since then, many types of self-rolled-up tubes made by semiconductors [17, 18], dielectrics [19-21], polymer [22] and metals [23] have been demonstrated. Their structures and material system are versatile with the application of different nano-membrane deposition methods, like plasma enhanced chemical vapor deposition (PECVD), metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE), etc. A general planar structure that is able to roll up must contain a strained layer and a sacrificial layer underneath it. The material system for the strained layer can be amorphous films, epitaxial single-crystal films, strained polymer bilayers or hybrid material systems. Epitaxially deposited lattice-matched heterojunctions, spun-on layers and semiconductor substrates can be used as sacrificial layers. A net force must be generated from all of the sub-layers to obtain large enough momentum to begin and maintain the rolling process until the strained layer is fully
released. The releasing of the strained layer is usually done by removing the sacrificial layer, such as wet or dry etching the semiconductor substrates or stripping away the spun-on photoresist (PR) layer. RUN-tubes have been successfully used in many practical applications, including III-V quantum dot microtube lasers [24], metamaterials [25], RF transformers [26], super capacitors [27], optical resonators [28], biological sensors [29], and more.
CHAPTER 2: RUN-TUBE DESIGN AND MODELING

2.1 Device Structure

Compared to the 2D planar spiral structure, the microtube is a tightly rolled-up 3D spiral structure. The curvature of the microtube is determined by the material’s mechanical properties and the side-wall thickness of each strained sub-layer [30, 31]. The inner diameter of the microtube is usually in between 3-100 μm, and the wall thickness of a single turn is usually 30-700 nm. The metal layer is deposited using e-beam evaporation on top of the strained layers; afterwards, it can be rolled up with the other strained layers to form metal spirals. Because the wall thickness of each single turn is negligible compared to the inner diameter, all the metal spirals are strongly coupled to each other when an RF signal is applied. The induction of the electromotive force can be expected to be much more efficient in the microtube structure compared to the 2D spiral structure. Furthermore, there is a little overlap between the metal spirals and the substrate, so the capacitive coupling and eddy current due to magnetic coupling are negligible on any kind of substrate. These intrinsic advantages of microtubes make them highly suitable as a new platform for superior compact and high performance on-chip lumped inductor design.

Figure 2.1a shows a schematic diagram of the microtube inductor structure before rolling. Square-wave-like patterned 5 nm nickel/100 nm gold bilayer thin film is deposited on top of a high frequency (HF) SiNx layer by electron-beam evaporation. Nickel thin film works as an intermediate layer to improve the adhesion and surface morphology of the gold thin film. The gold film shows a resistivity just 1.3 times larger than that of bulk gold. Nickel and gold films actually help the rolling due to their large tensile residual stress ~ 798.4 MPa and 379 MPa.

respectively. Low frequency (LF) and HF SiNₓ films with same thickness ~ 20 nm are deposited on top of a 10 nm thick germanium thin film layer. The germanium layer holds the LF and HF SiNₓ layers on top before rolling and slowly releases them after being etched away. The silicon substrate is oxidized to have a 1 µm thick SiO₂ layer on top, which serves as an insulation layer to electrically isolate the microtube inductor with the substrate. This structure design leads to a 3D multiple turn spiral structure with an inner diameter ~ 10 µm. The number of turns can be controlled by predefining the rolling length of SiNₓ films. In Figure 2.1b, metal strips have been rolled up together with SiNₓ films to form a 3D structure with multiple turns and spirals.

![Diagram](image)

**Figure 2.1** Schematic diagrams of microtube inductor structures before and after rolling up, with structure parameters labeled. (a) 2D pattern with current flowing through conductive metal strips. (b) 3D view of a rolled up 4-cell structure [32].
2.2 Physical Equivalent Circuit Model

A compact, accurate physical model is desired for on-chip inductor design insights and optimization. The difficulty of modeling is to identify the relevant parasitic and their effects. The most successful approach is to use a lumped circuit elements network to represent the complexity of high-frequency phenomena such as substrate effects and crosstalk between interconnects. Figure 2.2a shows the lumped circuit physical model for two adjacent spirals which considers the cancellation mutual inductance $M$ between them due to their opposite current flow directions. Lumped capacitor $C_c$ models the strong EM interference between turns, and lumped element $L$ models the self-inductance of a spiral. The metal layer in the microtube inductor is just $\sim 100$ nm thick, which is much smaller than the skin depth at working frequency even up to 40 GHz. Therefore, the eddy current effect can be ignored and the resistance $R$ of one spiral becomes frequency independent. Lumped elements $R_c$ and $L_c$ model the resistance and inductance effects of a single connection line.

EM wave propagation in the substrate could be skin effect mode, surface wave mode, or quasi-TEM mode depending on the doping level of the substrate from high to low. The EM wave propagation can be modeled by a network constructed by lumped elements $C_s$ and $R_s$ as shown in the dotted box in Figure 2.2a.
Figure 2.2 Lumped circuit physical model for microtube inductor. (a) Model for two adjacent cells. (b) Model for entire microtube inductor by ignoring the connection line inductance effect and substrate loss. (c) Concentric cylinders approximation structure. (d) Mutual induction between two cylinders separated by distance \( l_c \). [32]
$R_s$ models the substrate loss and can be calculated by equation $R_s = 2/sG_{sub}$. $C_{ox}$ models the capacitive effect between the bottoms of the outmost metal spiral and the doped substrate. $C_s'$ and $C_{ox}$ are calculated by $C_s' = sC_{sub}/2$ and $C_{ox} = s \cdot \varepsilon_{ox}/(2t_{ox})$, where $s$ is the effective overlapping area of the outmost spiral with the substrate, $G_{sub}$ and $C_{sub}$ are the conductance and capacitance per unit area for doped substrate. $G_{sub}$ and $C_{sub}$ are functions of the substrate dielectric constant and doping level. The fabricated microtube inductor has all the cells exactly the same, so the physical model for the entire structure can be built as shown in Figure 2.3b by ignoring the connection line inductance $L_c$ and substrate loss $R_s$.

As shown in Figure 2.3c, concentric cylinders are used to approximately model the electrical behavior of spirals due to the radius change of each turn is negligible. If the mutual inductance $M_{ij}$ of two cylinders separated by distance $l_c$ as shown in Figure 2.3d is known, the self-inductance of a cell can then be calculated by $L = \sum_{i=1}^{N_t} \sum_{j=1}^{N_t} M_{ij,l_c}=w_s$ and the cancellation mutual inductance of adjacent cells can then be calculated by $M = \sum_{i=1}^{N_t} \sum_{j=1}^{N_t} M_{ij,l_c}>0$, where $N_t$ is the number of turns. The magnetic flux density $B$ is assumed to be uniform in slice 2 and its value equals that at its center point $O$. The magnetic flux density $B'$ generated by slice 1, if considering its thickness $t$, can be calculated by equation (2.1).

$$B'(l,l') = \int_{R}^{R+t} \frac{\mu_0 \rho^2 I}{2w_s t \left[ \rho^2 + (l_c + w_s + l' - 2)^2 \right]^{3/2}} d\rho$$

(2.1)

The total magnetic flux density $B$ generated by cylinder $i$ passing through slice 2 can be then calculated by the following integral.
\[ B(l') = \int_0^{w_s} B'(l, l') dl \]  
\hspace{1cm} (2.2)

Considering the length of cylinder \( j \), the mutual inductance \( M_{ij} \) can be calculated by equation

\[ M_{ij} = \int_0^{w_s} B'(l, l') \frac{\pi R^2}{w_s l} d l' = \frac{\pi \mu_0 R_i^2}{4t w_s^2} \cdot D_{ej} \]  
\hspace{1cm} (2.3)

where

\[ D_{ej} = (l_c + 2w_s)^2 \ln \left( \frac{R_j + t + \sqrt{(R_j + t)^2 + (l_c + 2w_s)^2}}{R_j + \sqrt{R_j^2 + (l_c + 2w_s)^2}} \right) \]
\[ - 2(l_c + w_s)^2 \ln \left( \frac{R_j + t + \sqrt{(R_j + t)^2 + (l_c + w_s)^2}}{R_j + \sqrt{R_j^2 + (l_c + w_s)^2}} \right) \]
\[ + l_c^2 \ln \left( \frac{R_j + t + \sqrt{(R_j + t)^2 + l_c^2}}{R_j + \sqrt{R_j^2 + l_c^2}} \right) \]
\[ + (R_j + t) \sqrt{(R_j + t)^2 + (l_c + 2w_s)^2} - R_j \sqrt{R_j^2 + (l_c + 2w_s)^2} \]
\[ - 2(R_j + t) \sqrt{(R_j + t)^2 + (l_c + w_s)^2} + 2R_j \sqrt{R_j^2 + (l_c + 2w_s)^2} \]  
\hspace{1cm} (2.4)

with \( R_i = R_1 + (i-1) \Delta R \), \( i=1,2,3,... \), \( R_j = R_1 + (j-1) \Delta R \), \( j=1,2,3,... \).
Figure 2.2a shows the lumped equivalent circuit of any two adjacent spiral cells in microtube inductor. Assuming all the cells are exactly the same, the lumped equivalent circuit of the microtube inductor is shown in Figure 2.2b, which is a two-port \( \pi \)-type admittance network with dotted boxes. By ignoring the inductance \( L_c \) (when \( l_s \gg l_c \)), the admittance matrix of the network is derived as

\[
Y = \begin{bmatrix}
Y_p + Y_S & -Y_S \\
-Y_S & Y_p + Y_S
\end{bmatrix}
\]  

(2.5)

where

\[
Y_p = j\omega N \left( C_c + C_p \right)
\]  

(2.6)

\[
Y_S = \frac{1}{N} \cdot \frac{R}{R^2 + \omega^2(L')^2} + \frac{1}{N} \cdot j\omega \left[ C - \frac{L'}{R^2 + \omega^2(L')^2} \right]
\]  

(2.7)

\( N \) is the number of spiral cells, \( L' = L - 2(1-N^2)M \). Matrix \( Y \) can be obtained from the feed lines de-embedded S parameters. The total effective inductance \( L_{\text{total}} \), Q factor \( Q_{\text{total}} \) and resonant frequency can then be derived from the matrix \( Y \) as shown in (2.8), (2.9) and (2.10) [32].

\[
L_{\text{total}} = \frac{\text{Im} \left( \frac{-1}{Y_{12}} \right)}{\omega} = \frac{\text{Im} \left( \frac{1}{Y_S} \right)}{\omega} = \frac{N[L' - C[R^2 + \omega^2(L')^2]]}{1 + \omega^2C^2[R^2 + \omega^2(L')^2] - 2\omega^2CL'}
\]  

(2.8)
Because the spacing between each turn is very small ($t_{SiN}<60\ \text{nm}$), the adjacent turns are not equipotential when the inductor is under high frequency operation. Therefore the crosstalk capacitance $C$ cannot be ignored. The value of $C$ is considered to be similar to that of a coaxial capacitor whose capacitance can be calculated by equation (2.11).

$$C = \left\{ \sum_{i=2}^{N_t} \ln \left[ \frac{1 + \frac{\Delta R(i-1)}{R_1}}{2\pi \varepsilon_{SiN} w_s} \right] \right\}^{-1} \approx \frac{2\pi \varepsilon_{SiN} w_s}{\ln \left[ 1 + \frac{\Delta R(N_t-1)}{R_1} \right]}$$

### 2.3 Simulated RUN-inductor Performance

By using physical model, the performance of designed RUN-inductor can be predicted before fabrication. Also, dimension parameters (inner diameter, number of turns, metal strip thickness) can be optimized to obtain the best desired inductor performance. Figure 2.3a shows the relationship between the effective inductance and the operating frequency for RUN-inductors with different number of turns and lateral unit cells. Figure 2.3b shows the relationship between the $Q$ factor and the operating frequency for RUN-inductors with different number of turns and lateral unit cells. Devices simulated here are assumed to have 100 nm thick, 15 $\mu$m wide Ag, 3 $\mu$m inner diameter, 40 nm thick SiN$_x$ bilayer and 15 $\mu$m separation distance between cells.
Figure 2.3 Performance of RUN-inductor as a function of structural parameters. (a) Effective inductance vs. operating frequency for devices with different number of turns and cells. (b) $Q$ factor vs. operating frequency for devices with different number of turns and cells [32].
Large effective inductance can be obtained easily by increasing the number of turns or cells. Strong mutual coupling between turns makes the effective inductance increase dramatically when linearly adding more turns in each cell. The $Q$ factor and resonant frequency remain high when having more lateral cells connected in series due to the extremely small substrate capacitance, which is also implied in equations (2.9) and (2.10). A super compact on-chip footprint can be realized when RUN-inductors have similar performances to their planar counterparts. As seen in Figure 2.3, a 45-turn 2-cell inductor with an effective inductance of 10 nH, maximum $Q$ factor 21 at 15 GHz, resonant frequency at 25 GHz only covers $45 \times 16 \ \mu m^2$ wafer area which is 0.45% of that of a planar spiral inductor ($400 \times 400 \ \mu m^2$, 8 nH inductance, maximum $Q$ factor ~ 6 at 3GHz) [5]. The extreme stand-alone structure is a 2-cell device, like the 56-turn 2-cell RUN-inductor. It is able to reach 10 nH inductance, 23 maximum $Q$ factor at 11 GHz, but only occupies $15 \times 19 \ \mu m^2$ on-chip area, which is 1000x smaller of that of its planar counterpart [5].

When metal thickness is fixed, the resistance of RUN-inductor is determined by the width of metal strips and metal resistivity. As reported, the resistivity more than 300 nm is able to reach low resistivity ~ $2 \ \mu \Omega \cdot cm$ for Ag thin film. The resistivity of gold thin film can reach ~ 1.6x times larger than its bulk value when the deposition thickness is ~ 100 nm. Figure 2.4a shows the relationship between the $Q$ factors and operating frequency when different material systems are used. A RUN-inductor made by reported Ag-W thin film can have a maximum $Q$ factor ~ 8 at 14 GHz. Material does not have any effect on the effective inductance as shown in Figure 2.4b. Figure 2.4c shows the effect of the width of the metal strip on the effective inductance and $Q$ factor. Increasing the width of the metal strip drops the magnetic induction and therefore drops the inductance. On the other hand, wider metal strips introduce more parasitic
substrate capacitance and lower the resonant frequency. However, the increasing of metal strips drops the resistance of the inductor. The dropping of resistance and the increasing of inductance finally result in a small increase of the $Q$ factor as shown in Figure 2.4d.

![Figure 2.4](image)

**Figure 2.4** $Q$ factor and effective inductance vs. operating frequency with different metal strip resistivity and width. (a) Effect of resistivity on $Q$ factor. (b) Effect of resistivity on effective inductance. (c) Effect of metal strip width on effective inductance. (d) Effect of metal strip width on $Q$ factor.
CHAPTER 3: EXPERIMENTAL PROCEDURES

3.1 Device Fabrication

The proposed inductor design is based on the silicon nitride (SiNₓ) self-rolled-up microtube platform because it is cost-effective to fabricate and compatible with CMOS integrated circuits. PECVD is widely used in microelectronics research to deposit high quality SiNₓ thin-film on large wafers with high deposition rate under a relatively low temperature (300 °C). The in-film residual stress of SiNₓ can be tuned by setting up different deposition parameters, such as operating frequency, input power, and gas flow rate, etc. In SiNₓ film, which is deposited using ammonia (NH₃) / silane (SiH₄) / nitrogen (N₂) PECVD system, N-H, Si-H, and Si-N bondings exist at the same time. The content of the bonded hydrogen (combination of NHₓ and SiH) determines the type and value of residual stress. Tensile stress decreases and compressive stress increases with an increase of the bonded hydrogen content. The bonded hydrogen content is determined by the deposition parameters. For the PECVD system used in the microtube inductor fabrication, low frequency compressive strain (-1168 MPa) SiNₓ film (LF SiNₓ) is deposited at 380 kHz and high frequency tensile strain (406 MPa) SiNₓ film (HF SiNₓ) is deposited at 13.56 MHz. Compared to bulk silicon nitride, PECVD thin film SiNₓ using ammonia (NH₃) / silane (SiH₄) / nitrogen (N₂) plasmas contains a high amount of amine fragments, which results in a Young’s modulus ~ 180 GPa and ~ 170 GPa for LF SiNₓ and HF SiNₓ thin films [8].

Silicon nitride tube inductor samples are fabricated by depositing thin film layers in sequence on doped silicon wafers. Silicon wafers with different resistivity (1~5 Ω·cm, 10~20 Ω·cm, 40~60 Ω·cm) are used to examine the substrate immunity of tube inductors. A 1µm thick silicon dioxide layer is grown by thermal oxidation to electrically insulate the tube inductor from the doped substrate, followed by a 20nm germanium (Ge) sacrificial layer deposited by E-beam
evaporation and 20nm silicon nitride thin film by PECVD in low frequency mode. A rectangular mesa is then defined by the optical lithography and reactive ion etching. A 30 nm SiN\textsubscript{x} thin film is then deposited by PECVD in high frequency mode to cover the entire mesa. Finally, a serpentine metal line is deposited by e-beam evaporation and metal lift-off technology. The material structure of the metal line includes a 100nm gold (Au) layer on top of a 5nm nickel (Ni) layer, with residual stresses +600MPa and +300MPa, respectively.

Importantly, unidirectional releasing and rolling is indispensable for multi-turn tubular inductors. Although several methods have been developed to realize unidirectional rolling, they suffer from the difficulties (challenges) of precise control, compatibility with traditional planar processing techniques, and the limitation of strained thin film material available. In experiment, the strained silicon nitride bilayer structure proposed is capable of acting as a universal unidirectional rolling carrier (bus) and gives the freedom to roll up the conductive patterned metal layer on top or any thin film adhesive to it. First, as shown in Figure 3.1, dry etch along the edge at one end of the bilayer mesa is performed, exposing the Ge sacrificial layer at the bottom. Then, the sample undergoes a lateral wet etching process in hydrogen peroxide at 90 °C. Once the removal of the exposed sacrificial layer initiates, the opposing strain within the bilayer generates a net momentum, driving the planar membrane to scroll up and continue to roll into a tubular structure. The momentum also tears apart the HF SiN\textsubscript{x} sidewalls protecting the Ge sacrificial layer from all-around etching as the removal of sacrificial layer continues. This dynamic tearing process ensures unidirectional multiple-turn rolling throughout the wet etching, and stops at the location where the sacrificial layer is fully released. Since the inner diameter can be well predicted by the model, the turns of the inductor can be precisely engineered by tuning the length of the strained bilayer. The pre-defined gold strips wrap around the longitudinal axis.
and serve as inductor cells.

**Figure 3.1** Schematic diagrams illustrating the process of fabricating rolled-up inductors. (a) 1 µm silicon oxide layer (Si substrate not shown). (b) Deposition of 20nm Ge sacrificial layer. (c) Deposition of 20nm LF SiNx thin film. (d) Mesa defined using optical lithography followed by dry etch. (e) Mesa covered by 30nm HF SiNx thin film. (f) Deposition of 5nm Ni and 100nm Au on top of the mesa. (g) Dry etch along the edge of one side of the mesa to expose sacrificial layer for unidirectional etching [9].
3.2 Measurement and Characterization

Two port S-parameters are measured by using Agilent PNA8363C purpose network analyzer with cascade microtech air coplanar ground-signal-ground probes in frequency range from 0.1 GHz to 40 GHz. To do the RF measurement of the tube inductor, the test fixture is designed as shown in Figure 3.2. Parasitic effects introduced by feedlines need to be removed to obtain the real performance of the device under test (DUT). Open-through de-embedding technique is used here to calibrate out the feedline effects. Lumped equivalent circuit model is constructed to represent the physics of parasitic effects. As the RF measurement goes up to 40 GHz, feedlines are designed as short as possible to minimize the distribution effect. Open-through de-embedding patterns are shown in Figure 3.2. As shown in Figure 3.2(a), an admittance Π-network is used to model the capacitive effects between the contact pads and the surrounding environment including the substrate and RF ground. Series connected impedance network is used to model the resistance and inductance of the feedlines. Figure 3.2(a), 3.2(b) and 3.2(c) show the schematic view of patterns with the DUT, without the DUT (open case) and shorted. Corresponding lumped equivalent circuits are constructed to model the RF performance of each pattern. The narrow branches of feedlines are bent 90 degrees to avoid using additional lines to connect the two feedlines.
Figure 3.2 Open-through de-embedding patterns and their corresponding lumped equivalent circuits. (a) Test pattern with DUT. (b) Open pattern. (c) Short pattern.

Mathematical procedure to do the open-through de-embedding is shown in Figure 3.3. Figure 3.3 shows the first step which abstracts the admittance Π-network (open pattern) from the original data. The result still contains the parasitic resistances and inductances (Z1 and Z2) whose total effect can be calculated by doing step 2 shown in Figure 3.3. Finally, the real performance of the DUT can be obtained by doing step 3.
Figure 3.3 Mathematical procedure to do the open-through de-embedding. (a) Subtract measured data of open pattern from raw data with DUT. (b) Subtract measured data of open pattern from data of through pattern. (c) Subtract data obtained from step 2 from data of from step 1.
CHAPTER 4: EXPERIMENTAL RESULTS

4.1 Fabricated Samples

To prove the advantages of RUN-inductors, samples with different number of turns and cells are designed and fabricated on silicon substrates with different doping level and on sapphire substrate which is considered to be an ideal insulation substrate. Fabricated sample structures include 2-cell-3-turn, 4-cell-3-turn, 6-cell-3-turn, 2-cell-9-turn, 4-cell-9-turn, 6-cell-9-turn and 2-cell-15-turn, 4-cell-15-turn, 6-cell-15-turn. All the samples have the same dimension of the metal strips and the SiN$_x$ bilayer. The dimension of metal strip is 15 µm, 30 µm or 20 µm wide. The connection line length is 20 µm, and its width is 10 µm. Metal strip is constructed by 5 nm Ni and 100 nm Au. The thicknesses of LF and HF SiN$_x$ layer are 20 nm and 30 nm, respectively. The inner diameter of all samples is ~ 10 µm. The optical images of a rolled-up 15-turn-6-cell tube inductor with RF testing pads before and after rolling up are shown in Figure 4.1.

Figure 4.1 A microscopic overview of a tube inductor with 6 metal strips, $W_s=20\mu m$, $L_c=20\mu m$ and $W_c=10\mu m$, N=15, (a) un-rolled-up 2D tube inductor pattern, (b) rolled-up tube inductor, (c) a schematic diagram of the metal serpentine line, which is composed by strip lines and connecting lines [9].
Figure 4.2(a) and 4.2(b) show the side wall SEM pictures of two rolled up tube inductors with different number of turns. The on-chip footprints which is defined as the projection area on the substrate of the 3 and 15-turn tube inductors are $240\times11\mu m^2$ and $240\times13\mu m^2$, respectively.

**Figure 4.2** Cross-sectional-view SEM images of rolled up tube inductors, with the metal strips clearly seen on the inner wall of the tubes. Inner diameter (ID) and outer diameter (OD) geometry $W_S=20\mu m$, $L_c=20\mu m$ and $W_C=10\mu m$, (a) 3 turns tube inductor, (b) 15 turns tube inductor [9].
4.2 Electrical Performance

Figure 4.3 shows the Smith charts of measured $S_{11}$ parameters of the tube inductors. Figure 4.3 (a) and (b) are data before and after de-embedding for samples with 6 cells but with different number of turns. Figure 4.3 (c) and (d) are data before and after de-embedding for samples with 15 turns but with different number of cells. It can be found that resonant frequency increases greatly after calibrating out the feedlines. Up to 40 GHz, fabricated devices show inductive performance but with relatively large resistances.

**Figure 4.3** Smith charts of measured $S_{11}$ parameters of the tube inductors, with 3, 9 and 15 turns and with 6 metal strips at $W_s=20\mu m$, $L_c=20\mu m$, before (a) and after (b) de-embedding; with 2, 4, 6 cells or metal strips and 15-turns at $W_s=40\mu m$, $L_c=20\mu m$, before (c) and after (d) de-embedding [9].
Following the mathematical extraction procedure, effective inductance and $Q$ factor versus frequency of all samples can be obtained, and the resonant frequency can be then found when the $Q$ factor vanishes. Those three parameters describe the overall performance of any kind of inductor. In the case of a tube inductor, their values depend on structural parameters like the number of turns, the number of cells and the metal strip width when the thickness of the metal strip is fixed and the cancellation mutual inductance between adjacent cells can be ignored.

Figure 4.4(a) and 4.4(b) show the relationship between the extracted effective inductance and $Q$ factor curves with frequency of samples with 3, 9 and 15 turns and with 6 metal strips at metal strip width $W_s=20\mu m$, connection line length $L_c=20\mu m$ and sample with 2, 4, and 6 cells or metal strips and 15 turns at metal strip width $W_s=40\mu m$, connection line length $L_c=20\mu m$. Figure 4.4(c) shows the relationship of the effective inductance and $Q$ factor of samples with different number of cells versus the number of turns on 40~60 $\Omega\cdot$cm silicon substrate. The effective inductance is the sum of self-inductances of all turns and mutual inductances between every two different turns. When more turns are coiled up, mutual inductance will be greatly enhanced leading to dramatically increased of effective inductance shown in Figure 4.4(c). The $Q$ factors are measured at 10 GHz where they have not reached their maximum values. The increase of $Q$ factor when more turns are rolled up is further evidence to show the strong mutual coupling property of the tube inductor. To obtain a desired inductance, the tube inductor can be designed to be less-cell-more-turn structure or more-cell-less-turn structure. Shown in Figure 4.4(c), the 4-cell-9-turn and the 2-cell-15-turn samples indicated by marker 1 and 2 have similar inductance $\sim 1$ nH, but the $Q$ factor of the 2-cell sample is much higher than that of the 4-cell one. This is due to faster increase of inductance than resistance when more turns are added. Therefore, for a same inductance tube inductor, it is better to design fewer-cell-more-turn
structure rather than more-cell-fewer-turn structure to fully take advantage of strong mutual coupling. It can be further inferred that the extreme optimized case of tube inductor design is to use two-cell structure.

Strong mutual coupling is also the key factor to obtain large inductance with ultra-compact on-wafer footprint. The frequency dependent trend of effective inductance is determined by the crosstalk capacitance between adjacent turns, and the resonant frequency is determined by the crosstalk capacitance between adjacent turns, oxide layer parasitic capacitance, and the substrate parasitic capacitance which depends on the tube projection area on substrate and the doping level of the substrate. The measured overall crosstalk capacitances of all samples have very small value about several femtofarads, which makes the value of effective inductance a constant value over a wide frequency range that is up to millimeter-wave frequencies. Shown in Figure 4.4(d) are the relationships among the effective inductance and resonant frequency versus the width of metal strip on different doping level substrates. The effective inductances of all samples are exactly the same and their resonance frequencies are slightly different on all kinds of substrates, which means the values of substrate parasitic capacitance and oxide layer parasitic capacitance are negligible even if the tube inductor is put on a heavily doped silicon wafer (1~5 Ω·cm). The phenomenon of tube inductor having similar performance on silicon substrates with different doping levels is called substrate immunity.
Figure 4.4 Experimental results of RUN-inductors. (a) Extracted effective inductance and $Q$ factor curves vs. frequency of samples with 3, 9 and 15 turns and with 6 metal strips at metal strip width $W_s=20\mu$m, connection line length $L_C=20\mu$m. (b) Extracted effective inductance and $Q$ factor curves vs. frequency of samples with 2, 4, 6 number of cells or metal strips and 15 turns at metal strip width $W_s=40\mu$m, connection line length $L_C=20\mu$m. (c) Plots of inductance as a function of number of turns and metal strip width. (d) Measured effective inductance and resonant frequency vs. width of metal strip line for a 6-cell-9-turn sample on substrate with different resistivity. Inductance and resonant frequency are both immune to substrate [9].
4.3 Model Comparison

In Figure 4.5(a) and 4.5(b), measured effective inductances and Q factors versus frequency from 0.01GHz to 40 GHz are plotted and compared to modeled data obtained from our previously published physical model. Samples with 9 turns but different number of cells or 4 cells but different number of turns are fabricated on 40–60 Ω-cm silicon substrate. Good agreement between the measured and modeled data can be found indicating the high accuracy and reliability of the physical model. Even with large resistance due to narrow cross section of metal layers, the maximum values of Q factor of all samples are acceptable in practical RFIC design. 100 nm thick gold thin film is able to make the surface of the metal strip very smooth to obtain resistivity just 1.3 times larger than its bulk value. Skin effect and proximity effect can both be negligible because the gold layer is thinner than its skin depth even at 40 GHz. So the resistance of the tube inductor can then be considered as a constant value over the whole working frequency range, and the Q factor is therefore totally determined by the resistivity of the conduction layer.

![Figure 4.5](image.png)

*Figure 4.5* The lumped circuit model for two adjacent cylindrical cells connected in series. Derived mathematical expressions for inductance $L$, $Q$ factor, and self-resonant frequency $f_0$. Comparison between the experimental and modeled data for various geometries [9].
CHAPTER 5: CONCLUSION

In conclusion, employing the built-in strain in SiNₓ bilayer and Ni/Au metal conductor, on-chip self-rolled-up tube inductors are demonstrated on silicon substrates with resistivity ranging from ~ 1 to ~ 60 Ω·cm and sapphire substrate by unidirectional scrolling nanofabrication technique. Such rolled-up tube inductors have achieved record inductance/area density, due to the strong mutual coupling effect. The footprint of the tube inductors demonstrated is more than one order of magnitude more compact than the planar spiral inductors with the same inductance. The strong confinement of electromagnetic field within the tube prevents distribution into the substrate. As a result, even on heavily doped silicon substrate, all samples show high self-resonant frequencies, beyond the range achievable by any reported planar counterparts of the same inductance, confirming the high immunity to substrate parasitic effect. Figure 5.1 shows the benchmark of 3D tube inductors demonstrated so far. By comparing to the state-of-the-art planar spiral inductors fabricated by 0.18 μm and 32 nm node CMOS technology with different metal material and thicknesses, the 3D tube inductor shows much higher maximum working frequency with much smaller on-wafer footprint and comparable maximum Q factor, even when made on a heavily doped silicon substrate. In addition, the measured data of all samples on different doping level substrates can be fitted very well with the previously proposed physical model. The combination of theoretical prediction and successful experimental demonstration makes the tube inductor platform realistic in future RFIC designs.
Figure 5.1 Benchmark 3D plot. Inductance, footprint, Q factor, and frequency at Qmax of rolled-up 3D tube inductors are plotted together with those for planar spiral inductors in the 0.18 µm and 32 nm node CMOS technology with different metal materials and thicknesses as indicated [9].
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