Analog filter design using Ring Oscillator Integrator (ROI) in 180nm CMOS

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Abstract

In this thesis, a novel technique of implementing an integrated active analog filter is discussed. It employs a ring-oscillator integrator (ROI) as a key element to build an on-chip low-pass filter. The motivation is to implement an analog filter using integrated circuit technology instead of discrete components to achieve area-saving, which is a key constraint for wearable electronics. The traditional operational amplifier (op-amp) based active filter is largely limited by the finite gain of the op-amp itself and the non-ideality of transistors. Scaling also contributes to the unreliability of the op-amp based filter because the output resistance of a transistor is severely reduced. ROI, on the other hand, has much better DC gain, which is approximately infinite at low frequency and independent of process scaling. This unique property could greatly compress the non-ideality that exists in op-amp circuits.

The design is first simulated in MATLAB/SystemVerilog to construct system-level requirements. Then the circuit-level simulation is performed using 180nm CMOS technology with 1.8V power supply in Cadence. The achieved bandwidth is 10MHz.

Subject Keywords: analog filter, ring oscillator integrator, 180nm CMOS

Acknowledgments

This project is a collaboration of Danyang Wang and Junheng Zhu, under the supervision of Prof. Pavan Hanumolu. Junheng worked mainly on system-level design using SystemVerilog and Danyang worked mainly on circuit-level design using Cadence. We would like to thank Prof. Hanumolu and his graduate student Mrunmay Talegaonkar and Guanghua Shu for their invaluable input and advice.

Contents

1. Introduction

The analog filter is the key component in analog signal processing. Traditional filter design includes an RLC based passive filter and operational amplifier (op-amp) based active filer, both designed off-chip using discrete components. The advantage is that the bandwidth could be as low as hundreds or tens of hertz because big passive component values are available, at the expense of more area and less flexibility. As technology and the need for wearable electronics continue to grow, however, on-chip analog filter is becoming increasingly more favorable. The difficulty is that the range of passive component values from Integrated Circuit (IC) fabrication technology is severely limited compared with discrete circuits, making it extremely hard to design a low bandwidth filter. Therefore, the motivation of this work is to build an on-chip low-pass filter with bandwidth less than 10MHz.

2. Literature Review

The literature on analog filter design mainly includes some basic analog filter design papers and textbooks, plus the paper covering ROI filter design by Brian Doris [2].

For system and circuit-level design of first and second order filters, the text "Design of analog filters" by Mac E. Van Valkenburg [1] and the app note "A basic introduction to filters-Active, Passive and Switch capacitor" by National Semiconductor [4] provide an in-depth introduction and instruction on op-amp based active filter and RLC based passive filter design.

For the ROI filter design, the main reference is the paper "Design of analog filter using ring oscillator integrator" by Brian Doris [2], published in Journal of Solid State Circuits. His master's thesis at Oregon State University [3] provides more details and insights in designing ROI filters.

3. Description of Research Results

3.1 Filter Design Fundamentals

In this section, the fundamentals of analog filter design are covered. They include: passive first and second order low-pass filter, active second order low-pass filter, and the comparison between them.

3.1.1 Passive first-order low-pass filter

The simplest way to design a low-pass filter is to use a resistor and a capacitor, as shown in Figure 1.

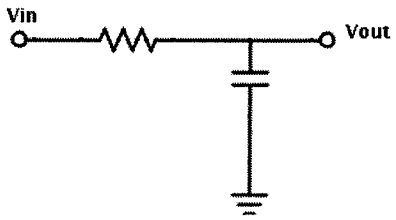


Figure 1: First order RC low-pass filter

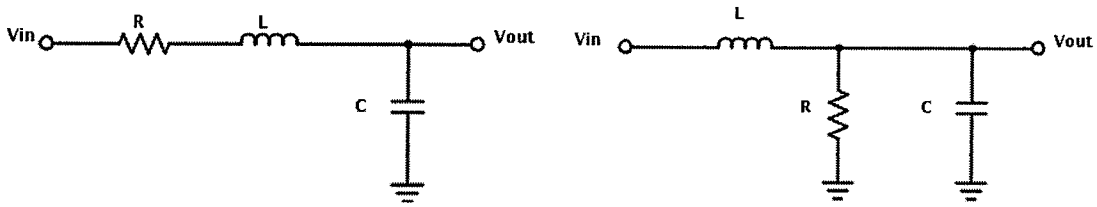
The transfer function of this system can be easily derived to be

$$\mathrm{H(s)} = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+sRC} = \frac{1}{1+\frac{s}{\omega_0}}$$

From the expression above, the 3dB bandwidth of this filter is described as $\omega_0 = \frac{1}{RC}$. After the frequency goes higher than this frequency (pole), the gain will decrease by a magnitude of -20dB/decade.

3.1.2 Passive second order low-pass filter

Although the first order low-pass filter is simple to implement, it sometimes cannot meet the need of faster damping as the magnitude only decreases by 20dB/decade after the frequency passes the pole. To remedy that, the second pole can be introduced into the system, forming a second order low-pass filter, or a "bi-quad". The circuit schematics are shown in Figure 2.



(a) (b)

Figure 2: Second order low-pass filter

Although the transfer functions of the two schematics are not the same, they can be generalized into one single expression.

$$H(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

$$Q = \begin{cases} \frac{\sqrt{L}}{\sqrt{C}R} & for\ (a) \\ \frac{R\sqrt{C}}{\sqrt{L}} & for\ (b) \end{cases}$$

$$\omega_0 = \frac{1}{\sqrt{LC}}\ for\ both$$

The term Q is defined as the "quality factor". It describes how under-damped a system is and characterizes the system bandwidth. Higher Q indicates lower rate of energy loss. The formal definition is

$$Q = 2\pi * \frac{Energy\ Stored}{Energy\ Dissipated\ Per\ Cycle} = 2\pi f_0 * \frac{Energy\ Stored}{Power\ Loss} = \frac{1}{2\zeta}$$

where ζ is the damping ratio.

The two poles of the second order low-pass filter therefore can be expressed as

$$s = -\omega_0\zeta \pm \omega_0\sqrt{\zeta^2 - 1}$$

Q not only affects the pole locations and the damping ratio, but also the peaking effect in low-pass filters as shown in Figure 3. As the value of Q increases, the peaking effect becomes more significant.

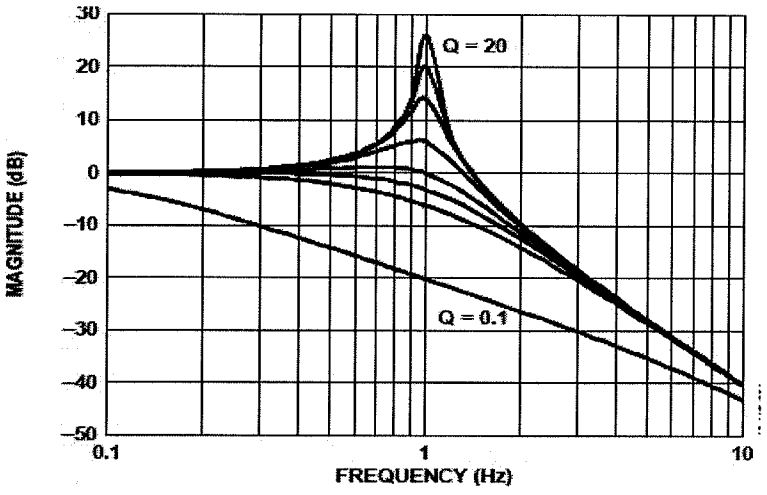


Figure 3: Peaking effect vs Q [4]

3.1.3 Active second order low pass filter (sallen key)

An analog filter built from passive elements is power saving and easy to implement. It also has less non-linearity and noise. However, several factors limit its performance. First of all, there is no gain from passive elements. If a certain gain is desired, then an amplifier must be added before the filter. Second, passive elements are lossy, especially for inductors (high-Q inductors are very expensive). More importantly, severe loading effect further deteriorates its application. As a result, the op-amp based active analog filter has been developed to remedy those drawbacks.

One popular implementation of a biquad low-pass filter is the Sallen-Key configuration as shown in Figure 4.

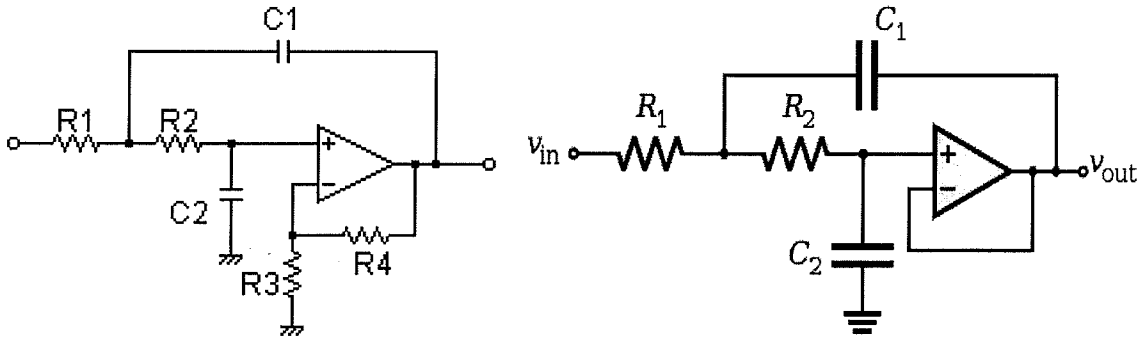


Figure 4: (a) Sallen-Key low-pass filter (b) Simplified version

The transfer function of Figure 4(a) is therefore

$$H(s) = \frac{A/(R1R2C1C2)}{s^2 + s\left[\frac{\left(\frac{1}{R1}+\frac{1}{R2}\right)}{C1} + \frac{1-A}{R2C2}\right] + \frac{1}{R1R2C1C2}}$$

$$A = 1 + \frac{R3}{R4}$$

where A is the low frequency gain. For the simplified version, its transfer function is given as

$$H(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}$$

$$\omega_0 = \frac{1}{\sqrt{R1R2C1C2}} = \frac{1}{RC} \; if \; R1 = R2, \; C1 = C2$$

$$Q = \frac{\sqrt{R1R2C1C2}}{C2(R1 + R2)} = 0.5 \; if \; R1 = R2, \; C1 = C2$$

3.1.4 Comparison of passive and active biquad filters

Based on the expressions from the previous sections, we could calculate for a specific 3dB bandwidth what component values should be chosen. Table 1 summarizes some possible choices for the biquad low-pass filters.

Table 1: Summary of possible component choices

R(kΩ)	L(pH)	C(pF)	Bandwidth(MHz)
1	100	100	10
100	1	1	10

(a)

R1(kΩ)	R2(kΩ)	C1(nF)	C2(nF)	Bandwidth(MHz)
0.1	0.1	9	9	10
10	10	0.1	0.1	10

(b)

Clearly, the component values are not practical to be integrated on chip.

3.2 System-Level Design of Ring Oscillator Integrator

Ring oscillator built from CMOS inverters has the property of infinite DC gain, which is much preferred over op-amp. Thus, ROI is proposed to design an active analog filter. The most common way to design a CMOS ring oscillator is to use three inverters in a feedback loop, as shown in Figure 5.

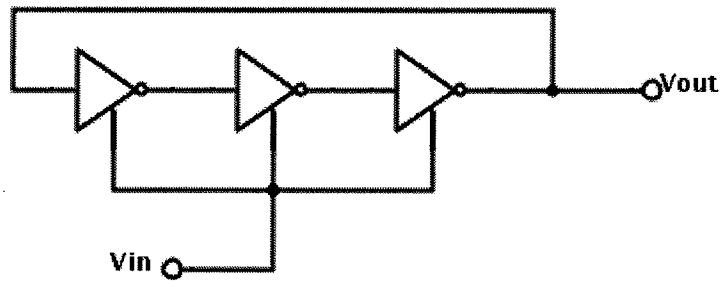


Figure 5: 3-stage inverter based voltage controlled ring oscillator

The transfer function of the output frequency to the input voltage could be expressed as

$$H_{VCO}(s) = \frac{\omega_{out}(s)}{v_{in}(s)} = K_{VCO}$$

where K_{VCO} is the oscillator gain. In terms of phase, the transfer function can be expressed as

$$H_{VCO}(s) = \frac{\phi_{out}(s)}{v_{in}(s)} = \frac{K_{VCO}}{s}$$

To use the oscillator gain, a phase detector is needed to convert the output phase to pulse-width modulated (PWM) voltage. The way the phase detector works is illustrated in Figure 6.

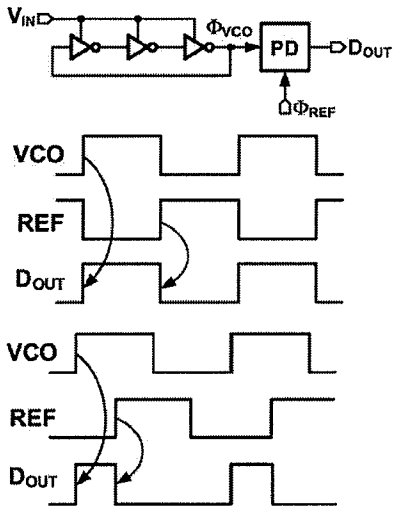


Figure 6: Phase to PWM conversion using phase detector [2]

The transfer function of the phase detector can be written as

$$H_{PD}(s) = \frac{\phi_{out}(s)}{\phi_{in}(s)} = K_{PD}$$

The phase detector gain K_{PD} is a constant and unitless, depending on which type of phase detector it is. For the simplest XOR phase detector, the gain is equal to $\frac{2}{\pi}$. In this design, the two-state phase detector is used and its gain is equal to $\frac{1}{\pi}$. This will be discussed later in more detail.

Finally, a charge pump is cascaded after the phase detector to convert the PWM voltage signal to PWM current. The gain of the charge pump is simply equal to the current that the charge pump provides. That is,

$$H_{CP} = K_{CP} = I_{CP}$$

Having each part of the integrator, the whole integrator schematic is shown in Figure 7 and the transfer function can be written as

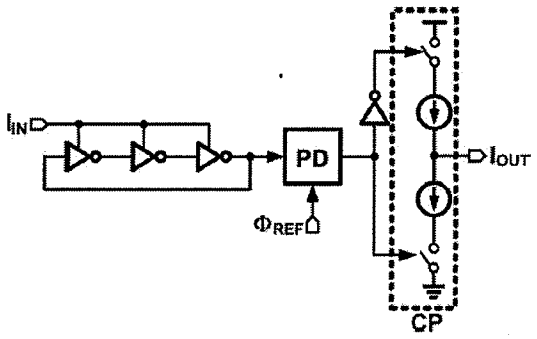


Figure 7: Ring oscillator integrator system-level schematic [2]

$$H_{INT}(s) = \frac{K_{CCO}K_{PD}K_{CP}}{s}$$

where K_{CCO} denotes current controlled oscillator gain instead of voltage controlled oscillator. The reason to work with current is that the oscillation frequency is mainly decided by the current through the oscillator. Although the input is still voltage, there is a simple way to convert the input voltage into current. The biasing point of the VCO could be viewed as an AC ground, and therefore a simple resistor could perform the conversion, as illustrated in Figure 8.

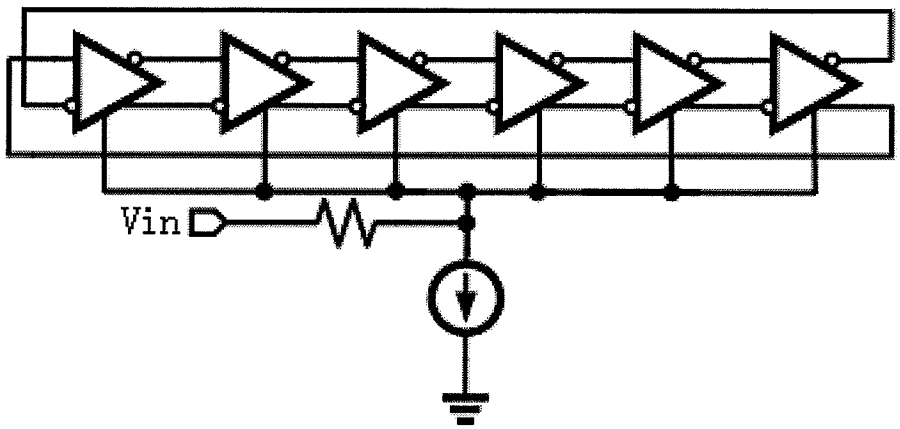


Figure 8: Input voltage-to-current conversion

$$I_{in} = \frac{V_{in}}{R}$$

3.3 System-Level Design of ROI Filter in SystemVerilog

This part is mainly done by Junheng Zhu. The overall system-level schematic is shown in Figure 9.

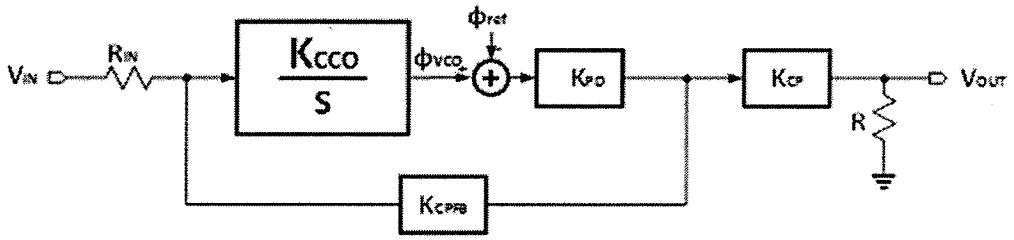


Figure 9: System-level schematic of ROI filter

The transfer function is therefore

$$\mathrm{H(s)} = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{R_{in}K_{CP}} \frac{1}{1 + \frac{s}{K_{CCO}K_{CP}K_{PD}}}$$

and the bandwidth is $K_{CCO}K_{CP}K_{PD}$.

3.4 Circuit-Level Implementation of ROI Filter in 180nm Cadence

With the system-level implementation of the low-pass filter completed, the next step is to implement it in transistor-level circuitry. Each individual circuit component is discussed, followed by the simulation result in 180nm CMOS using Cadence. The overall circuit schematic is shown in Figure 10.

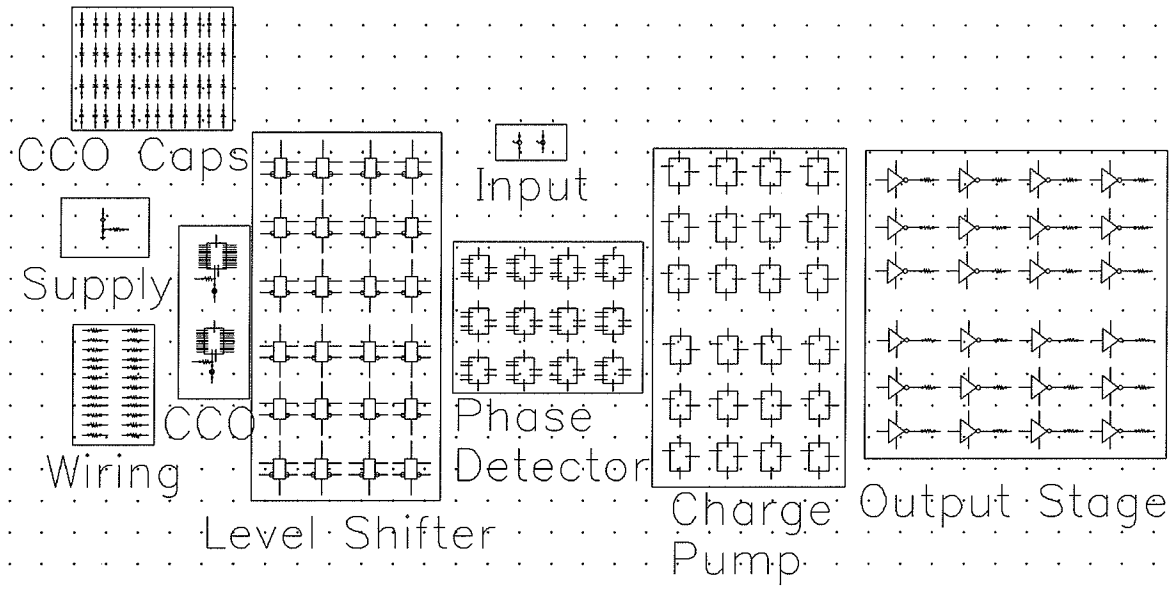


Figure 10: Overall circuit schematic

3.4.1 Delay cell

Delay cell is the key component of the oscillator. Since the standard CMOS inverter only has one input/output and two differential inputs/outputs are needed, a new topology should be used to achieve this. As shown in Figure 11, the differential delay cell is composed of two inverters and two feed-forward transmission gate logics that act as two resistors.

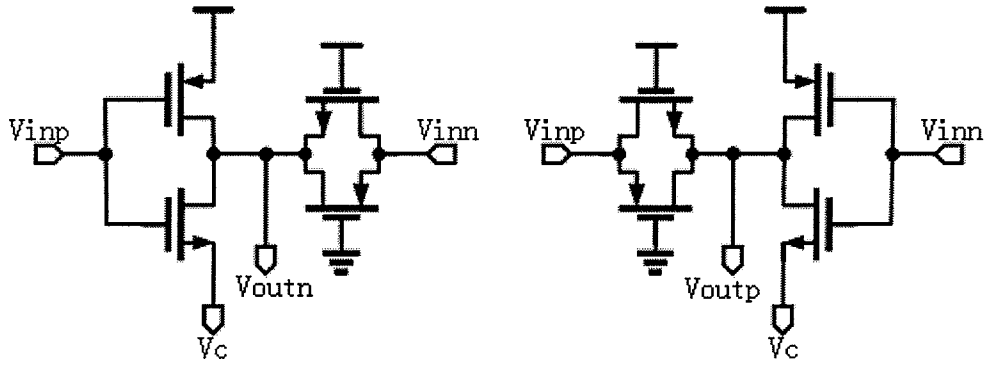


Figure 11: Differential delay cell schematic

The constraint is that the feed-forward paths should be large enough such that the oscillator does not latch up [3]. Since the effective resistance of the transmission gate largely depends on the W/L ratio instead of the output voltage, thus R_{on} can be adjusted by varying the W/L ratio of the transmission gate to ensure that latch up does not occur.

3.4.2 Multi-phase differential ring oscillator

In this design, 12 stages of delay cells and 24 phases are used. The circuit schematic is shown in Figure 12.

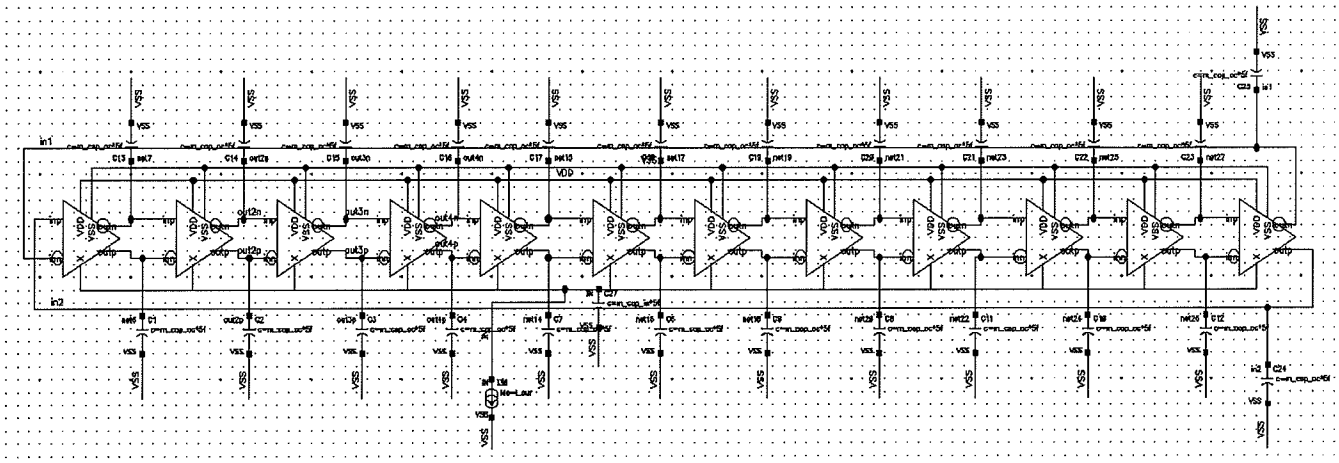


Figure 12: 12-stage ring oscillator schematic

The coupling capacitors at the output of each stage are used to add delay such that the oscillation frequency is of interest and therefore the K_{CCO}.

3.4.3 Level shifter

As shown in Figure 12, the current controlled ring oscillator requires a current source at the bottom, which also requires some biasing voltage to make it operate normally. As a result, each oscillator output cannot achieve full swing and is limited by the biasing voltage of the current source. Thus, a level shifter is employed to drive each oscillator output to full swing. Its schematic is shown in Figure 13.

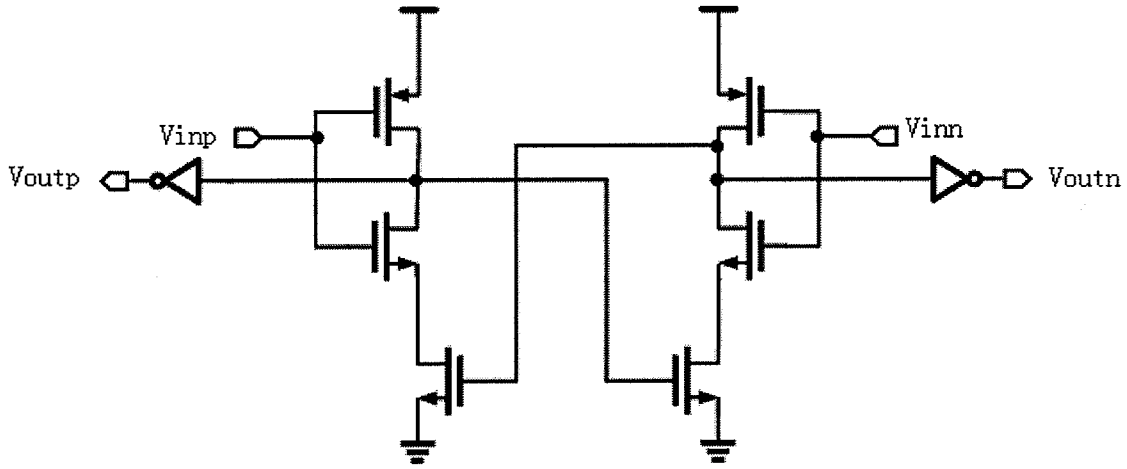


Figure 13: Level shifter

One constraint of the level shifter is that the minimum value of the input voltage should be as small as possible. In other words, the biasing voltage of the current source should be as small as possible; otherwise, the level shifter could not function normally. For example, if Vin- is small enough, only PMOS will be on. This will turn on the left bottom NMOS, which in turn pulls the input of Vout+ to ground. However, when Vin+ is VDD and Vin- just exceeds the threshold

voltage of NMOS, both the top NMOS and PMOS on the right branch will be on. During a short time period when the intermediate node on the left branch has not been pulled down, the right bottom NMOS will be on, which causes data contention at the right intermediate node. Since the top NMOS at the right branch is only weakly on, the pull-down ability of the left branch is much stronger than that of the right branch, and eventually the left intermediate node will reach ground. Nevertheless, the right intermediate node could also be pulled down to a small enough value less than the threshold of the inverter, which will make both Vout+ and Vout- to be ground.

3.4.4 Phase detector

The phase detector in this design is chosen to be the two-state phase detector. The schematic is shown in Figure 14.

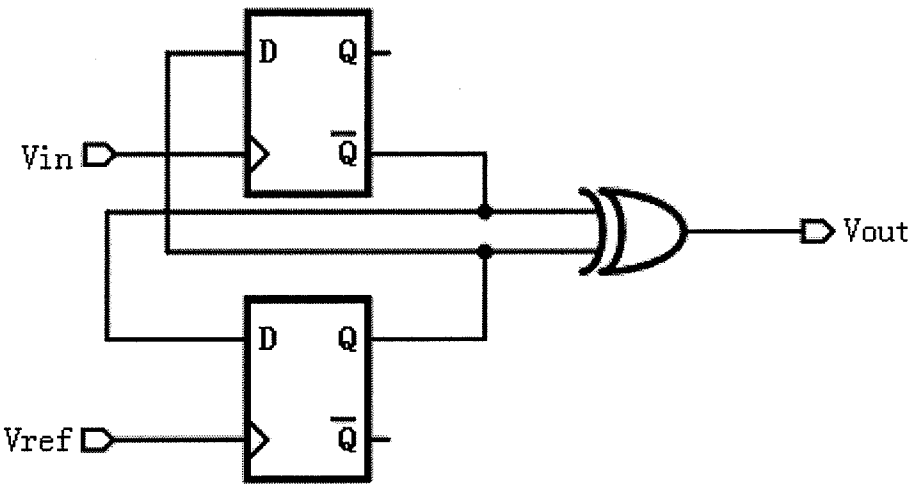


Figure 14: Two-state phase detector schematic

It is composed of two differential D flip-flops and an XOR gate. The phase detector input is connected to the CLK of D flip-flop instead of D and the circuit will settle down after a short time. The phase detector output is the same as the XOR, and the last inverter is just used to generate the complement signal.

The main advantage over an XOR-only phase detector is that it has half the output frequency and gain, thereby reducing the power dissipation in switching charge pumps [3].

3.4.5 Differential D flip-flop

Since differential signals are applied in this filter, the D flip-flop of the phase detector also should support such characteristics. A good example is illustrated in [5] and the schematic is shown in Figure 15.

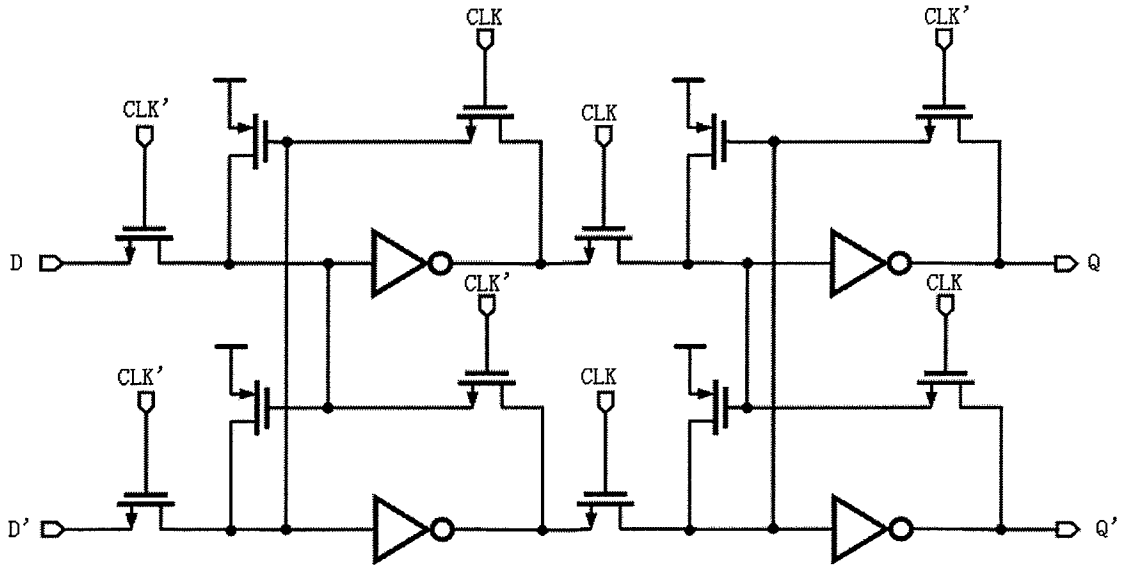


Figure 15: Differential D flip-flop schematic [5]

This kind of differential D flip-flop exhibits less power and moderate delay compared with a sense amplifier flip-flop and static single-transistor clocked flip-flop [5]. It also requires both the

CLK signal and its complement, which is more favorable for this phase detector since the input is connected to the CLK port instead of D. For other applications where exact timing is needed and the complement of CLK is not preferred, this differential D flip-flop might not be favorable.

3.4.6 Symmetric XOR

There are several possible schematics for the XOR gate, as shown in Figure 16, that require only six transistors. However, the problem is that complementary inputs are not available. Also, the delay time for different input patterns will vary largely.

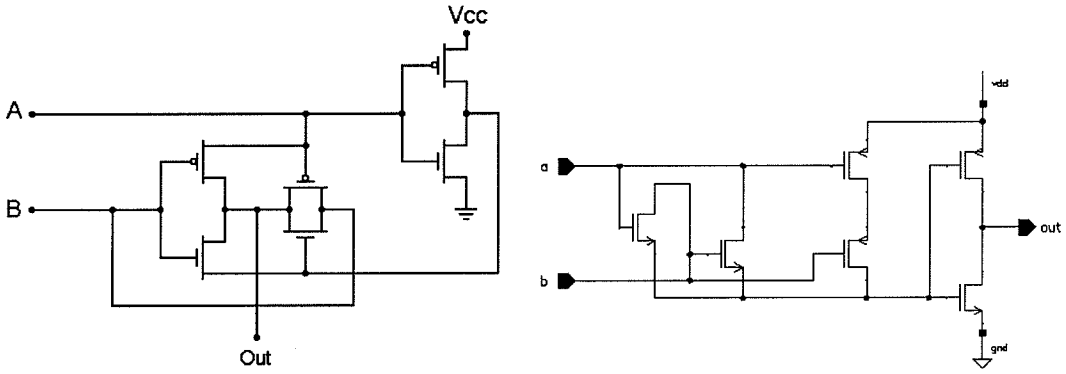


Figure 16: Sample XOR gate schematics with fewer transistors

To remedy these effects, a symmetric XOR is proposed as shown in Figure 17.

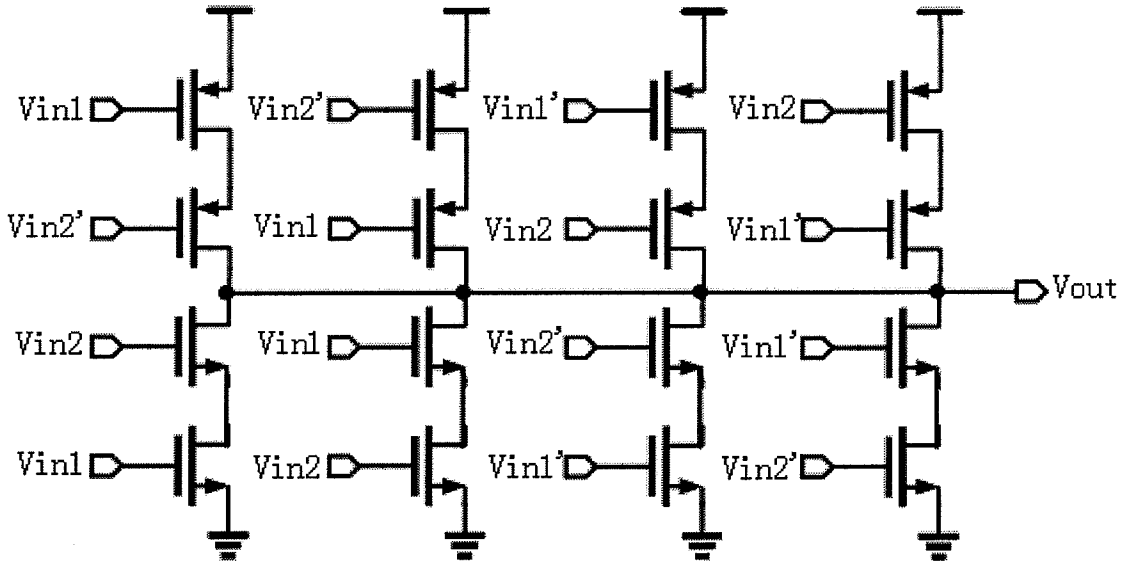


Figure 17: Symmetric XOR gate schematic

It has both two input signals and their complements. In addition, the right side, which is the dual of the left side, ensures that the delay is the same for all input patterns. However, the drawback is also obvious: more transistors are needed.

3.4.7 Charge pump

The charge pump, shown in Figure 18, converts the PWM voltage signal into PWM current.

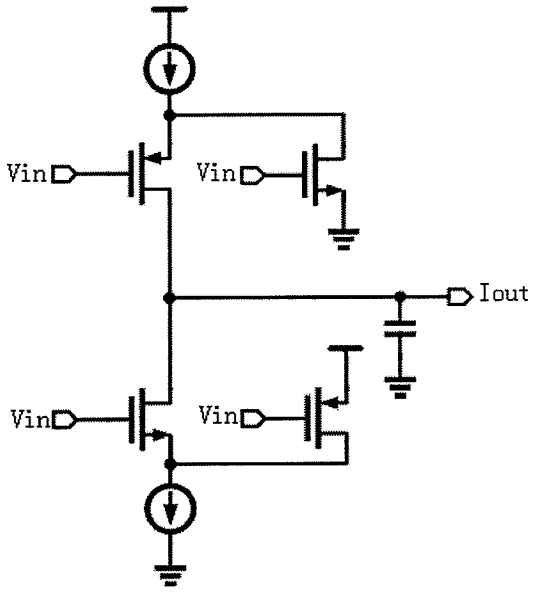


Figure 18: Charge pump schematic

When input is high, the two PMOS are off and the two NMOS are on, which makes the bottom current source connected to the output. This will force more current through the CCO. On the contrary, when input is low, the two PMOS are on and the two NMOS are off, which makes the top current source connected to the output. This will draw the same amount of current from the CCO. The capacitor at the end of the charge pump is to filter out the high frequency noise and glitches.

3.4.8 Output stage

The output stage for each stage is composed of an inverter and a resistor as shown in Figure 19. All phase outputs are connected in parallel. By choosing the same resistor value for each phase, this technique will make sure that the output is the average of all phases.

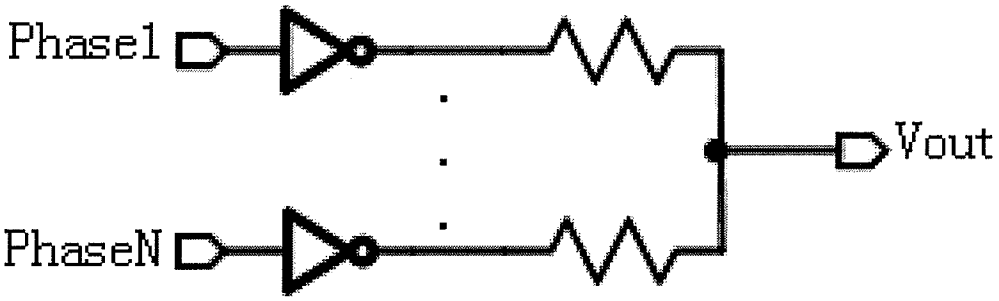


Figure 19: Output stage

3.5 Design Knobs of ROI Filter

In this section, the design knobs are discussed. They include: K_{CCO}, K_{PD}, R_{in}, and some common issues related to these parameters.

3.5.1 K_{CCO}

The oscillator can be either regarded as a voltage controlled oscillator or a current controlled oscillator because its oscillation frequency depends on the biasing voltage/current. Doris [3] provides a rigorous study on how K_{VCO} and K_{CCO} are performed, revealing that K_{VCO} is proportional to the electron/hole mobility and inversely proportional to the number of stages and square of channel length. The expression is shown below:

$$K_{VCO} \propto \frac{\mu}{ML^2}$$

where μ denotes the electron/hole mobility, M denotes the number of stages and L denotes the channel length.

For K_{CCO}, it could be derived from K_{VCO}. The expression is

$$K_{CCO} = \frac{K_{VCO}}{G} \propto \frac{1}{MC_{OX}WL(2V - V_{TH})}$$

$$G = \frac{dI}{dV} \propto \frac{\mu C(2V - V_{TH})}{L^2}$$

where G is the transconductance and C denotes the output capacitance. The expression reveals that the CCO gain is less linear than VCO gain because it does depend on the supply voltage.

The expression of K_{CCO} also shows that it depends on the oscillation frequency. For smaller K_{CCO}, either the number of stages is smaller or the size of each stage is smaller. Both indicate that the oscillation frequency is smaller. Thus, when K_{CCO} is chosen to set up a certain bandwidth, it has to be ensured that the oscillation frequency is much higher than the bandwidth. Otherwise the common-mode signal from the oscillator will appear in the output, which might totally deteriorate the message.

The simulated K_{CCO} at 120MHz oscillation frequency is shown in Figure 20. The top figure shows the oscillation frequency vs input current, and the bottom figure shows the CCO gain by taking the derivative of the top one.

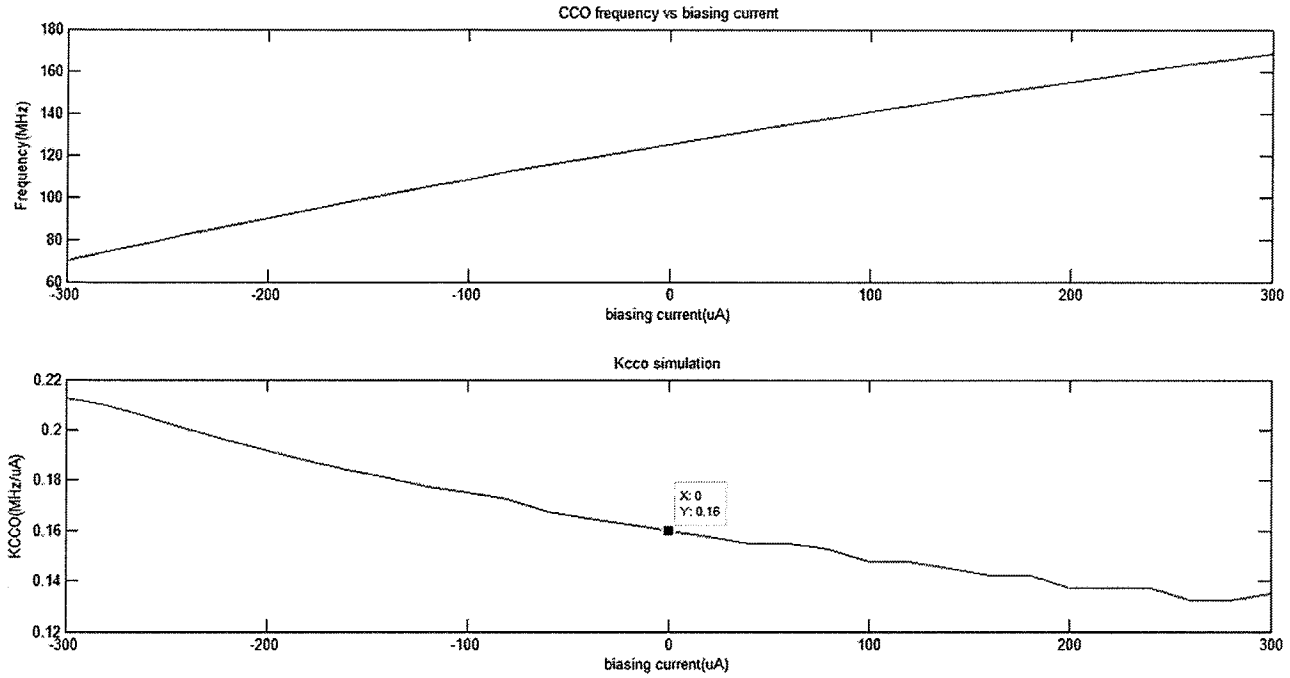


Figure 20: K_{CCO} at 125MHz oscillation frequency

The x-axis is change of biasing current, which ranges from the least to the most possible amount of current that can be drawn from the charge pump. Although K_{CCO} is not a constant throughout the whole range, it is expected that the system will be stabilized to a point where the average total current drawn from the charge pump is small enough such that K_{CCO} will not change. Table 2 summarizes all K_{CCO} that are used in the simulation.

Table 2: K_{CCO} summary

Oscillation frequency	Load capacitance	Biasing current	K_{CCO}
40MHz	1pF	1.6mA	17GHz
105MHz	0.3pF	1.6mA	46GHz
125MHz	0.12pF	0.56mA	160GHz

3.5.2 K_{CP}

The charge pump gain is simply equal to the number of stages times the current provided by each stage. Namely,

$$K_{CP} = M * I_{CP}$$

Since there are multiple phases, the total charge pump current must be far less than the biasing current. Otherwise the large input current will drive the oscillator out of small signal regime.

3.5.3 R_{in}

As explained before, R_{in} is to convert the input voltage into current. R_{in} cannot be too small, which is the same as saying the input voltage cannot be too big. Otherwise if the input current is comparable with the biasing current, the system will be driven into nonlinear regime. On the other hand, if too big, the system gain will be small and it will also introduce a second pole at the input.

3.6 Simulation Result

The result is simulated by applying different voltage sources, running transient analysis (pss analysis does not converge), using FFT to figure out the gain at each input frequency, and connecting them together. Figure 21 shows the procedure in Cadence. The upper two plots are the time domain input and output signal, and the lower two plots are the frequency domain input and output signal. From the right bottom figure, it is clear that the oscillation frequency has been pushed to N times higher (N*120MHz = 1.44GHz).

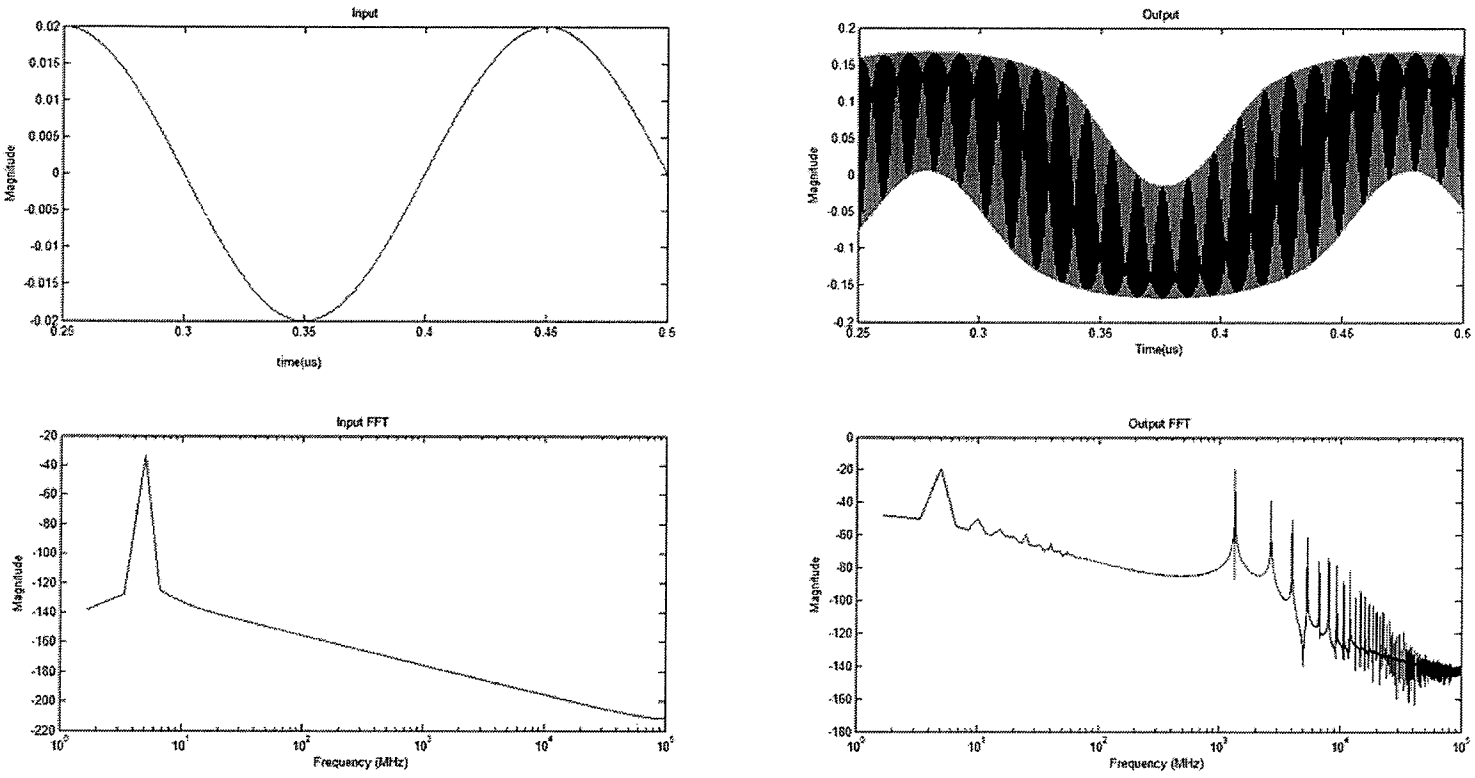


Figure 21: Input/output time/frequency domain analysis

There are some problems with this method. First, it is very hard to know exactly where the 3dB frequency is since only a certain number of input frequencies are used. Also, EWS does not have enough disk space to run transient analysis for a long enough time, which may introduce some uncertainty in FFT. Nevertheless, it gives a rough estimation of the system performance.

The simulated transfer function is shown in Figure 22 and also summarized in Table 3.

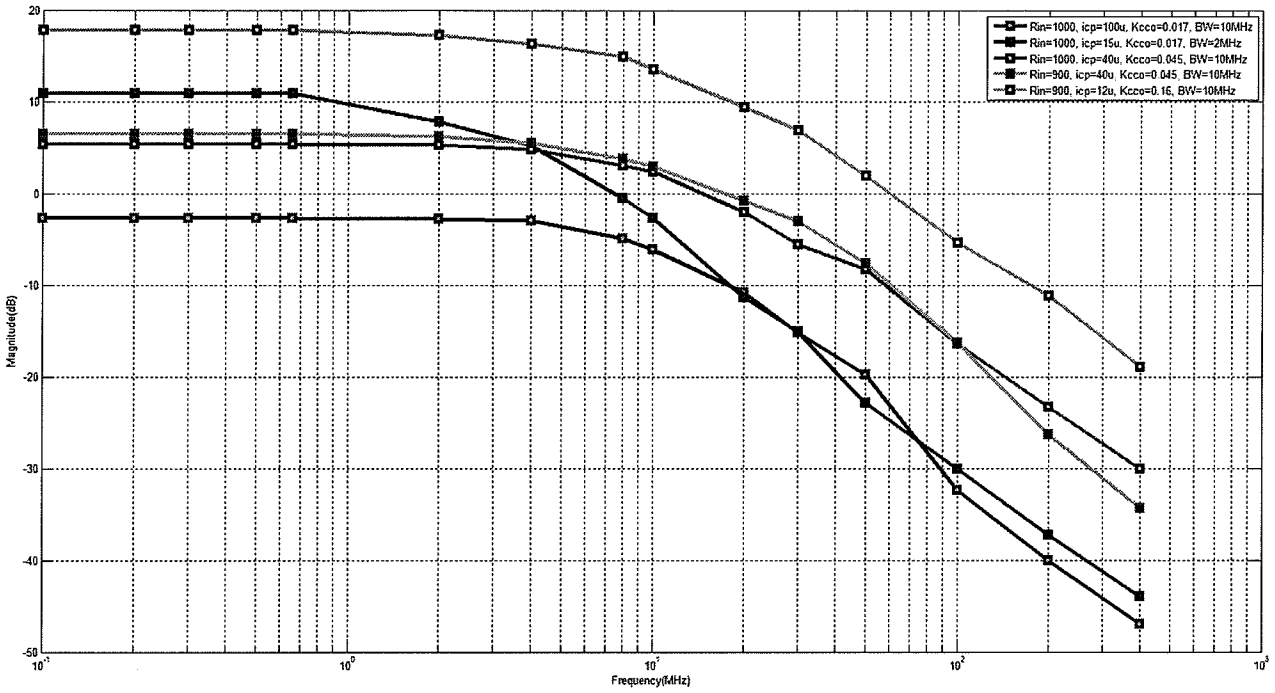


Figure 22: Transfer function simulation results

Table 3: Summary of transfer function simulation results

Rin(kΩ)	icp(μA)	Kcco(GHz)	Bandwidth(MHz)	Gain(dB)
1	100	17	10	-2.6725
1	18	17	2	10.8912
1	40	46	10	5.3891
0.9	40	46	10	6.54
0.9	12	160	10	17.7687

It can be clearly seen that the results and the filter transfer function match very well. For example, comparing with row 1 and row 2 the only difference is the charge pump current, which reduces to nearly 1/5. As a result, the bandwidth of row 2 reduces to 1/5 of that of row 1.

For non-linearity simulation, the Spurious Free Dynamic Range is simulated to be 49.1867dB (mainly limited by the third harmonic tone) and the Total Harmonic Distortion is 0.521% (-45.65dB). The input amplitude is 170mV.

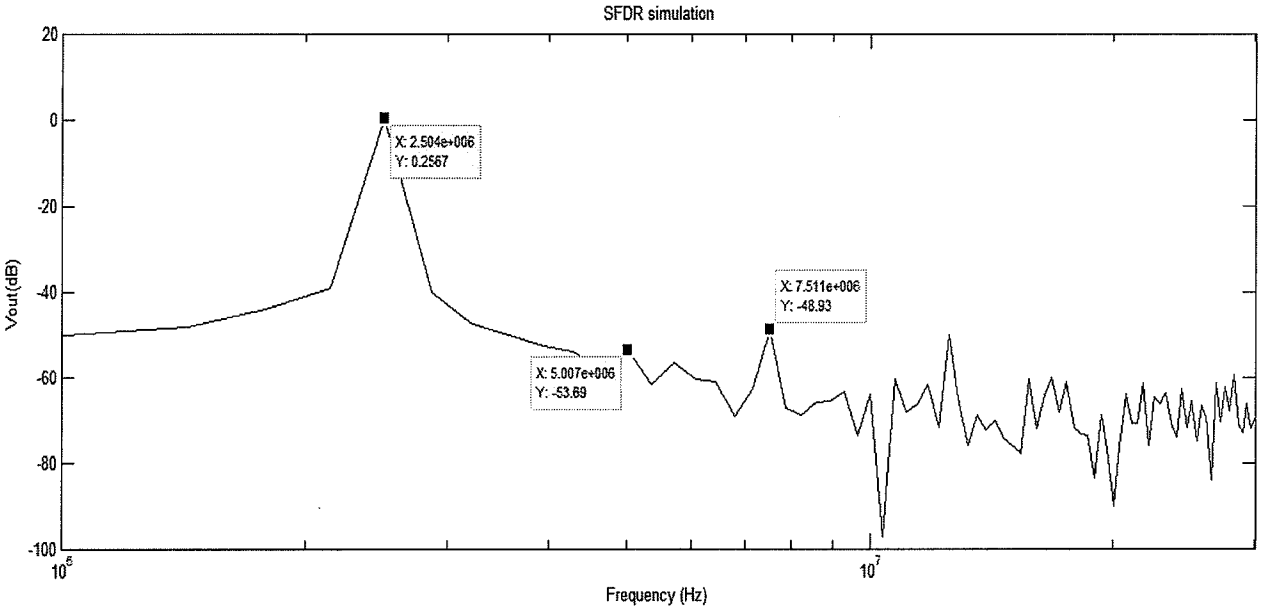


Figure 23: Non-linearity simulation

The measured rms current for the last case in Table 3 is 3.967mA, and therefore the power dissipation is $\mathrm{VDD} * I_{rms} = 1.8 * 3.967m = 7.14mW$.

4 Future Work

4.1 Noise analysis

All the work done previously assumes that the environment is perfect and free of noise. However, in the real world, there are different kinds of noise that could degrade the circuit performance. In this design, the noise comes from all three parts of the integrator: CCO, phase detector, and charge pump. In [2], the input-referred noise is summarized to be

$$S_i = S_{\Phi,\mathrm{CCO}}\left|\frac{s}{K_{CCO}}\right|^2 + S_{PD}\left|\frac{s}{K_{CP}K_{CCO}}\right|^2 + S_{i,CP}\left|\frac{s}{K_{CCO}\ K_{CP}K_{PD}}\right|^2$$

Nevertheless, due to the constraint of EWS itself (insufficient disk quota), the matrix that captures noise, SNR, could not be well simulated.

4.2 Higher order filters

Only first-order filter is achieved in this work. However, this is usually insufficient for analog signal processing. The next step therefore can be building a biquad or even higher order filters by using more than one ring oscillator integrator.

4.3 Biasing

There are many ideal current sources in the circuit (two for CCO, two for each charge pump) that can operate regardless of what voltage appears across it and always exhibit infinite output resistance. However, in the real world, these current sources must be built from current mirror. This indicates that the output impedance is limited and a certain voltage drop is required to maintain normal operation. An advanced biasing technique such as Vt-reference, Widlar current source, and bandgap reference should be applied to minimize possible mismatches.

5 Conclusion

In summary, the filter exhibits reasonable and expected behavior at both system-level and circuit-level. There is still some interesting work that could be done in the future.

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