RING OSCILLATOR INTEGRATOR BASED ANALOG FILTER: SYSTEM LEVEL DESIGN AND MODELING USING VERILOG-AMS

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Abstract

Filters are important building blocks in many analog signal processing systems. Traditional filter implementation involves the applications of two commonly used analog integrators, the Gm-C integrator and the Opamp-RC integrator. The DC gain of the two conventional analog integrators are greatly limited by the gain of operational amplifier (Opamp) used in Opamp-RC integrator or operational transconductance amplifier (OTA) used in Gm-C integrator. Furthermore, process scaling of technology available for integrated circuits is beneficial for smaller area and higher density of integrated circuits yet inevitably reduces the output impedance of the transistors, therefore further exacerbating the performance of Opamp and OTA.

This thesis features applying ring oscillator integrators (ROIs) in the design of analog. ROIs implemented using simple CMOS inverters can achieve infinite DC gain at low supply voltage independent of transistor non-idealities and imperfections such as the finite output impedance. Consequently, ROI based analog filter design scales more effectively into newer technology process. The project starts with an overview of background theory of analog filter design, followed by high order analog filter topologies constructed based on Opamp-RC integrators along with system-level behavioral simulations using MATLAB focusing on second order filters. In the second part, ROI based analog filter design is proposed with system-level analysis. The suggested filter topology is then verified by system-level Verilog-AMS simulation for first order and second order analog filter design. In the third part, we will implement our proposed ROI analog filter at circuit-level using 180 nm TSMC models. We then verify and analyze the performance of ROI analog filter with Cadence Virtuoso. Finally, we conclude our project with summary and evaluation of the research results and suggestions of possible future research and improvements of our project.

Subject Keywords:

Analog filters; analog signal processing; continuous time filters; integrator; ring oscillator; ring oscillator integrator.
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Contents

1. INTRODUCTION ................................................................................................................................. 1
   1.1 Passive Low Pass Filter Design ..................................................................................................... 2
       1.1.1 Passive First Order Low Pass Filter ....................................................................................... 2
       1.1.2 Passive Second Order Low Pass Filter .................................................................................. 3
   1.2 Active Second Order Low Pass Filter ............................................................................................ 5
       1.2.1 Sallen-Key Biquad ..................................................................................................................... 6
       1.2.2 Tow-Thomas Biquad .................................................................................................................. 7
   1.3 Project Motivation ............................................................................................................................ 8

2. LITERATURE REVIEW .......................................................................................................................... 10

3. ROI BASED LOW PASS FILTER: THEORETICAL BASIS ................................................................. 12
   3.1 Ring Oscillators as Integrators ....................................................................................................... 12
   3.2 Ring Oscillator Integrator Based Low Pass Filter ......................................................................... 14
       3.2.1 First Order Low Pass Filter Using Ring Oscillator Integrator ............................................... 15
       3.2.2 Tow-Thomas Biquadratic Low Pass Filter Using Ring Oscillator Integrator ......................... 16
   3.3 Voltage Controlled Oscillator Modeling and Simulation Results .................................................. 16
   3.4 Phase Detector Modeling and Simulation Results ......................................................................... 18
   3.5 Charge Pump Modeling and Simulation Results ............................................................................ 21

4. ROI BASED LOW PASS FILTER: VERILOG-AMS SIMULATION .................................................... 23
   4.1 Tow-Thomas Biquadratic Low Pass Filter Design ......................................................................... 23
   4.2 Ring Oscillator Integrator Based Low Pass Filter ......................................................................... 24

REFERENCES ........................................................................................................................................... 32

APPENDIX A: FAST FOURIER TRANSFORM FOR PWM DEMODULATION ............................................ 33

APPENDIX B: VERILOG-AMS CODES ..................................................................................................... 35
1. INTRODUCTION

This thesis presents the design and simulation of a ring oscillator integrator based analog low-pass filter. Simple analog filters could be implemented using passive elements of resistors, inductors, and capacitors only, but such implementation of filters are usually not favored as they suffer severely from loading effect. In other words, the behavior of the filters are not consistent as specified for different connections of load. Matching networks are usually required, but they only serve well for a limited range of frequencies. Besides, the bulky volume of passive elements filters are not suitable for integrated circuit design. At integrate circuit level, analog filter designs involve the usage of analog integrators. Analog integrators are key building blocks in signal processing with two most commonly used integrators, the Gm-C integrator and the Opamp-RC integrator. The performance of these two types of the integrators are closely dependent on the operational transconductance amplifiers (OTAs) contained in the circuit, and the OTAs result into performance degradation on the filters due to the non-idealities of transistors in integrated circuit design. In view of the drawbacks of OTA-based integrators, we propose to use CMOS inverter-based ring oscillators to implement integrators (ROIs) with infinite DC gain independent of transistor dimensions and supply voltage. The “digital” natures of the ROIs allow them to operate with low supply voltages and scale better with process than conventional OTA-based designs. The viability of the ROIs will be first analyzed and verified from both system- and circuit-level simulations throughout this project.

As for the contents of the thesis, we focus on the design and implementation of low pass filter. Chapter 1 of this thesis first presents background information about analog filter designs using passive elements for first and second order design Section 1.1, and Opamp-RC integrators based second order filter designs in Section 1.2. Chapter 2 documents the literature review that we have done following Professor Hanumolu’s instruction. Next, Chapter 3 starts by a background theory introduction about the ring oscillator as integrator. The modeling and simulation results using Verilog-AMS of each individual block, mainly voltage controlled oscillator, phase detector, and charge pump, are also described in this Chapter. Then Chapter 4 covers examples of conventional LPF design with tables summarizing the component values necessary to achieve the requirements. Observation from the conventional LPF design would illustrate the motivation for this thesis, and I will begin the discussion about the Verilog-AMS design and simulation of our proposed ROI-based filter. Transistor-level design would be documented in Danyang Wang’s thesis and the discussions about circuit-level design is referenced to his document. Finally, Chapter 5 concludes my thesis project work and elaborates on potential future improvements and research ideas of our
project. In Appendix A, a brief discussion of spectral analysis using FFT is given, and simulation models and MATLAB codes are attached to serve as reference in Appendix B.

1.1 Passive Low Pass Filter Design

I will start our discussion about analog filter design with a brief overview about the design of passive low pass filter (LPF). Each subsection in the following part of this chapter would cite one example of the corresponding circuit to illustrate the design specifics for each type of LPF [1].

1.1.1 Passive First Order Low Pass Filter

The simplest way to design a LPF is to use a resistor and a capacitor, as shown in Figure 1.1.

![Passive First Order Low Pass Filter](image)

Figure 1.1: Passive First Order Low Pass Filter

The LPF behavior could be read from the transfer function of this network. The transfer function of this system is easily derived to be the following:

\[ H_{LPF1}(s) = \frac{1}{1 + sRC} \]  \hspace{1cm} (1.1)

where R and C denote the resistance and capacitance respectively. From the obtained expression, we notice that the gain of system, \( |H_{LPF1}(s)| = \frac{|V_{out}(s)|}{|V_{in}(s)|} \rightarrow 0 \), gets greatly attenuated as \( s = j\omega \rightarrow \infty \), which is characterized as a low pass filter. The -3 dB bandwidth of the filter is equal to:

\[ \omega_{-3\,dB} = \frac{1}{RC} \]  \hspace{1cm} (1.2)

The filter bandwidth is set by the choice of resistor and capacitor. It is worth notice here that such passive filter circuits suffer from the load connected at the output node, as we only consider the existence of the capacitor when analyzing the voltage divider expression. Depending on the loading, the filter network would have the load impedance connected in parallel with the capacitor so that the filter shows different transfer functions and functions with varying bandwidth. The varying transfer function would negatively
influence the system’s functioning if the filter’s bandwidth fails to satisfy the system’s requirement. The susceptibility to loading effect poses a huge disadvantage on the utility of such passive networks.

1.1.2 Passive Second Order Low Pass Filter

Another disadvantage of first order LPF is that designers only have the control over the bandwidth of the filters. In most cases, filter designs also come with requirement for specific attenuation rate of the filter’s transition from pass band towards stop band. The second degree of freedom is introduced once designers have access to second order LPF, or biquadratic LPF (referred as “biquad” for the rest of the thesis), and the schematics of two common topologies are shown in Figure 1.2.

![Figure 1.2: Passive Second Order Low Pass Filter](image)

The two topologies show the following transfer characteristics respectively:

\[ H_{LPF2,a}(s) = \frac{1}{s^2 + \frac{R}{L} s + \frac{1}{LC}} \]  \hspace{1cm} (1.3)

\[ H_{LPF2,b}(s) = \frac{1}{s^2 + \frac{1}{RC} s + \frac{1}{LC}} \]  \hspace{1cm} (1.4)

Readers can verify that as \( s = j\omega \to \infty \), \(|H_{LPF2}(s)| \to 0\). Slightly different transfer functions represent the same behavior, so people observe that the transfer functions of second order LPF could be generalized as:

\[ H_{LPF2}(s) = \frac{\omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \]  \hspace{1cm} (1.5)
where \( Q \) denotes the quality factor of the filter and \( \omega_0 \) denotes the -3 dB bandwidth. In this case, for the two topologies proposed, we have:

\[
Q_a = \frac{1}{R} \sqrt{\frac{L}{C}} \\
Q_a = R \sqrt{\frac{C}{L}} \\
\omega_{0,a} = \omega_{0,b} = \frac{1}{\sqrt{LC}}
\]

(1.6) (1.7) (1.8)

The quality factor is defined to describe the performance of the filter. Higher Q comes along with sharper peaking in the frequency response of the LPF. Yet, peaking is not a factor that seems to suit the purpose of the LPF as we are more familiar with a flat pass band response. Therefore, a more general definition of the Q factor is proposed to describe the importance of the peaking for LPF:

\[
Q = 2\pi \times \frac{\text{Energy Stored}}{\text{Energy Dissipated Per Cycle}} = 2\pi f_0 \times \frac{\text{Energy Stored}}{\text{Power Loss}} = \frac{1}{2\zeta}
\]

(1.9)

where \( \zeta \) is the damping ratio. Q factor is characterize to be the ratio of energy stored to energy dissipated per cycle in the system, thus higher Q indicates lower rate of energy loss and the peaking becomes an important tradeoff with the flatness of the pass band in the process of LPF design. Following this definition, the two poles of the second LPF from Equation (1.5) could therefore express as

\[
s = -\omega_0 \zeta \pm \omega_0 \sqrt{\zeta^2 - 1}
\]

(1.10)

At last, the peaking effect occurs in the frequency response of the LPF is summarized in Figure 1.3 to show how the peaking effect affects the shape of the filter’s frequency response.
1.2 Active Second Order Low Pass Filter

Active LPF design introduces OTA integrator based analog filter. Conventional integrators are Gm-C and Opamp-RC integrator, of which the schematics are depicted in Figure 1.4:

![Conventional Integrators: (a) Gm-C Integrator and (b) Opamp-RC Integrator](image)

The transfer function of the integrator is equal to:

\[ H_{Gm-C}(s) = \frac{G_m}{sC} \]  
\[ H_{Opamp-RC}(s) = -\frac{1/(RC)}{s} \]  

Gm-C integrator functions with low noise, high bandwidth but poor linearity, which Opamp-RC integrator provides the contrary features of higher noise, lower bandwidth but better linearity. One common thing about these two topologies is that both require operational transconductance amplifiers (OTAs). The advantage of active filter design over the passive element design lies in the great minimization of the loading effect that influences the passive element filter’s performance. High DC gain is achievable for the OTA, but consequently more power is drawn in the system and bandwidth is rather limited. In the
following Section 1.2.1 and 1.2.2, two commonly used topologies, Sallen-Key and Tow-Thomas biquadratic filters, will be discussed to further illustrate the design process of active second order LPF design. Notice that the derivation of the design equations all assume that the operational amplifier used has infinite gain at DC.

1.2.1 Sallen-Key Biquad

The Sallen-Key Biquad LPF is commonly used to implement a second order active LPF at the advantage of its simplicity of the topology. The schematic of the Sallen-Key LPF is depicted in Figure 1.5:

The transfer function of this LPF can be derived to be:

\[
H_{Sallen-Key}(s) = \frac{A}{s^2 + \left( \frac{1}{R_1C_1} + \frac{1}{R_2C_2} \right) + \frac{1 - A}{R_2C_2} s + \frac{1}{R_1R_2C_1C_2}}
\]

\[A = 1 + \frac{R_3}{R_4}\]

These expressions are quite complicated, but we are able to work with a simplified version of Sallen-Key topology with \(A = 1\), and the revised schematic is depicted in Figure 1.6:
With the simplified topology, the design equations are more easily defined in the form of Equation (1.5) with parameter expressions as follows:

\[
\omega_0 = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \quad (1.14)
\]
\[
Q = \frac{\sqrt{R_1 R_2 C_1 C_2}}{C_2 (R_1 + R_2)} \quad (1.15)
\]

The resistor and capacitor values would be selected appropriately following design Equations (1.13) and (1.14) so that the frequency response of the LPF satisfies the specifications.

### 1.2.2 Tow-Thomas Biquad

Another important active LPF topology is the Tow-Thomas biquad filter. The topology schematic is shown in Figure 1.7:

![Tow-Thomas Low Pass Filter](image)

**Figure 1.7: Tow-Thomas Low Pass Filter**

The design equations, including the transfer function, -3 dB cut-off frequency, and the quality factor, are derived to be the following:

\[
H_{Tow-Thomas}(s) = \frac{H_{DC}\omega_0^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2} \quad (1.16)
\]
\[
\omega_0 = \frac{1}{\sqrt{R_2 R_4 C_1 C_2}} \quad (1.17)
\]
\[
Q = \frac{R_1}{\sqrt{R_2 R_4} \sqrt{C_1 C_2}} \quad (1.18)
\]
\[
H_{DC} = \frac{R_2}{R_3} \quad (1.19)
\]
Following the listed design equations, designers could choose the elements values appropriately to achieve the required filter specifications.

1.3 Project Motivation

From the discussion above, advantages of active biquadratic filters are obvious in terms of the designer’s control over both the cut-off frequency and the quality factor in order to produce desired frequency response. With access to high DC gain Opamp, designers are able to implement the filters with much more resistivity to the loading effect. Common gain improvement techniques includes cascaded OTA and multi-stage OTA, as described in Figure 1.8:

![Cascoded OTA and Multi-Stage OTA](image)

Figure 1.8: Increasing OTA Gain (a) Cascoded OTA and (b) Multi-Stage OTA

Cascoded OTAs give designer low noise and power, but the headroom of the circuit is very limited. On the contrary, multi-stage OTAs provide reasonable headroom at the cost of higher noise and power consumption compared to cascaded topology. Also, the design of multi-stage OTAs require complex compensation methods, which may also lead to reduced bandwidth.

However, a more important issue that troubles the circuit designers is the technology process scaling, which has negative influence on designer’s access to such high gain topologies. The decrease of process nodes greatly reduce the output impedance of the transistor as well as the voltage swing that is available to the designers. A plot for the trend of supply voltage versus process node is shown in Figure 1.8:
As shown in the figure, the decreasing supply voltage greatly affects the swing of the circuit, therefore techniques used for improving integrator gain have very limited applications. As a result, the DC gain is greatly compromised, naturally leading to a degradation in the performance of conventional integrators which rely heavily on OTAs. This situation motivates this thesis project to discover the possibility of using ring oscillator to function as an analog integrator. In the following part of the thesis, Chapter 2 focuses on the discussion about ring oscillator integrator and Chapter 3 starts discussion about the implementation of LPF with ROI as the key component.
2. LITERATURE REVIEW

Integrators are functioning block of great importance in a number of analog signal processing circuits. In this thesis, we focus on the application of integrators in implementing analog filters. In order to prepare for project, we first start with learning about system-level knowledge about analog filter design. To accomplish this study, we have consulted the textbook *Analog Filter Design* by Mac Elwyn Van Valkenburg. For the first three chapters, *Analog Filter Design* [1] covers the basic theory behind and gives a thorough explanation about this subject including bilinear transformation and the realization using passive elements, interpretation of zeros, poles, and Bode plots, and first and second order passive filters and analog filters in system level. This textbook also contains numerous design examples which start with hand calculations for the filter parameters based on the derived expressions and implements the filter using CAD simulation tools to better illustrate the design process. While following the instruction documented in the textbook, we also managed to apply the equations to design LPF with cut-off frequency of 100 Hz and 100 kHz respectively and to run MATLAB simulation to verify the behavior of our designs. We benefited from reading these chapters and prepared ourselves with enough background knowledge to continue the thesis project with ROI integrator based analog filter design.

In the next step, our focus was switched to learn about ring oscillator basics, which we studied most from the Master thesis *Time-Based Analog Signal Processing* [2] by Brian G. Drost from Oregon State University. Ring oscillators have been an important research topic in the world of analog integrated circuit (analog IC) design. Especially, voltage- or current-controlled ring oscillator (VCO or CCO) has been used extensively in phase-locked loops (PLLs) to perform frequency modulation, and then this clock signal is demodulated by the phase detector (PD) once it is compared with the input clock signal. This application characterizes the conventional use of ring oscillator. Other applications of VCOs in recent researches have been using VCOs as quantizers and pulse-width modulator (PWM). As mentioned in B. Drost’s thesis, such applications use VCOs to perform an operation on an analog signal. Since in all the applications, VCOs can be modeled as a voltage to phase integrator, B. Drost conducted his research to investigate using ring oscillators as an analog integrator. He, Mrunmay Talegaonkar, and Professor Hanumolu have proposed prototype filter design in *Analog Filter Design Using Ring Oscillator Integrators* [3] while they work with Professor Hanumolu. This thesis project is the application of the idea to implement a ROI based analog low pass filter of low bandwidth of 100 kHz. And paper by B. Drost, M. Talegaonkar, and P. K. Hanumolu is our reference for most of part of the project as it guides us through the theory and how to set up the models and simulations. In the meanwhile, we also consulted a reference book discussing about spectral
analysis using Fast Fourier Transform (FFT) to better understand how to demodulate PWM signals so that input sinusoidal wave could be recovered and observed in the frequency domain. This reference book, *Understanding Delta-Sigma Data Converters*, provides detailed discussion in the appendix about spectral estimation using FFT [4], and this method is used to perform frequency domain analysis of the output PWM signals of the ROI based filter. In order to perform the analysis, we have exported the output waveforms of the analog filter from Verilog-AMS simulation via Cadence Virtuoso. These generated data files are read as the input to the MATLAB code which essentially runs pulse width modulated signals demodulation and plots the output in frequency domain. The output is observed at the specified frequency consistent of the input signal, and the magnitude of the spectral peak is documented. With multiple simulation tests, we are able to extract the frequency response of the system, which will be recognized as LPF.

Through Chapter 2 and 3 of the thesis project, the performance of ROI based filter is examined from both system-level and transistor-level perspectives. A goal of the project is establishing the advantages of the ROIs, which are particularly suitable for filter designs in integrated circuit level with current technology process.
3. ROI BASED LOW PASS FILTER: THEORETICAL BASIS

The theoretical basis for ROI is presented at the beginning of the chapter followed by an overview of the system-level block diagrams is given to discuss about how the low pass behavior is realized using ROI [3]. Section 3.1 features the analysis of a first order LPF filter and a Tow-Thomas biquad implementations. To implement the ROI based analog filter, each component required in the system has to be properly modeled and tested. Specifically, voltage-controlled oscillator, phase detector, and charge pump are modeled in Verilog-AMS [5] and tested, and the results will be documented in the following three sections, Section 3.3, 3.4, and 3.5, respectively.

3.1 Ring Oscillators as Integrators

Consider a simple inverter-based three-stage ring oscillator shown in Figure 3.1 (a). The magnitude response of input voltage to phase output transfer function is plotted in Figure 3.1 (b).

From Figure 3.1, we can see that input voltage, $V_{IN}$, controls the oscillator frequency, $\omega_{out}$, such that:

$$\frac{d\omega_{out}}{dv_{in}} = K_{VCO}$$  \hspace{1cm} (3.1)

where $K_{VCO}$ is referred to as the oscillator gain. Since $\omega_{out}$ indicates the output frequency of the ring oscillator, and phase is the integral of frequency, the oscillator can be viewed as an integrator with the following transfer function:
Equation (3.2) reveals that ROI has infinite DC gain as \( \frac{\phi_{out}(s)}{v_{in}(s)} \to \infty \) as \( s = j\omega \to 0 \). And this expression also indicates that infinite DC gain is obtained independent of transistor dimensions and supply voltage. Given with the above reasoning, ring oscillator acts as an integrator in phase domain. Therefore, a phase-to-voltage/current converter is needed in order to connect ROI with other building blocks which usually take voltage or current as input signals. In this case, a phase detector (PD) is used, as illustrated in Figure 3.2, in order to convert VCO output phase to a PWM signal.

PD operates only on rising edges of the VCO and reference signal. If the two input phase signals are \( \pi \) radians out of phase, the PWM output signal \( D_{OUT} \) has 50% duty cycle. Different phase errors correspond to varying duty cycle ratio of the output. Since the phase difference could only vary from 0 to \( 2\pi \) radians, input signals have to be checked carefully so that the phase difference would not exceed the limit.

Finally, charge pump is added to accomplish a current input and current output ring oscillator based integrator. Notice that VCO now is replaced with CCO as the input control signal is current. The schematic is shown in Figure 3.3.
Charge pump (CP) serves to convert the PD output to PWM current, and the gain of CP is characterized to be

\[ K_{CP} = I_{CP} \]  

(3.3)

where \( I_{CP} \) is the CP bias current. Now, at frequency domain the oscillator is described by the block diagrams as follows in Figure 3.4.

The transfer function of the ROI can be directly read from the block diagram and is equal to:

\[ H_{ROI}(s) = \frac{K_{CCO}K_{PD}K_{CP}}{s} \]  

(3.4)

### 3.2 Ring Oscillator Integrator Based Low Pass Filter

With the discussion on the ROI in Section 3.1, starting in Section 3.2 the discussion will target on the application of ROI in low pass filter design. In particular, topology of both first order and second order LPF will be given in this subsection and the transfer functions are also derived and compared with the general
form shown in Chapter 1. For the second order LPF, this topology is given to show a transfer function corresponding to that of the Tow-Thomas biquadratic LPF.

3.2.1 First Order Low Pass Filter Using Ring Oscillator Integrator

Designing LPF follows the same method as documented in Chapter 1. The only difference here is that the pole existing in the transfer function is no longer produced by either RC or Opamp-RC. Instead, the pole now is introduced with the placement of ROI in the system. The system-level architecture of the proposed first order LPF is shown in Figure 3.5.

![Figure 3.5: Voltage-Based First Order ROI Based LPF](image)

The input voltage, $V_{IN}$, is converted to current input with the resistance $R_{IN}$. The charge pump CP is used to convert the PWM output of the phase detector into PWM current output, which is then running through the resistor $R$, and the output voltage $V_{OUT}$ will be measured. The feedback is accomplished by another charge pump CPFB. Following this system-level block diagram, it is possible to derive that the transfer function of the first order LPF is given by:

$$H_{ROI\text{LPF}_1}(s) = \frac{1}{R_{IN}K_{CPFB}} \frac{1}{1 + \frac{s}{K_{CCO}K_{PD}K_{CPFB}}} \tag{3.5}$$

where $K_{CCO}$, $K_{PD}$, and $K_{CPFB}$ denote the gain of the CCO, PD, and feedback CP respectively. The -3 dB frequency of this LPF is equal to:

$$\omega_{-3\,\text{dB}} = K_{CCO}K_{PD}K_{CPFB} \tag{3.6}$$

From the expression of the -3 dB frequency, ROI based first order LPF also gives another vantage other than the independence of transistor dimensions that designer is able to tune the filter bandwidth conveniently by adjusting the feedback charge pump current. Because the charge pump non-linearity is independent of its current, tuning does not degrade distortion performance of the filter [3]. This will greatly benefit when it comes to the circuit level implementation using MOSFETs. Also, the gain of the
filter is also possible to adjust with a proper selection of input resistance and feedback charge pump current.

3.2.2 Tow-Thomas Biquadratic Low Pass Filter Using Ring Oscillator Integrator

The implementation of Tow-Thomas biquad is following the same method as shown in the case for first order LPF. The system-level schematic is shown in Figure 3.6.

![Figure 3.6: ROI Based Tow-Thomas Low Pass Filter](image)

Given that $K_{CCO1}$, $K_{PD1}$, $K_{CP1}$, $K_{CCO2}$, $K_{PD2}$, and $K_{CPFB2}$ denote the gain of CCO$_1$, PD$_1$, CP$_1$, CCO$_2$, PD$_2$, and CPFB$_2$, the transfer function of the ROI based Tow-Thomas LPF is derived as follows:

$$H_{ROI\text{LPF}_2}(s) = \frac{1}{R_{IN}K_{CPFB1}} \left( \frac{s^2}{K_{CCO1}K_{CCO2}K_{PD1}K_{PD2}K_{CP1}K_{CPFB1}} + \frac{K_{CPFB2}}{K_{CCO1}K_{PD1}K_{CP1}K_{CPFB1}} + 1 \right)$$ (3.7)

The -3 dB bandwidth of the filter could be extracted when comparing Equation (3.7) with Equation (1.5).

Notice that in the design of Tow-Thomas LPF, the designer now has more degrees of freedom in terms of how to achieve the requirements for the LPF. The coefficients of the filter could be realized by appropriately selecting the charge pump currents.

3.3 Voltage Controlled Oscillator Modeling and Simulation Results

VCO modeling in Verilog-AMS is a behavioral description of the VCO circuit. In order to model the VCO, the following parameters are provided by the design to ensure a proper function of the VCO model:

- Definition of the input and output signal. In this case, both input and output would be voltage signals, and they are easily access using Verilog-AMS function.
- Amplitude and DC offset of the output are specified. For example, since we are expecting an output of sinusoidal wave, we could specify the amplitude $V_{\text{ampl}} = 900 \text{ mV}$ and the DC offset of the voltage $V_{\text{offset}} = 900 \text{ mV}$ so that the output signal of the VCO will be a sine wave with magnitude changing from 0 to 1.8 V at the desired frequency. The unit of these two parameters are given in Volt [V].
• Center frequency $f_{\text{center}}$ of the VCO is specified. This frequency represents the oscillator’s output signal frequency when the input is 0 V. The unit of $f_{\text{center}}$ is given in Hertz [Hz].

• $K_{VCO}$ is specified directly. This is one important design parameter as we have seen from the design equations (3.5) and (3.7). The unit of the gain of VCO is given in Hertz/Volt [Hz/V].

Provided with all the above parameters, the VCO model first calculate the frequency of the output voltage as:

$$f_{VCO} = f_{\text{center}} + K_{VCO} \times V_{in} \quad (3.8)$$

Then, the phase is calculated as the integral of the frequency. A special function provided by Verilog-AMS is applied which calculates the modular integral of the frequency so that the phase ranges from $-\pi$ to $+\pi$ radians. Finally, the output is generated:

$$V_{out}(t) = V_{\text{ampl}} \sin(2\pi f_{VCO}) + V_{\text{offset}} \quad (3.9)$$

The block diagram in Figure 3.8 further illustrates the VCO modeling:

![Figure 3.7: Verilog-AMS VCO Modeling](image)

The test bench circuit constructed in Cadence Virtuoso is shown in Figure 3.8. The VCO symbol is generated from the Verilog-AMS simulator.

![Figure 3.8: Voltage Controlled Oscillator Test Schematic](image)
As shown in Figure 3.8, a piece-wise linear voltage source is selected to be the input, and the measured output of the oscillator would show corresponding frequency change in Figure 3.9:

3.4 Phase Detector Modeling and Simulation Results

Phase detector is more straightforward comparing to VCO modeling. Since the Verilog-AMS simulator is able to run mixed signal simulation, the phase detector is implemented using two D flip-flops (DFF) and an XOR/XNOR gate. The PD model is implemented by first implementing DFF and XOR/XNOR models and then connecting these sub-level blocks as they are wired in the schematic, which is shown in Figure 3.10.
The outputs of the XOR/XNOR gate are the PWM signals generated by the PD. INC represents “increment” which indicates that the frequency of the oscillator is increased over the reference frequency, while DEC represents “decrement” which indicates that the frequency of the oscillator is decreased below the reference frequency.

The test bench circuit constructed in Cadence Virtuoso is shown below in Figure 3.11, where two voltage sources have been selected to be input phase and reference phase respectively.

In the implementation of the PD block, a threshold parameter is included so that the PD would detect the rising edges of the signal based on the comparison of the input voltage level with the threshold point. Verilog-AMS detects in which direction the input voltage level approaches the threshold value through “cross” function with “+1” indicating rising edge and “-1” indicating falling edge. “0” associated with cross function would detect both edges, but this is not useful in my implementation as rising edge detection is required. The threshold value makes it possible to detect the phase difference between two different types of input signal, such as the square wave reference signal and sinusoidal wave oscillator output signal.
This phase difference detection is illustrated in Figure 3.12, where (a) represents the case when two square waves are input and (b) represents two inputs of triangular wave and square wave.

Figure 3.12: Phase Detector: (a) Two Square Wave Inputs and (b) Triangular Wave and Square Wave Inputs
3.5 Charge Pump Modeling and Simulation Results

As explained in Section 3.1, charge pump is used to convert the PWM voltage into a PWM current signal. As a result, the CP is modeled so that it has differential outputs with each output corresponding to the input signals coming from PD outputs. Specifically, CP_{OUT} follows the INC from PD while CP_{NOUT} follows the DEC from PD. The test bench circuit constructed in Cadence Virtuoso is presented in Figure 3.13 for reference.

![Figure 3.13: Charge Pump Test Schematic](image)

The simulation results in Figure 3.14 show both the PD outputs and CP outputs in order to justify the proper conversion accomplished by using CP.

![Figure 3.14: Charge Pump](image)
Now the inputs are changed to be the output from PD. The resulting schematic and simulation results are included to verify the performance of the CP model used in this thesis project:

![Figure 3.15: Phase Detector with Charge Pump: (a) Test Schematic and (b) Simulation Result](image)

Again, threshold value $V_{TH}$ is set for the charge pump. The CP output follows INC input and takes an output with magnitude equal to the bias current $I_{BIAS}$ when only INC $> V_{TH}$ and DEC $< V_{TH}$, and CP output follows DEC input with magnitude equal to $-I_{BIAS}$ when only INC $< V_{TH}$ and DEC $> V_{TH}$. Otherwise, charge pump outputs would remain zero. Thus, as shown in Figure 3.15 (b), the last waveform strip indicates the charge pump output takes the output range from -1 mA to 1 mA with $I_{BIAS} = 1$ mA.
4. ROI BASED LOW PASS FILTER: VERILOG-AMS SIMULATION

In this chapter, simulation results are summarized for both conventional Opamp-RC integrator based and ring oscillator integrator based low pass filter. At the beginning, tables will document element values of resistors and capacitors used in Opamp-RC integrator based biquadratic LPF design. Frequency response of the corresponding filters are also simulated using MATLAB. Next, simulation results of ROI based LPF design are documented including first order and second order designs. Two design methodologies and results are compared to better illustrate the advantages and motivation for using ROI as discussed in Chapter 3.

4.1 Tow-Thomas Biquadratic Low Pass Filter Design

The OTA-integrator based LPF design features Tow-Thomas biquadratic filter. Other topologies would follow the corresponding design equations and the same method applies, therefore the discussion on conventional LPF design takes Tow-Thomas biquad as an example. The resulting frequency responses are plotted in Figure 4.1 with the gain of the filter designed to be 1 at DC.

![Figure 4.1: OTA Integrator Based Tow-Thomas Low Pass Filter](image)

Since the conventional LPF design is not the focus of this thesis, details on how to use the design equations are not presented here but calculated parameters with target bandwidth are summarized in Table 4.1:
Table 4.1: 100 kHz -3 dB Bandwidth Tow-Thomas Biquadratic Low Pass Filter

<table>
<thead>
<tr>
<th>Q</th>
<th>R₁ (kΩ)</th>
<th>R₂ (kΩ)</th>
<th>R₃ (kΩ)</th>
<th>R₄ (kΩ)</th>
<th>R₅ (kΩ)</th>
<th>C₁ (pF)</th>
<th>C₂ (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.707</td>
<td>11.24</td>
<td>15.90</td>
<td>15.90</td>
<td>15.90</td>
<td>15.90</td>
<td>10.0</td>
<td>10.0</td>
</tr>
<tr>
<td>0.867</td>
<td>13.80</td>
<td>15.90</td>
<td>15.90</td>
<td>15.90</td>
<td>15.90</td>
<td>10.0</td>
<td>10.0</td>
</tr>
<tr>
<td>2.50</td>
<td>39.75</td>
<td>15.90</td>
<td>15.90</td>
<td>15.90</td>
<td>15.90</td>
<td>10.0</td>
<td>10.0</td>
</tr>
</tbody>
</table>

With proper selection of resistor and capacitor values, the design expressions could be greatly simplified. However, if the circuit is supposed to be implemented in integrated circuit scale, the designer would run into numerous difficulties:

- The frequency response plotted in Figure 4.1 assumes that extremely high DC gain is provided by the Opamp, and this is very hard to achieve as the process scales down. Consequently, the performance of the LPF would be largely degraded.
- The lump elements, especially capacitors, pose difficult tasks as the circuit implementation moves to the stage of layout. Capacitor values of 10 pF as listed in the table would take a large amount of chip area, which negatively impacts the density and usefulness of the integrated circuit as LPF would require connections with other circuits in the communication systems. In some cases, ultra-low bandwidth filter would be required, and even large capacitor values are needed, making the circuit less preferable in integrated circuit design.
- The bandwidth tuning is hard to achieve. Except for changing the resistor and capacitor values directly, there is no other way that the designer could adjust the -3 dB bandwidth associated with the LPF without worrying about the possible effect on other parts, such as the operational amplifiers, of the circuit.

Next in Section 3.4, Verilog-AMS simulation of ROI based filters are provided. Along with the circuit implementation documented in Danyang Wang’s thesis, we are able to demonstrate that designers would be able to comfortably handle the difficulties mentioned above with ROI low pass filters.

### 4.2 Ring Oscillator Integrator Based Low Pass Filter

Before talking about the schematic of the ROI based LPF, note that while the connections between function blocks are following the block diagram in Figure 3.5, the actual implementation prefer multiphase structure over single phase. The proposed ROI outputs as a PWM signal which contains additional tones near the modulation frequency $F_{\text{PWM}}$ and other integer multiples of $F_{\text{PWM}}$ [2]. The spurious tones phenomenon is better illustrated with the figure from B. Drost, M. Talegaonkar, and Professor Hanumolu’s paper [3], as shown in Figure 4.2.
In order to deal with this issue, I would like to introduce the multi-phase PWM scheme employed in the implementation in which many out-of-phase PWM signals are summed to generate the final output. In the process of summation, higher order tones would be canceled out except tones near $M \times F_{OSC}$, where $M$ indicates the number of phases chosen to have in the implementation.

As discussed in Section 3.2.1, the first order ROI based LPF is implemented following the block diagram in Figure 3.5. A general description of the first order ROI filter schematic implemented in Cadence Virtuoso is shown in Figure 4.3:

As shown in Figure 4.3, $M$ phases are chosen to be the references into the phase detector, where $M$ will be even. The reference phases are provided using $V_{PULSE}$ sources which generate square wave inputs at frequency equal to the center frequency of the oscillator, but have proper delay to create the phase shift with respect to each other. Even number of reference phases are chosen so that two of the phases will be placed $\pi$ radians out of phase, so that the PWM spurious tones get cancelled out as expected. In the circuit
implementation, the CCO is realized with delay cells. For N delay cells, the output at each delay cell will be $\frac{2\pi}{N}$ radians out of phase with respect to the output phase of the next delay cell in the chain. Another thing that is worth pointing in the simulation is that the CCO is modeled using VCO with current controlled voltage source (CCVS) connected. The reason for doing this is due to the fact that it is more comfortable to work with voltage signals in Verilog-AMS.

Before running simulations to check the filtering function of the circuit, lock test for the PD is first run to ensure that the input phase difference at the PD is within $2\pi$ radians. Also, based on the schematic of the PD that has been used in the project, the lock point is $\pi$ radians apart between input and reference signal, and this can be observed in Figure 4.4 that eventually input sine wave and reference are $\pi$ radians out of phase.

![Figure 4.4: Phase Detector Lock Test](image)
Once proper locking is observed for the lock test, the LPF is ready for running simulations with sinusoidal input. The input is selected based on the requirement for PWM demodulation. The output PWM signal is exported into data file which is then fed to a MATLAB code running Fast Fourier Transform (FFT) spectral analysis so that the input signal is recovered in the frequency domain. Explanation of FFT spectral estimation is included in Appendix A for reference. To demonstrate the test results, the following elements are included:

- Output PWM waveforms are shown in Figure 4.5 and 4.6 respectively. The two figures are the time domain representation of the filter output. Since we are more interested in the spectrum of the filter output, time domain outputs are attached to illustrate the resolution improvement due to introductions of multiple phases.
- A MATLAB-generated FFT spectral analysis is attached to show the expected frequency domain spectrum as well as the tone cancellation introduced by multiphase implementation.
- A table is provided to summarize the test input frequency and the measured output magnitude.
- The ROI based LPF frequency response is plotted based on the results obtained from FFT analysis.

In the following, the results are included according to the sequence just presented:

![Figure 4.5: Pulse Width Modulation Output Using Two Phases](image)

![Figure 4.6: Pulse Width Modulation Output Using Ten Phases](image)
For the output examples given, the input signal is at frequency equal to $f = 100$ kHz, or period of $T = \frac{1}{f} = 10 \mu s$. Notice in Figure 4.5, the PWM output waveform resembles more like the shape of the sinusoidal input. This improvement in the resolution of the output PWM is an advantage brought by the introduction of multiphase implementation. The measured period of the outputs are both approximately 10 μs, reflecting the input signal’s period.

Next, the FFT spectrum is analyzed using MATLAB is attached. In order to make it convenient to measure the input spectrum magnitude, specific frequency is selected following method introduced in Appendix A. For the two examples shown in the thesis, bin 157 is selected, which is supposed to give strong peak at $f = 93579$ Hz. The magnitude of this peak is read and recorded as the corresponding output response if the signal is passed through the filter. Another thing that is worth pointing out is that on the right side of the figures, multiple pulses are shown located at integer multiples of 100 MHz. 100 MHz is selected to be the reference frequency of our filter to modulate the signal. These peaks are the modulation tones. In consistence of our discussion in Chapter 3, the two-phase scheme causes tone peaks to start at 200 MHz, while the ten-phase scheme forces the tone peaks to start at 1 GHz, as shown in Figure 4.7 and 4.8.

![Figure 4.7: FFT Spectrum Analysis of Two-Phase Scheme](image)
Figure 4.8: FFT Spectrum Analysis of Ten-phase scheme

Finally, summary of the test input frequencies and output magnitudes are documented in Table 4.2 (a) and (b). Here, two sets of simulations are included with different feedback charge pump bias current $I_{\text{CPFB}}$. As mentioned in Chapter 3, the tuning of the bandwidth is easily achieved by adjusting $I_{\text{CPFB}}$ and this is clearly shown in Figure 4.9 about the transfer function constructed for the ROI based low pass filter.

Table 4.2: ROI-Based Low Pass Filter with (a) $I_{\text{CPFB1}}$, (b) $I_{\text{CPFB2}} < I_{\text{CPFB1}}$

<table>
<thead>
<tr>
<th>Bin</th>
<th>Input Frequency (Hz)</th>
<th>FFT Output (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>79</td>
<td>47087.6694</td>
<td>-26.0205</td>
</tr>
<tr>
<td>103</td>
<td>61392.7841</td>
<td>-26.0233</td>
</tr>
<tr>
<td>157</td>
<td>93579.2923</td>
<td>-26.0322</td>
</tr>
<tr>
<td>211</td>
<td>125765.8005</td>
<td>-26.0450</td>
</tr>
<tr>
<td>269</td>
<td>160336.4944</td>
<td>-26.0626</td>
</tr>
<tr>
<td>389</td>
<td>231862.0682</td>
<td>-26.1126</td>
</tr>
<tr>
<td>587</td>
<td>349879.2648</td>
<td>-26.2326</td>
</tr>
<tr>
<td>773</td>
<td>460743.9041</td>
<td>-26.3849</td>
</tr>
<tr>
<td>991</td>
<td>590682.0297</td>
<td>-26.6068</td>
</tr>
<tr>
<td>1201</td>
<td>715851.7838</td>
<td>-26.8584</td>
</tr>
<tr>
<td>1787</td>
<td>1065135.0021</td>
<td>-27.6877</td>
</tr>
<tr>
<td>3331</td>
<td>1985430.7175</td>
<td>-30.1631</td>
</tr>
<tr>
<td>5099</td>
<td>3039240.8371</td>
<td>-32.6849</td>
</tr>
<tr>
<td>7919</td>
<td>4720091.8198</td>
<td>-35.8476</td>
</tr>
<tr>
<td>9887</td>
<td>5893111.2289</td>
<td>-37.7295</td>
</tr>
</tbody>
</table>

(a)
Table 4.2: (Continued)

<table>
<thead>
<tr>
<th>Bin</th>
<th>Input Frequency (Hz)</th>
<th>FFT Output (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>79</td>
<td>47087.6694</td>
<td>-6.5622</td>
</tr>
<tr>
<td>103</td>
<td>61392.7841</td>
<td>-6.9038</td>
</tr>
<tr>
<td>157</td>
<td>93579.2923</td>
<td>-7.8493</td>
</tr>
<tr>
<td>211</td>
<td>125765.8005</td>
<td>-8.9106</td>
</tr>
<tr>
<td>269</td>
<td>160336.4944</td>
<td>-10.0620</td>
</tr>
<tr>
<td>389</td>
<td>231862.0682</td>
<td>-12.2648</td>
</tr>
<tr>
<td>587</td>
<td>349879.2648</td>
<td>-15.2159</td>
</tr>
<tr>
<td>773</td>
<td>460743.9041</td>
<td>-17.3769</td>
</tr>
<tr>
<td>991</td>
<td>590682.0297</td>
<td>-19.4079</td>
</tr>
</tbody>
</table>

(b)

Notice the difference in the number of entries are selected as the transfer functions will be properly presented in the same range. The ROI-based LPF transfer functions are plotted using normalized output values to better show the accessible tuning with the change of $I_{CPFB}$:

![Figure 4.9: ROI-Based Low Pass Filter Transfer Function](image)

Figure 4.9: ROI-Based Low Pass Filter Transfer Function
REFERENCES


APPENDIX A: FAST FOURIER TRANSFORM FOR PWM DEMODULATION

Fast Fourier Transform is chosen to perform the PWM demodulation to recover the input signal at the output port. In the appendix, the MATLAB code used will be included and the method in choosing the parameters in order to specify the FFT spectral analysis is explained here as well.

To be able to retrieve the input frequency at the output, I have to first choose the sampling period of the sampling performed on output waveform. Denote the strobe period (function provided in Cadence Virtuoso) as $T_{strobe}$, then the sampling frequency is equal to:

$$f_s = \frac{1}{T_{strobe}}$$  \hfill (A.1)

Next, number, $N$, is chosen and FFT will performed $2^N$ points analysis. With this selection, the FFT spectrum is distributed over $2^N$ bins, and each bin will be represents a frequency increment, $f_{step}$, equal to:

$$f_{step} = \frac{f_s}{2^N}$$  \hfill (A.2)

The last step in FFT spectral analysis is to choose sufficient time of running the simulation so that enough information is collected to recover the spectrum. The length of simulation time, $T_{sim}$, is calculated as:

$$T_{sim} = 2^N \times T_{strobe}$$  \hfill (A.3)

And the input frequency should be selected to lie with the range:

$$0 < f \leq (2^N - 1)f_s$$  \hfill (A.4)

where DC component is usually removed during the analysis. One last notice about FFT spectral analysis is that as I have mentioned the frequency spectrum will be located at specific bin. Therefore, to have the best results, suggestion of selecting the input frequency would make the frequency lie exactly at one specific bin. Furthermore, a prime number bin would be preferred so that no harmonics would be folded into the same bin, as the FFT is symmetric. One way to choose the input frequency is as follows:

$$f_{in} = \frac{f_s}{2^N} \times B$$  \hfill (A.5)

where $B$ is the prime number that the designer selects and $B \leq 2^N$. 

33
The MATLAB code is attached for reference:

```matlab
%% FFT Spectral Analysis

clear
clc

% Read in data
data = csvread('twophase_bin157_100p_2ms.csv', 1, 0);
Time = data(:, 1);
Wave = data(:, 2);

% FFT
N = 24;
Points = 2^N;
Period = 100e-12;
Frel = 1 / Period;
Freq = (0: Frel / Points: (Freq1 * (Points - 1) / Points));

% Taking FFT
wave = Wave - mean(Wave);
fftout = abs(fft(wave(1:end), Points)) / Points;
fftoutdb = 20 * log10(fftout);

% Plot
semilogx(Freq(1: Points / 2), fftoutdb(1: Points / 2));
```
APPENDIX B: VERILOG-AMS CODES

Code for voltage controlled oscillator with two output phases:

```verilog
`include "constants.vams"
`include "disciplines.vams"

Module vco_twophi (out1, out2, in);
    input in; electrical in;                   // input terminal
    output out1, out2; electrical out1, out2; // output terminals; 180 degree difference
    parameter real ampl = 0.9;                // output voltage amplitude
    parameter real offset = 0.9;              // DC offset at the output of VCO
    parameter real vco_cf = 100M;             // output frequency when input is zero
    parameter real kvco = 400M from (0:inf);  // Kvco [Hz/V]
    parameter real phi1 = 0;                  // phase for output1
    parameter real phi2 = 0.5;                // phase for output2
    real freq, phase1, phase2;

    analog begin
        freq = vco_cf + kvco * V(in);       // compute the freq from the input voltage
        $bound_step(0.01/freq);              // bound time step to assure no cycles are skipped
        // phase is the integral of the freq modulo 2pi
        phase1 = 2 * M_PI * idtmod(freq, phi1, 1, -0.5);
        phase2 = 2 * M_PI * idtmod(freq, phi2, 1, -0.5);
        // generate the output
        V(out1) <+ ampl * sin(phase1) + offset;
        V(out2) <+ ampl * sin(phase2) + offset;
    end
endmodule
```
Code for D flip-flop:

```verbatim}
`include "constants.vams"
`include "disciplines.vams"

Module dff (q, qb, clk, d);
    output q;       // Q output
    output qb;      // Q bar output
    input clk;      // Clock input, rising edge triggered
    input d;        // D input
    electrical q, qb, clk, d;
    parameter real td = 100p from (0:inf);    // delay from clock to q
    parameter real tt = 100p from (0:inf);    // transition time of output signals
    parameter real vh = 1.8;                   // output voltage in high state
    parameter real vl = 0;                     // output voltage in low state
    parameter real vth = (vh + vl) / 2;        // threshold voltage at inputs, value set so that it
                                                // checks crossing based on voltage level
    parameter integer dir = +1;                // rising clock edge triggers flip flop
    real state;

    analog begin
        @(cross(V(clk) – vth, dir, 1e-12))
            state = (V(d) > vth);
            V(q) <+ transition( state ? vh : vl, td, tt);
            V(qb) <+ transition( state ? vl : vh, td, tt);
    end
endmodule
```
Code for XOR/XNOR gate:

```vhdl
#include "constants.vams"
#include "disciplines.vams"

module axor_axnor (axor, axnor, in1, in2);
    output axor, axnor;
    input in1, in2;
    electrical axor, axnor, in1, in2;

    parameter real vh = 1.8;  // output voltage in high state
    parameter real vl = 0;    // output voltage in low state
    parameter real vth = (vh + vl) / 2;  // threshold voltage at input
    parameter real td = 100p from (0:inf);  // delay to start of output transition
    parameter real tt = 100p from (0:inf);  // transition time of output signals

    analog begin
        @(cross(V(in1) – vth, 0, 1e-12) or cross(V(in2) – vth, 0, 1e-12))
        

        V(axor) <+ transition( ((V(in1) > vth) ^ (V(in2) > vth)) ? vh : vl, td, tt );
        V(axnor) <+ transition( ((V(in1) > vth) ^ (V(in2) > vth)) ? vl : vh, td, tt );

    end
endmodule
```
Code for charge pump:

```vhdl
`include "constants.vams"
`include "disciplines.vams"

module cp (out, inc, dec);
    input inc, dec; electrical inc, dec;
    output out; electrical out;
    parameter real cur = 1m; // output current (A), gain of charge pump
    parameter real vh = 1.8; // input voltage in high state
    parameter real vl = 0; // input voltage in low state
    parameter real vth = (vh + vl) / 2; // threshold voltage at input
    parameter real tr = 100p;
    parameter real tf = 100p;
    real state;

    analog begin
        if ((V(inc) > vth) && (V(dec) < vth))
            state = 1;
        else if ((V(inc) < vth) && (V(dec) > vth))
            state = -1;
        else
            state = 0;
        l(out) <+ -transition(cur*state, 0.0, tr, tf);
        l(out) <+ V(out) / 1T; // Add gmin to output to avoid convergence issues
    end
endmodule
```
Code for current controlled voltage source:

```vhdl
`include "constants.vams"
`include "disciplines.vams"

module ccvs (out, inp, inn);
    input inp, inn;
    electrical inp, inn;
    output out;
    electrical out;
    parameter real gain = 1 from (0:inf); // gain of CCVS
    parameter real rin = 1k from (0:inf); // input impedance for the input voltage
    parameter real tr = 100p from (0:inf);
    parameter real tf = 100p from (0:inf);
    real cin;

    analog begin
        cin = V(inp) / rin – I(inn); // Compute the input current

        // Assign the output voltage based on the input current
        V(out) <+ -transition(cin*gain, 0.0, tr, tf);
    end
endmodule
```
Code for current adder with two input currents:

```
`include “constants.vams”
`include “disciplines.vams”

module addc (out, in1, in2);
  output out;
  electrical out;
  input in1, in2;
  electrical in1, in2;
  parameter real rout = 1k;
  parameter real direction = -1;

  analog
    l(out) <+ dir * (l(in1) + l(in2)) ;

endmodule
```