A PATTERN RECOGNITION COMPUTER
USING ALL-MAGNETIC LOGIC

prepared by
J. Divilbiss

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This thesis describes the development of a pattern recognition computer consisting of a control computer and a pattern recognition unit or PRU. The role of the PRU in the combined system is analogous to that of the arithmetic unit in a conventional digital computer. The three principal divisions of the PRU are 1) a two-dimensional shift register of \( N \times N \) bits, 2) a \( k \)-word memory with \( N^2 \) bits per word, and 3) a bubbler consisting of \( N^2 \) bubble registers of length \( r \). Each bubble register is a linear "self-ordering" register, that is, a register in which a fixed number of identical operations will order the information with all "ones" at one end of the register, all "zeros" at the other end. The control computer is of conventional design and is not treated at length. Examples of simple pattern recognition routines are given.

A considerable part of the paper is devoted to developing a catalog of logical circuits using only transfluxors (multiaperture ferrite cores) and connecting wire. These circuits include negation, \( XY \), the exclusive or function and others. Two logical networks, a two-dimensional shift register and a bubble register, are used to illustrate the procedure for interconnecting these magnetic circuits. Additionally, the bubble register is used to demonstrate an important aspect of all-magnetic logic, namely, that a network with simple, fixed wiring can perform a variety of operations if the sequence of clock pulses is appropriately modified. The transfluxor bubble register (using three cores per register location) can bubble, shift either direction, provide...
the digit-wise complement function and perform other useful operations. Experimental results from a transfluxor bubble register are included.

Certain aspects of the engineering design (as opposed to the logical design) of magnetic circuits are treated. In particular, it is shown both theoretically and experimentally that flux division in multiaperture magnetic devices is dependent upon the risetime of the setting current.
INTRODUCTION

Modern arithmetic digital computers, for all their speed and complexity, remain essentially devices for imitating human problem-solving processes. They are, of course, quite successful in this sphere. In recent years digital computers have also been adapted with reasonable success to a number of non-arithmetic problems such as language translation, game strategy, the composition of music and the tracking of aircraft. The nonarithmetic problem considered in this paper is the recognition of characters and events with a two-dimensional pattern.

Of the nonarithmetic problems cited, pattern recognition has been especially difficult to achieve in arithmetic digital computers. First, the problem frequently is not well defined. Human visual perception is an extremely subtle process so little understood that it cannot yet serve as a prototype. (Contrast this with the arithmetic case where the computer can always be programmed to imitate the computational algorithms of a human problem solver.) Second, the organization of present day arithmetic computers is based on the processing of numbers or one-dimensional arrays of bits. Thus, a two-dimensional pattern must be analyzed piecemeal with attendant loss of efficiency.

To be useful, rather than merely interesting, pattern recognition by computers must be superior to human recognition in speed and accuracy. The speed requirement almost certainly dictates a computer organized to process patterns as two-dimensional arrays rather than as numbers. The logical design of such a computer is the central purpose of this paper.

Before proceeding to the logical design of the pattern recognition computer, however, we will first develop a catalog of logical circuits and
networks. In this way the final logical realization will be strongly influenced by the advantages as well as the limitations of the logical element selected. The logical design given in Chapter IV is based on realization with multiaperture ferrite cores (transfluxors). This design could be translated into transistor circuitry in a straightforward way, but this would not make the best use of certain transistor properties, such as fanout capability.

The transfluxor is an enormously complex device, despite its simple appearance. It combines all the complexity of the memory core (which has been and continues to be the object of extensive research)\textsuperscript{7,12} with complications arising from the plurality of paths. Since the principal object of this paper is the development of a logical design, the transfluxor will be presented in the simplest possible form. Complicating details will be added (chiefly in Chapter V) only as they are necessary to bring the simplified model into closer agreement with measured results.
CHAPTER I. THE TRANSFLUXOR

In 1955, Jan Rajchman and Arthur Lo of RCA Laboratories introduced a new circuit element which they called the transfluxor. The function of this element is suggested by the subtitle of the original paper, "A magnetic gate with stored variable setting." That is, the authors thought of the transfluxor as a variable transformer in which the coupling between windings could be set with a single current pulse. Although the inventors of the transfluxor pointed out its potential usefulness as a logical element for digital computers, few applications have been made in that area. Transfluxors are sometimes used in nondestructive core memories and in shift registers, but both these applications are characterized by their logical simplicity.

H. D. Crane and others of Stanford Research Institute have used multi-aperture cores to build a small arithmetic unit but the technique used does not seem well suited to the logical circuits required here. Briefly, the Crane circuits enjoy greater speed but at the expense of operating tolerances and logical flexibility.

The explanation of the transfluxor given in this chapter will emphasize the logical properties of the element, both those established by other authors and those developed here to solve specific problems. The treatment of the transfluxor as an idealized logical element will lead most readily to the development of logical circuits in subsequent chapters. The final chapter will deal with the engineering realities of magnetic circuit design. Two-hole transfluxors will be ignored as they have limited logical utility.
I.1 Conventions and Assumptions

In dealing with multiaperture magnetic devices it has become customary to use a number of conventions and simplifying assumptions. For example, the flux in a multiaperture core is not likely to be distributed as neatly as is indicated by our simplified flux diagrams. This does not seriously limit the usefulness of such diagrams.

These, then, will be the assumptions:

1. Flux lines lie entirely within the core.
2. The B-H characteristic of the material is perfectly rectangular.
3. Flux reversals will occur along permissible paths of minimum length.

Consider the magnetic structure shown in figure 1, initially unmagnetized and with three legs of equal cross sectional area. A current circling leg one will force flux downward in leg one and, by assumption one, this change must be accompanied by an upward flux change in legs two and/or three. Assumption 3 is that all the flux change will occur in leg two, path 12 being shorter than path 13. Experimental structures similar to the one given as an illustration have shown the flux to divide between legs two and three in the ratio of 2:1:1 when leg one was driven to saturation.5

If the flux can be reversed in all portions of a path, the path will be called a permissible flux reversal path. The permissibility of a path depends on the state of the core, which aperture or apertures carry current and the direction of that current. Examples given in the next section will clarify this concept.

In treating the transfluxor as a logical element (rather than as a variable transformer) we will consider only those states in which all legs are saturated. To specify any state it is then necessary only to show the direction of flux in each of the legs. Only six such states are possible
FIGURE 1. TWO APERTURE FERRITE CORE
in the three-hole transfluxor shown in figure 2. Any other combination of flux directions would violate the requirement of flux continuity within the core. As the drawing is intended to suggest, the four numbered legs are of equal cross sectional area. Five of these states form the basis for most of the subsequent development. The sixth state, anticleared, is included only for completeness.

1.2 Forward Isolation

Having introduced flux diagram notation we can now consider transitions between the flux states. The first of these transitions occurs when a cleared core is set by means of a current through the input minor aperature. In figure 3, as in the remainder of the paper, the cleared state of a core is represented by a flux pattern clockwise around the major aperature.

The set pulse does not induce a voltage in the output winding, since the flux change in leg 1 is accompanied by a flux change in (the 'nearer') leg 3. There is, of course, no change in leg 2 as it is already saturated in the upward direction. For this particular transition, paths 13 and 14 might be called competitive permissible paths, with 13 winning because of its shorter length. "Competitive" refers to the fact that the paths share a common leg and therefore cannot both switch. (This follows from assumptions one and two and from the restriction on cross sectional area.)

Forward isolation (i.e., the set pulse did not induce an output voltage) can be described more compactly. For a cleared core, 13 and 14 are the only permissible paths linking the input aperature. The set current will cause switching around the shorter of these paths, 13, which does not link the output winding.
FIGURE 2. POSSIBLE FLUX STATES IN A THREE HOLE TRANSFLUXOR
FIGURE 3. FORWARD ISOLATION
1.3 Backward Isolation

By backward isolation we mean that the interrogation of a core will not induce a voltage in the set winding. This property will be explained first for the nondestructive read case. The first two flux states in figure 4 were explained in the preceding section. In the next step, the prime current links the competitive permissible paths 24 and 34. Path 34 is much shorter than 24; consequently, flux is reversed around the output aperture. Essentially the same argument holds for the drive (interrogate) pulse, i.e., the drive current will reverse flux around the output aperture only. Thus, backward isolation is inherent for the nondestructive mode of operation.

Note that state 4 is identical to state 2. This makes it possible to repeat the prime-drive pair repeatedly without loss of information or, as defined, nondestructively.

In the absence of a set pulse the "input-output" cycle is described by states 5 through 8 in figure 4. With no set current, states 5 and 6 are, of course, identical. They are shown separately here to aid comparison with states 1 and 2. The prime current could cause a flux reversal in the next step (path 24) but does not because its magnitude is maintained below the threshold for that path. In short, for a core which has not been set, no flux reversals occur from interrogation. This is, of course, nondestructive also.

The circuit requirements for the destructive mode are somewhat different, as will be seen in figure 5. Backward isolation for this circuit is achieved through the use of an antiprime current through the input aperture applied at the same time as prime. The antiprime resets leg 1 so that the clear pulse does not cause a flux reversal in leg 1. It is true, of course, that voltages may be induced in both input and output windings by the prime and antiprime.
Cleared state | \[\uparrow \uparrow \downarrow \downarrow \] State 1
---|---
**Set**
Set prime | \[\downarrow \uparrow \uparrow \downarrow \] State 2
---|---
**Prime**
Output primed state | \[\downarrow \uparrow \downarrow \uparrow \] State 3
---|---
**Drive**
Set state | \[\downarrow \uparrow \uparrow \downarrow \] State 4
---|---
Cleared state | \[\uparrow \uparrow \downarrow \downarrow \] State 5
---|---
Cleared state | \[\uparrow \uparrow \downarrow \downarrow \] State 6
---|---
**Prime**
Cleared state | \[\uparrow \uparrow \downarrow \downarrow \] State 7
---|---
**Drive**
Cleared state | \[\uparrow \uparrow \downarrow \downarrow \] State 8
---|---

**FIGURE 4. BACKWARD ISOLATION, NONDESTRUCTIVE READ**
<table>
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<tr>
<th>State</th>
<th>Cleared state</th>
<th>Set state</th>
<th>Prime + antiprime</th>
<th>Fully primed state</th>
<th>Clear</th>
<th>Cleared state</th>
<th>Set state</th>
<th>Prime + antiprime</th>
<th>Cleared state</th>
<th>Clear</th>
<th>Cleared state</th>
<th>Set state</th>
<th>Prime + antiprime</th>
<th>Cleared state</th>
<th>Clear</th>
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<td>State 1</td>
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<tr>
<td>State 2</td>
<td>↓</td>
<td>↑</td>
<td>↑</td>
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<td>↓</td>
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<td>State 4</td>
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<td>State 7</td>
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<td>State 8</td>
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**FIGURE 5. BACKWARD ISOLATION, DESTRUCTIVE READ**
currents but if these currents are small, switching will proceed slowly and the induced voltages will be small.

The function of the prime is to reverse the flux in legs 3 and 4 so that there will be an output during the clear pulse, assuming the core was set. The antiprime reverses flux in legs 1 and 2 so that there will not be a voltage induced in the set winding during the clear pulse, hence, antiprime. The prime and antiprime designations also serve as a reminder that the two currents thread the core in opposite directions.

In the remainder of this paper the term "prime" will normally refer to both prime and antiprime currents with exceptions noted. No confusion should result and it is convenient to treat the two currents together as they generally occur at the same time and are of the same magnitude.

I.4 Current Constraints

It is important to think of the transfluxor as a threshold device. For every permissible flux reversal path there is a current threshold which is the product of the path length and a constant determined by the core material. Thus, the set current must be greater than some minimum value determined from the length of path 13. There is no maximum value for the set current; when leg 1 has fully reversed, switching stops irrespective of the magnitude of the set current.

In general, the various currents used with the transfluxor have only lower boundaries. The exception is the prime current which has both minimum and maximum limits. Referring back to figure 4, we see that the prime must be large enough to ensure switching around 34 in a core that has been set and yet small enough not to cause switching around 24 in a cleared core. In the latter case, excessive prime current which causes switching around 24
is called **spurious setting**. In the actual device, the spread between minimum and maximum prime currents is determined by core geometry and by the square-ness of the B-H characteristic. The constraints on prime current are discussed at greater length in Chapter V.

I.5 **The Inhibit Winding**

The introduction of another winding through the input aperture makes it possible to gate the setting signal.

Consider, case by case, the effect of this inhibit signal on the flux distribution within the core. If the inhibit is applied while the core is in a cleared state there will be no flux change, leg 1 being already saturated in the upward direction. This is to say that paths 13 and 14, linking the inhibit current, are not permissible paths for that current sense. If the inhibit occurs together with set pulse there will be no net setting current. Exact cancellation is unnecessary; the inhibit may be arbitrarily large since an excess of inhibit current merely brings us back to case one. If the inhibit occurs after the core has been set but before it has been primed, the flux in legs 1 and 2 will reverse. This case (shown in figure 6) does not destroy the information held in the core. The argument for the final case, inhibit occurring after prime, is the same as for case one. The four cases cited are not equally important but have been included here to establish an important inhibit property. The inhibit signal can gate the setting pulse, but by itself cannot alter the binary state of the core, the two binary states being cleared (zero) and non-cleared (one).

The last assertion is worth restating because of its use in subsequent sections. A current in the inhibit direction through a minor aperture cannot set a cleared core nor can it clear a core that has been set. It is a curious
Cleared state
• Set
Set state
• Inhibit
Input antiprimed
• Prime
Fully primed
• Drive
Input antiprimed

FIGURE 6. THE INHIBIT WINDING
and useful fact that a current in the set direction through a minor aperture can change the binary state of a core, whereas a current in the opposite sense cannot change the binary state. The binary state is simply a means of specifying whether or not interrogation will cause an output.

Inhibit and antiprime, it will be noted, thread the same aperatures and in the same sense. The distinction between them is one of function; antiprime is a slow, limited amplitude pulse that occurs during prime and inhibit is a fast pulse used during the set operation.

I.6 Various Set Methods

While the specific wiring arrangement developed up to this point has considerable logical flexibility, it does not represent the only possible approach. As an example, figure 7 shows five methods of setting a core, together with a tabulation of the principal characteristics of each. Each of these circuits has an application for which it is well suited, although not all will be used in the logical designs of this paper.

Circuit number 1 has been previously described and will continue as the basic set circuit. In circuits number 2 and number 3 the setting current must be large enough to cause switching around path 23 but not so large as to switch path 14.

The chief virtue of circuit number 4 is the economy of wiring. The same wire can be used for either the prime function or, by increasing the current to more than the threshold value for path 24, for setting. This is the "spurious setting" of earlier mention turned to an advantage.

Circuit number 5 combines the coincident current properties of circuit number 3 and the wiring simplicity of circuit number 4. The set current must occur at prime time rather than before the prime. During setting, the prime current is its normal value.
FIGURE 7. VARIOUS SET METHODS
II.1 Basic Logical Model

Several commercially available cores have four minor apertures, rather than two. With these cores it is convenient to use three of the minor apertures as inputs and the fourth as an output. To aid in the discussion of this five-hole device the extra legs will be numbered as shown in figure 8.

In the case of a three-hole core it was shown that a set pulse linking leg 1 would cause a flux reversal in leg 3 rather than in leg 4. Similarly, the minimum path rule shows that legs 6 and 7 will change when leg 1 is set. (Path 1637 is the shortest permissible path linking the set₁ aperture.) There are two important consequences of this. First, the set₁ signal does not induce a voltage in the other set windings. Second, the set₂ and set₃ apertures may be inhibited without any inhibiting effect on set₁. It is easily shown that this independence is true of all three inputs and that other combinations, such as two inputs occurring together, do not raise difficulties. For example, if set₁ and set₂ occur together the reversal path is 1537, the shortest permissible path linking both set currents. This path does not link the lower input aperture, hence, no voltage is induced in the set₃ winding. Moreover, the lower input aperture may be inhibited without affecting the setting action of set₁ and set₂ since this inhibit current would lie outside path 1537. The basic logical model for the transfluxor follows from this principle of independent inputs.

Figure 9 is a pictorial statement of the major transfluxor properties: memory, independent gating of inputs, forward and backward isolation and the facility for either destructive or nondestructive interrogation. The dual function of the clear signal is to establish the binary state of the core and
FIGURE 8. FIVE HOLE TRANSFLUXOR
FIGURE 9. BASIC LOGICAL MODEL FOR FIVE HOLE TRANSFLUXOR
also to interrogate it. To show that this does not lead to a race condition it has been necessary to include a delay in the equivalent logical circuit.

Figure 9 further shows the correspondence between the nine named signal lines of the logical diagram and their wiring counterparts. Missing from both the logical diagram and the physical picture, however, is any mention of prime or antiprime, signals essential to the operation of the circuit. To make figure 9 correct we must state that every interrogating pulse, drive or clear, is preceded by a combined prime and antiprime pulse.

II.2 Basic Transfer Circuit

In addition to its other properties, the transfluxor can be thought of as a power amplifier. The energy required to set a core is fixed, at least in the sense that it is independent of the amount of energy extracted later during the interrogate operation. (The actual energy expended in setting a core depends on the amplitude of the set current. The minimum energy requirement is one half the area of the B-H characteristic of the setting path.) During interrogation, energy available from the output winding is limited, in principle, only by the amplitude of the interrogating signal. The appropriate reversal path (path 34 for nondestructive read, path 2647 for destructive read) can be likened to a transformer with the interrogating winding as the primary, the output winding as the secondary. Note that the prime signal supplies only sufficient energy to effect the necessary flux reversals within the core; the drive or clear signal supplies energy to both the core and the output winding. It is this power gain resulting from large clear and drive signals that makes possible the interconnection of transfluxors into complex arrays.

The basic coupling loop or transfer circuit is shown in figure 10. The previously separate prime and drive windings have been combined here into a
A and B initially cleared
A set to one
Contents of A non-destructively transferred to B

FIGURE 10. BASIC TRANSFER CIRCUIT
single winding. This simplifies the drawing and, in an actual network, simplifies the wiring.

The coupling loop is drawn to show the sense of the winding but not the number of turns through a specific aperture. When the number of turns is greater than one it is shown as a small number near the aperture. The arrow within the coupling loop indicates the direction in which the information is transferred; the arrow on the coupling loop wire indicates the current sense during transfer.

From the standpoint of wiring ease, a 1:1 coupling loop ratio would be desirable. The 2:1 ratio shown is necessary because of coupling loop losses. A more precise statement of the restrictions on coupling loop ratios is given in Appendix A.

A few comments on the mechanism of transferring a one are appropriate here. In the first transition, the flux reversed by the set A current does not link the coupling loop, thus demonstrating the principle of forward isolation. In the second transition, when A is primed, a small coupling loop current flows. This loop current passes through B in the inhibit direction, leaving B unchanged. In the last transition, the clearing of A reverses the flux in leg 4 which in turn induces a loop current large enough to set B. If A had been nondestructively read, leg 4 would have been reversed with the same result to B but with the binary state of A unchanged.

II.3 Fanout

If a logical device is to be useful in other than very restricted applications it must be capable of driving two or more similar units. For a transfluxor circuit the fanout must be expressed as two numbers: the logical fanout or the number of inputs that can be connected to the output
of a core, and the **simultaneous fanout** or the number of inputs that can be set simultaneously from a single core. This dual definition of fanout is illustrated in figure 11 by a circuit used in the pattern recognition unit of Chapter IV.

This circuit has a simultaneous fanout of one since the operation of the network requires that two of the three inputs be inhibited during any drive pulse. The driving core can transfer its information to any of the three receiving cores but it can set only one of these with a single drive pulse.

In spite of appearances, the loop equations for figures 10 and 11 are identical. This is so because the two inhibited cores of figure 11 cannot switch under the influence of the set (coupling loop) current. For compactness we will say that the inhibit current "short-circuits" the input winding, since no voltage is induced in the winding by the set current.

In principle, the circuit of figure 11 could have a simultaneous fanout of two or more if the coupling loop turns ratio were increased from $2:1,1,1$ to $2N:1,1,1$. Unfortunately, the engineering difficulties associated with this procedure make it unattractive for $N$ larger than two. In addition to the difficulty of threading $2N$ turns through a small aperture there would be the necessity of increasing the drive current so that the net drive remained constant.

**II.4 Net Drive**

Net current (net drive, net clear, etc.) is the algebraic sum of currents linking a specified flux reversal path. Figure 12 shows a core that can be interrogated either destructively or nondestructively. The core is assumed to be set and primed.
FIGURE 11. CIRCUIT WITH LOGICAL FANOUT OF THREE
FIGURE 12. NET DRIVE--NET CLEAR
For nondestructive read, using the drive signal shown, the flux reversal path is $34$ and the net drive is $I_{DR} - 2I_o$. For destructive read, using the clear signal, the flux reversal path is 2647 and the net clear is $I_{CL} - 2I_o$. It would be this value even if there were set or inhibit currents in the input apertures during the clear pulse. Path 2647 links only two apertures; currents lying outside these apertures do not enter into the expression for net clear. This does not mean that switching around this path necessarily occurs whenever the net clear exceeds the threshold for the path. For example, the addition of a set current during the clear may create a competitive path situation. It does mean that if switching occurs around a specified path, the rate of switching is determined by the net current. Complex multipath situations are analyzed in more detail in Chapter V.

II.5 Negation

Many ingenious designs for special purpose multiaperture devices have appeared in the literature, among them the "negative MAD." Interrogation of this negative element would give the complement of the information set into the core. The only disadvantage of this approach is that cores of this peculiar geometry are not commercially available.

Figure 13 shows a negation circuit in which both sending and receiving cores are standard five hole transfluxors. The negation circuit differs from the basic transfer circuit in two major respects, the orientation of the coupling loop and the sequence of clock pulses. The negative transfer action can be demonstrated with two examples.

**Case one -- sending core cleared**

As a starting condition both cores are cleared as shown in the simplified flux diagram of figure 13.
Starting condition

After set R

After prime S

After drive S

After prime R

After drive R

FIGURE 13. NEGATION CIRCUIT
1) Set receiving core to one
   
   With the negation circuit this operation tends to set the sending core to a one, as application of Lenzes law quickly demonstrates. This unwanted back-propagation of information is prevented by applying a drive pulse to the sending (left hand) core during the set pulse. Double arrows indicate a change from the preceding flux diagram.

2) Prime sending core
   
   The prime current does not reverse any flux in a cleared core.

3) Drive (or clear) sending core
   
   Neither of these currents will alter the flux distribution of a cleared core.

4) Prime receiving core
   
   The prime current causes only local switching about legs 3 and 4.

5) Drive (or clear) receiving core
   
   Either interrogation signal will result in an output from the receiving core. Drive will have no effect on the coupling loop but clear will induce an opposing current in the loop. This opposing current will not tend to set the sending core but will, of course, subtract from the net clear current.

Case two -- sending core set to one

As a starting condition the sending core is set to one but not primed; the receiving core is cleared.

1) Set receiving core to one
   
   As in the previous case, the sending core is driven during the set pulse.
2) Prime sending core

The prime current is small and causes the indicated flux reversal to occur so slowly that the voltage induced in the coupling loop can be neglected.

3) Drive (or clear) sending core

This is the key step of the negation operation. Note that while the coupling loop links the entire right core, the loop current that results from this step causes a flux reversal in only part of the receiving core. In fact, the quantity of flux reversed is the same in the two cores. The 2:1 coupling loop ratio is necessary only to compensate for coupling loop losses, just as it was in the basic transfer circuit.

No output voltage is induced in the receiving core by this step (i.e., there is no flux reversal in leg 4), because the receiving core, while set, had not yet been primed. This is equivalent to saying that the negation circuit enjoys forward isolation.

4) Prime receiving core

No flux reversals result from priming a cleared core.

5) Drive (or clear) receiving core

No flux reversals result from driving a cleared core.

II.6 The XY Transfer Circuit

Even more useful than the negation circuit is the XY transfer circuit shown (in part) in figure 14. It is, of course, a simple voltage cancellation scheme with the single coupling loop oriented so that core X tends to set the right hand core and core Y opposes that action. Only the nondestructive mode of operation will be discussed in this section, the extension of the arguments to the destructive case being generally obvious.
FIGURE 14. XY TRANSFER CIRCUIT
A peculiarity of this circuit is that while the drive current is common to both sending cores, the prime winding threads only core X. The necessity of this will be demonstrated after the various input combinations are discussed.

\[ X = 1, \quad Y = 1 \]

During the prime pulse, the flux reversal in leg 4 of X induces a current in the coupling loop. This loop current passes through core Y in the prime direction and can easily be made large enough to prime Y. Thus, because of the orientation of the coupling loop, both cores are primed by the prime winding threaded through X alone. (During the prime pulse the loop current enters the receiving core in the inhibit direction, consequently the state of the receiving core is unaffected.)

During the drive pulse the output voltages of X and Y cancel with resultant zero loop current. The requirements for cancellation are that the two sending cores have the same magnetic structure and that they are simultaneously subjected to the same net drive.

\[ X = 1, \quad Y = 0 \]

Again, coupling loop current will be induced during prime time. This induced current is not so large that there is any danger of spuriously setting core Y.

During the drive pulse, current will flow in the coupling loop in a direction to set the receiving core. Note that the loop current adds to the net drive of Y while subtracting from the net drive of X.

\[ X = 0, \quad Y = 1 \]

No coupling loop current flows during prime time for this case since core X is unaffected by the prime pulse. Thus the prime pulse leaves X still
cleared and Y unprimed. Both of these states (cleared and unprimed) yield zero output when driven so that no loop current results during drive.

\[ X = 0 \quad Y = 0 \]

In this case neither core is primed and neither core has an output during the drive pulse.

To show the necessity of priming only X consider again the second case, where \( X = 1 \) and \( Y = 0 \). We have shown that the coupling loop provides a current in the prime direction through Y at prime time. If a prime current (from the same source as the prime for X) were added to this, the net prime would be so large as to spuriously set Y.

The XY transfer circuit retains the three major properties of the basic transfer circuit: forward and backward isolation and the gating facility.

II.7 The Half Adder

The half adder (figure 15) is obtained by making a very slight change in the coupling loop of the XY transfer circuit. To obtain the half adder function both X and Y must be primed. This is a short way of saying that current must pass through the output apertures in a direction which would prime them if they were set. It is not possible to prime X and Y simultaneously since, as was shown, some combinations of information in X and Y would result in spurious setting. X and Y are therefore primed consecutively. This may result in a core being subjected twice to a priming current, once from the coupling loop and again from the clock source, but this is equivalent to a prime pulse of longer duration and is not logically significant.

During the driving pulse if X and Y are in the same state there will be voltage cancellation and no loop current. If X and Y differ, the resulting loop current will be in the set direction through one of the inputs of the
FIGURE 15. THE HALF ADDER

Transfer functions:
- $X \oplus Y$
- $XY$
- $\bar{X}Y$
- $XY$
- $\bar{X}Y$
receiving core. Either or both of these inputs may be inhibited but there are more attractive ways of achieving the same end. Suppose, for example, that the desired transfer function is $XY$ rather than $X \oplus Y$. This can be obtained by inhibiting the set input of the receiving core during the drive pulse. It can also be obtained by simply omitting the prime $Y$ pulse with a consequent saving in time.

If we prime $X$ and at the same time antiprime the output aperture of $Y$ two things are certain. $X$ will be primed and $Y$ will not. The drive pulse that follows will then transfer the contents of $X$ to the receiving core. This is a useful variation on the $XY$ circuit where we have guaranteed that the output of $Y$ will be zero during drive. Under these conditions the output of $Y$ is called a pseudo zero output since it does not depend on the binary state of the core.

In a somewhat similar manner it is possible to transfer $\bar{X}$. This requires $Y$ to be set to one before driving (most conveniently, by means of overprime set). The rather severe limitation of this scheme is that the information in $Y$ is destroyed in the process.

The half adder is an excellent example of the logical flexibility that is possible in magnetic circuits. By the selection of appropriate clock pulses a total of seven different transfer functions can be obtained in a circuit with simple, fixed wiring.

II.8 Multiple Output Circuits

It was mentioned earlier that the basic transfer circuit can be modified (by increasing the turns ratio) to provide a simultaneous fanout of two or more. The two circuits discussed in this section are examples of alternative methods of securing greater fanout.
The first of these circuits (shown in figure 16) has two output windings and is to be interrogated destructively. With the exception of prime, the operation of this circuit parallels that of the basic circuit. Both output apertures must be primed. They cannot be primed simultaneously with the usual prime current as this would spuriously set a cleared core. Specifically, both prime currents lie within the flux reversal path 1647. For a cleared core this is a permissible path and while a single prime does not exceed the threshold for 1647, two primes together will. (To speed the prime operation, prime current is usually close to the maximum permissible value.) The two output apertures must be primed in sequence although this nearly doubles the operating time, largely defeating the purpose of multiple output.

A second limitation of this circuit is that the two output circuits are not really isolated. Although physically separate they share flux reversal path (1647 again) during the clear operation. Thus, the loop current of one output subtracts from the net clear of both. This makes it impractical to have either output winding connected to a single input which can be inhibited. An inhibited input winding would virtually short circuit both outputs.

The sole advantage of the circuit of figure 16 is that it reduces the number of turns in an output aperture. The clear current must be just as large as if the two output windings occupied the same hole.

The second multiple output circuit (shown in figure 17) features three isolated output windings and is read nondestructively.

In circuits using multiple simultaneous currents, subtle questions arise, questions which cannot be answered with the simple theory of minimum path length. This is essentially the case here for the drive current. A simplified explanation, useful in analyzing subsequent logical networks, can be made from the basic assumptions. A more comprehensive theory of multipath switching is included in Chapter V.
FIGURE 16. DOUBLE OUTPUT CIRCUIT
Set—As shown

Prime—Prime
output apertures
in sequence

Drive—Drive output
apertures
simultaneously

After set

After prime

After drive

FIGURE 17. TRIPLE OUTPUT CIRCUIT
Each of the drive currents, if applied alone, would cause flux reversal in just two legs. That is, the output circuits would be isolated if interrogated individually. When all three drives are applied simultaneously, six legs switch but in three separate pairs rather than in one long path. Paths 56, 34, and 78 switch at individual rates (depending on the net drive for each) rather than path 548736 switching uniformly. This is important if any of the outputs are used in \( XY \) transfer circuits where net drive must be specified. The isolation between output windings also allows them to be used with inhibited inputs, unlike the circuit of figure 16.

If a particular application requires that a multiple output circuit be interrogated destructively the \textit{pseudo-destructive} read can be used. This consists of a drive pulse followed immediately by a clear pulse. The drive effects the transfer (with the output windings isolated from each other) and the clear pulse resets the core without inducing voltages in any of the input or output windings.

II.9 \textbf{Loading}

The loading effect of a coupling loop on the output of a transfluxor can usually be characterized in one of four ways.

The \textit{unit load} refers to the normal case where the output of a core is used to set one core. The output voltage equals the \( \frac{d\psi}{dt} \) of the receiving core plus the IR drop of the loop. The inductance of the loop can nearly always be neglected.

The \textit{short circuit load} refers to the case where the output is connected to an inhibited input or a series of inputs, all inhibited. The output voltage is absorbed entirely in the IR drop.
The open circuit load occurs only in XY and similar transfer circuits using voltage cancellation. Open circuit load is equivalent to zero loop current.

The reverse load likewise occurs only in cancellation circuits. When the loop current flows in a direction to aid the drive current this will be called a reverse load.
CHAPTER III. LOGICAL NETWORKS

III.1 A Two Dimensional Shift Register

Using the catalog of magnetic circuits developed in the preceding chapter we now proceed to the design of logical networks. The first of these, the two-dimensional shift register, forms an important part of the pattern recognition computer. In this register, an entire field of digits can be translated, in parallel, in any of four directions.

In many respects the organization of a two-dimensional shift register is similar to that of a conventional linear shift register. There must be two memory elements for each bit shifted and means of gating information between the two sets of memory elements. (In the general case only one of the two memory elements must be an explicit memory element; the other can be temporary storage in a capacitor. Capacitor storage or one-core-per-bit designs are not considered here.)

In figure 18, squares marked $S$ represent the memory elements of the main register and squares marked $S^*$ represent the auxiliary (aux) register. Explicit representation of the gating elements is not necessary for simple, iterated logical networks of this type. It is sufficient to provide control signals such as "transfer up-right" which would enable all transfer paths represented by arrows pointing upward and to the right. Strictly speaking, with transfluxors we do not "enable" a desired path; we inhibit all undesired transfer paths.

Assume as a starting condition that the information is held in the main register, the aux register is cleared and single gating is to be used. Shifting to the right (for example) is accomplished by

1. transferring information from the main register upward and to the right to the aux register,
FIGURE 18. LOGICAL ORGANIZATION OF A TWO DIMENSIONAL SHIFT REGISTER
2. clearing the main register,
3. transferring information from the aux register downward and to the right to the main register and
4. clearing the aux register.

The four possible shift directions are summarized schematically in figure 19.

The realization of this two-dimensional shift register with transfluxors is straightforward. The elements of both main and aux registers are basic transfluxor circuits used in the destructive mode. Figure 20 shows the wiring for the coupling loops only, since the clock wiring can be conveniently tabulated.

The example given (of a right shift) would be accomplished in this circuit by the following sequence of clock signals. Assume as a starting condition that the information is in S, primed and that $S^*$ is cleared.

- **Clear S**
- **Inhibit $S^*$**
- **Prime $S^*$**
- **Antiprime $S^*$**
- **Antiprime $S^*$**

The S register is destructively interrogated by a clear pulse applied to every $S_5$ aperture. During this clear pulse every $S^*_2$ aperture is inhibited, which has the practical effect of short circuiting that part of every coupling loop linking $S^*_2$. Thus, the output of every $S$ core is steered upward and to the right to the uninhibited $S^*_4$ input. In terms of the logical diagram of figure 18, the use of this inhibit removes all arrows pointing downward and to the left. Note that while every $S^*_2$ aperture is inhibited, this does not prevent $S^*$ cores from being set through the $S^*_4$ apertures.

The prime signal must precede every interrogation. The antiprime prevents back propagation in the step to follow.
FIGURE 19. SHIFT DIRECTIONS

Left shift

Right shift

From shift

To shift
FIGURE 20. TRANSFLUXOR WIRING FOR 2D SHIFT REGISTER
Clear S* \{ This transfers the contents of the S* register downward
Inhibit S4 \{ and to the right.

Prime S3 \{ At the conclusion of this clock time both registers are
Antiprime S2 \{ in the starting condition except, of course, for the informa-
+ Antiprime S4 \{ tion being shifted one place to the right.

In the second clock pulse, the antiprime S*4 signal was necessary to
prevent back propagation when S* was cleared. The antiprime S*2 signal, on
the other hand, was applied to the S*2 aperture, which could not have been
set in the preceding step. Since S*2 was not set, there is no danger of back
propagation from this aperture and the antiprime S*2 signal is, strictly
speaking, unnecessary. Application of an antiprime signal to an aperture
that has not been set does not result in flux reversals in the core. In
short, the antiprime S*2 signal is unnecessary but harmless.

For a right shift, neither of the two clock signals marked + serves any
logical purpose. Their use here is defended on the grounds that if both
inputs are always antiprimed during the prime pulse then it will be un-
necessary to select the input to antiprime. This simplifies the control
logic without in any way affecting the information in the register. The
direction of shifting is then determined solely by the choice of inhibit
signals in clock times one and three.

III.2 The Bubble Register

One of the operations required in pattern recognition data processing
is a count of "ones" held in a register. Two methods are generally used to
accomplish this function in a general purpose machine. The simplest method,
at least conceptually, is to shift the contents of the register and count
the ones as they emerge. Another procedure is to decode the contents of
the register by combinatorial circuitry. This second method, while generally
faster, has limited usefulness since the decoding equipment is extremely
complex for all but very short registers. Neither of these methods is well
adapted to all-magnetic logic because of the fanout required.

The bubble register represents a third approach to this problem, an
approach governed both by the limitations and the advantages of all-magnetic
logic. The logic of this design could, of course, be realized by other means,
such as by transistors.

The bubble register is a "self-ordering" register, a register in which
a fixed number of identical operations will order the contents of the
register so that all ones are at one end of the register, all zeros at the
other end. For many applications this ordering is equivalent to the counting
operation.

III. 3 Description of Bubbling

For a physical picture of the bubbling process consider a vertically
oriented linear register containing mixed ones and zeros. Examine all ad-

djacent pairs of digits and replace every 0 pair by a 1 pair. All other
digits remain unchanged. Clearly this operation neither creates nor destroys
ones but does tend to move ones to the top. For an N-bit register a maximum
of N-1 such operations are required to completely order the information.

Figure 21 shows an example of bubbling in which four operations
completely order the register. Subsequent operations do not change the
register so it is not necessary to sense the completion of ordering. The
register is shown oriented vertically to strengthen the analogy that ones
are bubbles moving to the top, hence the term "bubbling."
FIGURE 21. SUCCESSIVE STEPS IN THE BUBBLING PROCESS
The derivation of logical functions from this pictorial description is straightforward and yields the following expressions for a register of length $N$:

$$X'_1 = X_1 \lor X_2$$

$$X'_k = X_{k-1} X_k \lor \overline{X}_{k} X_{k+1} \quad (\text{for } k = 2, 3\ldots, N-1) \quad (1)$$

$$X'_{N} = X_{N-1} X_{N}$$

In words, each operation replaces every bit by a function of that bit and its nearest neighbors. The functions have been specified here so that ones will gravitate to the $X_1$ end of the register.

For the remainder of this paper a somewhat neater terminology will be used. The greater compactness of this "ABC notation" should more than compensate for any lack of mathematical elegance. Restated in this notation expression (1) is:

$$\text{top} \quad B' = B \lor C$$

$$\text{all interior} \quad B' = AB \lor \overline{BC} \quad (2)$$

$$\text{bottom} \quad B' = AB$$

where $B$ is any register position and $A$ and $C$ are adjacent positions ($A$ above and $C$ below).

Figure 22 is a highly simplified logical diagram of a short, complete bubble register. A register of four bits is sufficiently long to show the difference between interior stages and the end stages. The simplification in the drawing results from the omission of gating signals and the use of certain other conventions explained below.

Each square represents a single-gated storage element with from one to three identical outputs. Each of these elements can be set to a one by any input (arrowhead) and set to zero by a clear signal not shown. With the
FIGURE 22. LOGICAL DIAGRAM OF A FOUR DIGIT BUBBLE REGISTER
exception of \( X \), the central column of storage elements will be referred to collectively as the principal or "P" register; the auxiliary registers at either side will be designated \( L \) and \( R \).

As a starting condition assume that the information to be processed is held in \( P \) and \( X \) and that \( L \) and \( R \) are cleared. A single bubble operation is described by the following four steps:

1) single gate contents of \( P \) into \( L \)
   single gate contents of \( \overline{P}, \overline{X} \) into \( R \)
2) clear \( P \) (but not \( X \))
3) single gate \( f(L,R) \) into \( P \) and \( X \)
4) clear \( L \) and \( R \)

III.4 Operations of the Transfluxor Bubbler

The logical diagram of figure 22 can be thought of as a "solution" to (2) with the constraint that the logical circuits within it be realizable with all-magnetic logic. The wiring in figure 23 shows the interconnection of the various magnetic circuits described in Chapter II to form a transfluxor bubbler. Again, only coupling loops are shown since the clock wiring is more conveniently listed in tabular form.

A simplified explanation of bubbler operation will be given here with a more detailed analysis being deferred to Chapter V. This delayed development will permit the introduction of engineering modifications which, while important in improving circuit performance, do not change the logical properties of the bubbler.

Assume as a starting condition that the information is in \( P \) and \( X \), primed, that \( L \) is cleared and that \( R \) is set but not primed.
FIGURE 23. COUPLING LOOP WIRING FOR TRANSFLUXOR BUBBLE REGISTER
Coupling loop $W$ transfers $\bar{X}$ into the upper core of the $R$ register, that is, if $X$ is one, $R$ is cleared at this time. This is the negation circuit of section II.5.

Except for the lower digit of $P$, a one in any $P$ core will cause a loop $Z$ current in the direction shown. This current will set the associated $L$ core and at the same time clear the associated $R$ core. Thus, loop $Z$ ties $L$, $P$ and $R$ together in a combination basic transfer and negation circuit. Note that the $Z$ coupling loop ratio is sufficient to permit this simultaneous fanout of two.

The lower digit of $P$ is transferred to the associated $L$ core with the basic transfer circuit.

This prepares $L$ and $R$ for the interrogation to follow.

Loop $Y$ is part of an $XY$ transfer circuit. Current will flow in the indicated direction only if the lower $L$ core (of the two $L$ cores linked by loop $Y$) contains a one and the upper $L$ core is cleared. This means that any principle register core, $B$, will be set if $\bar{B}C = 1$.

Loop $T$ is also part of an $XY$ transfer circuit. Current will flow in the indicated direction if the $L$ core contains a one and the $R$ core is cleared. Recall here that the $R$ core holds complemented information. Thus, loop $T$ transfers the function $AB$ to the $P2$ input of core $B$ in the principle register.
III.5 Other Operations

Table 1 lists six additional operations that can be done in the bubble register by using different clock pulse sequences. Two of these operations are conventional (shift up and shift down) and require little explanation. The other operations do not have any parallel in conventional computer designs. They will be described briefly in terms of their effect on the pattern of digits in a register. The work "pattern" is emphasized because the contents of a register will rarely be interpreted as a binary number.

In general, all the operations performed in the bubbler are defined by the effect of the operation on an interior digit of the register. Where this relationship (e.g., $B' = AB \lor BC$ for bubble) does not hold for the upper or lower digit of a register, it is so noted in the table. Later, when the bubbler is connected to other logical networks, these end functions may change. As far as possible, the seven operations have been made similar to simplify the control logic. All of the operations start from, and end in a standard condition so that any operation may follow any other operation.

III.6 Contract and Expand

The contract operation ($B' = AB$) is so called because it removes the upper one from every group of ones, thus shortening or contracting the group.
<table>
<thead>
<tr>
<th>Operation</th>
<th>Code</th>
<th>Top</th>
<th>Interior</th>
<th>Bottom</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bubble</td>
<td>B</td>
<td>BV C</td>
<td>AB v BC</td>
<td>AB</td>
</tr>
<tr>
<td>Shift Up</td>
<td>U</td>
<td>C</td>
<td>C</td>
<td>0</td>
</tr>
<tr>
<td>Shift Down</td>
<td>D</td>
<td>0</td>
<td>A</td>
<td>A</td>
</tr>
<tr>
<td>Contract</td>
<td>C</td>
<td>B</td>
<td>AB</td>
<td>AB</td>
</tr>
<tr>
<td>Expand</td>
<td>E</td>
<td>BV C</td>
<td>BV C</td>
<td>B</td>
</tr>
<tr>
<td>Group Count</td>
<td>G</td>
<td>BV C</td>
<td>BC</td>
<td>0</td>
</tr>
<tr>
<td>Complement (Negate)</td>
<td>N</td>
<td>B</td>
<td>B</td>
<td>B</td>
</tr>
</tbody>
</table>

**TABLE 1. BUBBLE REGISTER OPERATIONS**
("Group" here means a contiguous group of ones bounded by zeros on either side.) A single contract operation removes all isolated ones; N successive operations will remove all groups of length N or less.

The expand operation adds a one to the top of each group of ones, by itself not a very exciting result. However, the sequences of operations C, E (contract followed by expand) removes all isolated ones while leaving the pattern otherwise unchanged. The sequence $C^2E^2$ (two contracts followed by two expands) removes isolated ones and isolated pairs of ones. The sequence $E^2C^2$ fills in all gaps of length one and two.

The EC and CE family of operations can be thought of as removing the fine detail from the pattern. Other interpretations are possible, depending on the physical significance of the pattern.

III.7 Group Count and Complement

The group count operation, G, replaces every group of ones with a single one. The single one appears one digit above the upper one of the associated group.

The complement operation, N, replaces the contents of the register with the digit-wise complement, except for the upper digit. The complement is important because of its use in subroutines. As an example, K-l bubble operations, $B^{K-1}$, will completely order a register at length K, with ones at the top. The sequence (or subroutine) $N, B^{K-1}, N$ will similarly order the information but with ones at the bottom.* It is certainly easier to program the direction of bubbling than it is to design a register that will bubble either direction.

* The expression $N, B^{K-1}, N$ ignores for the moment the end digit which is not complemented.
CHAPTER IV. THE PATTERN RECOGNITION UNIT

IV.1 Introduction

We start by calling attention to the distinction between the pattern recognition computer (the overall system) and the pattern recognition unit or PRU. The function of the PRU in the total system is roughly analogous to that of the arithmetic unit in a conventional digital computer. Figure 24, showing the division of functions in the two types of computers is, of course, a simplification.

Very little will be said here about the control computer. In principle it could be designed with all magnetic logic but in practice the logical and engineering problems that would result militate against this approach. Magnetic logic is best adapted to large iterative networks of limited fanout. Briefly then, the control computer is of conventional design, supplies control (clock) signals to the PRU and interrogates the PRU before conditional transfer orders. A memory of conventional design is included as part of the control computer.

Often, in order to make the explanation of a PRU operation meaningful, it will be necessary to refer to a specific recognition problem. The specific problem so cited will sometimes be, the interpretation of nuclear bubble chamber photographs, since it was this problem that provided the original motivation for the machine design. At other times, the recognition of alphabetical characters will be used to facilitate the explanation of the order code. Conceivably the PRU design has been biased in favor of the bubble chamber problem although the unit is not restricted to this problem. The examples of pattern processing given will, of necessity, tend to be trivial since useful recognition routines will require programs of considerable length.
GENERAL PURPOSE COMPUTER

Control

Memory

Arithmetic unit

PATTERN RECOGNITION COMPUTER

Control computer

Pattern recognition unit

FIGURE 24. COMPUTER ORGANIZATION
Because the PRU is presented as a practical (although primitive) design, we take note here of the constrains on the fabrication technique.

1) The PRU should be constructed of an iterative array of identical modules.
2) Construction should be by planes, i.e., three dimensional wiring should be minimized.
3) The number of control lines should be related to the flexibility of the order code and independent of the register size.

These constraints are met with reasonable success in the transfluxor design given here. More advanced designs using integrated semiconductor circuits, cryogenics, or evaporated magnetic films will, in general, be subject to the same constraints. Of these techniques, the evaporated magnetic film technique (Appendix B) in particular appears promising.

IV.2 General Organization

The general organization of the PRU is suggested by figure 25. The S register is an N x N horizontal 2D shift register which is used for input and other functions not easily classified. Since the PRU is constructed of all-magnetic circuitry, every signal line connecting the PRU with nonmagnetic equipment (control computer, input device) involves either a read amplifier or a write driver. Because \( N^2 \) is very large in the projected design, it is undesirable to provide a write driver for every bit in S. If S were modified slightly to include circular edge connections, it would be possible to load S from one corner. However, it is equally undesirable to load the register one bit at a time because of the time that this would require. The best compromise for N large is to load one line at a time, hence the pattern to be processed will be loaded into one edge of S and the information shifted across.
FIGURE 25. ORGANIZATION OF PATTERN RECOGNITION UNIT
Suspended from every location in S is a bubble-register of length R. Thus, there are $N^2$ bubble registers unconnected to each other aside from common clock wiring. Sole connection between any bubble register and the rest of the PRU is through the topmost or X digit. Collectively the X digits make up the X plane or register which corresponds very approximately to the accumulator in a conventional machine.

Above every location in S is a linear register of length K, circularly connected and with bi-directional shifting facility. Each of these registers is connected to the rest of the unit through one digit, M, the digit physically nearest the S plane. Since the registers are controlled from a common clock source it is convenient to think of this array as a K-word memory with $N^2$ bits per word. Unlike most serial memories, the search operation can proceed in either direction. This, together with the small size of K (say 32 or 64), will keep the access time reasonable compared to other operation times.

The memory unit is used principally for storage of intermediate results but also for storage of multiple input patterns. The latter occur in the digital cross-correlation of strongly correlated patterns such as successive television frames or corresponding areas from alternate stereo views.

A more precise guide to the interconnection of the various parts of the PRU is shown in figure 26. In fact, the PRU is merely $N^2$ identical modules of the type shown. The only interconnection between modules is through S and $S^*$, the main and aux cores associated with one register location in the S plane. This limited interconnection is important in terms of facilitating construction. The functions of W, Y and Z are discussed in Section IV.3.

Figure 27 shows the connection between one module and the associated pair in the S plane. It has been necessary to modify the 2D shift register from the design given in Chapter III. The previously unused input aperture
FIGURE 26. ONE MODULE OF PRU
FIGURE 27. MODULE--S PLANE CONNECTION
of the aux core has become line A of figures 26 and 27. The unused minor aperture of the main core now serves as a nondestructive output aperture (line B).

To prevent information from being lost off the edges of the S register during shifting, a guard ring G digits wide is provided. This means the 2D register is actually \((N + 2G) \times (N + 2G)\) in size rather than \(N \times N\) as originally stated. We will still refer to the \(N^2\) bits of S, however, since we restrict the S register to mean the interior part of the larger shift plane. The digits in the guard ring are used only to prevent overflow; they have neither associated bubble registers nor memory registers. Since the guard ring digits do not communicate with either the rest of the PRU (except at the boundary of S) or with external equipment, they do not appear in the order code.

IV.3 Order Code

Most of the orders listed in table 2 have been discussed in preceding sections. Note that the memory orders are used only to index the memory, that is, to circularly shift the memory registers until the desired word resides in the M plane. Writing into M and reading from M are accomplished by transfer orders. A transfer order is any order used to transfer information between the three major divisions of the PRU. The use of three extra registers, W, Y, and Z, allows us to place complementing gates in all the major transfer paths. The resulting multitude of orders is listed in tables 3, 4, 5 and 6.

Consider, as an example, the \(X_{12}\) order \((X' = (M \oplus S) \lor X)\) listed in table 3. The simplified sequence of this order is as follows:

1) Clear Z and Y but not X (X and W are inhibited to make this a "clear-without-transfer.")
<table>
<thead>
<tr>
<th>MEMORY ORDERS</th>
<th>( v^+k )</th>
<th>( k ) VERTICAL SHIFTS UP</th>
</tr>
</thead>
<tbody>
<tr>
<td>( v^-k )</td>
<td></td>
<td>( k ) VERTICAL SHIFTS DOWN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>S PLANE ORDERS</th>
<th>L</th>
<th>LEFT SHIFT</th>
</tr>
</thead>
<tbody>
<tr>
<td>R</td>
<td>RIGHT SHIFT</td>
<td></td>
</tr>
<tr>
<td>T</td>
<td>TO SHIFT</td>
<td></td>
</tr>
<tr>
<td>F</td>
<td>FROM SHIFT</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BUBBLER ORDERS</th>
<th>B</th>
<th>BUBBLE ONES UPWARD</th>
</tr>
</thead>
<tbody>
<tr>
<td>U</td>
<td>UP SHIFT</td>
<td></td>
</tr>
<tr>
<td>D</td>
<td>DOWN SHIFT</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>BUBBLER ORDERS</th>
<th>C</th>
<th>REMOVE TOP ONE FROM EACH GROUP OF ONES</th>
</tr>
</thead>
<tbody>
<tr>
<td>E</td>
<td>EXPAND</td>
<td></td>
</tr>
<tr>
<td>G</td>
<td>GROUP COUNT</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>COMPLEMENT</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TRANSFER ORDERS</th>
<th>( x_n )</th>
<th>( X ) REPLACED BY SOME ( f(Y,S,M,X) ) SPECIFIED BY ( n )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( m_n )</td>
<td>( M^* ) REPLACED BY SOME ( f(Y,S,M^*,X) ) SPECIFIED BY ( n )</td>
<td></td>
</tr>
<tr>
<td>( y_n )</td>
<td>( Y ) REPLACED BY SOME ( f(Y,S,M,X) ) SPECIFIED BY ( n )</td>
<td></td>
</tr>
<tr>
<td>( s_n )</td>
<td>( S ) REPLACED BY SOME ( f(Y,S,M,X) ) SPECIFIED BY ( n )</td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 2. PRU ORDERS**
<table>
<thead>
<tr>
<th>X REPLACED BY</th>
<th>INFORMATION DESTROYED IN</th>
<th>EXECUTION TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0</td>
<td>Y</td>
<td>1</td>
</tr>
<tr>
<td>2 1</td>
<td>Y</td>
<td>1</td>
</tr>
<tr>
<td>3 S</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>4 $S$</td>
<td>Z,Y</td>
<td>2</td>
</tr>
<tr>
<td>5 $S v X$</td>
<td>Z,Y</td>
<td>2</td>
</tr>
<tr>
<td>6 $\overline{S} v X$</td>
<td>Z,Y</td>
<td>2</td>
</tr>
<tr>
<td>7 $M$</td>
<td>Z,Y</td>
<td>3</td>
</tr>
<tr>
<td>8 $M\oplus S$</td>
<td>Z,Y</td>
<td>4</td>
</tr>
<tr>
<td>9 $\overline{MS}$</td>
<td>Z,Y</td>
<td>3</td>
</tr>
<tr>
<td>10 $MS$</td>
<td>Z,Y</td>
<td>3</td>
</tr>
<tr>
<td>11 $M v X$</td>
<td>Z,Y</td>
<td>3</td>
</tr>
<tr>
<td>12 $(M\oplus S) v X$</td>
<td>Z,Y</td>
<td>4</td>
</tr>
<tr>
<td>13 $\overline{MS} v X$</td>
<td>Z,Y</td>
<td>3</td>
</tr>
<tr>
<td>14 $MS v X$</td>
<td>Z,Y</td>
<td>3</td>
</tr>
<tr>
<td>15 $S\oplus X$</td>
<td>Z,Y</td>
<td>5</td>
</tr>
<tr>
<td>16 $S\oplus \overline{X}$</td>
<td>Z,Y</td>
<td>5</td>
</tr>
<tr>
<td>17 $S\overline{X}$</td>
<td>Z,Y</td>
<td>4</td>
</tr>
<tr>
<td>18 $\overline{S}\overline{X}$</td>
<td>Z,Y</td>
<td>4</td>
</tr>
<tr>
<td>19 $\overline{S}X$</td>
<td>Z,Y</td>
<td>4</td>
</tr>
<tr>
<td>20 $\overline{S}X$</td>
<td>Z,Y</td>
<td>4</td>
</tr>
<tr>
<td>21 $X$</td>
<td>Z,Y</td>
<td>4</td>
</tr>
</tbody>
</table>

**TABLE 3. X TRANSFER ORDERS**
<table>
<thead>
<tr>
<th>M*</th>
<th>REPLACED BY</th>
<th>INFORMATION DESTROYED IN</th>
<th>EXECUTION TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>Y</td>
<td>1</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>3</td>
<td>X</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>X</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>X + Y</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>XY</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>XY</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>8</td>
<td>X v M*</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>9</td>
<td>X v M*</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>10</td>
<td>(X + Y) v M*</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>11</td>
<td>XY v M*</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>12</td>
<td>XY v M*</td>
<td>Y</td>
<td>2</td>
</tr>
<tr>
<td>13</td>
<td>S + X</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>14</td>
<td>S + X</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>15</td>
<td>SX</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>16</td>
<td>S X</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>17</td>
<td>S X</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>18</td>
<td>S X</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>19</td>
<td>S</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>20</td>
<td>S</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>21</td>
<td>(S + X) v M*</td>
<td>Y</td>
<td>4</td>
</tr>
<tr>
<td>22</td>
<td>(S + X) v M*</td>
<td>Y</td>
<td>4</td>
</tr>
<tr>
<td>23</td>
<td>SX v M*</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>24</td>
<td>SX v M*</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>25</td>
<td>SX v M*</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>26</td>
<td>SX v M*</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>27</td>
<td>S v M*</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>28</td>
<td>S v M*</td>
<td>Y</td>
<td>3</td>
</tr>
</tbody>
</table>

**Table 4. M Transfer Orders**
<table>
<thead>
<tr>
<th>Y REPLACED BY</th>
<th>INFORMATION DESTROYED IN</th>
<th>EXECUTION TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 0</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>2 1</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>3 s</td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>4 s</td>
<td>Z</td>
<td>1</td>
</tr>
<tr>
<td>5 s v Y</td>
<td>Z</td>
<td>1</td>
</tr>
<tr>
<td>6 s v Y</td>
<td>Z</td>
<td>1</td>
</tr>
<tr>
<td>7 m</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>8 m</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>9 M+ s</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>10 M s</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>11 M s</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>12 M v Y</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>13 M v Y</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>14 (M+ s) v Y</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>15 M s v Y</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>16 M s v Y</td>
<td>Z</td>
<td>2</td>
</tr>
<tr>
<td>17 s+ x</td>
<td>Z</td>
<td>4</td>
</tr>
<tr>
<td>18 s+ x</td>
<td>Z</td>
<td>4</td>
</tr>
<tr>
<td>19 s x</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>20 s x</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>21 s x</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>22 s x</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>23 (s+ x) v Y</td>
<td>Z</td>
<td>4</td>
</tr>
<tr>
<td>24 s x v Y</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>25 s x v Y</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>26 x</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>27 x</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>28 x v Y</td>
<td>Z</td>
<td>3</td>
</tr>
<tr>
<td>29 x v Y</td>
<td>Z</td>
<td>3</td>
</tr>
</tbody>
</table>

**TABLE 5. Y TRANSFER ORDERS**
<table>
<thead>
<tr>
<th>S REPLACED BY</th>
<th>INFORMATION DESTROYED IN</th>
<th>EXECUTION TIME</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>Y</td>
<td>1</td>
</tr>
<tr>
<td>2.1</td>
<td>Y</td>
<td>1</td>
</tr>
<tr>
<td>3.X</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>4.\overline{X}</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>5.X \lor S</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>6.\overline{X} \lor S</td>
<td>Y</td>
<td>3</td>
</tr>
<tr>
<td>7.X \lor Y</td>
<td>Y</td>
<td>4</td>
</tr>
<tr>
<td>8.X \overline{Y}</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>9.\overline{X} \overline{Y}</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>10. (X \lor Y) \lor S</td>
<td></td>
<td>4</td>
</tr>
<tr>
<td>11.X \overline{Y} \lor S</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>12.\overline{X} \overline{Y} \lor S</td>
<td></td>
<td>3</td>
</tr>
<tr>
<td>13.X \lor S</td>
<td>Y</td>
<td>5</td>
</tr>
<tr>
<td>14.X \lor \overline{S}</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>15.XS</td>
<td>Y, Z</td>
<td>4</td>
</tr>
<tr>
<td>16.X\overline{S}</td>
<td>Y</td>
<td>4</td>
</tr>
<tr>
<td>17.\overline{X}S</td>
<td>Y</td>
<td>4</td>
</tr>
<tr>
<td>18.\overline{X}\overline{S}</td>
<td>Y, Z</td>
<td>4</td>
</tr>
<tr>
<td>19.S \lor M \lor X</td>
<td>Y, Z</td>
<td>7</td>
</tr>
<tr>
<td>20.SM \lor X</td>
<td>Y, Z</td>
<td>6</td>
</tr>
<tr>
<td>21.\overline{S}M \lor X</td>
<td>Y, Z</td>
<td>6</td>
</tr>
<tr>
<td>22.SM X</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>23.\overline{S}MX</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>24. (\overline{S} \lor M)X</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>25.(S \lor \overline{M})X</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>26.S \lor M</td>
<td>Y, Z</td>
<td>6</td>
</tr>
<tr>
<td>27.SM</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>28.\overline{S}M</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>29.M \lor S</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>30.M</td>
<td>Y, Z</td>
<td>5</td>
</tr>
<tr>
<td>31.\overline{M}</td>
<td>Y, Z</td>
<td>5</td>
</tr>
</tbody>
</table>

**TABLE 6. S TRANSFER ORDERS**
2) \( M \rightarrow Z \)
3) \( (Z \oplus S) \rightarrow Y \)
4) \( Y \rightarrow X \)

(This is interpreted as "contents of \( Y \) transferred to \( X \)," not "\( X \) replaced by \( Y \)." In magnetic logic all transfers are of necessity single gated.)

All of the \( X_n \) orders of the third group (\( X_7 \) through \( X_{14} \)) are merely variations of this sequence. In a sense, the \( X_{12} \) order could be called the basic order of the third \( X \) group, although the programmer is unlikely to so regard it.

Table 7 shows the required modifications in the transfer sequence.

<table>
<thead>
<tr>
<th>( X )</th>
<th>( X' )</th>
<th>Modification</th>
</tr>
</thead>
<tbody>
<tr>
<td>( X_7 )</td>
<td>( X' = M )</td>
<td>clear ( X ) in step 1</td>
</tr>
<tr>
<td>( X_7 )</td>
<td>( X' = \text{M} \oplus S )</td>
<td>clear ( X ) in step 1, pseudo zero from ( S ) in step 3</td>
</tr>
<tr>
<td>( X_9 )</td>
<td>( X' = \overline{M}S )</td>
<td>clear ( X ) in step 1, omit prime ( M ) before step 3</td>
</tr>
<tr>
<td>( X_{10} )</td>
<td>( X' = MS )</td>
<td>clear ( X ) in step 1, omit prime ( S ) before step 3</td>
</tr>
<tr>
<td>( X_{13} )</td>
<td>( X' = \overline{M}S \lor X )</td>
<td>pseudo zero from ( S ) in step 3, omit prime ( M ) before step 3</td>
</tr>
<tr>
<td>( X_{14} )</td>
<td>( X' = MS \lor X )</td>
<td>omit prime ( S ) before step 3</td>
</tr>
</tbody>
</table>

Table 7: Modifications in the Transfer Sequence

Two orders missing from table 3 are \( X' = \overline{M} \) and \( X' = \overline{M} \lor X \). These orders were omitted because they require either shifting or destroying information in the \( S \) register. Their absence should not handicap the programmer since complemented information can be stored in \( M \) from either \( X \) or \( S \).
The orders in tables 3 through 6 are grouped according to transfer paths, all orders within a group using the same transfer paths in the same sequence. Most of the transfers in an order must be preceded by a single prime; the exceptions are "exclusive or" transfers where the operand cores must be primed in sequence. In $X_{12}$, for example, the first transfer, $M \rightarrow Z$, must be preceded by prime $M$; the second transfer, $(Z + S) \rightarrow Y$, must be preceded by prime $Z$ and prime $S$. Execution time for an order is listed as the number of prime pulses required since the prime takes much longer than any of the other clock pulses.

Registers $W$, $Y$ and $Z$ were added to the design so that complementing gates could be used in all the major transfer paths. Register $Y$ also serves a purpose not obvious from the order code. $Y$ can control the lower complementing gate (the one between $X$ and $W$ in figure 26) for an extended series of transfers. If, for example, the contents of the bubbler are to be shifted up and into the memory (with the memory shifting up at the same time and the circular connection, $C$, broken) the transfer path from $X$ to $M$ can be controlled for the entire series. In a similar way, $Z$ can control a series of transfers between $S$ and $X$. "Control" may mean allow-or-inhibit or any mean complement-or-noncomplement depending on the use of the appropriate inhibit signal.

IV.4 Composite Orders

In order to minimize processing time, it is desirable to execute two or more orders simultaneously where possible. This is always possible when the orders refer to different parts of the PRU and are nontransfer orders. This is to say that (for example) bubbler orders and $S$ plane orders can proceed independently of (and hence, concurrently with) each other.

Where transfer orders are involved, the question is more complex. From the list of orders developed thus far, a large number of composite orders
could be proposed. For obvious reasons not all of these combinations could be realized. Even with the logically and technically permissible combinations it is necessary to specify exactly what transfers occur as this is not always clear from the specification of the orders considered separately. For this reason, only a few composite orders having considerable utility are listed in tables 8, 9 and 10.

IV.5 Template

The template routine is a suitable point of departure for examining programing since it can be used to demonstrate a simple type of pattern recognition in a routine of reasonable length. It should be repeated here that the examples of pattern processing in this chapter tend to be trivial, since these serve the purpose of explanation better than complex but useful programs would.

Consider the array of ones and zeros in Figure 28. Required: to find and mark every location on the array where the pattern is exactly that of the template. This is the same as applying the template to every possible location in the array and looking for agreements. In those cases where the template projects beyond the array, the register positions outside of \( i \times j \) are defined as being zero. This means only that the guard ring is initially cleared.

The realization of this task proceeds easily in the PRU. The pattern to be examined is in \( S \); the template information is in the control computer and both PRU memory and bubbler are empty. The sequence of orders for the required template operation is given in table 11. Orders one through nine in table 11 "trace out" the template and load the pattern into the bubbler. At this point, each of the \( N^2 \) bubble registers contains nine digits from the
COMPOSITE ORDER $\ U M_n V^{+k}$

LOAD MEMORY FROM BUBBLER

Bubbler and memory shift up k digits as one register.

Circular connection of memory is broken (inhibit C, figure 26).

Transfer from X to $M^*$ is determined by $M_n$ where $n = 3, 4, 5, 6, 7$. See table 4.

<table>
<thead>
<tr>
<th>MEMORY</th>
<th>TRANSFER NET</th>
<th>BUBBLER</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRANSFER UP RIGHT</td>
<td>$f(X,Y) \rightarrow W$</td>
<td>$P \rightarrow L$</td>
</tr>
<tr>
<td>TRANSFER LEFT</td>
<td>$W \rightarrow M^*$</td>
<td>$L \rightarrow P, X$</td>
</tr>
</tbody>
</table>

TABLE 8. LOAD MEMORY FROM BUBBLER
COMPOSITE ORDER \( V^{-k} X_n D \)

LOAD BUBBLER FROM MEMORY

Bubbler and memory shift down \( k \) digits as one register.

Circular connection of memory is broken (inhibit \( C \), figure 26).

Transfer from \( M \) to \( X \) is determined by \( X_n \) where \( n = 7, 8, 9, 10 \). See table 3.

<table>
<thead>
<tr>
<th>MEMORY</th>
<th>TRANSFER NET</th>
<th>BUBBLER</th>
</tr>
</thead>
<tbody>
<tr>
<td>EXECUTE ONCE</td>
<td>TRANSFER DOWN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RIGHT</td>
<td></td>
</tr>
<tr>
<td>TRANSFER LEFT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M \rightarrow Z</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EXECUTE ( k ) TIMES</td>
<td>TRANSFER DOWN</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RIGHT</td>
<td></td>
</tr>
<tr>
<td>TRANSFER LEFT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f(Z, S) \rightarrow Y )</td>
<td>( X, \bar{F} \rightarrow R )</td>
<td></td>
</tr>
</tbody>
</table>

| TABLE 9. LOAD BUBBLER FROM MEMORY |
COMPOSITE ORDERS  $DX_n^L$, $DX_n^R$, $DX_n^T$, $DX_n^F$

TEMPLATE FORMERS

Logically equivalent to down shift followed by complemented ($n = 4$) or uncomplemented ($n = 3$) transfer from $S$ to $X$ followed by $S$ plane shift.

<table>
<thead>
<tr>
<th>S PLANE</th>
<th>TRANSFER NET</th>
<th>BUBBLER</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S \rightarrow S^*$</td>
<td>$f(S, Z) \rightarrow Y$</td>
<td>$\overline{X}, \overline{F} \rightarrow P$</td>
</tr>
<tr>
<td>$S^* \rightarrow S$</td>
<td>$Y \rightarrow X$</td>
<td>$\overline{R} \rightarrow P$</td>
</tr>
</tbody>
</table>

TABLE 10. TEMPLATE FORMERS
<table>
<thead>
<tr>
<th>ORDER</th>
<th>BUBBLER</th>
<th>TRANSFER</th>
<th>S-PLANE</th>
</tr>
</thead>
<tbody>
<tr>
<td>1) $\text{DX}_4\text{L}$</td>
<td>DOWN</td>
<td>$\overline{s} \rightarrow x$</td>
<td>LEFT</td>
</tr>
<tr>
<td>2) $\text{DX}_4\text{L}$</td>
<td>DOWN</td>
<td>$\overline{s} \rightarrow x$</td>
<td>LEFT</td>
</tr>
<tr>
<td>3) $\text{DX}_4\text{T}$</td>
<td>DOWN</td>
<td>$\overline{s} \rightarrow x$</td>
<td>TO</td>
</tr>
<tr>
<td>4) $\text{DX}_2\text{R}$</td>
<td>DOWN</td>
<td>$s \rightarrow x$</td>
<td>RIGHT</td>
</tr>
<tr>
<td>5) $\text{DX}_2\text{R}$</td>
<td>DOWN</td>
<td>$s \rightarrow x$</td>
<td>RIGHT</td>
</tr>
<tr>
<td>6) $\text{DX}_4\text{T}$</td>
<td>DOWN</td>
<td>$\overline{s} \rightarrow x$</td>
<td>TO</td>
</tr>
<tr>
<td>7) $\text{DX}_4\text{L}$</td>
<td>DOWN</td>
<td>$\overline{s} \rightarrow x$</td>
<td>LEFT</td>
</tr>
<tr>
<td>8) $\text{DX}_2\text{L}$</td>
<td>DOWN</td>
<td>$s \rightarrow x$</td>
<td>LEFT</td>
</tr>
<tr>
<td>9) $a_4$</td>
<td>DOWN</td>
<td>$\overline{s} \rightarrow x$</td>
<td></td>
</tr>
<tr>
<td>10) $b^8$</td>
<td>BUBBLE</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11) $u^8$</td>
<td>UP SHIFT</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**TABLE 11. EXAMPLE OF TEMPLATE ORDER CODE ROUTINE**

A--LOAD BUBBLER ACCORDING TO TEMPLATE

B--PUT LOGICAL PRODUCT OF TOP NINE BUBBLER DIGITS IN X
FIGURE 28. ARRAY AND TEMPLATE
S plane, the nine digits being the 3 x 3 group for which that bubble register is in the reference position. Because of the placement of the complementing transfers, a bubbler in the reference position for a "perfect" 3 x 3 group will contain nine ones. There are two perfect 3 x 3 groups in the pattern given, with reference positions 01 and 63 (ij coordinates in figure 28). Consequently, bubble registers 01 and 63 will each have nine ones; all other registers will have nine digits of mixed ones and zeros.

Orders ten and eleven merely test the bubble registers for nine ones. Any register containing nine ones will be unaffected by \( B^8 \) since the digits are already ordered. The \( U^8 \) shift order will leave a one in X for such a register. (There is no transfer from X during U; digits shifted beyond X are lost.)

The result of this template operation, two ones in the X register at positions 01 and 63, can now be transferred to the memory. The original pattern is still in S (unchanged except for being shifted) and can be subjected to further processing.

The template is not restricted to a specific shape nor is it even necessary that it be a connected group of digits. Template with gaps merely require S plane shifts without transfer to X. Obviously, the arrangement of ones and zeros within the template is completely arbitrary. The execution time of a template routine is determined solely by the complexity of the template. A fixed number of orders will mark all occurrences of template agreement irrespective of the size of the pattern or the number of occurrences.

If the final order of table 11 had been \( U^7 \), the X register would have marked the location of bubble registers containing eight or more ones. In terms of the original pattern this means the X register would also have marked groups of near-perfect agreement; i.e., groups differing from the
template by only one digit. In the same way the use of $U^6$, $U^5$, etc., would cause increasingly approximate agreements to be marked. The order list of table 11 is an example of absolute template agreement; subsequent examples using $U^7$, $U^6$, etc., are examples of threshold template agreement.

It may not be economically feasible to provide bubble registers long enough to accommodate the largest template used. Large templates can be processed in pieces, using a variety of techniques. A large absolute template would be processed as follows in a bubbler of $R$ bits:

1) load first $R$ bits of template
2) $B^{R-1}$
3) $U^{R-1}$
4) load next $(R-1)$ bits of template
5) jump to step 2 and repeat cycle until template entirely loaded.

This procedure of forming the product $R$ bits at a time makes it unnecessary to use the memory to store intermediate results. However, the example is for most applications likely to be more interesting than useful. The interesting recognition problems deal with patterns that are noisy and in such patterns one is unlikely to find absolute template agreements if the template is very large.

For threshold template the programmer can specify the agreement conditions in a number of ways. For example, with a template of $r$ digits, it can be required that a certain subset, $k$, be in perfect agreement while the remainder, $r-k$, meet a specified threshold. Or it can be required that the complete template meet some specified threshold. If a threshold template is larger than the bubbler it will generally be necessary to use the memory to store intermediate results.
IV.6 Masking

A masking order replaces the contents of a two-dimensional register with the digit-wise product of two registers or with the complement of the product. The action of masking order $M_{x}$, ($M^{*} = SX$), is illustrated in figure 29. Of course, the distinction as to which of the operands is the pattern and which is the mask is purely one of convenience.

One useful property of the masking orders is that they permit the removal of successive portions of the input pattern as they are identified. As an example of how this might proceed, consider figure 30. The original pattern is intended to represent three 's, and $X$ and a hollow square scattered through the $S$ plane. The immediate object of the recognition program is to locate, identify and delete all 's from the pattern.

1) Using the first template and the absolute template operation, form in $X$ the location of all '. $X$ will have ones at locations 29, 52, and 95.
2) Store contents of $X$ in memory location 1.
3) Store contents of $S$ in memory location 2.
4) Clear $S$.
5) Generate the first mask using orders $S^{-}$, $L$, $S^{-}$, $R$, $T$, $S^{-}$, $F$, $S^{-}$, $T$, $R$, $S^{-}$. $L$, $R$, $T$ and $F$ are $S$ plane shift orders and $S^{-}$ is defined as $S' = X \lor S$.
6) Use making order $S_{28}$, ($S' = SM$), to form the first stage of the reduced pattern in $S$. $M$ refers to memory location 2.

One reason for successive deletion of identified areas is that it makes "unidentifiable" areas stand out. Suppose that the original pattern of figure 30 was to have been examined only for '+'s and 's. The '+'s were identified and removed by the sequence of steps just described. The same sort
FIGURE 29. THE MASKING OPERATION
FIGURE 30. SUCCESSIVE DELETION OF IDENTIFIED AREAS
of procedure will find and remove the lone X, again storing the location of this character in the memory. Anything remaining in S at this point can be categorized as "other," transferred to the control computer (by means to be discussed) and there tested against a much larger library of possible forms. This division of functions between the PRU and the control computer makes the most efficient use of each. The function of the PRU here is to identify all occurrences of a given character in parallel; the control computer identifies the rarely-encountered characters serially.

Real programs of successive deletion will be much more complicated than the example given. First, because actual patterns are generally noisy, the template operation will be a threshold operation or a series of related template operations. Second, the generated masks will not reproduce the templates exactly but will be modified to take into account the statistical variation in characters to be masked. And third, the masking operation will leave isolated bits throughout the pattern where character and mask failed to match perfectly. These bits will be removed by a smoothing operation.

IV.7 Smoothing

The first part of any smoothing routine will generally be the elimination of noise, i.e., isolated ones that are not part of any track or character. Since these noisy bits are isolated, their elimination by means of a template operation is simple. Each $S'_{ij}$ will be a one if and only if $S_{ij}$ was one and at least $k$ bits neighboring $S_{ij}$ were one. The definition of the neighboring region and the threshold $k$ are, of course, inherent in the threshold template operation.

The smoothing process is completed by filling in gaps in the pattern. Intuitively, a gap is any part of a pattern where the insertion of a one will
yield a more coherent track or character. This definition is necessarily vague since we have not yet restricted it to a specific recognition problem. For the bubble chamber recognition problem we will define a gap as being a single zero embedded in a straight line of \( k \) ones. This leads, not to a single template operation as did the noise removal operation, but to a series of template operations, one each for the possible orientations of the line.

IV.8 The Uniform Logical Transformation

A uniform logical transformation is any operation that replaces every digit in a two-dimensional array by a specified Boolean function of the digit and its neighbors. The transformation is called "uniform" because the relative neighbors involved and the Boolean dependence are independent of position within the array.

Both of the template operations are examples of the ULT. For a threshold template the Boolean statement may be very lengthy, but it exists, nonetheless. (The Boolean expression for a 16 bit template with a threshold of 13 would have 560 terms of 16 variables each if stated as the sum of fundamental products.) Actually, the template operations do not fit the definition for the ULT unless the "answer" in register \( X \) replaces the pattern in \( S \). We will, however, use the term ULT to describe operations where the result replaces the initial pattern or could replace the pattern.

While template, mask and other operations form a very important class of ULT's, they do not exhaust the set. A brute force method of achieving the completely arbitrary ULT is described briefly here. First, state the Boolean function in the less common canonical form, the product of fundamental sums. Second, by shifting and transferring form the first of these sums in \( X \), using \( X' = S \lor X \) and \( X' = \overline{S} \lor X \). Third, shift down one place and repeat step
two for the second fundamental sum. Fourth, when all fundamental sums have been loaded, bubble and shift up to form the logical product in X. Since this is an absolute operation the product may be formed piecemeal if necessary, that is, if the number of terms exceeds the length of the bubbler.

In principle, the arbitrary ULT is a powerful operation. Unfortunately its use will be severely restricted by the time required for the many shift operations. The previously cited example of a 16 bit template with threshold of 13 would have 64,976 terms of 16 variables each if stated in the required canonical form. This unwieldy Boolean expression can be reduced to 560 terms by taking the complement of the required function and then complementing the answer after forming the product. Assembling even these 560 terms and forming the product would involve somewhat more than $10^4$ shifts and transfers. Obviously, this is not the way to form a threshold template. The arbitrary ULT is best held in reserve as a deus ex machina for the programmer.

IV.9 Sensing

Figure 31 shows the $N^2$ cells of the X plane divided into $N^2/16$ macrocells of 4 x 4 bits each. For each of these macrocells there is a single line connecting the control computer with the 16 bits of that macrocell.

To lapse momentarily into a discussion of hardware, each sensing line is threaded through the 16 X cores of its cell. The clock signal "drive X" has been split into 16 drive signals, drive $X_a$, drive $X_b$, etc., where $X_a$ refers to the lower left-hand cell of every macrocell. (For all operations except sense these X clock signals occur in unison, consequently earlier explanations of transfers are still valid.)

This arrangement effectively converts the X register to a 16 word, random access, nondestructive memory of $N^2/16$ bits per word. If the A word is to be
FIGURE 31. ORGANIZATION OF THE X PLANE
sensed, all X cores are primed and the drive $X_a$ line energized. If the entire $X$ plane is to be sensed rapidly, we again prime all X cores and then sequentially energize the 16 $X$ drive lines. Note that only one prime interval is required to read the $X$ plane. The drive pulses are very short compared with the prime time so that the entire read $X$ operation takes about one shift time.

IV.10 Partitioning

The first step in the automatic processing of bubble chamber photographs is the conversion of the photograph to digital form. The sizes of events within the pattern are such that a raster of 4000 x 4000 bits is required to digitize the photograph with adequate resolution. This is, by any standard, a very large "word." No existing construction technique, magnetic, semiconductor or other can be used to build an actual computer with registers of $1.6 \times 10^7$ bits each. Thus, the programmer inevitably must divide the original pattern into subpatterns small enough to be processed in a realizable machine.

There is a definite limitation to this partitioning process, arising from the relation between the size of the partition and the size of the subpattern. Figure 32 shows the original pattern divided into 16 partitions. The shaded area represents one subpattern consisting of a partition surrounded by a protective margin, $\Delta$. It is this subpattern which is loaded into the S register for processing.

To illustrate the purpose of the margin, consider briefly the problem of identifying typewritten characters. If there were no margin, a character split by a partition line would not be identified correctly in either partition. To avoid this, a margin must be provided that is at least half as wide as the widest character to be identified. With such a margin every character will be entirely contained in at least one subpattern.
**FIGURE 32. PATTERN PARTITIONING**
A similar, but somewhat more complex, argument applies to the bubble chamber recognition problem since the "character" to be identified may be as long as the original pattern. The margin provided here will be large enough to take care of local events such as electron spirals and multiprong events. The global events, tracks passing through several partitions, will be handled in a different way although margin is equally essential here. At the conclusion of processing of a subpattern there will be stored in the control computer the orientation and partition line intercepts of each track in that subpattern. Two tracks having the same general orientation in adjacent partitions and intercepting the common partition wall in the same place will be considered two segments of the same track.

Margin should not be confused with guard ring. Margin is provided (by programming) to prevent characters and events from being split by partition lines, with the size of this margin determined by character size. Guard ring is provided (by physical extension of the S plane) to prevent the loss of information during shift operations, the guard ring size being determined by the size of template used.
CHAPTER V. ENGINEERING

V.1 Introduction

The fourfold purpose of this chapter will be to examine the validity of the assumptions made in Chapter I, to establish design criteria for a class of magnetic circuits, to introduce circuit innovations that improve performance of these circuits and to summarize the measured performance of a typical transfluxor network. For the sake of concreteness, reference will often be made to specific values of threshold current, switching time, etc. These values were obtained from measurements made on AMP, Inc. type 395813-1 cores and on RCA XF3668 cores.

V.2 Path Length

An unstated assumption of Chapter I was that for every path (described by a sequence of legs traversed) there is an explicit length. In effect, the reader was asked to accept an intuitive notion of path length until it could be more precisely defined. We undertake this definition now, starting with the conventional memory core shown in figure 33. For this core there is a spectrum of circular paths with lengths ranging from \(2\pi r_1\), the shortest path encircling the aperture, to \(2\pi r_2\), the longest path. If the core is uniformly saturated, the percentage of flux enclosed by any path (the shaded portion of figure 33) is given in figure 34. The linear relation of flux and length results from the cylindrical shape of the core.

For a symmetric five-hole transfluxor there are 32 reversal paths involving unit flux, where a unit of flux is defined to be the saturation value for one leg. By elimination of images equivalent under a rotation, the set of 32 paths is reduced to the 10 distinct types shown in figures 35, 36, 37, and 38. For the simpler path types, such as types 1, 2, and 10, the
FIGURE 33. MEMORY CORE
FIGURE 34. PATH LENGTH PICTURE FOR MEMORY CORE
Path lengths for RCA XF3668

Type 1
Minpath 0.600 cm
Maxpath 0.802 cm

Type 2
Minpath 0.167 cm
Maxpath 0.369 cm

Type 3
Minpath 0.723 cm
Maxpath 0.925 cm

FIGURE 35. TYPES OF REVERSAL PATHS
FIGURE 36. TYPES OF REVERSAL PATHS

Type 4
Minpath 0.604 cm
Maxpath 0.830 cm

Type 5
Minpath 0.833 cm
Maxpath 1.036 cm

Type 6
Minpath 0.847 cm
Maxpath 1.049 cm
FIGURE 37. TYPES OF REVERSAL PATHS
FIGURE 38. TYPES OF REVERSAL PATHS

Type 10
Minpath 1.040 cm
Maxpath 1.242 cm
computation of the minimum and maximum values is straightforward. Calculation of minimum path length for the remaining seven types follows easily from its definition as the shortest line enclosing specified apertures. The minimum path (minpath) is shown as a heavy line in figures where it is not the same as the inner boundary of the shaded area. It can be visualized as a rubber band stretched over rods in the aperture positions.

The maximum path (maxpath) is not so easily visualized as is the minpath. It is the shortest path enclosing specified apertures but always at least a distance T away from these apertures and, of course, remaining within the core. The perimeter of the shaded area fulfills these requirements for each of the ten types.

In addition to the extremes, minpath and maxpath, we can develop an entire family of intermediate path lengths as a function of t where 0 < t < T. Each intermediate path would be defined as maxpath was, with t substituted for T. Successive stages in this process are shown in figure 39 together with a flux vs path length curve. Flux is proportional to t if uniform saturation and uniform core thickness are assumed.

At the present time no means exist for determining, either analytically or empirically, the flux distribution within a multiaperture core of other than very simple geometry. In this absence the validity of the foregoing procedure must be established by experiment. Table 12 lists the threshold currents and path lengths for some of the more important reversal paths in a five-hole transfluxor. For each path type the smaller current listed is the current that just initiates switching around the path; the larger current is the current required to completely switch the path. It will be noted that in every case the field required for complete switching is slightly greater than the field that initiates switching. This is a consequence of the non-squareness of the magnetic material.
FIGURE 39. DEVELOPMENT OF PATH LENGTH VS FLUX CHARACTERISTIC FOR TYPE 5 PATH
<table>
<thead>
<tr>
<th>PATH TYPE</th>
<th>LENGTH IN CM</th>
<th>CURRENT IN AMPERES</th>
<th>AMPS/CM</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 MIN</td>
<td>.600</td>
<td>.40</td>
<td>.67</td>
</tr>
<tr>
<td>MAX</td>
<td>.802</td>
<td>.60</td>
<td>.75</td>
</tr>
<tr>
<td>2 MIN</td>
<td>.167</td>
<td>.11</td>
<td>.66</td>
</tr>
<tr>
<td>MAX</td>
<td>.369</td>
<td>.25</td>
<td>.68</td>
</tr>
<tr>
<td>3 MIN</td>
<td>.723</td>
<td>.46</td>
<td>.64</td>
</tr>
<tr>
<td>MAX</td>
<td>.925</td>
<td>.60</td>
<td>.65</td>
</tr>
<tr>
<td>5 MIN</td>
<td>.833</td>
<td>.52</td>
<td>.62</td>
</tr>
<tr>
<td>MAX</td>
<td>1.036</td>
<td>.70</td>
<td>.67</td>
</tr>
<tr>
<td>6 MIN</td>
<td>.847</td>
<td>.52</td>
<td>.61</td>
</tr>
<tr>
<td>MAX</td>
<td>1.049</td>
<td>.70</td>
<td>.67</td>
</tr>
<tr>
<td>8 MIN</td>
<td>.943</td>
<td>.57</td>
<td>.60</td>
</tr>
<tr>
<td>MAX</td>
<td>1.145</td>
<td>.78</td>
<td>.68</td>
</tr>
<tr>
<td>10 MIN</td>
<td>1.040</td>
<td>.66</td>
<td>.63</td>
</tr>
<tr>
<td>MAX</td>
<td>1.242</td>
<td>.90</td>
<td>.72</td>
</tr>
</tbody>
</table>

ALL VALUES FOR RCA XF3668 CORE

AVERAGE OF MIN THRESHOLDS - .63 AMPS/CM
AVERAGE OF MAX THRESHOLDS - .69 AMPS/CM

TABLE 12. EXPERIMENTAL VALUES OF SWITCHING THRESHOLDS
Additional verification of this simple model was obtained by measuring threshold currents in two different ways for path types 5, 6, and 8. Current was measured first with conductors threading the apertures necessary to cause reversal around the indicated path. Currents were then remeasured with the unused legs of the transfluxor physically removed. For example, the number 6 path type is shown in figure 36 as path 1647. The removal (by means of a high speed diamond tool) of legs 2, 3, 5, and 8 reduces the transfluxor to a single path device, the path being, of course, path 1647. It is significant that the currents measured in these two ways are identical within the limits of measurement accuracy.

V.3 First Flux Division Mechanism

A point frequently overlooked in discussion of multiaperature devices is the risetime dependence of the flux division between competitive paths. In this and the next section we will show that two distinct mechanisms account for the "minimum path rule" cited in Chapter I. To illustrate the first mechanism we again employ a memory core as shown in figure 40. The core is initially in the cleared state. Applications of a large amplitude, fast risetime, short duration current pulse will partially switch the core. Large amplitude is defined as an amplitude in excess of threshold for the maxpath. Fast risetime and short duration both imply times short compared to the switching time of the core for the amplitude used.

A core set in this way will have domains of reversed flux scattered throughout the interior of the core. The distribution will not be uniform, however, since domains nearer \( r_1 \) are subjected to a greater H field and consequently switch faster during the brief current pulse. While it is common to say that a short pulse may switch a core by (say) 30 percent, it
FIGURE 40. FLUX DISTRIBUTION RESULTING FROM SHORT, FAST RISETIME CURRENT PULSE
should be understood that the percentage of flux reversed may vary from 5 percent to 50 percent as a function of radius. A general picture of this radial dependence is shown in figure 40.

Now consider a similar experiment to be conducted with a three-hole transfluxor as shown in figure 41. Again, the core is initially in the cleared state. Application of a large amplitude, fast risetime set pulse of unlimited duration will reverse the flux in leg 1 and partially reverse the flux in legs 3 and 4. This can be explained by the following sequence of steps. At the time the set pulse is applied, paths 13 and 14 are both permissible. The amplitude of the set pulse is in excess of threshold for both paths and consequently both begin switching. Switching proceeds until the total flux reversed in legs 3 and 4 equals the saturation value of leg 1. At this time the magnetic circuit is effectively "open circuited" by leg 1 and no further switching can occur.

No analytic procedures are presently known for determining the ratio of flux switched in legs 3 and 4. Clearly, in some imprecisely defined way path 13 is shorter than 14, is subjected to a greater magnetomotive force than 14 and will consequently switch faster than 14. Or, stated differently, the percentage of domains reversed in leg 3 will be greater than the percentage reversed in 4.

Experimental evidence of the first flux division mechanism was obtained for both RCA and AMP cores using the circuit shown in figure 42. The use of mercury relays together with a moderately high voltage source ensured risetimes of the order of 5 ns, a time very short compared with the switching time of the cores. Experimental results are given in figure 42.
FIGURE 41. TRANSFLUXOR SET BY FAST RISE TIME PULSE
FIGURE 42. MEASUREMENT OF FIRST FLUX DIVISION MECHANISM
V.4 Second Flux Division Mechanism

Returning to the by now familiar memory core (figure 43), we now consider the flux distribution that results from a set pulse with a long rise-time. At $t = 0$ a ramp function of set current is applied to the cleared core. At $t = t_1$ the current reaches the threshold for switching around the minpath. At $t = t_x$ the current is just sufficient to cause switching around path $X$. At $t = t_2$ the current is the threshold value for the maxpath and switching ceases. During the interval from $t_1$ to $t_2$ a clearly defined boundary or wall moves outward from the inner circumference. At $t = t_x$ this wall divides the region inside, having counterclockwise flux orientation, from the region outside, having clockwise (or cleared) orientation.

Armed with this picture of wall motion we can now consider the effect of a long ramp set current applied to a transfluxor. It is clear from figure 44 that the set current must be at least as large as $I_3$ if path $13$ is to be completely set. $I_3$ is, however, larger than $I_2$, the minpath threshold for path $14$. This overlap in the path spectrums makes it appear at first that I cannot be adjusted in value to set path $13$ exclusively. Fortunately, path $13$ is set independently of path $14$ when the setting current has a long risetime. This independence is explained by a step-by-step consideration of flux reversals in the core as shown in the next paragraph.

At $t = t_1$ switching commences around the minpath for path $13$. At $t = t_1 + \Delta$ switching has progressed by wall motion to the perimeter of the shaded area. At this point we redefine all of the path parameters. Since the shaded area has already switched, it no longer enters into the calculation of thresholds; it is exactly as if the shaded area were physically removed from the core. The new value of $13$ minpath is the perimeter of the shaded area. The value of $13$ maxpath is unchanged. The crux of this development
FIGURE 43. MEMORY CORE SET BY RAMP OF CURRENT
\[ \text{FIGURE 44. TRANSFLUXOR SET BY RAMP FUNCTION OF CURRENT} \]

- \( I_1 \): Threshold of minpath 13
- \( I_2 \): Threshold of minpath 14
- \( I_3 \): Threshold of maxpath 13
- \( I_4 \): Threshold of maxpath 14
is that the new value of $14$ minpath has increased from its old value. Thus, as path $13$ is progressively set by wall motion, the threshold $I_2$ races ahead of the setting current. It can be shown for both AMP and RCA cores that a slow rising set current will never "catch" the $I_2$ threshold since this threshold ceases to exist when path $13$ is completely switched. Experimentally, flux division ratios of $50:1$ are easily obtainable.

Actual logical networks do not use such slow rising currents that $50:1$ ratios are common. Neither do real circuits use currents with risetimes in the nanosecond region leading to ratios of $4:1$. Practical circuits have ratios somewhere between these extremes and if the in-between figure is less than ideal, there are ways of improving it. One of these ways is the topic of the next section.

V.5 Directed Flux Division

Directed flux division refers simply to the use of a bias current to steer flux between competitive paths. The competitive paths most familiar to the reader at this point are paths $13$ and $14$. (There are other competitive paths.) Figure 45 is much like the preceding figure except for the addition of a new winding. The transfluxor is initially cleared. The bias current, being in the drive direction, has no effect on the core during interval $t_1$. During the set pulse, interval $t_2$, the net set current for path $13$ is $I_3$; the net set current for path $14$ is $I_3 - I_B$. During the interval $t_3$ the bias has no effect; i.e., no permissible paths exist for $I_B$.

$I_B$ could be chosen to be the same amplitude as $I_3$, thus reducing the net setting current for path $14$ to zero. In practice, a much smaller value of $I_B$ is nearly as effective. Actually, it is rarely necessary to use a bias current at all because most logical networks provide their own "biasing."
FIGURE 45. DIRECTED FLUX DIVISION
Figure 46 shows two transfluxors connected by a coupling loop. If a set pulse applied to core A causes a partial flux reversal in leg 4 of A, the resulting loop current, $I_L$, will act as a bias to minimize the leg 4 reversal. Note that $I_L$ passes through core B in the inhibit direction and consequently sees core B as a short circuit. For other circuits, such as the half adder, the picture is less favorable but where the loop current does exist it improves the flux division ratio.

V.6 Multipath Switching

For a multiaperture core threaded by a single current carrying conductor it is a straightforward procedure to enumerate the competitive permissible paths and select the shortest. From that point, analysis of switching can proceed according to the appropriate flux division mechanism. The analysis of biased circuits is scarcely more complicated if we restrict "bias" to mean a current which by itself cannot affect the state of the core either before or after the transition in question.

The analysis of circuits using multiple simultaneous currents requires a somewhat more detailed approach. Two circuits from Chapter II will serve to illustrate the method. The first of these examples is a rather artificial situation alluded to in the section on net drive. Figure 47 shows a transfluxor with clear and set currents simultaneously and instantaneously applied. The flux arrows indicate the state of the core before the application of the currents. The currents $I_C$ and $I_S$ are of equal magnitude and are large relative to any path threshold.

Taken alone, $I_C$ would reverse flux around path 4627. Similarly, $I_S$ by itself would switch path 12. (Path 1538 is not a permissible path because the net current enclosed is zero.) The one leg common to the permissible
Flux state before set pulse

FIGURE 46. COUPLING LOOP "BIASING"
FIGURE 47. COMPETITIVE PATHS
paths is leg 2, so it seems clear that any switching that results from $I_S + I_C$ must include leg 2. Viewed in this way, leg 2 is certain to switch, with 1 and 746 as competitive return paths. Competition is not keen for these paths. Path 12 is much shorter and therefore switches more rapidly than 4627 under the combined influences of $I_C$ and $I_S$. Bear in mind that the net current had the same value for the competing paths even though from different conductors.

This example was introduced to show that multiple currents sometimes lead to an easily interpreted competitive path situation. Before dismissing the topic, however, it is important to call attention to two potential hazards in this method of analysis.

The first of these is in the interpretation of "simultaneous." The currents $I_S$ and $I_C$ in figure 47 are simultaneous if they are in fact the same current, i.e., if the set and clear windings are connected in series and driven from one current source. Under this restriction, $I_S$ and $I_C$ need not be identical, but they must be rationally related since the clear and set windings can have only an integral number of turns. If $I_S$ and $I_C$ are supplied by independent clock sources and are only nominally simultaneous, a three part analysis is required. The three required parts are "$I_S$ preceding $I_C$", "$I_C$ preceding $I_S$" and the simultaneous case. This three-part analysis will often show that where absolute (common wire) simultaneity cannot be used, it is desirable to guarantee the sequence in which nominally simultaneous pulses are applied.

The second hazard lies in the selection of the flux division mechanism. Figure 47 was explained on the basis of the (simpler)first mechanism, that is, the currents had zero risetime. In typical circuits, both mechanisms operate but the net result is closer to the second mechanism than to the
first. In place of reexamining Figure 47, we will examine instead another circuit from Chapter II, this time considering multiple currents with non-zero risetime.

Figure 48 shows a triple output circuit just before application of the drive current. The point to be established is that the three output paths, 34, 56, and 78, switch independently of each other and not as one long path 456378. At \( t = t_1 \) each \( I_1 \) reaches the threshold for switching around its minor aperture. The net current enclosed by 456378 at this time is far below the threshold of the minpath. At \( t = t_1 + \Delta \) a small region surrounding each output aperture has been set. This yields a new, larger value of 456378 minpath. The threshold of this minpath continues to increase in this way, always staying ahead of the \( 3I_{DR} \) enclosed, until switching is completed and the long minpath ceases to exist.

Of course, analysis of this circuit is more complicated if the drive currents are not identical. In principle, however, even complex current arrangements will yield to step-by-step reevaluation of thresholds. In practice, the multiple output circuit will have coupling loops connected to the output apertures and the net drive vs. time is not easily specified. Aside from experiment, the simplest way to establish that isolation between apertures does exist is to recompute the flux distributions for figure 48 with a shorted coupling loop through one of the output apertures. The shorted loop has the dual advantage of being a severe test and at the same time making the computation of net drive simpler than it is in the general case. With such a shorted loop in place, it will be found that the switching rate of the unloaded apertures is unchanged from the originally determined values. In an actual circuit using the AMP core, the output from an unloaded aperture is influenced very slightly (perhaps 2 per cent) by the presence of a shorted loop linking one of the other output apertures.
$I_1 = \text{Threshold of Minpath 34}$

$I_2 = \text{Threshold of Minpath 456378}$

**FIGURE 48. TRIPLE OUTPUT CIRCUIT**
V.7 Prime and Antiprime

The greatest disadvantage of all-magnetic logic is its inherent slow speed. The most time consuming part of every transfer cycle is the prime operation and, as is shown in Appendix A, the prime has a minimum time determined solely by the constants of the magnetic material. Until greatly improved magnetic materials are made available, prime times will remain in the vicinity of 20 μsec.

With some circuits, the prime operation can be speeded by using a major aperture antiprime current during the prime operation. This allows the use of a larger prime current and hence a shorter prime time. Figure 49 shows the basic transfer circuit with three-hole cores used to simplify the flux diagrams. The extension of the argument for five-hole cores is obvious.

In previous discussions, the upper bound on the prime current was set by the threshold of the 2^k minpath in a cleared core, that is, prime was limited to avoid spurious setting. Now, with \( I_p \) and \( I_A \) simultaneously applied during the prime phase, the net spurious setting current is \( I_p - I_A \). Why not make \( I_p \) and \( I_A \) large and equal in value and thus eliminate the spurious setting problem altogether? This can in fact be done but only if the core so treated does not have a coupling loop on the output. This is occasionally the case when magnetic circuits are coupled to transistors or other relatively high impedance devices.

To see why both \( I_A \) and \( I_p \) must be limited in amplitude for the circuit of figure 49, consider the flux diagram of condition 2. Here the sending core is set but not primed and the receiving core is cleared. When large prime and antiprime currents are applied, the flux reversal in leg 4 of the sending core induces a loop current \( I_L \). This loop current sees the receiving core as a short circuit and consequently almost cancels \( I_p \). With a small
Condition 1

Condition 2

FIGURE 49. MAJOR APERTURE ANTI PRIME
net current in the output aperture and a large $I_A$ in the clear direction, the sending core tends to be **spuriously cleared**.

Why is the problem of spurious clearing not applicable when the primed core has no coupling loop on the output? The explanation follows very closely that given for the first example of multipath switching. Large, equal $I_p$ and $I_A$ currents will reverse the flux in leg 3 with legs 1 and 4 competitive return paths. The difference in length for paths 13 and 34 is so great that the flux division will be essentially perfect irrespective of mechanism. When legs 3 and 4 have reversed, no permissible paths will remain; all reversal paths will enclose either zero current or current in the wrong sense.

For coupling loop circuits, the largest $I_A$ that can be used is the threshold of 13 minpath. This value of $I_A$ is added to the older value of $I_p$ to obtain a new maximum prime current. The penalty paid for this increased prime speed is loss of flexibility. For condition 2 of figure 49, it is impossible to prime the output, antiprime the major aperture and antiprime the input aperture all at the same time. To do so would exceed the threshold of spurious clearing around path 13 since both antiprimes are enclosed by that path. One solution to this problem is brought out in a subsequent section where the bubbler is discussed in detail.

V.8 **Nonsquareness Effects**

In the first four chapters of this paper, it was assumed that the B-H relationships of the paths within a transfluxor were perfectly rectangular. In V.3 this picture was modified by the definition of path length as a spectrum of lengths ranging from minpath to maxpath. Figure 50 shows a greatly simplified B-H characteristic for the path 1548. In this picture
B is flux density averaged over cross section of path
\[ H = kI \]

FIGURE 50. IDEALIZED B-H CHARACTERISTIC OF PATH 1548
H₁ and H₂ represent the fields necessary to switch the minpath and maxpath respectively. This is to say that the slope of BC is determined essentially by the geometry of the core rather than by the B-H characteristic of the magnetic material. Having thus accounted for the slope of the "verticals" in figure 50 we now consider the slope of the "horizontal" line DE.

In the literal sense, no magnetic material is ever saturated. For any flux density the application of a stronger H field in the appropriate direction will increase B. The customary figure of merit for square loop materials is Bₘ/Bₛ (the squareness ratio), expressed for some value of H. For the AMP core, Bₘ/Bₛ is .93 at H = 2H₀; .87 at H = 10 H₀ and .77 at H = 50 H₀.

The first consequence of DE's slope is that interrogation of a cleared core results in a small output. A clear current applied to an already cleared core will cause an excursion from E to D and (when the clear current ceases) back to E again. The voltage induced in the output loop by this excursion is called the shuttle voltage, a term often used in describing the same operation in memory cores. How large will this shuttle voltage be? If the clear current is no more than ten times the threshold value, the shuttle voltage can generally be ignored. [At H = 10 H₀, Bₛ = 1.15 Bₘ. The maximum flux change for a zero stored would be .15 Bₘ; the maximum change for a one stored would be 2.15 Bₘ.]

The shuttle voltage becomes more of a problem when cores are interrogated nondestructively. The drive current must be approximately as large as the clear current was in the preceding paragraph. (A more specific statement of current requirements is part of Appendix A.) Now, however, the drive is influencing the flux around path 3K. Path 3K has a much lower threshold than 1548, especially the minpath of 3K. It is not unusual to apply drive currents that are 50 to 100 times the threshold of the 3K minpath. The actual
situation is more complicated than this and apparently worse. While the drive current is increasing the flux density in leg 4, leg 3 is being driven out of saturation. This means that only the leg 4 portion of path 34 limits the flux change around that path. Since the H distribution in this region cannot be determined, a more precise statement is impossible.

If sufficiently large, the shuttle voltage can cause a loop current which will partially set the receiving core. Usually, the high threshold for setting and losses in the coupling loop minimize this danger. In fact, the elastic excursion along DE in figure 50 may be considered an advantage. Since this elastic flux change is added to \(2B_R\) to form the "one" output, it helps promote the transfer of a one. When the drive current ceases, the core relaxes along DE. The small loop current induced by this flux change will be in the inhibit direction and will not affect the receiving core.

Somewhat different considerations apply in the case of the \(XY\) transfer circuit. There can be no problem of shuttle voltages causing partial setting since such voltages cancel in the loop. The problem arises in the non-destructive transmission of a one, where X has a one output and Y has a shuttle voltage. The shuttle voltage cancels part of the output voltage of X and thus impedes the transfer. Moreover, Y is being driven by the drive current plus the loop current and consequently has a larger than normal shuttle voltage. The solution to this problem is to increase the coupling loop ratio from 2:(-2):1 to 3:(-3):1. The extra turn on the X core provides enough voltage to compensate for the shuttle voltage.

Destructive interrogation of the \(XY\) transfer circuit does not eliminate the shuttle voltage problem. With \(X = 1\) and \(Y = 0\), the output of X is slightly reduced because of the smaller elastic flux contribution. The output of Y, however, is nearly as large as in the nondestructive case since it
is being driven by the loop current. This problem could be solved by adjustment of the coupling ratio but a better solution is given in the next section.

V.9 The Bubble Operation

Figure 51 shows the coupling loop wiring of a short bubble register. The diagram is essentially the diagram given earlier (figure 23) with relatively minor modifications made necessary by the nonsquareness effects cited in the preceding section. Additionally, coupling loop T has been modified to permit a much more efficient realization of the complement operation. During all other operations, however, loop T functions exactly as it did in figure 23.

Table 13 lists the seven steps that make up one bubble operation. The standard starting condition is: information in P and X, primed; L cleared and R set to one but not primed.

In the first step information is transferred from P and X into the auxiliary registers. The principle register is driven and cleared simultaneously in this clock time. The drive current ensures a large one output because of the elastic flux component; the clear current sets the binary state of the core, as is logically necessary in this step. The X core is interrogated nondestructively and transfers its information to \( R_1 \) through a standard negation circuit. All Ll apertures are driven during this step to prevent the back propagation of information from \( P_4 \) which might otherwise result. This point will be further clarified in step seven.

In the second step the Ll apertures of odd numbered L cores are primed.

Consider any odd L core set in the first step. When this core is primed, a current in loop Y flows through the (even) core above in the prime direction. If this even core were to be primed at the same time, the two currents could exceed the threshold for spurious setting.
FIGURE 51. FOUR DIGIT BUBBLE REGISTER
<table>
<thead>
<tr>
<th>L_{ODD}</th>
<th>L_{EVEN}</th>
<th>P</th>
<th>X</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
</tr>
<tr>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
</tr>
<tr>
<td>1 D D D C D</td>
<td>2 P A A</td>
<td>3 A P A</td>
<td>4 P A P</td>
<td>5 D D D C D D C</td>
</tr>
<tr>
<td>6 C C D D S</td>
<td>7 P A P A</td>
<td>8</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 \( P \rightarrow L \) \( \bar{P}, \bar{X} \rightarrow R \)
2 prime \( L_1 \) odd \( A \) - ANTIPRIME
3 prime \( L_1 \) even \( C \) - CLEAR
4 prime \( L_2 \) \( D \) - DRIVE
5 \( f(L,R) \rightarrow P, X \) \( P \) - PRIME
6 set \( R_1 \) \( S \) - SET
7 prime \( P_3, X_3 \)

TABLE 13. THE BUBBLE OPERATION
The major aperture of $L_{\text{ODD}}$ is antiprimed in this step to allow the use of a larger prime and hence speed the prime operation. $L^3_{\text{ODD}}$ cannot be antiprimed at this time because of the possibility of spurious clearing. Instead, $L^3_{\text{EVEN}}$ is antiprimed (to prevent back propagation).

In the third step priming of the $L_1$ apertures and antipriming of the $L_3$ apertures is completed. The comments of step two apply exactly if the words "even" and "odd" are interchanged.

In the fourth step all $L_2$ apertures are primed. Loop T is part of a half adder, here used as an $XY$ transfer circuit. For the $XY$ transfer operation no "prime $R^4$" pulse is used; where logically necessary $R^4$ will be primed by the coupling loop current during this step. $L_5$ is antiprimed to allow the use of a larger prime and hence shorten the prime time. It is not necessary to antiprime $R_5$ since the coupling loop current will be smaller than the prime $L_2$ current by approximately the threshold of switching around the $L_2$ aperture.

In the fifth step information is transferred from $L$ and $R$ back to $P$ and $X$. Combined drive and clear currents are used here for the reason given in step one. It is not logically necessary to clear $R$ at this time but if $L$ is cleared, $R$ must also be cleared to obtain proper cancellation in loop T.

For any interior core, B, in the principle register, the Y loop transfers the function $\overline{BC}$ to the $P_4$ input; the T loop transfers $AB$ to the $P_2$ input. The upper left-hand core is a dummy, a core with an output winding but no inputs. It is used to make the upper stage more nearly like the interior stages. Clock pulses are supplied to the dummy exactly as they are to any other $L_{\text{ODD}}$ core.

In the sixth step the $R$ register is set to restore it to the starting condition. Both $P$ and $X$ are driven at this time to prevent back propagation.
from R5. This back propagation is inherent in negation circuits. In addition to P3 and X3, L3 also tends to be set at this time although to a lesser extent because of the turns ratio. A small clear current through L5 is sufficient to prevent setting.

In the seventh step P and X are primed using a simultaneous major aperture antiprime. The antiprime improves the speed but makes it impossible to antiprime the input apertures. Thus, in step one it was necessary to drive LI to avoid back propagation.

V.10 Other Operations in the Bubbler

Tabular listings of clock pulses for the six remaining bubbler operations are given in tables 14 through 19. For the most part, these operations can be thought of as attenuated versions of the bubble operation. For example, the replacement function for contract, B' = AB, is but a part of the bubble function, B' = AB v BC. For this reason the six remaining operations have been tabulated in a way that emphasizes their similarity. Starting and ending conditions are the same for all operations. In a few places pulses have been included which are not logically necessary but which simply make the operations more uniform. The object of this is, of course, to simplify the control logic of the clock source.

V.11 Experimental Results

An eight digit bubble register was constructed from AMP 395813-1 cores according to the wiring shown in figure 51. Measured values of current, speed and other factors for this register are listed in table 20.

The tolerance for each current was determined by varying that current while holding all other currents at their nominal values. For any current
<table>
<thead>
<tr>
<th>L_{ODD}</th>
<th>L_{EVEN}</th>
<th>P</th>
<th>X</th>
<th>R</th>
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</tbody>
</table>

1. \( P \rightarrow L \) \( \bar{P}, X \rightarrow R \)
2. prime L1 odd
3. prime L1 even
4. \------\
5. \( L \rightarrow P, X \)
6. set Rl
7. prime P3, X3

**TABLE 14. THE UP SHIFT OPERATION.**
<table>
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<th>L_{ODD}</th>
<th>L_{EVEN}</th>
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<th>X</th>
<th>R</th>
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</tr>
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<td>PAH</td>
<td>PAH</td>
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<td>DDC</td>
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<td>DC</td>
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<td>D</td>
</tr>
<tr>
<td>7</td>
<td>P A</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

1. \( P \rightarrow L \), \( \overline{P}, \overline{X} \rightarrow R \)
2. --------------
3. --------------
4. prime + maj ap set L2
5. \( \overline{R} \rightarrow P \)
6. set R1
7. prime P3

**TABLE 15. THE DOWN SHIFT OPERATION**
<table>
<thead>
<tr>
<th></th>
<th>( I_{\text{odd}} )</th>
<th>( I_{\text{even}} )</th>
<th>( P )</th>
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<tr>
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<td>P</td>
<td>A</td>
<td>A</td>
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</tbody>
</table>

1. \( P \rightarrow L \) \( \overline{P}, \overline{X} \rightarrow R \)
2. antiprime \( L_3 \) even \( A \) - \( \text{ANTIPRIME} \)
3. antiprime \( L_3 \) odd \( C \) - \( \text{CLEAR} \)
4. prime \( L_2 \) \( D \) - \( \text{DRIVE} \)
5. \( f(L, R) \rightarrow P \) \( P \) - \( \text{PRIME} \)
6. set \( R_l \) \( S \) - \( \text{SET} \)
7. prime \( P_3, X_3 \)

**TABLE 16. THE CONTRACT OPERATION**
<table>
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<th></th>
<th>( L_{\text{ODD}} )</th>
<th>( L_{\text{EVEN}} )</th>
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<th>( X )</th>
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<tr>
<td>1</td>
<td>D</td>
<td>D</td>
<td>D C</td>
<td>D</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>P</td>
<td>A</td>
<td>A A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>AA</td>
<td>P</td>
<td>A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>P</td>
<td>A</td>
<td>P A</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>D D</td>
<td>D C</td>
<td>D D</td>
<td>D C</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>C</td>
<td>C</td>
<td>D</td>
<td>D</td>
<td>S</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>P A</td>
<td>P A</td>
<td></td>
</tr>
</tbody>
</table>

1 \( P \rightarrow L \quad \overline{P}, \overline{X} \rightarrow R \)

2 prime \( L_1 \) odd                A - ANTI PRIME
3 prime \( L_1 \) even               C - CLEAR
4 prime \( L_2 \)                    D - DRIVE
5 \( f(L, R) \rightarrow P, X \)     P - PRIME
6 set \( R_1 \)                      S - SET
7 prime \( P_3, X_3 \)               

TABLE 17. THE EXPAND OPERATION
<table>
<thead>
<tr>
<th>L_{ODD}</th>
<th>L_{EVEN}</th>
<th>P</th>
<th>X</th>
<th>R</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 2 3 4 5</td>
<td>1 2 3 4 5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>C</td>
</tr>
<tr>
<td>2</td>
<td>P</td>
<td>A</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>A</td>
<td>P</td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>C</td>
</tr>
<tr>
<td>6</td>
<td>C</td>
<td>C</td>
<td>D</td>
<td>D</td>
</tr>
<tr>
<td>7</td>
<td>P</td>
<td>A</td>
<td>P</td>
<td>A</td>
</tr>
</tbody>
</table>

1. \( P \rightarrow L \)  \( \overline{P} \),  \( \overline{X} \rightarrow R \)
2. prime \( L \) odd  \( A \) - antiprime
3. prime \( L \) even  \( C \) - clear
4. \( f(L, R) \rightarrow P, X \)
5. set \( R \)  \( D \) - drive
6. prime \( P \), \( X \)  \( P \) - prime
7. \( S \) - set

**TABLE 18. THE GROUP COUNT OPERATION**
### Table 19. The Complement Operation

<table>
<thead>
<tr>
<th>$L_{\text{odd}}$</th>
<th>$L_{\text{even}}$</th>
<th>$P$</th>
<th>$X$</th>
<th>$R$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 D</td>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td></td>
<td>PH</td>
</tr>
<tr>
<td>5 D D D C</td>
<td>D D D C</td>
<td></td>
<td>DC</td>
<td></td>
</tr>
<tr>
<td>6 C</td>
<td>C</td>
<td>D</td>
<td>D</td>
<td>S</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>P A</td>
<td>P A</td>
<td></td>
</tr>
</tbody>
</table>

1. $P \rightarrow L$, $\overline{P}, \overline{X} \rightarrow R$
2. --------------
3. --------------
4. prime + maj ap set R4
5. $f(L, R) \rightarrow P, X$
6. set R1
7. prime P3, X3

A - antiprime
C - clear
D - drive
H - half select (in set direction)
P - prime
S - set
<table>
<thead>
<tr>
<th>STEP</th>
<th>DURATION</th>
<th>OPERATION</th>
<th>APERTURE</th>
<th>NOM</th>
<th>MAX</th>
<th>MIN</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>6 μsec</td>
<td>CLEAR</td>
<td>P5</td>
<td>10</td>
<td>&gt;13</td>
<td>6.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVE</td>
<td>P3</td>
<td>10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVE</td>
<td>L1</td>
<td>.72</td>
<td>1.8</td>
<td>.24</td>
</tr>
<tr>
<td>2</td>
<td>35 μsec</td>
<td>PRIME</td>
<td>L1 ODD</td>
<td>.72</td>
<td>.87</td>
<td>.50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ANTIPR</td>
<td>L3 EVEN</td>
<td></td>
<td>.94</td>
<td>.53</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ANTIPR</td>
<td>L5 ODD</td>
<td>.30</td>
<td>.39</td>
<td>.19</td>
</tr>
<tr>
<td>3</td>
<td>35 μsec</td>
<td>PRIME</td>
<td>L1 EVEN</td>
<td>.72</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ANTIPR</td>
<td>L3 ODD</td>
<td></td>
<td>.94</td>
<td>.53</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ANTIPR</td>
<td>L5 EVEN</td>
<td>.30</td>
<td>.36</td>
<td>.05</td>
</tr>
<tr>
<td>4</td>
<td>35 μsec</td>
<td>PRIME</td>
<td>L2</td>
<td>.72</td>
<td>.91</td>
<td>.49</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ANTIPR</td>
<td>L5</td>
<td>.30</td>
<td>.42</td>
<td>.07</td>
</tr>
<tr>
<td>5</td>
<td>6 μsec</td>
<td>CLEAR</td>
<td>R5</td>
<td>5.4</td>
<td>&gt;10</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVE</td>
<td>R4 + L2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLEAR</td>
<td>L5</td>
<td>5.4</td>
<td>&gt;10</td>
<td>3.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVE</td>
<td>L1 + L4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>6 μsec</td>
<td>SET</td>
<td>R1</td>
<td>1.3</td>
<td>&gt;2.3</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CLEAR</td>
<td>L5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DRIVE</td>
<td>P3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>35 μsec</td>
<td>PRIME</td>
<td>P3</td>
<td>.60</td>
<td>.75</td>
<td>.54</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ANTIPR</td>
<td>P5</td>
<td>.30</td>
<td>.43</td>
<td>.12</td>
</tr>
</tbody>
</table>

Table 20. Measured Performance of 8 Digit Bubble Register
within the range listed, the register would correctly bubble any digit pattern loaded (in parallel) into the P5 apertures. Where two operations are listed in the same box (e.g., clear and drive in step 1) the windings associated with these operations are connected in series. In a few cases, the maximum current was not accurately established because of limitations in the clock source.
REFERENCES


APPENDIX A. RESISTANCE AND SPEED DERIVATIONS

For the purposes of the derivation we assume that a core subjected to a uniform switching current will switch at a uniform rate. Or, stated differently, a core switched by a step function of current will have a constant $\frac{d\phi}{dt}$ from the onset of the switching current until the core has completed switching.

First, to determine the properties required of the coupling loop, consider the transfer circuit shown in figure 52, where core 1 contains a one and is primed, core 2 is cleared. The one in core 1 is to be transferred to core 2 as $I_c$ clears core 1. In order that the maximum amount of flux be transferred, core 2 must switch at least as fast as core 1 at this time; that is, $\dot{\phi}_2 > \dot{\phi}_1$. Otherwise, core 2 will not have completed switching by the time core 1 is fully switched, and, therefore, the transfer will be incomplete. This requirement can be expressed as

$$i_t > I_c - n_i$$

Equation (3) expresses the fact that the setting current acting on core 2 must equal or exceed the net clear acting on core 1. (Note that the reversal path of the sending core, path 24, and the reversal path of the receiving core, path 13, are of equal length.)

Furthermore, considering voltages around the coupling loop

$$i_t = \frac{n(\phi_1)_t - (\phi_2)_t}{R}$$

when subscripts 1 and 2 refer to their respective cores and the subscript $t$ indicates that these are the switching rates during transfer. For the
FIGURE 52. CIRCUIT DURING TRANSFER
limiting case where \( \phi_2' = \phi_1' \)

\[
i_t = \frac{(n-1)\phi_1'}{R} \tag{5}
\]

If we let \( \Phi \) be the total flux reversed, the initial assumption yields

\[
\Phi = \frac{\Phi}{\tau} , \tag{6}
\]

the switching time \( \tau \) being given in turn by the Menyuk-Goodenough relationship

\[
\tau = \frac{S_L W}{4\pi(I_c - nI_t - I_o)} \tag{7}
\]

where \( S_w \) is the switching constant of the material, \( L \) is the length of path 24 and \( I_o \) is the threshold current for switching path 24.

Combining (5), (6), and (7) yields

\[
i_t = \frac{(n-1)}{R} \frac{4\pi \Phi}{S_L W} (I_c - nI_t - I_o) . \tag{8}
\]

Combining (8) with (3) to eliminate \( i_t \) and assuming that \( I_c \gg I_o \), we obtain as a necessary condition

\[
R \leq \frac{4\pi \Phi}{S_L W} (n-1) \tag{9}
\]

We can now consider the requirements of the prime operation. In this case \( I_p \) in figure 53 must be limited to below the threshold for path 24 to prevent spurious setting.

\[
I_p < I_o \tag{10}
\]

The current induced in the coupling loop during prime is limited only by the resistance of the loop since no switching can occur in the receiving
FIGURE 53. CIRCUIT DURING PRIME
core at this time. This is expressed as

$$i_p = \frac{n(\Phi)}{R} = \frac{n}{R} \frac{4\pi}{S_w} (I_p - i_o)$$  \hspace{1cm} (11)

where $i_o$ is the current threshold for path 34 and is equal to $I_o \frac{d}{L}$, $d$ and $L$ being the lengths of paths 34 and 24 respectively. Combining (10) and (11) and noting that the reciprocal switching speed $1/\tau_p = \frac{4\pi}{S_w} (I_p - i_o)/L$, it follows that

$$\frac{1}{\tau_p} < \frac{I_o (1 - d/L)}{(S_w d/4\pi) + (\Phi n^2/R)}$$  \hspace{1cm} (12)

or, taking into account the limitation on $R$, in (9), the limiting speed obtained by making $L \gg d$ is given by

$$\tau_p > \frac{S_w}{H_o} \frac{n^2}{n-1}$$  \hspace{1cm} (13)

where $H_o = \frac{4\pi I_o}{L}$ and is the threshold field for the material.

All quantities in these derivations are expressed in electromagnetic units.
APPENDIX B. THE THIN FILM TRANSFLUXOR

Introduction

Among the reasons why all-magnetic logic circuits have not been used extensively is the difficulty of fabrication. Threading of windings through ferrite cores is at present a hand operation with the wiring of coupling loops being especially time consuming. It is the purpose of this appendix to consider methods of forming magnetic logic circuits using evaporation techniques to facilitate automatic production.

The Deposited Memory Cell

Broadbent has shown that multiaperture magnetic memory cells can be built up by multiple evaporation of magnetic, conducting and insulating layers on a suitable substrate. He employs these cells in a coincident-flux memory to achieve switching times of .1 µsec for 250 ma drive. The Broadbent memory cell demonstrates that the advantages of a closed magnetic circuit (signal to noise ratio, logical flexibility) need not be sacrificed to gain the production advantage of evaporation.

The Four Layer Model

By extension of the techniques just cited it should be possible to form "thin film transfluxors" (TFT). One possible geometry is suggested by figure 54, an edge view of a device with four minor apertures and one major aperture. It should be understood that figure 54 is a highly formalized representation of the TFT and that dimensions have been distorted for clarity.

The formation of such a multi-layer cell would require a minimum of 16 separate layers to be deposited. While this would present a formidable
FOUR LAYER TFT-EDGE VIEW

ORDER OF DEPOSITING FILMS

- INSULATION
- LOWER MAGNETIC FILM
- INSULATION
- CONDUCTORS
- INSULATION
- MAGNETIC FILM
- INSULATION
- CONDUCTORS
- INSULATION
- CONDUCTORS
- INSULATION
- MAGNETIC FILM
- INSULATION
- CONDUCTORS

FIGURE 54. FOUR LAYER TFT
problem in masking and film thickness control, it does not seem insurmountable. Broadbent's memory cells (of much simpler geometry) required 19 layers and were successfully fabricated in an array of 160 cells.

Comparison with Ferrite Cores

Discussion of the operation of the TFT will be aided by the sketches of the TFT and ferrite transfluxor shown in figure 55. The two devices are topologically equivalent since the TFT can be obtained by a continuous deformation of the ferrite device. This equivalence can be seen easily by noting the one-to-one correspondence between the five holes, the eight (numbered) regions of unit cross-sectional area and the four regions of two (or more) units cross-sectional area.

Actually, the statement above goes beyond that necessary to establish topological equivalence. The fact that corresponding regions have the same flux limiting properties means that the devices have some degree of magnetic equivalence. They are not magnetically identical, however, as corresponding path lengths are not preserved. For example, in the ferrite core a minimum length path through legs 1, 6, 3, and 7 is shorter than a minimum length path through 1, 5, 3, and 8. This is not true in the TFT as these paths are nearly identical in length. (Remember that vertical dimensions have been exaggerated.)

Comparison in Operation

Referring again to figure 55, assume both devices to be in the cleared state ↑↑↓↓. In both devices a set current linking leg 1 will reverse the flux in that leg and in leg 3 (minimum path rule). In the ferrite core, legs 6 and 7 will reverse while 5 and 8 will be unaffected by the set pulse.
FIGURE 55. FERRITE TRANSFLUXOR AND TFT
This will not hold true for the TFT since the path through 6 and 7 is no shorter than the path through 5 and 8. This means only that it will be necessary to use bias currents to steer flux through the required legs. A small inhibit current applied to the upper and lower minor apertures of the TFT while the left aperture is being set will guarantee switching around path 1637. In some circuits, the self-biasing provided by coupling loops may be sufficient to direct flux around the correct path.

The Three Layer Model

A slightly different topological distortion of the ferrite transfluxor yields the TFT of figure 56. The term "three layer" comes from the number of separate magnetic films that are required to fabricate the cell. No less magnetic material is involved, however, as one of the films is of double thickness.

Operation of the three layer model TFT is the same as for the four layer model with one exception. During the time any input is being set, the other input apertures must be inhibited and the output aperture must be driven. The currents required for this inhibiting function need not be large as they merely steer the flux between two paths of equal length. Ordinarily these inhibiting functions will not require additional circuitry (i.e., conductors through the TFT) though they may require a slightly more complex clock source.

The real differences between the three and four layer models are not as much magnetic as they are geometric. The simpler geometry of the three layer TFT reduces to eleven the minimum number of films that must be deposited to make up a cell. Moreover, the structure of the three layer device may permit the use of larger conductors for a given overall device size. The importance of this relationship will be treated in the section on size.
ORDER OF DEPOSITING FILMS

LOWER FILM (DOUBLE THICKNESS)
INSULATION
CONDUCTORS
INSULATION
MIDDLE FILM
INSULATION
CONDUCTORS
INSULATION
CONDUCTORS
INSULATION
TOP FILM

CONDUCTOR
INSULATION
MAGNETIC FILM

FIGURE 56. THREE LAYER TFT
The Single Layer Model

The first thing likely to be noticed in figure 57 is the strong resemblance the single layer TFT bears to the four layer model. Actually, the single layer model is nothing more than the four layer model with the various magnetic paths arranged side by side rather than on top of each other. Magnetic equivalence for the two forms should be expected except perhaps for leakage flux.

If conductors and magnetic films are kept to the same width in the two devices it is clear that the single layer TFT will occupy at least twenty times the area of the four layer model. Generally this will be a disqualifying flaw though there may be applications where simplicity of formation is more important than size. The single layer TFT can be built up with a minimum of five layers.

Circuit Restrictions

It has been tacitly assumed thus far that not only are TFT's to be deposited but also the associated interconnections are to be formed at the same time. Where transfluxors are to be combined into logical networks, restrictions must be placed on the resistance of conductors. Specifically, for circuits whose operation is dependent on having some coupling loop resistance (sometimes called MAD-\(R^2\) circuits) this resistance must meet the condition derived in Appendix A:

\[
R \leq \frac{4\pi \Phi}{S \cdot L} (n-1)
\]

In words, the maximum coupling loop resistance for transfluxor circuits of the MAD-R class is governed by the total flux reversed, the mean path...
ORDER OF DEPOSITING FILMS

CONDUCTOR
INSULATION
MAGNETIC FILM
INSULATION
CONDUCTOR

CONDUCTOR
INSULATION
MAGNETIC FILM

FIGURE 57. SINGLE LAYER TFT
length of the magnetic circuit, the switching constant of the material and
the turns ratio of the coupling loop.

The immediate importance of the foregoing relation is that the entire
circuit must be specified before appropriate dimensions for a TFT can be
given. The interdependence of the factors in the resistance equation can
perhaps be illustrated best by an example.

Size

It is not suggested that the following design is optimum. It is intended
only as a starting point from which we can reach some conclusions about the
lower bound on TFT size.

For concreteness, let us examine a two-dimensional shift register, con­
sidering for the moment only the transfluxors and coupling loops. A portion
of the register with one coupling loop is shown in figure 58. Since this
particular application requires only a four aperture transfluxor, we might
simplify the three layer model slightly to obtain the TFT design shown in
figure 58.

Assume the following dimensions and parameters:

<table>
<thead>
<tr>
<th>Dimension</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TFT size</td>
<td>1 cm square</td>
</tr>
<tr>
<td>center to center spacing</td>
<td>3 cm</td>
</tr>
<tr>
<td>L (magnetic path length for clear operation)</td>
<td>2 cm</td>
</tr>
<tr>
<td>magnetic film thickness</td>
<td>40,000 Å</td>
</tr>
<tr>
<td>( B_R ) (permalloy)</td>
<td>9,000 gauss/cm²</td>
</tr>
<tr>
<td>( S_W ) (permalloy)</td>
<td>( 2 \times 10^{-7} ) OE-Sec</td>
</tr>
<tr>
<td>( H_O ) (permalloy)</td>
<td>1 OE</td>
</tr>
</tbody>
</table>

\[
\phi_R = 9000 \times 4 \times 10^4 \times 10^{-8} \times .1 = .36 \text{ maxwells}
\]
FIGURE 58. TFT SHIFT REGISTER
or, in terms of ohms (in place of e.m.u. ohms), the coupling loop resistance must be less than .23 ohms.

For a TFT of unit size (square) we can estimate from the sketch that the coupling loop length must be roughly sixteen units, four units within the TFT's and twelve without. The most effective way to reduce loop resistance for a given TFT size is to widen and/or thicken the loop conductors outside the TFT's. In this way the total loop resistance can be reduced to perhaps half of what it would be with conductors of uniform cross section. If we choose as a conductor size inside the TFT .01 cm wide and .002 cm thick, the total loop resistance will be .112 ohms for aluminum.

Having produced a model which handily meets the resistance requirement, we can now consider methods of reducing the size of the unit. Generally it is not possible to simply scale down a TFT model as this increases $R$ by the scale factor while decreasing the right-hand side of (9) by the scale factor. For the design just cited, reducing all dimensions by a factor of 1.4 increases the loop resistance to 1.57 ohms while reducing the maximum allowable resistance to 1.60 ohms. Clearly, this represents the limit of simple scaling for this particular design.

On the other hand, if all thicknesses are held constant, the unit can be scaled in the remaining two dimensions without altering either side of (9). The problem then becomes one of purely mechanical considerations, i.e., how narrow a conductor can be deposited for a given film thickness. Without any supporting evidence, assume it possible to deposit conductors with thickness equal to one half the width. Acting on this assumption will allow us to scale the unit by an additional factor of 2.5, as the original design called for a width/thickness ratio of 5:1.
The two scaling operations together have reduced conductor width from .01 cm to .0029 cm and overall cell size by the same ratio. The value .0029 cm is attainable by standard masking and depositing techniques. The lower limit on conductor widths can be as little as .0005 cm if considerable care is exercised in forming the masks and in depositing.

**Speed**

The speed of circuits employing only transfluxors and connecting wire is ultimately limited by the switching constant and threshold of the magnetic material. Equation (13) from Appendix A is repeated here for convenience.

\[
\tau_p > \frac{S_w}{H_o} \left(\frac{n^2}{n-1}\right).
\]

Thus, while evaporation techniques can reduce size and power requirements, miniaturization does not, of itself, bring an increase in speed.

For the materials considered in the size example, the outlook is not cheering. Substitution of those values of \(H_o\) and \(S_w\) into (13) yields a minimum prime time of 8 psec. A complete shift operation (two transfers) would require slightly in excess of 16 psec. The answer to this problem lies in finding magnetic materials with improved properties. Of the two, \(H_o\) seems to offer the most promise, i.e., \(H_o\) can be varied over a considerable range by altering the composition and method of depositing. While considerable effort has been expended in this area, much of it has had as a goal memory devices where (to reduce power requirements) it is desirable to minimize \(H_o\). Films especially composed for TFT use might have threshold coercivities as high as ten oersteds. If we assume such films to meet reasonable requirements on the other magnetic parameters, \(B_{R,w}\), \(S_w\), and loop squareness, shift operation times on the order of 1 µsec seem feasible.
Power

Power requirements for the TFT will be modest as the energy required to reverse the flux in a magnetic element is proportional to the amount of magnetic material involved. Gianola\(^5\) gives, as the average power for the advance pulse

\[
P = \frac{S \cdot \phi \cdot L \cdot 10^{-7}}{\pi \cdot t \cdot T}
\]

where \(S\), \(\phi\), and \(L\) have been previously defined. \(T\) is the repetition interval, \(t\) is the time of the advance pulse and \(P\) is power in watts. Power for the prime pulse is small compared to the advance pulse power and can conveniently be neglected.

Applying (15) to the initial design of the section on size yields a power of 57 \(\mu\)W for an advance pulse of 1 \(\mu\)sec and a repetition interval of 16 \(\mu\)sec. Scaling down of the second kind (where thicknesses are held constant) will reduce the power per element at the same rate as the area is reduced, i.e., power per unit area is unchanged. Scaling of the first kind results in an improved power/area figure.

Increasing the speed of operation by a factor of ten increases the power requirement by one hundred, bringing the power level up to about 1.1 \(w/cm^2\). Speed increases beyond this might require the substrate to be cooled or a deliberately reduced packing density.

Conclusion

For the shift register design considered and with materials currently available, it seems likely that TFT's can be constructed with a surface packing density of about 200 elements/cm\(^2\) and a speed of 8 \(\mu\)sec/operation.
Improvement in both of these figures will come about largely through the use of improved materials especially composed for TFT use.