A CURRENT MODE DA CONVERTER

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ABSTRACT

This report describes the design of a digital to analog converter using a current driven ladder instead of the more conventional voltage driven technique.

The constant current source is a standard Darlington configuration which is easily temperature compensated.

The converter specifications include a maximum worst case absolute error of less than 0.01%, long term stability better than 0.008%, 0 offset voltage, and a setting time of less than 1.8 μs. No trimming components are used.
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INTRODUCTION

One of the more popular digital to analog conversion (DA) techniques is the resistive ladder technique shown in Figure 1. The inputs to the ladder are switched between ground and some reference voltage. This technique, therefore, may be referred to as a voltage operated ladder.

The purpose of this paper is to investigate a DA technique using a current operated ladder. The technique will be analyzed in detail, the
sources of error identified, and finally the results of the analysis will be used in the design of a 10-bit DA converter.

CIRCUIT ANALYSIS

The circuit diagram for a \((n+1)\) bit, ladder type, current operated converter is shown in Figure 2. The current sources each supply a current \(I\) to the ladder when switch \(a_i\) is closed. Switch \(a_i\) will be closed if the corresponding bit in the digital input is a "1", and open if the bit is a "0". \(a_0\) is the least significant and \(a_n\) the most significant bit of the digital input. Each current source has the output admittance \(Y_o\). The analog output voltage is taken from node \(n\).
Before deriving the general expression for the analog output voltage, it will be helpful to simplify the circuit in Figure 2 to that of Figure 3 via the following relationships.

\[ \alpha = RY_o \]  
\[ V_{cc} = \frac{V_c}{Y_o} = \frac{V_c}{1+2\alpha} \]  
\[ R_x = \frac{2R}{1+2\alpha} \]  

\[ \frac{V_c}{1+a} \]

Figure 3. Simplified Converter.
Consider any node \( i (i \neq o, n) \) as shown in Figure 4.

\[
V_i = V_{cc} - I_i R_x
\]  
(4)

\[
I_i = a_i I + \frac{V_i-V_{i+1}}{R} - \frac{V_{i-1}-V_i}{R}
\]  
(4a)

Substituting Eq. (4a) into Eq. (4) and making use of Eqs. (2) and (3) gives

\[
V_i = \frac{V_{cc} - a_i I_2 R}{5+2\alpha} + \frac{2V_{i+1}}{5+2\alpha} + \frac{2V_{i-1}}{5+2\alpha}.
\]  
(4b)

Figure 4. Node i.

A similar treatment of nodes o and n will yield the following relationships:
Using Eqs. (4b) and (4c) and considerable algebra, it can be shown that the voltage at any node \( m \) (\( m = 0 \) through \( m = n-1 \)) is given by the following:

\[
V_m = \frac{1}{D_m} \left[ \frac{V_0 - a IR}{2 + \alpha} + \frac{V_n - a IR}{2 + \alpha} \right]
\]

(4c)

(4d)

where

\[
D_i = (5 + 2\alpha)D_{i-1} - 4D_{i-2}
\]

(5a)

\[
D_0 = 2 + \alpha
\]

(5b)

\[
D_{-1} = \frac{1}{2}
\]

(5c)

Substituting Eq. (5) with \( m = n-1 \) into Eq. (4d) and solving for \( V_n \) yields

\[
V_n = \frac{2^n}{D_0 D_{-1} - 2D_{-2}} \left[ V_0 \left\{ \frac{D_{n-1}}{2^n} + \frac{1}{2} \left[ 1 + \sum_{i=1}^{n-1} \frac{D_{i-1}}{2^i} \right] \right\} - \sum_{i=0}^{n} \frac{D_{i-1}}{2^i} a_i \right] .
\]

(6)

Let \( k_i = \frac{D_{i-1}}{2^i} \).

(6a)

Eq. (6) then becomes:

\[
V_n = \frac{1}{2(D_0 k_n - k_{n-1})} \left[ V_0 (2k_{n+1} + \frac{1}{2} \sum_{i=1}^{n-1} 2k_i) - \sum_{i=0}^{n} 2k_i a_i \right] .
\]

(6b)

Values of \( 2k_i \) are determined from Eq. (6a) and Eq. (5a). Note that \( D_0 \) and \( D_{-1} \) are defined by Eqs. (5b) and (5c), respectively.
The following examples illustrate the calculation of $2k_i$.

\[ i = 0 \quad 2k_0 = 2 \frac{D_0-1}{2^0} = 1 = 2^0 \]

\[ i = 1 \quad 2k_1 = 2 \frac{D_0}{2^1} = 2+\alpha = 2^1+\alpha \]

\[ i = 2 \quad 2k_2 = 2 \left[ \frac{D_1}{2^2} \right] = \frac{1}{2} \left[ (5+2\alpha)(2+\alpha) - 4 \left( \frac{1}{2} \right) \right] \]

\[ = \frac{1}{2} [8+9\alpha+2\alpha^2] \quad . \]

It will be assumed in all calculations that

\[ \alpha \leq .001 \quad . \]

This assumption can quite easily be met as will be shown later. Therefore, all $\alpha^2$ and higher order terms that arise in calculations for $2k_i$ can be neglected. Therefore:

\[ 2k_2 \approx \frac{1}{2} [8+9\alpha] = 2^2 + 4.5\alpha \quad . \]

Note that:

\[ 2k_1 = 2^i + j_i \alpha \quad . \]

Values of $2k_i$ are summarized in Table I.
Consider the factor \( \frac{1}{2(D - k - k - n)} \) in Eq. (6b).

\[
\frac{1}{2(D - k - k - n)} \rightarrow \frac{1}{2^n (3/2 + \alpha')} + \alpha (2j - j - n - 1) + j - \alpha^2.
\]

From values of \( j \) in Table I and making use of assumption (7), the above expression becomes

\[
\frac{1}{2(D - k - k - n)} \approx \frac{1}{2^n (3/2)}.
\]

Similarly, it may be shown, for the other factors in Eq. (6b)

\[
2k_n + 1 + \frac{1}{2} \sum_{i=1}^{n-1} 2k_i = 2^n (3/2) + \alpha \left[ j_n + \frac{1}{2} \sum_{i=1}^{n-1} j_i \right] \approx 2^n (3/2),
\]

\[
\sum_{i=0}^{n} 2k_i a_i = \sum_{i=0}^{n} 2^j a_i + \alpha \sum_{i=0}^{n} j_i a_i.
\]
Making use of the above approximations, Eq. (6b) becomes

\[ V_n = V_c - \frac{IR}{2^{n(3/2)}} \left[ \sum_{i=0}^{n} 2^i a_i + \alpha \sum_{i=0}^{n} j^i a_i \right]. \tag{9} \]

Equation (9) is the basic converter equation and it shows that for perfect DA conversion, infinite output impedance is required of the current sources \( \alpha = 0 \).

Assuming \( \alpha = 0 \), the following points of interest are noted:

a) \( V_n = V_c \) for a digital input of 0 (all \( a_i = 0 \));

b) \( V_n \approx V_c - \frac{4}{3} IR \) for a digital input of \( 2^{n+1} - 1 \) (all \( a_i = 1 \));

c) The total voltage swing \( \Delta V \approx -\frac{4}{3} IR \);

d) For each unit change in the digital input, the output analog voltage will change by an amount \( \frac{IR}{2^{n(3/2)}} \). This quantity is called the analog step size. The factor \( \frac{1}{2^{n(3/2)}} \) is sometimes referred to as the scale factor of the converter.

Table II shows the fractional value of current from each current source (10 bit A D) flowing in each vertical resistor of the ladder. From this data the maximum ladder voltage distribution curve in Figure 5 may be obtained. Note that the maximum voltage drop occurs for the center stages. This fact must be considered in the design of the current sources for the prevention of current source saturation.
\[ \frac{1}{2} \]

**Table II. Ladder Current Distribution**

<table>
<thead>
<tr>
<th>( I_0 )</th>
<th>( I_1 )</th>
<th>( I_2 )</th>
<th>( I_3 )</th>
<th>( I_4 )</th>
<th>( I_5 )</th>
<th>( I_6 )</th>
<th>( I_7 )</th>
<th>( I_8 )</th>
<th>( I_9 )</th>
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<tbody>
<tr>
<td>( \frac{1}{768} )</td>
<td>( \frac{1}{384} )</td>
<td>( \frac{1}{192} )</td>
<td>( \frac{1}{96} )</td>
<td>( \frac{1}{48} )</td>
<td>( \frac{1}{24} )</td>
<td>( \frac{1}{12} )</td>
<td>( \frac{1}{16} )</td>
<td>( \frac{2}{3} )</td>
<td></td>
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<tr>
<td>( \frac{1}{384} )</td>
<td>( \frac{1}{384} )</td>
<td>( \frac{1}{192} )</td>
<td>( \frac{1}{96} )</td>
<td>( \frac{1}{48} )</td>
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<td>( \frac{1}{12} )</td>
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<td>( \frac{1}{12} )</td>
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<tr>
<td>( \frac{1}{192} )</td>
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<td>( \frac{1}{96} )</td>
<td>( \frac{1}{48} )</td>
<td>( \frac{1}{24} )</td>
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<td>( \frac{1}{48} )</td>
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<tr>
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<td>( \frac{1}{6} )</td>
<td>( \frac{1}{3} )</td>
<td>( \frac{1}{6} )</td>
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<td>( \frac{1}{96} )</td>
<td>( \frac{1}{192} )</td>
<td>( \frac{1}{192} )</td>
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<tr>
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<td>( \frac{1}{24} )</td>
<td>( \frac{1}{48} )</td>
<td>( \frac{1}{96} )</td>
<td>( \frac{1}{192} )</td>
<td>( \frac{1}{384} )</td>
<td>( \frac{1}{384} )</td>
</tr>
<tr>
<td>( \frac{2}{3} )</td>
<td>( \frac{1}{6} )</td>
<td>( \frac{1}{12} )</td>
<td>( \frac{1}{24} )</td>
<td>( \frac{1}{48} )</td>
<td>( \frac{1}{96} )</td>
<td>( \frac{1}{192} )</td>
<td>( \frac{1}{384} )</td>
<td>( \frac{1}{768} )</td>
<td>( \frac{1}{768} )</td>
</tr>
</tbody>
</table>

| TOTAL \( (K) \) | \( 1.333 \) | \( .832 \) | \( .912 \) | \( .951 \) | \( .949 \) | \( .949 \) | \( .951 \) | \( .912 \) | \( .832 \) | \( 1.333 \) |

\( K = \) the factor, which, when multiplied by \( I \), gives the maximum current which flows in each vertical resistor
Figure 5. Ladder Voltage Distribution (All $a_i = "1"$)
ERROR ANALYSIS

The converter error is defined by Eq. (10)

\[ \text{ERR} = \frac{dV}{V} \]

\[ \frac{n(x)}{n(x)} \]

where \( V_n(x) = \text{converter output voltage for a digital input of } x \). Or in terms of Eq. (9):

\[ V_n(x) = V_c - \frac{IR}{2^n(3/2)} \left[ x + \alpha J(x) \right] \]

where

\[ J(x) = \sum_{i=0}^{n} j_i a_i(x) \] \tag{10a}

Differentiating the above equation,

\[ dV_n(x) = dV_c - \frac{IR}{2^n(3/2)} \left[ dx + \alpha dJ(x) + J(x) d\alpha \right] - \left[ \frac{x + \alpha J(x)}{2^n(3/2)} \right] [R dI + I dR]. \]

But \( dx \) and \( dJ(x) = 0 \); therefore:

\[ dV_n(x) = dV_c - \frac{IR}{2^n(3/2)} \left[ x + \alpha J(x) \right] \left[ \frac{J(x)}{x + \alpha J(x)} d\alpha + \frac{dI}{I} + \frac{dR}{R} \right] \]

\[ = dV_c + V_n(x) \left[ \frac{J(x)}{x + \alpha J(x)} d\alpha + \frac{dI}{I} + \frac{dR}{R} \right]. \]

But \( d\alpha = RdY_o + Y_o dR = \alpha \left( \frac{dY}{Y_o} + \frac{dR}{R} \right) \). Making this substitution and rearranging terms,

\[ \frac{dV}{V} = \frac{dV_c}{V} + \frac{dI}{I} + \frac{x + 2\alpha J(x)}{x + \alpha J(x)} \frac{dR}{R} + \frac{aJ(x)}{x + \alpha J(x)} \frac{dY}{Y_o}. \]
This expression is true for all inputs \((x)\) greater than \(0\). Also it may be shown that:

\[
\frac{x+2\alpha J(x)}{x+\alpha J(x)} = 1 \quad \text{for all } x > 0.
\]

Therefore,

\[
\frac{dv_{\nu(x)}}{v_{\nu(x)}} = \frac{dv_c}{v_{\nu(x)}} + \frac{dI}{I} + \frac{dR}{R} + \frac{e^J(x)}{x+\alpha J(x)} \frac{dy_o}{y_o}
\]

(10b)

Assuming \(dv_c = 0\), this expression will be maximum when the digital input is a maximum (all \(a_i = 1\)) or \(x = 2^{n+1}-1\).

\[
\frac{\text{ERR}_{\text{max}}}{v_{\nu(\text{max})}} = \frac{dv_c}{v_{\nu(\text{max})}} + \frac{dI}{I} + \frac{dR}{R} + \frac{\alpha J_{\text{max}}}{2^{n+1}-1+\alpha J_{\text{max}}} \frac{dy_o}{y_o}.
\]

(11)

<table>
<thead>
<tr>
<th>No. Bits</th>
<th>(J_{\text{max}})</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>5239</td>
</tr>
<tr>
<td>11</td>
<td>11839</td>
</tr>
<tr>
<td>12</td>
<td>26399</td>
</tr>
</tbody>
</table>

Table III. Values of \(J_{\text{max}}\).

Values of \(J_{\text{max}}\) found using Eq. (10a) and the values of \(j_i\) in Table I, are summarized in Table III for 10, 11, and 12-bit converters.

Since \(I\) and \(Y_o\) are determined by the current source, it is necessary to know the actual circuit before the analysis can be completed.
CURRENT SOURCE

The current source used in the converter is the Darlington circuit, shown in Figure 6. This circuit was chosen for possessing

1) very stable current gain, and
2) relatively high output impedance.

Transistors $T_1$ and $T_2$ should both be silicon planer expitaxial transistors chosen for

1) very low $I_{co}$,
2) very high output impedance, and
3) high $h_{fe}$; and in the case of $T_2$, high $h_{fe}$ at very low currents.

For the circuit of Figure 6, it can be shown that

$$I = \alpha I_e + I_{co}$$

(12)
where

\[ I = \frac{V_{ee} + V_r - (V_{be_1} + V_{be_2})}{R_e} \]  \hspace{2cm} (13)

\[ I_{co} = I_{co_1} (1 - \alpha_t) + I_{co_2} \approx I_{co_2} \]  \hspace{2cm} (14)

\[ \alpha_t = \frac{h_{fe_1}}{1 + h_{fe_1}} + \frac{h_{fe_2}}{1 + h_{fe_2}} - \frac{h_{fe_1} h_{fe_2}}{(1 + h_{fe_1})(1 + h_{fe_2})} \]  \hspace{2cm} (15)

Substituting Eq. (13) and (14) into Eq. (12) yields

\[ I = \frac{\alpha_t}{R_e} (V_{ee} + V_r - V_{be_1} - V_{be_2}) + I_{co_2} \]

Differentiating and dividing by I

\[ \frac{dI}{I} = \frac{\alpha_t}{R_e} \left[ dV_{ee} + dV_r - dV_{be_1} - dV_{be_2} \right] + \frac{\alpha_t}{I} d\alpha_t - \frac{\alpha_t}{I} \frac{dR_e}{R_e} - \frac{I_{co_2}}{I} \frac{dI_{co_2}}{I_{co_2}} \]

This equation can be simplified via the following approximations:

\[ \alpha_t \approx 1 \]

\[ I = \frac{\alpha_t}{R_e} \frac{V_{ee} + V_r - (V_{be_1} + V_{be_2})}{R_e} \]

Then

\[ \frac{dI}{I} \approx \frac{dV_{ee} + dV_r - dV_{be_1} - dV_{be_2}}{V_{ee} + V_r - (V_{be_1} + V_{be_2})} + \frac{\alpha_t}{\alpha_t} \frac{dR_e}{R_e} + \frac{I_{co_2}}{I} \frac{dI_{co_2}}{I_{co_2}} \]  \hspace{2cm} (16)

For the circuit of Figure 6 it may be shown that the output admittance is given by Eq. 17:
\[ Y_o = h_{ob_2} + h_{ob_1}(1-\alpha_2) + \frac{(h_{rb_1} + h_{rb_2} + h_{lb_1}h_{ob_2})(\alpha_1 + \alpha_2 - \alpha_1\alpha_2)}{R + h_{lb_1}h_{ob_2}} \]  

(17)

where the \(h_i\)'s are the small signal, common base \(h\) parameters for \(T_1\) and \(T_2\).

For typical values of these parameters and values of \(R\) in \(10k\Omega\) range or larger, Eq. (17) becomes

\[ Y_o \approx h_{ob_2} + h_{ob_1}(1-\alpha_2) \]  

(17a)

also

\[
\frac{dY_o}{Y_o} = \frac{h_{ob_2}}{Y_o} \frac{dh_{ob_2}}{h_{ob_2}} + \frac{(1-\alpha_2)h_{ob_1}}{Y_o} \frac{dh_{ob_1}}{h_{ob_1}} - \frac{\alpha_2 h_{ob_1}}{Y_o} \frac{d\alpha_2}{\alpha_2} .
\]  

(17b)

Substitution of Eqs. (16) and (17b) into Eq. (11) will yield the complete expression for the converter error.

Finally, to complete the error analysis, the temperature coefficient (TC) of the converter must be determined. This may be found by dividing Eq. (11) by \(dt\).

\[
TC = \frac{1}{V(n(\text{max})/V_{n(\text{max})})} \frac{dV}{dt} = \frac{1}{V(n(\text{max})/V_{n(\text{max})})} \frac{dV}{dt} + \frac{1}{R} \frac{dR}{dt} + \frac{\alpha J(\text{max})}{2^n+1} \frac{1}{\frac{dY_o}{Y_o}} .
\]  

(18)

An approximate TC may be found by assuming

\[
\frac{dV}{dt} = \frac{dY_o}{dt} = 0.
\]

Then,

\[
TC \approx \frac{1}{I} \frac{dT}{dt} + \frac{1}{R} \frac{dR}{dt} .
\]
But \( \frac{dR}{dt} = \theta_R R \) where \( \theta_R \) = temperature coefficient of the ladder resistors.

Therefore:

\[
TC = \frac{1}{I} \frac{dI}{dt} + \theta_R .
\]

(18a)

The effect of temperature on the current is determined by dividing Eq. (16) by \( dt \).

\[
\frac{1}{I} \frac{dI}{dt} = \frac{dV_{ee}}{dt} + \frac{dV_{r}}{dt} - \frac{dV_{be1}}{dt} - \frac{dV_{be2}}{dt} + \frac{d\alpha}{dt} - \frac{1}{R_e} \frac{dR_e}{dt} + \frac{1}{I} \frac{dI_{co2}}{dt} .
\]

If \( T_1 \) and \( T_2 \) are both silicon planar transistors, then

\[
\frac{dV_{be1}}{dt} \sim \frac{dV_{be2}}{dt}
\]

Also

\[
\frac{dR_e}{dt} = \theta_{R_e} \quad \text{where } \theta = \text{temperature coefficient of } R_e .
\]

Making these substitutions:

\[
\frac{1}{I} \frac{dI}{dt} \approx \frac{dV_{ee}}{dt} + \frac{dV_{r}}{dt} - \frac{2dV_{be}}{dt} + \frac{d\alpha}{dt} - \theta + \frac{1}{I} \frac{dI_{co2}}{dt} .
\]

(19)

DESIGN EXAMPLE

Consider now the actual design of a 10-bit A to D converter using the above results.
1. Power Supplies

a) Choose $V_c = 0$. This choice eliminates the first term of Eq. (11) and (18).

b) Choose $V_{ee} = -300$. This large value will reduce the effects of $V_{be}$ as shown in Eq. (16).

c) From Eq. (19) it is noted that if $\frac{dV_r}{dt} = \frac{2dV_{be}}{dt}$, then the effects of temperature on the current will be greatly reduced. A circuit for $V_r$ that meets this requirement is shown in Figure 7, where $D_1$ is an 8.2 volt diffused silicon zener diode having a temperature coefficient of approximately $4.4 \text{ mV/}^\circ\text{C}$.

For the circuit in Figure 7:

$$\frac{dV_r}{dt} = \frac{dV_z}{dt} = 4.4 \text{ mV/}^\circ\text{C} \approx \frac{2dV_{be}}{dt}$$
and

$$\frac{dV}{V} = -dV = -Z \frac{dI}{I}$$

where \( Z_r \) = zener diode impedance at \( = 10 \) ma

\( Z_r \approx 10\Omega \)

\( I \approx \frac{V_{ee}}{R} \)

then

$$\frac{dV}{V} \approx .009 \frac{dV_{ee}}{R} = \frac{.009}{30 \times 10^3} \frac{dV_{ee}}{R} = -.3 \times 10^{-6} dV_{ee}.$$  

2. I and \( R_e \)

A value of 5ma is chosen for I. Then for \( V_{ee} = 300\)v; \( R_e = 60\)k.

The following additional specifications are set for \( R_e \):

- Power rating = 3 watts (twice the actual dissipation)
- Resistance Tolerance = \( \pm .01\% \)
- Ratio Tolerance = \( \pm .005\% \)
- \( \theta = \pm 5\)ppm.

3. Ladder Resistors

R should be small to keep \( \alpha \) small (see Eq. (1) and (9)) and for fast conversion times.

R should be large enough, however, to provide an easily detectable change in the analog output for each increment of the digital input.

For this design choose:

\( R = 500\Omega \) (non-inductive)

Resistor Tolerance = \( \pm .01\% \)

\( \theta = \pm 5\)ppm.
4. Transistors

\[ T_1 = 2N3227 \]
\[ T_2 = 2N2586 \]

The pertinent characteristics of these transistors are summarized in Table IV. Manufacturer's data was used for \( I_{co} \) and \( h_{fe} \) while \( V_{be} \) and \( h_{ob} \) data was obtained in the laboratory.

From the table, the following design values are set:

For \( T_1 \)

\[ V_{be} = 700\text{mv} \pm 10\text{mv} \]
\[ h_{ob} = .6\mu\text{mho} \]
\[ \frac{dh_{ob}}{h_{ob}} = \pm 50\% \text{ (assumed)} \]
\[ I_{co} = 2\mu\text{a} \]
\[ \frac{dI_{co}}{dt} = 10\% \frac{I_{co}}{C^o} \]
\[ h_{fe} = 80 \text{ to } \infty \]
\[ \frac{dh_{fe}}{dt} = 10\% \frac{h_{fe}}{C^o} \]

For \( T_2 \)

\[ V_{be} = 500\text{mv} \pm 10\text{mv} \]
\[ h_{ob} = .025\mu\text{mho} \]
\[ \frac{dh_{ob}}{h_{ob}} = \pm 50\% \text{ (assumed)} \]
\[ I_{co} = 2\mu\text{a} \]
\[ \frac{dI_{co}}{I_{co}} = 100\% \text{ (assumed)} \]
\[ h_{fe} = 100 \text{ to } \infty \]
\[ \frac{dh_{fe}}{dt} = 10\% \frac{h_{fe}}{C^o} \]
Table IV. Transistor Characteristics

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<tr>
<th>TYPE</th>
<th>PARAMETER</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>TEST CONDITIONS</th>
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<tr>
<td>2N3227</td>
<td>$V_{be}$ (volts)</td>
<td>.702</td>
<td>.705</td>
<td>.706</td>
<td>$V_{cb} = 8v$</td>
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<tr>
<td></td>
<td>$I_{c}$</td>
<td>$I_{c} = 5ma$</td>
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<td></td>
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<tr>
<td></td>
<td>$f$</td>
<td>$f = 1kc$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$h_{ob}$ ($\mu$mho)</td>
<td>.485</td>
<td>.588</td>
<td>.776</td>
<td>$V_{cb} = 20v$</td>
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<td>$I_{co}$ (na)</td>
<td>200</td>
<td>$I_{c} = 5ma$</td>
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<td></td>
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<tr>
<td></td>
<td>$h_{fe}$</td>
<td>95</td>
<td>$I_{c} = 5ma$</td>
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<td></td>
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<tr>
<td>2N2586</td>
<td>$V_{be}$ (volts)</td>
<td>.486</td>
<td>.496</td>
<td>.596</td>
<td>$V_{cb} = 8v$</td>
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<td></td>
<td>$I_{c}$</td>
<td>$I_{c} = 10\mu$a</td>
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<td></td>
<td>$f$</td>
<td>$f = 1kc$</td>
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<td></td>
<td>$h_{ob}$ ($\mu$mho)</td>
<td>.023</td>
<td>.024</td>
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<td>$V_{cb} = 45v$</td>
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<td>$I_{co}$ (na)</td>
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<td>$I_{c} = 10\mu$a</td>
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<td></td>
<td>$h_{fe}$</td>
<td>120</td>
<td>$I_{c} = 10\mu$a</td>
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5. Calculations

a) Determine $Y_{o}$ from Eq. (17a)

$$Y_{o} = h_{ob2} + h_{ob1}(1-\alpha_2)$$

$$Y_{o} = .025 + .6(1 - \frac{100}{101})$$

$$Y_{o} = .031 \mu$mho

b) Find $\frac{dY_{o}}{Y_{o}}$ from Eq. (17b)

$$\frac{dY_{o}}{Y_{o}} = \frac{.025}{.031} (\pm 50) + (1 - \frac{100}{101})(.6) \frac{100}{.031} (\pm 50) - \frac{100}{.031} \frac{.6}{\alpha_2}$$

But $\frac{d\alpha_2}{\alpha_2} \approx 1\%$ ($\alpha$ varies from .99 to 1).

Therefore, omitting the last term,

$$\frac{dY_{o}}{Y_{o}} \approx \pm 40 \pm 10 = \pm 50\%$$
c) Find $\alpha$, using Eq. (1)

$$\alpha = RY_o$$

$$\alpha = 500(0.031) \times 10^{-6} = 15.5 \times 10^{-6}$$

d) Determine $\alpha_t$ from Eq. (15)

$$\alpha_{t_{\text{min}}} = \frac{80}{81} + \frac{100}{101} - \frac{80}{81} \frac{100}{101}$$

$$\alpha_{t_{\text{min}}} = 0.9998778$$

$$\alpha_{t_{\text{max}}} = 1 \quad (h_{fe1_{\text{max}}} = h_{fe2_{\text{max}}} = \infty)$$

$\alpha_t$ is then defined as

$$\alpha_t = 0.9999389 \pm 0.0000611$$

or

$$\frac{d\alpha_t}{\alpha} \approx 0.000611\%$$

e) Determine $\frac{dI}{I}$ from Eq. (16)

$$\frac{dI}{I} = \frac{dV_{ee} + dV_r}{300 + (-8.2) - (.7 + .5)} \pm 0.00000611 \pm 0.001 \pm \frac{2 \times 10^{-9}}{5 \times 10^{-3}}(1)$$

But $dV_r = -0.3 \times 10^{-6} dV_{ee}$

$$\frac{dI}{I} \approx \frac{dV_{ee}}{290.6} + \frac{20 \times 10^{-3}}{290.6} \pm 0.00010611$$

$$\frac{dI}{I} = \frac{dV_{ee}}{290.6} \pm 0.000175 = \frac{dV_{ee}}{V_{ee}} \pm 0.0175\%$$

This calculation shows that the % deviation in I is approximately .0175% plus the % variation of $V_{ee}$. Since $V_{ee}$ affects all stages, long term drifts in its value may be considered a change in the scale factor of the converter.
f) Determine converter accuracy from Eq. (11)

\[
% \text{error}(\text{max}) \approx \pm \left[ \frac{dV}{V_{ee}} + 0.175 \right] \pm 0.01 \pm \frac{(15.5 \times 10^{-6})(5239)}{2^{10} \cdot 1 + 15.5 \times 10^{-6} (5239)} \quad (50\%)
\]

\[
= \frac{dV}{V_{ee}} \pm 0.175 \pm 0.01 \pm 0.00415
\]

\[
% \text{error}(\text{max}) = \frac{dV}{V_{ee}} \pm 0.0317\% .
\]

g) Determine current variation due to temperature from Eq. (19)

\[
\frac{1}{I} \frac{dI}{dt} = \frac{dV_{ee}}{V_{ee} + V_{r}} - \frac{2dV_{be}}{(V_{be1} + V_{be2})} + \frac{d\alpha_t}{dt} - \frac{1}{I} \frac{dI}{co2} .
\]

But \( \frac{dV_t}{dt} \approx \frac{2dV_{be}}{dt} . \)

From Eq. (15),

\[
\frac{d\alpha_t}{dt} = \left( \frac{1}{1 + \h_{fe1}} \right) \left( \frac{1}{1 + \h_{fe1}} \right) \frac{2d\h_{fe1}}{dt} + \left( \frac{1}{1 + \h_{fe1}} \right) \left( \frac{1}{1 + \h_{fe2}} \right) \frac{2d\h_{fe2}}{dt} .
\]

From specifications for \( T_1 \) and \( T_2 \):

\[
\frac{d\h_{fe1}}{dt} = +\h_{fe1} 10\%/C^0
\]

\[
\frac{d\h_{fe2}}{dt} = +\h_{fe2} 10\%/C^0 .
\]

Therefore

\[
\frac{d\alpha_t}{dt} \approx \pm \frac{2}{101} \left( \frac{1}{81} \right) 800 + \frac{2}{101} \left( \frac{1}{81} \right) 1000 \% / C^0
\]

\[
\frac{d\alpha_t}{dt} \approx \pm 0.0025 \% / C^0 ;
\]
also

\[ \frac{1}{I} \frac{dI_{co}}{dt} = \frac{I_{co}}{I} 10\%/C^0 \]

\[ \frac{1}{I} \frac{dI_{co}}{dt} = \frac{2 \times 10^{-9}}{5 \times 10^{-3}} 10\%/C^0 = 4 \times 10^{-6}\%/C^0. \]

This can be ignored. Also

\[ \frac{dV_{ee}}{dt} = T_v V_{ee} \]

where \( T_v \) = temperature coefficient of \( V_{ee} \) in \%/C^0.

\[ \frac{1}{I} \frac{dI_{\sim}}{dt} = - \frac{T_v V_{ee}}{V_{ee} + V_r - (V_{be1} + V_{be2})} + \frac{d\alpha_t}{\alpha_t} - \theta \]

or

\[ \frac{1}{I} \frac{dI_{\sim}}{dt} = T_v + \frac{d\alpha_t}{dt} - \theta \]

\[ \frac{1}{I} \frac{dI_{\sim}}{dt} \approx T_v + 0.0025 + 0.0005 = T_v + 0.003. \]

Substituting this value and the value of \( \theta_R \) into Eq. (18a) yields for the temperature coefficient

\[ T_C \approx T_v \pm 0.0035%/C^0 \]

The complete circuit diagram for the converter is shown in Figure 8. Transistor \( T_3 \) provides the switching action for the current source, i.e., a +3 volt input to \( T_3 \) will turn the current source "on," while a 0 volt signal will turn the current source "off."

This converter was constructed in the laboratory and the experimental results obtained are summarized in Table V.
Figure 8. Bit DA Converter
Table V. Experimental Results.

<p>| | |</p>
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<th></th>
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</thead>
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<tr>
<td>Offset Voltage</td>
<td>0.00000 volts</td>
</tr>
<tr>
<td>Max Output Voltage</td>
<td>3.22770 volts</td>
</tr>
<tr>
<td>% Error (max)</td>
<td>less than .01%</td>
</tr>
<tr>
<td>Stability (8 hours)</td>
<td>less than .008%</td>
</tr>
<tr>
<td>Temperature Coefficient (TC)</td>
<td>.0015 %/C°</td>
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<tr>
<td>Converter Settling Time</td>
<td>&lt;1.8μs</td>
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<tr>
<td>Analog Step Size</td>
<td>3.13mv ± .06mv</td>
</tr>
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</table>

Conclusion

It has been demonstrated that relatively high DA converter accuracy may be obtained with the use of a current operated ladder.

Further, this technique offers the following advantages:

1. High accuracy may be obtained without trimming and components.
2. Only three values of precision resistance are required; two in the ladder and one in the current source.
3. A simple current source which inherently has the important characteristics of a very high output impedance, very stable current gain, and is easy to duplicate.
4. A simple temperature compensation technique.

The disadvantages of this technique are:

1. The requirement of a large supply voltage for the current sources.
2. The rather heavy dependence on the stability of this supply.
3. The requirement of a high wattage resistor in the current sources.
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```
A CURRENT MODE DA CONVERTER

This report describes the design of a digital to analog converter using a current-driven ladder instead of the more conventional voltage-driven technique.

The constant current source is a standard Darlington configuration which is easily temperature compensated.

The converter specifications include a maximum worst case absolute error of less than .01%, long-term stability better than .008%, 0 offset voltage, and a setting time of less than 1.8 μs. No trimming components are used.
### Instructions

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<tr>
<th>LINK A</th>
<th>LINK B</th>
<th>LINK C</th>
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<tr>
<td>WT</td>
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**Digital analog converter**

**Current-operated ladder type**

### Key Words

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<th>WT</th>
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