ANALYSIS AND DESIGN OF HIGH POWER DENSITY RESONANT SWITCHED-CAPACITOR CONVERTERS

BY

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THESIS

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ABSTRACT

This thesis is motivated by the desire for power electronics designers to create power electronic converters that have high energy density (are very small) and high efficiency (few losses). Switched-capacitor (SC) topologies that utilize the high energy density of capacitors are a candidate for fulfilling these two criteria. However, there are inherent limitations in conventional switched capacitor converters where a designer is required to make a trade-off between efficiency and capacitor energy density utilization. One way to overcome this obstacle is to utilize resonance in a SC converter. This work proposes a resonant, voltage step-up Dickson SC converter. A single inductor is utilized to achieve zero current switching of all transistors, which allows for high switching frequency and high conversion efficiency. A split-phase control scheme is used in order to eliminate the current transients associated with the Dickson SC converter and the resultant power loss. Employing these techniques, a Dickson SC converter prototype is implemented with GaN transistors. The converter is able to achieve high power density while maintaining high efficiency because of the control techniques that are employed.
To my family and friends, for their love and support.
First and foremost, I thank all my family and friends who have supported me over the years. Your kindness, love, and encouragement inspire me, motivate me, and keep me grounded. I would like to give a special thank you to my advisor, Robert Pilawa-Podgurski for mentoring me, pushing me to aim for lofty goals, and setting an example of how hard one should work and how passionate one should be. I aspire to be like you one day. Finally, I also thank the entire Pilawa research group for their insights and compassion. Your wisdom has been invaluable to me, and I will always look back on my time at Illinois with nostalgia.
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Switched-capacitor (SC) converters have the potential to increase the power density of power electronic circuits [1, 2]. This is possible because capacitors have energy densities that are orders of magnitude greater than those of inductors, and in many cases, capacitors are also lighter and less costly. SC converters can also achieve high efficiency at high voltage conversion ratios due to the modular nature of the converter topologies. Because of these advantages, SC converters have been an active topic of research in the power electronics community [3, 4, 2, 5].

However, there are drawbacks associated with SC converters that must be addressed. One major challenge is the inherent charge sharing loss in the slow switching limit region of operation [6, 7, 8, 2], during the charging and discharging process of capacitors. When charging a capacitor with a voltage source or another capacitor, a transient current spike occurs due to the voltage difference between the two components, which causes high power loss. As a result, SC converters need high switching frequencies or large capacitors in order to minimize this voltage difference and the associated losses. Therefore, for highly efficient SC converters, the high energy density of capacitors is not utilized to its full potential due to the small capacitor voltage ripple required for efficient operation. Increasing the switching frequency introduces a trade-off between the switching losses and these charging sharing losses, while increasing the capacitor values introduces a trade-off between power density and the charge sharing losses. These trade-offs are fundamental to conventional SC converters and cannot be overcome with traditional design and control techniques.

Soft-charging SC converters [9, 10, 11, 12] and resonant SC converters [13, 14, 15, 16, 3, 17, 18] have been proposed to eliminate these current transients, both by introducing inductive elements in the SC converters. Resonant SC converters can eliminate the charge sharing loss while simultaneously
reducing the switching losses by achieving zero current switching. In resonant operation, the current through the switches naturally ramps down to zero before the switches are turned off, and current ramps up from zero after switches are turned on, eliminating the impulse current that causes the charge sharing loss. It also minimizes the loss incurred by having simultaneous high voltage across a switch and current through it during switching. Therefore, a resonant SC converter has the potential to achieve both higher efficiency and higher power density than a conventional SC converter. Resonant SC converters can be constructed with one [19, 14, 18] or more [20, 16, 15, 21] inductors. Considering the difficulty in parameter matching and desire for low converter volume, this thesis focuses on resonant SC converters with only one resonating inductor.

In order to achieve both high power density and high efficiency, a designer must carefully choose a SC topology. Important considerations include voltage ratings of switches and capacitors and the number of switches, capacitors, and inductor(s) required for resonant operation. This work presents a resonant, step-up Dickson SC converter with a single inductor. The device rating requirements in a Dickson converter also make it an attractive option. Zero current switching is realized on all switches, made possible by an inductor at the low voltage side and the split-phase control scheme [22] which is the key enabling technology that allows fully resonant operation with a single inductor. A 25 V to 100 V, 1.2 MHz converter prototype is implemented to demonstrate the effectiveness of the approach.
2.1 Two-Phase Resonant Dickson Converter Characteristics

The Dickson converter [23, 24] is a popular SC converter topology due to its efficient utilization of switches [25]. A circuit diagram of a 1-to-4 resonant Dickson converter is shown in Fig. 2.1. In phase 1 switches \( S_2, S_4, S_6, \) and \( S_8 \) are closed, and in phase 2, switches \( S_1, S_3, S_5, \) and \( S_7 \) are closed. The resultant equivalent circuit phases can be seen in Fig. 2.2. This topology achieves a 1-to-4 voltage conversion ratio while maintaining relatively low switch stresses. All switches are rated for the input (low voltage side) voltage except for switches \( S_6 \) and \( S_7 \), which are rated for twice the input voltage. The low voltage stress on the switches enables the Dickson converter to operate at high switching frequencies, thereby reducing the volume of the passive components and increasing the power density of the converter. However, the flying capacitors \( C_1, C_2, \) and \( C_3 \) are rated at \( V_{in}, 2 \times V_{in}, \) and \( 3 \times V_{in} \) respectively, having relatively large energy storage requirements and offset-

![Figure 2.1: Circuit diagram of a resonant 1-to-4 Dickson SC converter.](image)
Figure 2.2: Two-phase operation of a resonant 1-to-4 Dickson converter.

ting the benefit of high switching frequency. Therefore, Dickson converters would greatly benefit from resonant techniques, which reduce losses caused by current transients and significantly reduce the required capacitance of flying capacitors.

Resonance can be introduced in a Dickson converter by adding a small inductor in series with the input voltage source, as shown in Fig. 2.1. This concept is desirable because it could mitigate the undesirable current transients previously described. The cause of these lossy transients is well known [6, 7, 8, 2]. Since capacitors cannot change voltage instantaneously and energy is transferred from the input to output of a SC converter based on capacitors being charged by and discharged into other capacitors, capacitor voltage mismatches are applied across parasitic resistances of the converter. The addition of an inductor will reduce the magnitude of current transients caused by these voltage mismatches. This is because the rate of change of current in an inductor is proportional to the voltage across the inductor. The voltage mismatch is now across the inductor instead of being across parasitic resistances, which can greatly reduce losses in the converter.

This phenomenon can be shown by looking at the idealized model of a Dickson converter, which is shown in Fig. 2.3. The output impedance vs. frequency is plotted before and after adding the inductor in Fig. 2.4. To understand why the inductor is added, a Dickson converter without an inductor will be described first. At low frequencies, the output impedance (which is proportional to losses in the converter) approaches the slow switching limit (SSL) and is increasing exponentially because of the large spiky currents in the converter, as shown in Fig. 2.5. At high frequencies, the ou-
put impedance approaches the fast switching limit (FSL) which is a constant value. This is because the current within components during each phase is fairly constant as shown in Fig. 2.6. This phenomenon is well known in SC converters and gives a designer an inherent tradeoff between capacitor energy density utilization and efficiency.

In resonant operation, the inductor resonates with the flying capacitors of the converter, resulting in a rectified sinusoidal current through the inductor. Figure 2.7 illustrates this concept by showing the phase signal and input current of the proposed Dickson topology. As can be seen, the phase transitions occur at the moment the current becomes zero. Zero current switching eliminates the switching loss caused by the product of current through a switch and voltage across a switch at the switching instance because the current is zero. This increases system efficiency and enables increased switching fre-
Figure 2.7: Phase 1 signal and inductor current of the proposed SC converter.

As can be seen in the impedance plot (Fig. 2.4), resonant operation reduces the output impedance. This reduces losses in the converter allowing the converter to achieve higher power densities and higher efficiencies.

2.2 Two-Phase Resonant Dickson Converter

Limitations

Although the inductor successfully introduces a sinusoidal current waveform through resonance, current transients still occur in a two-phase Dickson converter as demonstrated in [26, 27] and shown in Fig. 2.8 and Fig. 2.9. This is because impulse current can circulate between parallel capacitor branches, and large current transients occur if two parallel branches are connected when the branches have different terminal voltages. As a result, resonant operation of the converter does not guarantee sinusoidal current in all the capacitors and switches at all times.
To further illustrate this, the capacitor voltage mismatch and capacitor current is shown in Fig. 2.10. Thus, current transients occur at the phase transitions even though the bulk of the switch and capacitor current waveforms take the shape of a rectified sinusoid. The current spike in capacitor $C_1$ occurs at the transition due to the charge sharing between $C_1$ and the series connection of $C_2$ and $C_3$ (Fig 2.2). In Fig. 2.10, it is shown that $V_{C3} - V_{C2}$ does not equal $V_{C1}$ at the start of phase 2. This is discussed in detail in [22]. Similarly, current transients occur during the transition from phase 2 to phase 1 because $V_{C2} - V_{C1}$ does not equal $V_{Cout} - V_{C3}$ at the transition. The currents in other switches are not shown, but all have waveforms similar that that shown in Fig. 2.8. Thus, despite the resonating inductor current, current transients are still inevitable in a two-phase Dickson converter, and resonant operation brings limited benefits. It is for this reason that resonant operation of a Dickson SC Converter has to date not been widely used.
Figure 2.10: Capacitor voltage mismatch and capacitor current during resonant two-phase operation.
CHAPTER 3

SPLIT-PHASE CONTROL
IMPLEMENTATION IN THE DICKSON CONVERTER

3.1 Control Methodology

The work in [22, 28, 18] presented a solution to eliminate the current transient of the Dickson converters by using split-phase control. With split-phase control, each of the two typical phases is split into a primary phase and a secondary phase. In this work, this technique is combined with resonance to achieve zero current switching in all the switches of a Dickson converter. A diagram of the four phases as a result of the split-phase control can be seen in Fig. 3.1.

It can be seen that the primary phases (‘a’ phases) of the four phase switching sequence are the same as the phases in Fig. 2.2, while the secondary phases (‘b’ phases) circuit connections are a subset of the primary phases. The switching sequence implemented in this work is:

\[ \text{Phase 1b} \rightarrow \text{Phase 1a} \rightarrow \text{Phase 2b} \rightarrow \text{Phase 2a} \]

Since the direct transition between phase 1a and phase 2a results in mismatch voltages among capacitors, split-phase control works by selectively charging and discharging the capacitors in phase 1b and phase 2b so that KVL can be satisfied before the transition to the primary phases. For example, at the end of phase 1a, the capacitor voltages are as in the two-phase operation:

\[ V_{C1} > V_{C3} - V_{C2}. \]

Instead of transitioning directly to phase 2a, and incurring charge sharing losses, the circuit transitions to phase 2b first. As can be seen in Fig. 3.1, in phase 2b, \(C_2\) discharges and \(C_3\) charges, and thus, \(V_{C3} - V_{C2}\) increases. The turn-on of switch \(S_5\), which connects \(C_1\) to \(C_2\) and \(C_3\), is delayed until

\[ V_{C1} = V_{C3} - V_{C2}. \]
Therefore, when $S_5$ turns on, which marks the transition from phase 2b to phase 2a, the two capacitor branches have equal terminal voltage, satisfying KVL and eliminating the current transient. Similarly, switch $S_8$ is delayed from the original two-phase control to achieve the transition from phase 2a to 1b and then to 1a. In split-phase control, switches $S_5$ and $S_8$ operate as diodes, blocking negative current and allowing positive current. In a GaN transistor implementation, while zero current turn-on is not achieved on $S_5$ and $S_8$, these two switches only turn on when the voltage across them is zero, and thus zero voltage turn-on is achieved.

### 3.2 Split-Phase Simulation

Simulations were performed to verify and demonstrate the results of split-phase control. After split-phase is introduced, current spikes that were described in the previous chapter were eliminated. The analog to the figure that shows the capacitor voltage mismatch at the transition (Fig. 2.10) for
Figure 3.2: Capacitor voltage mismatch elimination and capacitor current during resonant split-phase operation.

split-phase control is seen in Fig. 3.2. As one can see, the voltage mismatch is eliminated by the delayed turn-on of the switch. Figures 3.3 and 3.4 show split-phase signals and corresponding switch currents. This further demonstrates that current transients are eliminated in these switches. Figure 3.5 shows capacitor $C_1$ current during split-phase control. The current spikes are eliminated, and the current waveform is much more sinusoidal than in the two-phase resonant version of the converter.

After applying this technique, we can look again at the output resistance in the idealized model of the SC converter. This is shown in Fig. 3.6. At the resonant point of operation, the output resistance is further reduced when using split-phase control. This is very important because these reduced losses allow the designer to use smaller capacitors (increased energy density) and achieve higher efficiencies.
Figure 3.3: Control signals and switch $S_5$ current in split-phase resonance.

Figure 3.4: Control signals and switch $S_8$ current in split-phase resonance.

Figure 3.5: Capacitor $C_1$ current in split-phase resonance.
Figure 3.6: Simulated output impedance of the Dickson converter with split-phase control.
CHAPTER 4

HARDWARE RESULTS OF A RESONANT SPLIT-PHASE CONTROLLED DICKSON CONVERTER

4.1 Hardware Setup

A prototype of the described 1:4 Dickson converter was built and tested in order to validate the proposed technique. The test setup block diagram is shown in Fig. 4.1. A PC is used to both program the microcontroller and communicate with differential multimeters (DMMs). The microcontroller has PWM outputs that control switches with open loop control. A power supply provides power to the circuit while a variable resistive load is used to load the converter. Both input and output power measurements are made with DMMs which measure current and voltage. With this data, efficiencies at various operating points can be calculated.

Figure 4.1: High level block diagram level test setup for prototype.
The microcontroller generates high resolution PWM waveforms for the six control signals. A logic level translator is needed for this prototype because the microcontroller signals are based on 3.3 V logic while the level shifters require 5 V logic signals. Gate drivers are then used to turn the transistors on and off according to the control method. This digital data flow process is shown in Fig. 4.2.

Two circuit prototypes will be shown that implemented the described circuit. A system schematic of the circuit can be seen in Fig. 4.3. LS refers to level shifters while GD references gate drivers. The first layout was made to be able to test a variety of different capacitors and inductors while the second revision is compact. The power stage of the first revision of the converter can be seen in Fig. 4.4 and the updated revision is seen in Fig. 4.5. The total volume of the power stage of the most recent revision is 0.0707 in$^3$, including the thickness of the PCB, but not including the level-shifting circuitry or the microcontroller. For reference, the total volume of the microcontroller and
level-shifters was 0.037 in³. These components were not optimized for size and were laid out for easy debugging on the PCB. Moreover, in a commercial implementation, they would likely be implemented in a single package. The PCB used in this design is standard thickness, 0.062 inches, and the maximum component height is 0.047 inches, which results in over half of the converter volume taken up by the PCB. Thus, a thinner PCB would greatly reduce converter volume.

To gain a better understanding of what components take up what portion of converter area, Fig. 4.6 shows the relative area footprint of devices. The inductor makes up a small portion of the total area of the power stage while the capacitors footprint ($C_{in}$, $C_1$, $C_2$, $C_3$, and $C_{out}$) is more substantial. A complete component listing is presented in Table 4.1. It should be noted that the individual components were selected to handle a 100 V to 400 V step-up, but thermal limitations prevented this voltage level from being realized.
4.2 Experimental Results

The prototypes were tested to ensure functionality of the design and demonstrate the ability of the proposed control techniques to enable high power densities at high efficiencies. In order to verify the control, gate signals are shown. The gate signals demonstrating the aforementioned split-phase control can be seen in Fig. 4.7. The $P_2$ signal, which controls switches $S_1, S_3, & S_7$, and $P_1$ signal, which controls $S_2, S_4, & S_6$, are complementary, with dead times implemented. The nominal duty cycles for these two signals are 0.5. The split-phase signals for switches $S_5$ and $S_8$ are shown as $P_{1,SP}$ and $P_{2,SP}$. There is delayed turn-on of these switches, and the positive duty cycles of the switches are 0.375.

The control indeed produces the expected resonant inductor current waveform which can be seen in Fig. 4.8. One can see that the current waveform is the expected rectified sinusoid. In order to achieve full zero current switching in the presence of component value variations, the period of the converter was manually adjusted until the maximum systemwide efficiency was found. The same method was performed with the split-phase turn-on times in order to eliminate current transients between capacitors. Figure 4.9 shows a split-phase signal that turns on switch $S_5$ (which connects capacitor $C_1$ to
Table 4.1: Component Listing of the 1:4 Dickson Converter.

<table>
<thead>
<tr>
<th>Component</th>
<th>Part Number</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_1 - S_5, S_8$</td>
<td>EPC2016</td>
<td>100 V, 16 mΩ, 11 A</td>
</tr>
<tr>
<td>$S_6, S_7$</td>
<td>EPC2010</td>
<td>200 V, 25 mΩ, 12 A</td>
</tr>
<tr>
<td>$C_{in}$</td>
<td>GRM21AR72A334KAC5L</td>
<td>100 V, 0.33 µF</td>
</tr>
<tr>
<td>$C_1, C_2$</td>
<td>C1812C104K2RACTU</td>
<td>200 V, 0.1 µF</td>
</tr>
<tr>
<td>$C_3, C_{out}$</td>
<td>C1812V104KCRACTU</td>
<td>500 V, 0.1 µF</td>
</tr>
<tr>
<td>Gate drivers</td>
<td>LM5113</td>
<td>Half-bridge GaN driver</td>
</tr>
<tr>
<td>Gate resistors</td>
<td>ERJ-2GEJ1R1X</td>
<td>1.1 Ω</td>
</tr>
<tr>
<td>Gate driver caps.</td>
<td>C0402C105K9PACTU</td>
<td>1 µF</td>
</tr>
<tr>
<td>$L$</td>
<td>IHLP2020ABERR10M01</td>
<td>13.5 A, 0.1 µH</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Component</th>
<th>Part Number</th>
<th>Parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level-shifting</td>
<td>ADUM5210</td>
<td></td>
</tr>
<tr>
<td>Micro-controller</td>
<td>TMS320F28069</td>
<td></td>
</tr>
</tbody>
</table>

The series connection of $C_3 - C_2$ and the voltage of capacitor $C_1$. The current in $C_1$ cannot be easily directly measured, but the voltage across $C_1$ can be used to estimate the current. Large current spikes will cause large, sudden changes in capacitor voltage. It can be seen here that capacitor voltage does not have any abrupt changes (Fig. 3.2) at the transition time which would correspond to capacitor voltage mismatch (Fig. 2.10). This means the split-phase control is working as intended.

In the second revision of the converter, the maximum power output of this converter prototype is 104.4 W. The achieved converter performance of the second revision is tabulated in Table 4.2. The converter achieved 92 % peak efficiency by using the advanced control techniques to eliminate hard charging current transients. The measured efficiency of the converter is plotted in Fig. 4.10 and 4.11 for a nominal voltage step-up of 25 V to 100 V. The output impedance of the converter was also measured and can be seen in Fig. 4.12. The impedance was measured when the converter was operating without an
Figure 4.7: Control signals \( P_2, P_1, P_{2,SP}, P_{1,SP} \).

The inductor in the conventional hard-switched case and also during the proposed resonant split-phase operation. The output impedance is greatly reduced by using the proposed techniques. Figure 4.13 shows a thermal image of the converter in operation at 125 °C which is the rated temperature at which the GaN devices are able to operate. Thermal limitations prevented the converter from achieving higher power at the output. One advantage of switched capacitor converters is that switches are distributed throughout the circuit, so heat is also distributed throughout the circuit. This allows higher overall power dissipation in each switch compared to a boost converter.
Figure 4.8: Resonant inductor current at 25 V input, 1.5 A output, 100 V output.
Figure 4.9: Capacitor $C_1$ voltage 25 V input, 0.5 A output, 100 V output and split-phase signal.
Figure 4.10: Measured efficiency of the first revision of the resonant converter at the input voltage of 25 V, and nominal output voltage of 100 V.

Figure 4.11: Measured efficiency of the second revision of the resonant converter at the input voltage of 25 V, and nominal output voltage of 100 V.
Figure 4.12: Measured output impedance of the Dickson SC converter prototype.
Figure 4.13: Thermal photo of the first revision of the Dickson converter at the thermal limit.
This thesis presented a resonant Dickson SC converter which uses a single inductor at the low voltage side to create resonance operation. The split-phase control scheme is used to ensure zero current switching for all switches. With ZCS, both capacitor charge redistribution losses and switching losses are minimized, resulting in a converter with higher power density and higher efficiency than conventional designs. A discrete converter prototype is built using GaN transistors, which demonstrates the advanced control method described in this paper. The power stage of the most recent revision of the converter prototype achieves a high power density of 1470 W/in³ or 89.7 kW/L. This demonstrates a high efficiency, high power density resonant Dickson converter.

This work provides a proof of concept for high power density, high efficiency switched capacitor converters, and there are many opportunities to expand of this work. In the future, it should be demonstrated that these converters can made more efficient by reducing switching frequency. This could greatly reduce switching losses and make the topology practical for many applications. This converter topology is also bi-directional and can be tested as such. Further, output voltage regulation is possible in the Dickson converter, and a closed loop control method can be combined with resonance and split-phase control. Control schemes can also be implemented in the control to optimize the split phase times and dead times of switches. Finally, there are opportunities to create custom level shifting devices to drive transistors in a more efficient manner.
APPENDIX A

PROTOTYPE PCB SCHEMATICS

Figures A.1 and A.2 show schematics of the board layout. These schematics are made in Cadence OrCAD and contain all components of the PCB prototype.
Figure A.1: Schematic of PCB board for first prototype.
Figure A.2: Schematic of PCB board for second prototype.
APPENDIX B

PROTOTYPE PCB LAYER FILES

This appendix provides photos of artwork files of the first and second revisions of the PCB prototypes earlier described. Figures B.1, B.2, B.3, B.4, and B.5 show the first revision top copper, layer 2 copper, layer 3 copper, bottom copper, and silkscreen layers respectively. Figures B.6, B.7, B.8, B.9, and B.10 show the second revision top copper, layer 2 copper, layer 3 copper, bottom copper, and silkscreen layers respectively.
Figure B.1: Top copper layer of PCB board for first prototype.
Figure B.2: Layer two copper of PCB board for first prototype.
Figure B.3: Layer three copper of PCB board for first prototype.
Figure B.4: Bottom copper of PCB board for first prototype.
Figure B.5: Silkscreen layer of PCB board for first prototype.
Figure B.6: Top copper layer of PCB board for second prototype.
Figure B.7: Layer two copper of PCB board for second prototype.
Figure B.8: Layer three copper of PCB board for second prototype.
Figure B.9: Bottom copper of PCB board for second prototype.
Figure B.10: Silkscreen layer of PCB board for second prototype.
This appendix includes microcontroller source code that implemented the split-phase control strategy described in this thesis.

```c
#include "F2806x_Device.h" // F2806x Headerfile
#include "F2806x_Examples.h" // F2806x Examples Headerfile
#include "F2806x_EPwm_defines.h" // useful defines for initialization

void HRPWM1_Config(Uint16);
void HRPWM2_Config(Uint16);
void HRPWM3_Config(Uint16);
void HRPWM4_Config(Uint16);
void HRPWM5_Config(Uint16);
void HRPWM6_Config(Uint16);

Uint16 i, j, DutyFine, n, update;

Uint32 temp;
float D, DP1SP, DP2SP;
int delay2, delay3, delay4, delay5, delay6;
int T, MEP;

void main(void)
{
    InitSysCtrl();
    InitEPwm1Gpio();
    InitEPwm2Gpio();
    InitEPwm3Gpio();
    InitEPwm4Gpio();
    InitEPwm5Gpio();
}
```
InitEPwm6Gpio();

DINT;

InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
IER = 0x0000;
IFR = 0x0000;
InitPieVectTable();

update =0;
DutyFine =0;
EALLOW;
SysCtrlRegs.PCLKC0.bit.TBCLKSYNC = 0;
EDIS;

T=64;  // Period = 65 for .1uF, .1uH. period =225 for .2uF, 1uH
D = .49;  // duty is time in first position as indicated by 'down up' etc
DP1SP = .375;  //
DP2SP = .39;  //

delay2 = 4;
delay3 = 5;  // period + delay3
delay4 = 1;
delay5 = 2;
delay6 = 3;

MEP = 40;

HRPWM1_Config(T);  // ePWM1 target, Period = T, down up
HRPWM2_Config(T);  // ePWM2 target, Period = T, up down
HRPWM3_Config(T);  // ePWM3 target, Period = T, down up
HRPWM4_Config(T);  // ePWM4 target, Period = T, up down
HRPWM5_Config(T);  // ePWM5 target, Period = T, down up
HRPWM6_Config(T);  // ePWM6 target, Period = T, up down
EALLOW;
SysCtrlRegs.PCLKR0.bit.TBCLKSYNC = 1;
EDIS;

EPwm1Regs.CMPA.half.CMPAHR = MEP+15<< 8; // F, delay => shift to right
EPwm2Regs.CMPA.half.CMPAHR = MEP+20 << 8; // F
EPwm3Regs.CMPA.half.CMPAHR = MEP+12 << 8; // F
EPwm4Regs.CMPA.half.CMPAHR = MEP << 8; // F
EPwm5Regs.CMPA.half.CMPAHR = MEP+12 << 8; // F
EPwm6Regs.CMPA.half.CMPAHR = MEP+10 << 8; // F

while (1)
{
}
}

void HRPWM1_Config(Uint16 period)
{
    // ePWM1 register configuration with HRPWM
    // ePWM1A toggle low/high with MEP control on Rising edge

    EPwm1Regs.TBCTL.bit.PRDLD = TB.IMMEDIATE; // set Immediate load
    EPwm1Regs.TBPRD = period−1; // PWM frequency = 1 / period
    EPwm1Regs.CMPA.half.CMPA = period *D−2; // set duty 50% initially
    EPwm1Regs.CMPA.half.CMPAHR = (1 << 8); // initialize HRPWM extension
    EPwm1Regs.TBPHS.all = 0;
    EPwm1Regs.TBPHS.half.TBPHS = 0; // Time−Base Phase Register, master’s phase = 0
    EPwm1Regs.TBCTR = 0;

    EPwm1Regs.TBCTL.bit.CTRMODE = TB.COUNT_UP;
    EPwm1Regs.TBCTL.bit.PHSEN = TB.DISABLE; // EPwm1 is the Master
    EPwm1Regs.TBCTL.bit.SYNCOSEL = TB.CTR.ZERO;
    EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB.DIV1;
    EPwm1Regs.TBCTL.bit.CLKDIV = TB.DIV1;
EPwm1Regs.CMPCTL.bit.LOADMODE = CC_CTR_ZERO;
EPwm1Regs.CMPCTL.bit.SHWAMODE = CC_SHADOW;

EPwm1Regs.AQCTLA.bit.ZRO = AQ_SET; // PWM toggle
low/high
EPwm1Regs.AQCTLA.bit.CAU = AQ_CLEAR;

EALLOW:
EPwm1Regs.HRCNFG.all = 0x0;
EPwm1Regs.HRCNFG.bit.EDGMODE = HR_FEP; // MEP control on
Rising edge
EPwm1Regs.HRCNFG.bit.CTLMODE = HR_CMP;
EPwm1Regs.HRCNFG.bit.HRLOAD = HR_CTR_ZERO;

EDIS;
}

void HRPWM2_Config(Uint16 period) {

// ePWM2 register configuration with HRPWM

EPwm2Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE; // set
Immediate load
EPwm2Regs.TBPRD = period - 1; // PWM
frequency = 1 / period
EPwm2Regs.CMPA.half.CMPA = period * D+2; // set
duty 50% initially
EPwm2Regs.CMPA.half.CMPAHR = (1 << 8); // initialize HRPWM extension
EPwm2Regs.TBPHS.all = 0;
EPwm2Regs.TBPHS.half.TBPHS = delay2; // Time–Base
Phase Register, master’s phase = 0
EPwm2Regs.TBCTR = 0;

EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
EPwm2Regs.TBCTL.bit.PHSEN = TB_ENABLE; // EPwm2 is
the Slave
EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;
EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV1;

EPwm2Regs.CMPCTL.bit.LOADMODE = CC_CTR_ZERO;
EPwm2Regs.CMPCTL.bit.SHWAMODE = CC_SHADOW;
EPwm2Regs.AQCTLA.bit.ZRO = AQ.CLEAR; // PWM toggle low/high
EPwm2Regs.AQCTLA.bit.CAU = AQ.SET;

EALLOW;
EPwm2Regs.HRCNFG.all = 0x0;
EPwm2Regs.HRCNFG.bit.EDGMODE = HR.FEP; // MEP control on Falling edge
EPwm2Regs.HRCNFG.bit.CTLMODE = HR.CMP;
EPwm2Regs.HRCNFG.bit.HRLOAD = HR.CTR.ZERO;
EDIS;
}

void HRPWM3_Config(Uint16 period)
{
    // ePWM3 register configuration with HRPWM
    EPwm3Regs.TBCTL.bit.PRDLD = TB.IMMEDIATE; // set Immediate load
    EPwm3Regs.TBPRD = period - 1; // PWM frequency = 1 / period
    EPwm3Regs.CMPA.half.CMPA = period * (1 - DP1SP); // set duty 50% initially
    EPwm3Regs.CMPA.half.CMPAHR = (1 << 8); // initialize HRPWM extension
    // EPwm3Regs.TBPHS.all = 0;
    EPwm3Regs.TBPHS.half.TBPHS = delay3; // Time–Base Phase Register, master’s phase = 0
    EPwm3Regs.TBCTR = 0;

    EPwm3Regs.TBCTL.bit.CTRMODE = TB.COUNT.UP;
    EPwm3Regs.TBCTL.bit.PHSEN = TB.ENABLE; // EPwm3 is the Slave
    EPwm3Regs.TBCTL.bit.SYNOSEL = TB.CTR.ZERO;
    EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB.DIV1;
    EPwm3Regs.TBCTL.bit.CLKDIV = TB.DIV1;

    EPwm3Regs.CMPCTL.bit.LOADAMODE = CC.CTR.ZERO;
    EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC.SHADOW;
    EPwm3Regs.AQCTLA.bit.ZRO = AQ.CLEAR; // PWM
to
g
ggle

\begin{verbatim}
  toggle high/low
  EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;

  EALLOW;
  EPwm3Regs.HRCNFG.all = 0x0;
  EPwm3Regs.HRCNFG.bit.EDGMODE = HR_FEP;  // MEP
    control on falling edge
  EPwm3Regs.HRCNFG.bit.CTLMODE = HR_CMP;
  EPwm3Regs.HRCNFG.bit.HRLOAD = HR_CTR_ZERO;
  EDIS;
}

void HRPWM4_Config(Uint16 period)
{
  // ePWM1 register configuration with HRPWM
  EPwm4Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE;  // set
    Immediate load
  EPwm4Regs.TBPRD = period - 1;  // PWM
    frequency = 1 / period
  EPwm4Regs.CMPA.half.CMPA = period * D - 2;  // set
    duty 50% initially
  EPwm4Regs.CMPA.half.CMPAHR = (1 << 8);  // // initialize HRPWM extension
    // EPwm4Regs.TBPHS.all = 0;
  EPwm4Regs.TBPHS.half.TBPHS = delay4;  // Time-Base Phase
    Register, slave’s phase = phi
  EPwm4Regs.TBCTR = 0;

  EPwm4Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
  EPwm4Regs.TBCTL.bit.PHSEN = TB_ENABLE;  // EPwm1 is the master
  EPwm4Regs.TBCTL.bit.SYNCOSEL = TB_CTR_ZERO;
  EPwm4Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
  EPwm4Regs.TBCTL.bit.CLKDIV = TB_DIV1;

  EPwm4Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
  EPwm4Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;

  EPwm4Regs.AQCTLA.bit.ZRO = AQ_SET;  // PWM toggle
    low/high
  EPwm4Regs.AQCTLA.bit.CAU = AQ_CLEAR;
\end{verbatim}
EALLOW;
EPwm4Regs.HRCNFG.all = 0x0;
EPwm4Regs.HRCNFG.bit.EDGMODE = HR_FEP; // MEP control on Rising edge
EPwm4Regs.HRCNFG.bit.CTLMODE = HR_CMP;
EPwm4Regs.HRCNFG.bit.HRLOAD = HR_CTR_ZERO;
EDIS;
}

void HRPWM5_Config(Uint16 period) {
    // ePWM2 register configuration with HRPWM
    EPwm5Regs.TBCTL.bit.PRDLD = TB_IMMEDIATE; // set Immediate load
    EPwm5Regs.TBPRD = period − 1; // PWM frequency = 1 / period
    EPwm5Regs.CMPA.half.CMPA = period * D + 2; // set duty 50% initially
    EPwm5Regs.CMPA.half.CMPAHR = (1 << 8); // initialize HRPWM extension
    // EPwm5Regs.TBPHS.all = 0;
    EPwm5Regs.TBPHS.half.TBPHS = delay5; // Time−Base Phase Register, slave’s phase = phi
    EPwm5Regs.TBCTR = 0;
    EPwm5Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
    EPwm5Regs.TBCTL.bit.PHSEN = TB_ENABLE; // EPwm2 is the Master
    EPwm5Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;
    EPwm5Regs.TBCTL.bit.HSPCLKDIV = TB_DIV1;
    EPwm5Regs.TBCTL.bit.CLKDIV = TB_DIV1;
    EPwm5Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
    EPwm5Regs.CMPCTL.bit.SHADOWMODE = CC_SHADOW;
    EPwm5Regs.AQCTLA.bit.ZRO = AQ_CLEAR; // PWM toggle low/high
    EPwm5Regs.AQCTLA.bit.CAU = AQ_SET;
    EALLOW;
    EPwm5Regs.HRCNFG.all = 0x0;
    EPwm5Regs.HRCNFG.bit.EDGMODE = HR_FEP; // MEP
void HRPWM6_Config(Uint16 period) {
    // ePWM4 register configuration with HRPWM
    EPwm6Regs.TBCTL.bit.PRDL = TB_IMMEDIATE; // set
    EPwm6Regs.TBPRD = period - 1; // PWM
    EPwm6Regs.CMPA.half.CMPA = period * DP2SP; // set
duty
    EPwm6Regs.CMPA.half.CMPAHR = (1 << 8); // initialize HRPWM extension
    EPwm6Regs.TBPHS.half.TBPHS = period * (1 - D + DP2SP) + delay6; // Time–Base Phase Register, slave’s phase = phi
    EPwm6Regs.TBCTR = 0;
    EPwm6Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
    EPwm6Regs.TBCTL.bit.PHSEN = TB_ENABLE; // EPwm4 is the Master
    EPwm6Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_IN;
    EPwm6Regs.TBCLKDIV = TB_DIV1;
    EPwm6Regs.TBCTL.bit.CLKDIV = TB_DIV1;
    EPwm6Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
    EPwm6Regs.CMPCTL.bit.SHADOWMODE = CC_SHADOW;
    EPwm6Regs.AQCTLA.bit.ZRO = AQ_SET; // PWM
toggle
    EPwm6Regs.AQCTLA.bit.CAU = AQ_CLEAR;
    EALLOW;
    EPwm6Regs.HRCNFG.all = 0x0;
    EPwm6Regs.HRCNFG.bit.EDGMODE = HR_FEP; // MEP
    EPwm6Regs.HRCNFG.bit.CTLMODE = HR_CMP;
}
EPwm6Regs.HRCNFG.bit.HRLOAD = HR_CTR.ZERO;
EDIS;
}

appendix/code.c
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