CHARACTERIZATION OF GaN MOS-HEMT TRAP-RELATED EFFECTS FOR POWER SWITCHING APPLICATIONS

BY

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THESIS

Submitted in partial fulfillment of the requirements for the degree of Master of Science in Electrical and Computer Engineering in the Graduate College of the University of Illinois at Urbana-Champaign, 2015

Urbana, Illinois

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Abstract

This thesis presents the experiment setup and result of AlGaN/GaN Metal-Oxide-Semiconductor High-Electron-Mobility Transistors (MOS-HEMTs) characterization. Various aspects of GaN MOS-HEMTs, such as the DC characteristic, temperature dependency, breakdown behavior and trap-related effects, were studied. Multiple customized measurement setups and configurations, including hardware and software, are discussed. We have estimated trap distribution using the capacitance and the conductance method. Pulse measurements and stress tests with various bias conditions were used to understand trap-related degradations. Performance and trap-related comparisons between our device and the literature are also included.
Acknowledgments

I would like to thank my research advisor, Professor Elyse Rosenbaum, for her valuable guidance, encouragement and support in the past two years. I would like to thank several current and former students from my research group for their teaching and helpful discussion.

I would also like to thank Professor Kyekyoon Kim and his research group members for providing all the GaN samples for this thesis.
Contents

1. Introduction ........................................................................................................................................... 1

2. Literature Review ................................................................................................................................. 2
   2.1 HEMT Background ........................................................................................................................... 2
   2.2 MOS-HEMT ....................................................................................................................................... 3
   2.3 Reliability .......................................................................................................................................... 4

3. Sample Overview ................................................................................................................................. 5
   3.1 Fabricated Devices and Test Structures .......................................................................................... 5
   3.2 Gate Insulator and Substrate .......................................................................................................... 6

4. Measurement Setup ............................................................................................................................. 8
   4.1 Cable Configuration for Low Leakage Measurement ...................................................................... 8
   4.2 Measurement Noise .......................................................................................................................... 9
   4.3 High Voltage IV Measurement Setup ............................................................................................. 14

5. Device Performance ............................................................................................................................ 17
   5.1 Surface Passivation and Gate Oxide ............................................................................................... 17
   5.2 Typical DC Characteristics of MOS-HEMT .................................................................................... 18
   5.3 Drain Breakdown ............................................................................................................................... 20
   5.4 Gate Oxide ....................................................................................................................................... 22

6. Trap-Related Characterizations ........................................................................................................ 25
   6.1 Capacitance Method ....................................................................................................................... 25
   6.2 Conductance Method ....................................................................................................................... 29
   6.3 Pulse Measurement ......................................................................................................................... 32
   6.4 Transient Degradation .................................................................................................................... 36

7. Conclusion ............................................................................................................................................ 41

References .................................................................................................................................................. 42
1. Introduction

The AlGaN/GaN High-Electron-Mobility Transistors (GaN HEMTs) have attracted huge attention in power and RF applications because of their promising characteristics such as high breakdown voltage, low channel resistance and high switching speed [1, 2, 3]. Silicon (Si) substrates are the most commonly used in GaN fabrication since their cost is low and defect-free GaN substrate is not available. Since GaN and Si belong to two different material systems, growing one material on the other introduces a large amount of lattice mismatch and forms defects. Although there are transition layers that can be inserted in between, defect-related degradation is still the top concern of GaN devices. Moreover, HEMTs with a Schottky gate tend to have high sub-threshold leakage current and low breakdown voltage which disqualifies them for power applications. Thus, a gate oxide or other insulating material has to be inserted between the gate electrode and the semiconductor interface to form a Metal-Oxide/Insulator-Semiconductor HEMT (MOS/MIS-HEMT) to overcome those limitations. However, the additional oxide-semiconductor interface creates another location of lattice mismatch and brings in extra degradation mechanisms. All those defects mentioned above may cause reliability issues and limit the application of GaN HEMTs.

Although the reliability of GaN MOS-HEMTs is still one of the top concerns, a large number of RF and power applications have been demonstrated with superior performance using GaN HEMT or MOS-HEMT in the literature. For example, [4] reported a low noise / high power HEMT that operates stably at 40 GHz, [5] reported an E-mode MOS-HEMT with $10^{12}$ on/off ratio fabricated for power switching applications. Semiconductor companies also have released a few GaN power transistors with rating up to 650 V / 30 A [6, 7].

This thesis will cover some basic background of HEMT and MOS-HEMT, MOS-HEMT measurement setup, device characterization and trap-related study. Chapters 2 and 3 give additional information about the GaN HEMT, introduce some commonly seen reliability issues and provide detailed information about the samples used for this work. Chapter 4 discusses several measurement-related topics which are important for MOS-HEMT characterization as well as a customized developed high voltage test setup. Chapters 5 and 6 include DC, breakdown and reliability-related measurement results and discussion. Chapter 7 summaries of all the findings.
2. Literature Review

2.1 HEMT Background

The High-Electron-Mobility Transistor (HEMT), also known as the Heterostructure Field-Effect Transistor (HFET), contains a heterojunction which is formed by two different materials such as AlGaN and GaN. Due to the large bandgap energy difference between AlGaN and GaN, a quantum well is formed in the conduction band at the interface on the GaN side [8]. The electrons in the AlGaN layer will transfer to the GaN layer and confined by the polarization induced electric field to form a thin, around 10 nm, conduction layer. This layer of electrons is called the Two-Dimensional Electron Gas (2DEG). Since the GaN layer is undoped, electrons from 2DEG are able to move without any impurity collision, in contrast to the MOS Field-Effect Transistor (MOS-FET), and therefore the transistor can achieve high electron mobility. Figure 1(a) shows the formation of 2DEG.

![Illustration of 2DEG formation with AlGaN/GaN heterojunction](image1.png)

Figure 1 (a) Illustration of the 2DEG formation with AlGaN/GaN heterojunction [8]. (b) A cross-sectional view of a typical GaN HEMT with multiple surface passivation layers [9].

Figure 1(b) is the cross-sectional view of a typical HEMT fabricated on a non-GaN substrate. The AlN/GaN/AlN interlayer reduces the tensile stress induced by large lattice mismatch between the GaN and the SiC layer. Gate metal was deposited directly on the semiconductor layer to form a Schottky gate HEMT. A field-modulating plate (FP) was connected to gate terminal to reduce the peak electric field strength in the gate region. Multiple surface passivation layers were deposited to suppress leakage current and protect the device from
contaminations such as water vapor and oxygen. For a Schottky gate HEMT, the 2DEG is present at zero gate bias and can be depleted with reverse gate bias. Such a device operates in Depletion-Mode (D-Mode) in contrast to Enhancement-Mode (E-Mode).

Compared with other III-V and V semiconductors, GaN is the most promising material for high-power and high-frequency applications and it is expected to replace some Si-based devices [10]. Table 1 shows some material properties of four commonly used semiconductor materials.

Table 1 Power performance related material parameters of various materials [1].

<table>
<thead>
<tr>
<th></th>
<th>Si</th>
<th>SiC</th>
<th>GaAs</th>
<th>GaN</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandgap (eV)</td>
<td>1.1</td>
<td>3.26</td>
<td>1.42</td>
<td>3.39</td>
</tr>
<tr>
<td>Electron mobility (cm²V⁻¹s⁻¹)</td>
<td>1350</td>
<td>700</td>
<td>8500</td>
<td>1200 (Bulk) 2000 (2DEG)</td>
</tr>
<tr>
<td>Breakdown field (MV/cm)</td>
<td>0.3</td>
<td>3.0</td>
<td>0.4</td>
<td>3.3</td>
</tr>
<tr>
<td>Saturation velocity (10⁷ cm/s)</td>
<td>1.0</td>
<td>2.0</td>
<td>1.0</td>
<td>2.5</td>
</tr>
<tr>
<td>Polarization</td>
<td></td>
<td></td>
<td></td>
<td>High charge, carrier confinement</td>
</tr>
</tbody>
</table>

As indicated in Table 1, GaN has many outstanding properties compared with other materials. For example, its electron mobility is almost doubled compared with silicon and its breakdown field is an order of magnitude higher than GaAs and Si. Furthermore, the wide bandgap of GaN makes high temperature operation (e.g. 300 °C) possible for a GaN transistor while the application of the silicon device is limited.

2.2 MOS-HEMT

For a conventional HEMT, the Schottky gate causes relative high gate leakage current and the device exhibits D-mode operation with negative threshold voltage. By inserting an oxide layer between the gate and the semiconductor layer, a MOS-HEMT is formed and the leakage current is suppressed. Usually gate oxide materials with a high breakdown field and wide bandgap are used. Compared with GaN D-mode HEMTs used for RF applications, E-mode transistors are preferred for power switching applications since the fail-safe feature they have, that the transistor has a tendency to turn off under failure conditions such as a floating gate connection. Various techniques, such as recess etching the semiconductor layers in the gate
region to cut off the 2DEG [5] and implanting ions such as fluorine (F) into the gate oxide [11], can be used to convert a D-mode MOS-HEMT into E-mode.

2.3 Reliability

Although GaN HEMTs show promising potential, critical reliability issues such as leakage current and trap-related phenomena have to be solved [3]. A trap is a defect originating from a structural defect or the presence of an impurity or a sudden loss of continuity in the crystal lattice (as in interfaces), it disrupts the periodicity of the crystal lattice and introduces a discrete energy level in the bandgap of a semiconductor material [12].

Figure 2 indicates the location of some known traps in a GaN HEMT, including the dielectric interface, passivation interface, access region and buffer layer. Traps located at different places introduce their own degradation mechanism to the MOS-HEMT. For example, trapping centers near the 2DEG may capture electrons and become negatively charged which will deplete electrons in the channel and the access region [12]. Moreover, traps in GaN MOS-HEMT may not only contribute to recoverable device degradation, but also can be the cause of trap-related leakage and even breakdown, which results in permanent device damage. For the leakage current, both the gate leakage and drain sub-threshold leakage current need to be considered.

![Figure 2 Locations of known traps in a GaN MOS-HEMT](image)

Figure 2 Locations of known traps in a GaN MOS-HEMT [12].
3. Sample Overview

Several different batches of GaN HEMTs and MOS-HEMTs have been fabricated for this thesis with various gate insulators and substrates. This chapter gives detailed information of all the devices and samples that have been used.

3.1 Fabricated Devices and Test Structures

Figure 3 is the cross-sectional view and top view of the MOS-HEMTs that we have investigated. For the HEMT, the gate metal is deposited directly on the i-GaN cap layer without any gate insulator. Note that the surface passivation layer is not shown for simplicity.

![Cross-sectional view and top view of fabricated GaN MOS-HEMT](image)

For a typical MOS-HEMT, its gate dimension is $5 \times 50 \mu m$ and its capacitance is only a few pF ($10^{-12}$) which is difficult to measure accurately. Thus, dedicated Capacitance-Voltage (CV) test patterns were fabricated and used for capacitance-related experiments such as the carrier density extraction and trap estimation. The cross-sectional view and top view of CV test patterns are shown in Figure 4. The only difference between CV test pattern and MOS-HEMT is their top metal configuration, e.g. the drain and source terminal of the MOS-HEMT become the cathode and the gate become the anode.
Figure 4 Cross-sectional view (a) and top view (b) of the GaN capacitance test pattern, exact epitaxial layer thickness of samples used for the related studies are given in Chapter 6.

Device dimension of the MOS-HEMTs and CV test patterns are listed in Table 2. Although different substrates were used and several revision of masks were designed, the same set of dimension was used during the whole time and all fabricated devices have identical structure.

Table 2 Dimension of the fabricated test structures.

<table>
<thead>
<tr>
<th>Device</th>
<th>$L_{GS}$ [µm]</th>
<th>$L_G$ [µm]</th>
<th>$L_{GD}$ [µm]</th>
<th>$W$ [µm]</th>
<th>$D$ [µm]</th>
<th>$L_S$ [µm]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conventional MOS-HEMT</td>
<td>2</td>
<td>3, 5</td>
<td>5, 10, 15</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Symmetrical MOS-HEMT</td>
<td>2</td>
<td>5</td>
<td>2</td>
<td>50, 150, 250</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance test pattern</td>
<td></td>
<td></td>
<td></td>
<td>100, 150, 200</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

3.2 Gate Insulator and Substrate

Table 3 lists the gate oxide and substrate information for all the samples used in this study. All the substrates are silicon (111) based, and came with a pre-grown buffer layer and AlGaN/GaN layers (GaN-on-Si). Samples fabricated on Azzurro substrate with CVD SiO$_2$ gate oxide were most commonly used due to the large quantity of available devices we have. For all the gate oxide grown methods, Chemical Vapor Deposition (CVD) gives the highest oxide quality.
Table 3 Substrate and gate oxide information of the fabricated samples.

<table>
<thead>
<tr>
<th>Substrate vendor</th>
<th>Material</th>
<th>Grown method</th>
<th>Thickness [nm]</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>NTT-AT</td>
<td>None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NTT-AT</td>
<td>None</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>NTT-AT</td>
<td>$SiO_2$</td>
<td>Chemical Vapor Deposition (CVD)</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>NTT-AT</td>
<td>$TiO_2$</td>
<td>RF-sputtered</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Nitronix</td>
<td>$Hf_2O_3$</td>
<td>Atomic layer deposition (ALD)</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Nitronix</td>
<td>$Al_2O_3$</td>
<td>ALD</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Nitronix</td>
<td>$SiO_2$</td>
<td>CVD</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Nitronix</td>
<td>$SiO_2$</td>
<td>RF-sputtered</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>Azzurro</td>
<td>$Hf_2O_3$</td>
<td>ALD</td>
<td>50</td>
<td></td>
</tr>
<tr>
<td>Azzurro</td>
<td>$Al_2O_3$</td>
<td>ALD</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Azzurro</td>
<td>$SiO_2$</td>
<td>CVD</td>
<td>12</td>
<td></td>
</tr>
</tbody>
</table>
4. Measurement Setup

This chapter discusses all the measurement-related topics of this work, such as noise issues and customized measurement setups. Since all the samples we used were unpackaged, all the measurements were wafer level and performed inside a probe station in a dark environment at room temperature unless otherwise noted. The following instruments were used for characterizing GaN devices: Agilent 4155C Semiconductor Parameter Analyzer, Keithley 2410 SourceMeter®, and HP 4284A Precision LCR Meter. A Wentworth Labs model TC 100 hot chuck was used for high temperature measurements.

![Block diagram of the automatic test setup](image)

Figure 5 Block diagram of the automatic test setup developed for GaN MOS-HEMT characterization. Selection of measurement instruments and Device Under Test (DUT) depends on the experimental need.

A block of diagram of the measurement setup is shown in Figure 5. All laboratory instruments except the hot chuck’s temperature controller were connected to an 8-bit parallel multi-master interface bus, also known as IEEE-488 General Purpose Interface Bus (GPIB). Depending on the measurement need, one or more pieces of equipment may be running at the same time. To handle various measurement tasks, a fully customized C# control program was developed. It controls all the lab instruments through the GPIB bus, and it post processes and stores measurement data for further analysis.

4.1 Cable Configuration for Low Leakage Measurement

Pico ($10^{-12}$) ampere and lower level measurements are commonly used for MOS-HEMT characterization since the gate oxide greatly suppresses the drain sub-threshold leakage current and gate leakage current. At this current level, measurement accuracy not only depends on the instrument’s resolution limit but also depends on the cable leakage current, parasitic capacitance and other environmental factors.
Figure 6 shows the cross-sectional view of a coaxial and a triaxial cable. Compared with a coaxial cable, the triaxial cable has an additional guard layer between the inner and outer conductor. Measurement instruments such as Source Measure Unit (SMU) controls the potential of the guard layer to make it the same as the force (sense) conductor by using a feedback circuit. Since the potentials of those two conductors are the same, voltage between them is zero and no electric field exists in between. Therefore, the SMU eliminates the leakage current of the force/sense conductor. If probes have a triaxial connector, one can neglect the leakage current between the SMU and probe tips. However, the connector of most probes is the coaxial type that requires a triaxial to coaxial conversion adaptor. Since the primary goal is leakage current elimination, one should connect the outer conductor of the coaxial cable (common) to the middle conductor of the triaxial cable (guard) to ensure the continued guarding while the inner conductor (force/sense) of the coaxial and triaxial cables are tied together.

![Diagram of coaxial and triaxial cables](image)

**Figure 6** (a) Cross-sectional view of a coaxial cable with an inner conductor and outer conductor. (b) Cross-sectional view of a triaxial cable with an inner conductor, a guard layer and an outer conductor.

### 4.2 Measurement Noise

Unlike measuring packaged devices, wafer/probe level measurement is vulnerable to interferences and other noise sources from the environment since neither the probe nor the DUT have good shielding and there is no durable connection between them. This section discusses some identified noise sources and the corresponding suppression techniques used in this thesis.

#### 4.2.1 Power Line Noise

Usual IV measurements, such as a DC sweep to obtain transfer characteristic, can reject most of the power line noise since by default most Source Measure Units (SMUs) use 1 Power Line Cycle (PLC) as integration time which cancels out the coupling effect from the power line. Fast IV measurements, however, use a much smaller integration time (could be as low as 80 µs for Agilent 4155C) and the coupling effect from the power line may greatly degrade its measurement accuracy when the voltage/current being measured is low.
Figure 7 (a) Gate current waveform measured with a constant gate voltage applied with different probe station lamp and hot chuck configuration. (b) Frequency spectrum of the current waveform plotted in (a).

The probe station we have has a LED lamp used for illumination and a hot chuck for physically holding samples and controlling the temperature. Both pieces of equipment are connected to the corresponding controller via cable which installed outside the probe station, and both controllers are connected to the AC outlet by default. Figure 7 shows the result of an oxide stress test with an 80 µs sampling period. The actual DC current flowing through the gate is around 70 pA. When the lamp and hot chuck were set to off but their controller were connected to a dedicated AC outlet, a high amplitude sinusoidal waveform is added to the top of the DC current as the result of power line coupling. Strong power line frequency components, including the 60 Hz fundamental component and up to the 39th harmonic components at 2.34 kHz, can be identified in the spectrum plot. It is believed that the power line noise leaked into the probe station through the ground lines of the lamp and the hot chuck, which cannot be cut off by simply switching off the controller, and picked up by the probe. To reduce the power line coupling inside the probe station, unnecessary equipment which have a wired connection to the outside world, especially to the AC outlet, must be isolated. Figure 7 also compares the measurement result before and after all the unnecessary devices (e.g. probe station’s lamp and hot chuck) have been isolated, a more than 40 dB AC noise reduction was achieved. Note some of the high frequency noise components shown in the spectrum plot may be cause by the measurement instrument, such as quantization noise, instead of the AC interference.

4.2.2 Non-EM Related Noise

Wafer level measurements rely on probes to make a connection between instruments and a Device Under Test (DUT). When landing a probe on the sample, the quality of the contact directly determines the quality of the measured data. Compared with commercial fabricated
CMOS samples, probe pads of a GaN sample have lower surface quality leading to a less stable contact. Figure 8(a) shows the effect of moderate human activity near the probe station during a low current measurement, clearly the area close to the probe station must stay “quiet” by avoiding large body movements during such experiments.

![Figure 8(a)](image)

Figure 8 (a) Impact of human activity near a probe station during a high sensitivity measurement, peaks around 40 to 100 seconds are the result of people gently walked by the probe station while the peak around 140 seconds is the result of tapping the probe station’s shield. (b) Measurement noise caused by temperature fluctuation and vibration.

Other sources can also generate noise. In Figure 8(b), the measured drain current fluctuations at 60 °C is the result of junction temperature change. The hot chuck only heats the sample when its temperature falls out of a certain range, therefore the actual chuck’s temperature changes periodically. Besides, sudden jump of the measured drain current at 20 °C was the result of vibration. Cooling water was flowing through the chuck during this measurement, its pressure change caused vibration which has a severe impact on the contact quality.

Aside from vibration, contaminated probe tips and probe pads can also degrade the contact quality. The comparison is shown in Figure 9. Since the probe pad’s surface quality of GaN samples is lower than other the commercial CMOS samples, the probe tip requires frequent cleaning.
Figure 9 Comparison of transient noise due to cleanliness difference. Scratching the surface of a probe pad by pushing the probe tip back and forth on it removes oxide and contaminations on the DUT. Cleaning the probe tip removes metal residue and other contaminations on it.

4.2.3 Capacitance Measurement

Unlike IV measurements, high frequency (HF) capacitance measurements are usually performed with an LCR meter which measures the amplitude and phase of the AC current which flows through the DUT. Since the LCR meter does not use integrating Analog to Digital Converter (ADC), it cannot suppress low frequency noise from the power line or other sources by selecting a proper integration time. Moreover, since the capacitance of the devices that we are interested in are usually small, e.g. less than 100 pF, they have a high impedance at a low frequency which leads to a low level of AC current and makes it difficult to measure. Parasitic capacitances from the measurement setup also bring in extra error. Equation (1) [13] shows the simplified guaranteed accuracy expression at a low frequency for the LCR meter.

\[
A_e = \pm [A + (K_a + K_b) \times 100] \times K_e
\]

Here A is the basic accuracy, \(K_a\) and \(K_b\) are impedance proportional factors, \(K_e\) is the temperature factor. Since we encounter most of the measurement noise below 100 Hz, we calculate the guaranteed accuracy for a 50 pF capacitor measured by a 100 Hz AC signal with 30 mV Root-Mean-Square (RMS) amplitude for illustration. For this particular configuration, [13] gives

\[
A = 0.25
\]

\[
K_a = \frac{10^{-3}}{|Z_m|} \left( 1 + \frac{200}{V_s} \right)
\]

\[
K_b = |Z_m| 10^{-9} \left( 1 + \frac{70}{V_s} \right)
\]
Here $Z_m = 1/j\omega C$, $V_s$ is the RMS voltage of the AC test signal. By plugging numbers into Equations (1)-(4), the guaranteed accuracy is 10.7% which implies that part of the noise seen by the measurement comes from the instrument itself. Therefore, for low frequency capacitance measurement, proper isolation and data processing techniques are necessary for obtaining a clean result.

To reduce noise coupled from the environment, the hot chuck was replaced by a conventional floating chuck which has completely no electrical connection to the circuit or chassis ground. As can be seen in Figure 10(a), replacing the chuck has greatly suppressed the noise between 100 Hz and 3 kHz. Note that disconnecting the hot chuck’s controller from the AC outlet is not sufficient for CV measurement since its cable can still act as antenna to pick up AC noise from the environment. Besides, parasitic capacitances between the probe and chuck is eliminated once the chuck’s connection changes from grounded to floating.

![Figure 10](image_url)

Figure 10 (a) Capacitance measurement result with a hot chuck and a conventional floating chuck. (b) Capacitance measurement result of an identical device with 20 identical sweeps, data at certain frequencies has a relative large discrepancy.

Figure 10(b) shows the result of 20 identical capacitance-frequency sweeps, it can be noticed that certain frequency points are noisier than the others due to interference. Once those noisy frequencies are identified, one can avoid using them during the capacitance measurement to reduce error. However, such a frequency list should be updated regularly since the environmental interference may changes over time. Besides, taking an average of multiple sets of measurement data can achieve a more accurate result. Another observation during this study is that measurement using a long integration time does not provide a more accurate result than using a medium integration time. Therefore, when performing such a measurement, use of a medium
integration time and combine with multiple frequency/voltage sweeps for averaging is recommended to optimize the overall time consumption and data accuracy.

### 4.3 High Voltage IV Measurement Setup

A customized high voltage IV measurement setup was developed to characterize the high voltage behavior of GaN MOS-HEMTs, such as determining the off-state drain breakdown voltage. This setup includes the Agilent 4155C, the Keithley 2410, a current limiting resistor and a set of custom-made Zener protection adaptors. Mid-Power SMUs (MP-SMUs) in Agilent 4155C control the gate and source terminal of the DUT while the high-voltage SMU (HV-SMU) in Keithley 2410 controls the drain terminal.

Since the SMUs in Agilent 4155C are only rated up to ±200 V and can source voltage up to ±100 V, a customized Zener protection adaptor was designed to prevent them from exposing to hazard voltage. Each protection adaptor has a pair of back-to-back connected Zener diodes that clamps the terminal voltage at ±120 V and does not interfere with the SMU’s normal operation. For extra protection against the high voltage and possible high peak current, a 600 kΩ resistor was inserted between the DUT’s drain terminal and the HV-SMU. This resistor limits the amount of current that flows out from the HV-SMU to 1.9 mA even if there is a short circuit connection. All the diodes and resistor were mounted and sealed in aluminum boxes with BNC connectors for safety considerations. Figure 11(a) shows the circuit schematic of the measurement setup. Due to the existence of the current limiting resistor, the actual DUT drain voltage can be expressed as

$$V_{\text{actual}} = V_{\text{sense}} - I_{\text{sense}} \times R$$  \(5\)

Here $V_{\text{sense}}$ and $I_{\text{sense}}$ are the measured terminal voltage and current from the HV-SMU, $R$ is the resistance of the current limiting resistor.

We also made a customized 1.2 kV rated banana-to-triaxial cable conversion adaptor because the HV-SMU only has banana connectors and the probe station requires coaxial or triaxial connector. The circuit ground of the HV-SMU and MP-SMUs are connected together with a low impedance cable and connected to the chassis ground to avoid a floating circuit and ensure safely. A jumper was plugged into the interlock port of Agilent 4155C allowing the instrument to source voltage higher than ±40 V.
The detail of the backplane connection is shown in Figure 11(b). The trigger input/output (I/O) ports of Agilent 4155C and Keithley 2410 were configured in master-slave mode. Once the control software finishes configuration and initializes a high-voltage sweep, Keithley 2410 will take over. It controls itself for biasing, measurement and triggering the Agilent 4155C to take source and gate current measurement. Measurement data are retrieved by the control software once Keithley 2410 finishes the sweep. This control setup provides the lowest response time for handling over-current events, such as device breakdown, by shutting down the HV-SMU. It also provides a highest sweep rate since no data or command is exchanged over the GPIB bus during the measurement. Figure 12 shows the timing diagram of a typical HV-sweep.

Aside from the device breakdown, air breakdown may occur when performing a high voltage sweep. For example, when the probes are placed only tens of a micrometer away from each other and more than 1 kV is applied to them, the electric field strength is much higher than the air breakdown field limit and spark will appear. One can avoid this effect by placing probes...
away from each other on the DUT’s probe pad or placing the sample and probe tips in insulating fluid.
5. Device Performance

This chapter includes the DC measurement results of varies GaN HEMTs and MOS-HEMTs. Trap-related measurements and characterizations will be covered in Chapter 6.

5.1 Surface Passivation and Gate Oxide

We fabricated and measured HEMTs with a Schottky gate (with and without the $SiO_2$ surface passivation) and MOS-HEMTs with CVD $SiO_2$ gate oxide using an NTT-AT GaN-on-Si substrate to study the surface passivation and gate oxide. The measurement result is plotted in Figure 13. Surface passivation reduces the gate leakage current for more than 100x while there is no noticeable change in maximum drain current and threshold voltage. The insertion of gate oxide suppresses the leakage current by another $10^4$x but the device also exhibits an undesirable -6 V threshold voltage shift. The on/off ratio of the MOS-HEMT, which is measured by the drain current ratio with 0 and -10 V gate bias, is $6.2 \times 10^9$ implies high quality of the gate oxide.

![Figure 13](image)

Figure 13 Transfer characteristic (a) and gate leakage current (b) comparison of the unpassivated Schottky gate HEMT, surface passivated Schottky gate HEMT and MOS-HEMT.

Figure 14 compares the output characteristic ($I_D-V_D$) between a Schottky gate HEMT and a MOS-HEMT. With the same gate bias, drain current of the MOS-HEMT is always higher than the Schottky gate HEMT because the MOS-HEMT has a lower threshold voltage. Besides, the output characteristic of the MOS-HEMT has some noticeable kinks and regions with Negative Differential Resistance (NDR) while the output curve of the Schottky gate HEMT is smooth and monotonic. This difference is the result of trapping-related effects created by the gate oxide, which will be discussed in Chapter 7.
Figure 14 Output curve comparison of the (a) Schottky gate HEMT and (b) MOS-HEMT.

5.2 Typical DC Characteristics of MOS-HEMT

Figure 15 (a) Typical transfer characteristics with various $L_{GD}$. (b) Typical output characteristic.

Typical DC transfer and output characteristics of the GaN $SiO_2$ MOS-HEMTs fabricated on Azzurro GaN-on-Si substrate are plotted in Figure 15. For devices with $L_{GD} = 10 \mu m$, the drain current with $V_G = 0 \, V$ is 17.7 mA gives a current density of 354 mA/mm which is close to the values found in the published literature [5, 11, 14].

To study the device-to-device variation, we took drain current measurements on multiple devices with different $L_{GD}$ and plotted the result in Figure 16(a). As can be seen, drain current drops as $L_{GD}$ increases while the variation of drain current also decreases. This implies that the access regions of those devices have large variation in defect density or actual dimension, and this difference gets averaged and cancelled by longer $L_{GD}$. Figure 16(b) shows the temperature dependency of the MOS-HEMTs, where higher temperature reduces electron mobility and
increases the on-state resistance \( R_{on} \). Wellekens et al. report a 38% drain current drop at 120 °C compare with room temperature \([15]\) while our reduction is around 50%.

**Figure 16** (a) On-state drain current distribution versus \( L_{GD} \). (b) Normalized on-state drain current distribution versus temperature.

### 5.2.1 Fabrication Issue

When fabricating MOS-HEMTs, several gate oxides and deposition methods were compared. Professor Kim’s group fabricated devices with high on/off ratio using CVD and RF-sputtered deposition techniques with SiO\(_2\) and TiO\(_2\); however, devices with ALD Al\(_2\)O\(_3\) gate oxide consistently showed high gate leakage current. Figure 17 plots the transfer characteristic of the GaN MOS-HEMTs with ALD Al\(_2\)O\(_3\) gate insulator grown on different substrates; a high sub-threshold drain leakage current and low on/off ratio can be observed. We believe this is the result of a contaminated ALD system that Professor Kim’s group used for fabrication since there is no such issue for all the other fabricated samples, and other research groups \([5, 16, 17]\) have successfully demonstrated high performance MOS-HEMT with ALD Al\(_2\)O\(_3\) gate oxide.
Figure 17 Transfer characteristic of a MOS-HEMT with ALD $Al_2O_3$ gate oxide, high sub-threshold drain leakage current reflects low oxide quality.

5.3 Drain Breakdown

Off-state drain breakdown voltage directly determines the operational voltage of a power transistor. In this section, we use CVD $SiO_2$ MOS-HEMTs with NTT-AT substrate for the drain breakdown study since it has the lowest leakage current among all the fabricated samples. The customized high voltage measurement setup that was discussed in Chapter 4 was used to extract drain breakdown voltage of MOS-HEMTs. We first measured the breakdown voltage of a group of MOS-HEMTs with different drain-to-gate distance ($L_{GD}$), the result is plotted in Figure 18. As can be seen in Figure 18(a), most of the devices initially have a relative low drain leakage current except the one with $L_{GD} = 30 \mu m$, whose leakage current is about ten-thousand times higher than others. Pre-existing defects formed during the fabrication, which is likely located in the gate oxide, is the cause of this difference. As drain voltage increases, all devices breakdown eventually with a snapback which implies a short circuit was formed between the drain and source terminal. Moreover, the relationship between $L_{GD}$ and the breakdown voltage is not purely linear due to device-to-device variation, but it is clear that devices with larger $L_{GD}$ tend to have higher breakdown voltage because a longer access region reduces the electric field strength, and therefore reduces the stress. Besides, drain breakdown voltage is expected to stop increasing with $L_{GD}$ once the lateral breakdown voltage exceeds the vertical breakdown voltage.
Figure 18 (a) Off-state drain voltage sweep for the breakdown voltage extraction, the snapback occurs when a device is broken and shorted. (b) Extracted drain breakdown voltage versus $L_{GD}$.

Since the drain breakdown measurement shows relative large device-to-device variation, we measured several sets of devices with different $L_{GD}$ to obtain the average breakdown voltage (Figure 19). Although the measured breakdown voltages have a wide distribution (~30% variation), the average breakdown voltage increases as $L_{GD}$ does imply that lateral breakdown is the dominant breakdown mechanism for the $L_{GD}$ that we are using. Table 4 shows the drain breakdown voltage comparison with other work. Besides, temperature-controlled experiments in Figure 19(b) show that elevated temperature greatly reduces the breakdown voltage.

Figure 19 (a) Off-state drain breakdown voltage distribution versus $L_{GD}$. (b) Off-state drain breakdown voltage distribution versus temperature.
Table 4 Comparison of off-state drain breakdown voltage with published data.

<table>
<thead>
<tr>
<th>Author</th>
<th>Gate information</th>
<th>$L_{GD}$ [μm]</th>
<th>$V_{D,BD}$ [V]</th>
</tr>
</thead>
<tbody>
<tr>
<td>[5]</td>
<td>$Al_2O_3$ GI, recessed etched</td>
<td>6</td>
<td>450</td>
</tr>
<tr>
<td>[11]</td>
<td>$LaLuO_3$ GI, F plasma ion implant</td>
<td>10</td>
<td>474</td>
</tr>
<tr>
<td>[18]</td>
<td>$Al_2O_3$ GI</td>
<td>10</td>
<td>760</td>
</tr>
<tr>
<td>Ours</td>
<td>$SiO_2$ GI</td>
<td>10</td>
<td>580</td>
</tr>
</tbody>
</table>

5.4 Gate Oxide

This section covers the gate oxide related characterization of CVD 12 nm $SiO_2$ MOS-HEMT fabricated on Azzurro substrate. Compared with the thermal-grown $SiO_2$ in CMOS processes, $SiO_2$ grown on GaN using CVD usually has lower quality regarding defect density and breakdown electric field. Figure 20 is the gate leakage/breakdown measurement result of multiple devices. For positive gate voltage ramp, two obvious current step-ups can be seen in Figure 20(a). The first step-up occurs around 6 V with about a $10^5$ x gate leakage current increase and relative large step-up voltage variation. This step-up is the result of soft breakdown which corresponds to new defect formation in the gate oxide. The second step-up that occurs around 13 V corresponds to hard breakdown and its step-up voltage is more predictable. Moreover, the oxide hard breakdown is higher with a higher ramp-rate, which is consistent with conventional silicon CMOS research since a lower ramp-rate gives a longer stress time and forms more defects. We also performed reverse gate bias ramp on three devices. The breakdown voltage is much higher compared with the positive gate ramp since in this case the gate voltage was applied to a thicker film (both the gate oxide and the semiconductor layer) and the electric field strength was reduced.

Figure 20 Forward (a) and reverse (b) gate leakage/breakdown measurement of multiple devices.
5.4.1 Constant Voltage Stress and TDDB

Compared with gate breakdown measurement with a voltage ramp, monitoring the gate leakage current with a constant gate bias provides more information regarding the quality of the gate oxide. When a constant gate voltage is applied to the MOS-HEMT while the source and drain are grounded, gate oxide will break down after some amount of time. This failure mechanism is Time-Dependent Dielectric Breakdown (TDDB), which is caused by the new defects (leakage path) formation during the stress. Figure 21(a) plots a group of gate current waveforms of the same device with different applied bias voltage. With gate bias lower than 4 V, the gate current is very quiet and the noise is dominant by SMU’s quantization noise. With 4 V gate bias, the gate current become slightly noisy around 500 seconds indicates formation of new defects. Higher gate bias accelerated the defect-formation process resulting in a much noisier current reading and eventually leads to oxide hard breakdown at $t_{BD}$. Unlike conventional CMOS devices with high-quality gate oxide, gate oxide of GaN MOS-HEMT has a large number of defects which makes the transient current waveform noisier and creates multiple soft breakdowns before the hard breakdown occurs. An example of gate current transient waveform is shown in Figure 21(b).

![Figure 21](image)

Figure 21 (a) Gate current transient waveform of the same device with different applied gate bias. (b) Gate current transient waveform of a device under a constant gate voltage stress.

Multiple devices were stressed and their corresponding hard breakdown times were recorded to obtain a trend of $t_{BD}$ as the gate stress voltage decreases. Table 5 shows the result of this test. We use $J_{G,th} = 10 \text{ A/cm}^2$ as the definition of hard breakdown. Although we are unable to predict the oxide lifetime due to the limited sample availability, the relationship between the $t_{BD}$ and gate stress voltage can be seen clearly.
Table 5 Recorded hard breakdown time ($t_{BD}$) of constant gate voltage stress.

<table>
<thead>
<tr>
<th>Stress voltage [V]</th>
<th>Number of DUTs measured</th>
<th>$t_{BD}$ [second]</th>
<th>Average $t_{BD}$ [second]</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>2</td>
<td>$&gt; 2 \times 10^4$</td>
<td>$&gt; 2 \times 10^4$</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>$&gt; 2 \times 10^4$</td>
<td>$&gt; 2 \times 10^4$</td>
</tr>
<tr>
<td>5</td>
<td>3</td>
<td>4013, 5469, 2</td>
<td>3161</td>
</tr>
<tr>
<td>6</td>
<td>3</td>
<td>210.6, 136.4, 451.3</td>
<td>266</td>
</tr>
</tbody>
</table>

Lagger et al. reports an around 80 second gate oxide breakdown time for a constant 10 V gate stress using MOS-HEMTs with 30 nm $SiO_2$ gate oxide [19]. Compared with our result (12 nm $SiO_2$), the electric field applied to the gate oxide in [19] is lower and the oxide breakdown time is shorter. Wu et al. reports an around 25 second gate oxide breakdown time for a constant 10 V gate stress using MOS-HEMTs with 10 nm $Si_3N_4$ and 5 nm $Al_2O_3$ gate oxide [17].
6. Trap-Related Characterizations

This chapter discusses trap-related effects in GaN MOS-HEMTs together with measurement results. Unless otherwise noted, all the devices used in this chapter were fabricated on Azzurro substrate with 12 nm thick CVD grown SiO₂ as gate oxide. Figure 22 shows the epitaxial layer structure of the sample, permittivity of AlGaN was calculated using the expression given in [8], also listed in (6).

\[
\epsilon_{r,Al_{0.23}Ga_{0.77}N} = -0.5x + 9.5
\]  

<table>
<thead>
<tr>
<th>GATE</th>
<th>( \epsilon_r )</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂</td>
<td>12 nm</td>
</tr>
<tr>
<td>GaN</td>
<td>4 nm</td>
</tr>
<tr>
<td>Al_{0.23}Ga_{0.77}N</td>
<td>20 nm</td>
</tr>
<tr>
<td>AlN</td>
<td>1 nm</td>
</tr>
<tr>
<td>GaN</td>
<td>1.5 μm</td>
</tr>
<tr>
<td>Transition</td>
<td>4.2 μm</td>
</tr>
<tr>
<td>Si (111)</td>
<td></td>
</tr>
</tbody>
</table>

Figure 22 Cross-sectional view of MOS-HEMT’s gate region with layer thickness and relative permittivity labeled.

6.1 Capacitance Method

The capacitance method is one of the most convenient measurement techniques to estimate the trap distribution in a GaN MOS-HEMTs with moderate accuracy. This section discusses the capacitance measurement setup and the information extracted from the measurement data.

6.1.1 CV Sweep Setup

We used HP 4284A Precision LCR Meter for High-Frequency Capacitance Voltage (HFCV) measurement and Agilent 4155C Semiconductor Parameter Analyzer for Quasi-Static Capacitance Voltage (QSCV) measurement. For the QSCV sweep, the SMU calculates DUT’s capacitance by measuring displacement current in a given amount of time. For the HFCV sweep, LCR meter measures the impedance of the DUT and then converts it to a given capacitance and resistor (RC) model. LCR meter usually supports two-element RC models, as shown in Figure 23, for measurement result interpretation. We chose the parallel model for our measurement since the estimated minimum impedance of the capacitance test structure is around 1.59 j kΩ which is larger than the 1 j kΩ reference value provided in [13].
Figure 23 Parallel and series RC model used for the capacitance measurement result interpretation.

Figure 24(a) shows the HFCV and QSCV measurement result. As we expected, there are two capacitance step changes with increasing bias voltage. The one that occurs around the MOS-HEMT’s threshold voltage (-8 V) corresponds to the depletion of the 2DEG, where electrons located at the AlN/GaN interface (blue dash line in Figure 22) are no longer exist and do not contribute to gate capacitance. The other step up occurs at the positive bias voltage that causes the loss confinement of the 2DEG; consequently, electrons are located at the SiO$_2$/GaN interface (red dash line in Figure 22). The frequency dispersion can be seen for the second capacitance step-up, this trap related effect will be discussed later. Besides, as shown in Figure 24(b), a negative shift in both step up voltages can be seen at a higher temperature.

Figure 24 (a) Result of CV sweep with various test frequencies at room temperature. (b) Comparison of CV measurement result at room temperature and elevated temperature.

To verify the accuracy of measured data, we extracted the measured capacitance at -3 V and 3 V bias and compared them with calculated stack capacitance with electrons are confined in the 2DEG and present at the oxide-semiconductor interface. The comparison result listed in Table 6 indicates an accurate measurement.
### Table 6 Comparison of measured and theoretical calculated capacitance.

<table>
<thead>
<tr>
<th>Bias [V]</th>
<th>(C_{\text{measure}} ) [pF]</th>
<th>(C_{\text{calculate}} ) [pF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>-3</td>
<td>47.8</td>
<td>48.5</td>
</tr>
<tr>
<td>3</td>
<td>91.0</td>
<td>90.4</td>
</tr>
</tbody>
</table>

### 6.1.2 Carrier Density Extraction

For a GaN MOS-HEMT, it is expected to have a high electron density at the AlGaN/AlN interface (36 nm depth) where 2DEG is located and the SiO\(_2\)/GaN interface when 2DEG losses confinement at a high gate bias voltage. For a MOS-FET, carrier density of the semiconductor can be extracted from the measured CV data. Moreover, Ambacher et al. has shown that the C-V profiling technique is also applicable for a HEMT structure [8]. Carrier concentration and the corresponding depth can be calculated by the measured capacitance (Equations (7)-(8) [8]).

\[
N_{CV}(W) = -\frac{C^3}{q\varepsilon_0\varepsilon_r A^2} \frac{dV}{dC} \quad (7)
\]

\[
z_C = \frac{\varepsilon_0 \varepsilon_r(z_C)A}{C} \quad (8)
\]

Here \(N_{CV}\) is the free carrier concentration, \(C\) is the measured capacitance, \(A\) is the area of the test structure, \(z_C\) is the depth. For a silicon MOS-FET, since there is no other material present between the substrate and the gate oxide, the relative permittivity used in the calculation is fixed. For GaN devices, however, the relative permittivity is the effective permittivity of the material stack between the gate metal and \(z_C\), Equation (9) shows the expression of \(\varepsilon_r(z_C)\) for the few layers on top of the sample. To obtain the correct carrier density profile, \(z_C\) and \(\varepsilon_r(z_C)\) must be solved iteratively.

\[
\varepsilon(z_C) = \begin{cases} 
\varepsilon_{SiO_2}, & z_C \leq t_{SiO_2} \\
\frac{t_{SiO_2} + z_C - t_{SiO_2}}{\varepsilon_{SiO_2} - \varepsilon_{GaN}}, & t_{SiO_2} < z_C \leq t_{SiO_2} + t_{GaN} \\
\frac{t_{SiO_2} + t_{GaN} + z_C - t_{SiO_2} - t_{GaN}}{\varepsilon_{SiO_2} + \varepsilon_{GaN}}, & t_{SiO_2} + t_{GaN} < z_C \leq t_{SiO_2} + t_{GaN} + t_{AlGaN} \\
\vdots & \vdots \end{cases} \quad (9)
\]

To avoid the numerical error caused by measurement noise, e.g. quantization noise from the instrument, only the portion of CV data that has relative large derivative, e.g. \(\frac{dC}{dV} > 0.2 \frac{pF}{V}\), were used. The calculated carrier density profile is shown in Figure 25(b), which matches well with theoretical expectation. Our carrier density is similar to the result reported in the literature such as [16].
Figure 25 (a) HFCV measurement data used for carrier density extraction, data points with marker are selected for calculation. (b) Calculated carrier density profile using selected data points marked in (a).

6.1.3 Trap Estimation

A trap with a given time constant $\tau$, is able to respond to an AC signal for which the frequency is no higher than $f = 1/\tau$. Large frequency dispersion observed during HFCV measurements at the forward gate bias implies a wide distribution of the interface traps’ time constant, e.g. all traps can respond to the QSCV signal at a relatively low gate bias while only a small portion of them can respond to a 1 MHz HFCV signal even at the highest bias level. Trap density can be estimated by using the step-up voltage difference between those two measurement frequencies. Figure 26 shows the process of extracting the second step-up voltage $V_{fd}$ by extrapolating the linear region of the capacitance step up and calculate their corresponding $x$-intercept.

Figure 26 Zoom-in view of the CV sweep result emphasis on the second capacitance step up, data points with marker were used in a linear fit, fitting results are plotted as dotted lines and their $x$-intercepts with $C_p = C_{-3V}$ are the second step-up voltage $V_{fd}$.
The density of trap states can be estimated by using the $V_{fd}$ difference shown in Equation (10) and the trap energy level ($E_{CT} = E_c - E_T$) can be calculated from the emission time constant $\tau_e$ by Equation (11) [20].

$$D'_{it} = C_{ox} \cdot \Delta V_{fd}/q$$  \hspace{1cm} (10)

$$\frac{1}{f} = \tau_e = \frac{1}{v_{th} \sigma N_C} e^{(E_c - E_T)/kT}$$  \hspace{1cm} (11)

Here $C_{ox}$ is the gate oxide capacitance, $v_{th}$ is the thermal velocity, $\sigma_n$ is the electron capture cross section, $N_C$ is the effective density of states in the conduction band. For two sets of CV measurement data with different frequencies, the total density of traps that can respond to the lower frequency but not to the higher frequency can be calculated. When the frequency difference between those two measurements is relatively small, the corresponding trap energy level difference ($E_{CT1} - E_{CT2}$) is low. By assuming evenly distributed density of traps in each narrow energy level segment, the average trap density can be estimated by $\overline{D_{it}} = D'_{it} / (E_{CT1} - E_{CT2})$. The calculated interface trap state density is listed in Table 7 by assigning $N_C = 2.7 \times 10^{18} \text{ cm}^{-3}$, $v_{th} = 2 \times 10^7 \text{ cm/s}$, $\sigma_n = 1 \times 10^{-14} \text{ cm}^{-2}$ [20], and $kT = 25.9 \text{ mV}$. The extracted trap densities appear to be reasonable. Huang et al. reports $D_{it} = 4.1 \times 10^{12} \text{ cm}^{-2}$ for trap states between 0.40 eV and 0.46 eV, $D_{it} = 3.0 \times 10^{12} \text{ cm}^{-2}$ for trap states between 0.46 eV and 0.52 eV, $D_{it} = 2.0 \times 10^{13} \text{ cm}^{-2}$ for trap states deeper than 0.52 eV for a GaN MOS-HEMT with $Al_2O_3$ gate oxide [20]. The estimated trap density of our sample is in the same order of magnitude; our sample also has a lower gate leakage current allowing us to perform a QSCV sweep for the entire bias voltage range.

**Table 7 Estimated trap density and trap energy level by the capacitance method.**

<table>
<thead>
<tr>
<th>$D'_{it} \text{ [cm}^{-2}]$</th>
<th>$E_{CT} \text{ [eV]}$</th>
<th>$\overline{E_{CT}} \text{ [eV]}$</th>
<th>$\overline{D_{it}} \text{ [cm}^{-2}\text{eV}^{-1}]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$2.51 \times 10^{12}$</td>
<td>0.62 – 0.70</td>
<td>0.66</td>
<td>$3.24 \times 10^{13}$</td>
</tr>
<tr>
<td>$1.05 \times 10^{12}$</td>
<td>0.54 – 0.62</td>
<td>0.58</td>
<td>$1.26 \times 10^{13}$</td>
</tr>
<tr>
<td>$2.46 \times 10^{12}$</td>
<td>0.46 – 0.54</td>
<td>0.50</td>
<td>$3.17 \times 10^{13}$</td>
</tr>
<tr>
<td>$1.25 \times 10^{12}$</td>
<td>0.42 – 0.46</td>
<td>0.44</td>
<td>$3.01 \times 10^{13}$</td>
</tr>
<tr>
<td>$1.16 \times 10^{12}$</td>
<td>0.38 – 0.42</td>
<td>0.40</td>
<td>$3.24 \times 10^{13}$</td>
</tr>
<tr>
<td>$7.86 \times 10^{11}$</td>
<td>0.34 – 0.38</td>
<td>0.36</td>
<td>$1.89 \times 10^{13}$</td>
</tr>
</tbody>
</table>

### 6.2 Conductance Method

The conductance method provides the most accurate result for trap estimation. It measures the equivalent parallel conductance of the MOS capacitor which represents the loss
mechanism due to interface trap capture and emission of electrons [21]. Figure 27(c) is the equivalent circuit model of the MOS capacitor used for the conductance method.

\[
\tau_{it} = R_{it}C_{it} \quad [21]
\]

**6.2.1 Cf Sweep**

Multiple Capacitance-Frequency (Cf) sweeps were performed at different bias levels for trap characterization using the conductance method. Figure 28 shows the measurement result interpreted by a parallel capacitance-conductance model shown in Figure 27(a).

Since the conductance method needs to extract trap information from \( G_p \) but the LCR meter is only capable of converting the measurement result into a two-element RC model, a circuit model conversion is needed. By assuming a constant oxide capacitance, Equation (12) [21] can be used for the circuit model conversion.
\[ \frac{G_P}{\omega} = \frac{\omega G_m C_{OX}^2}{G_m^2 + \omega^2 (C_{OX} - C_m)^2} \] (12)

6.2.2 Trap Estimation

To extract the trap density and the corresponding time constant, the measured \( \frac{G_p}{\omega} \) data were fitted to the single trap energy model shown in Equation (13) [21].

\[ \frac{G_P}{\omega} = \frac{q\omega \tau_{it} D_{it}}{1 + (\omega \tau_{it})^2} \] (13)

As shown in Figure 29, measured and fitted data matches well around the peak and in the high frequency portion of the curves, implying that the single trap energy model is valid for our samples. The few outliers at the lower frequency band are the result of measurement noise.

![Figure 29](image)

**Figure 29** Comparison of the measurement result (markers) and fitting result (dashed lines) using the single trap energy model for the conductance method.

Trap densities and time constants were obtained directly from the model fitting are listed in Table 8. Our extracted trap density is in the middle of the data published by the other groups [14, 16, 22] which range from \( 2 \times 10^{12} \text{ cm}^{-2} \text{eV}^{-1} \) to \( 3 \times 10^{13} \text{ cm}^{-2} \text{eV}^{-1} \); the trap density is an increasing function of the energy level is also consistent with the literature.

<table>
<thead>
<tr>
<th>( V_{bias} ) [V]</th>
<th>( \tau_{it} ) [( \mu )s]</th>
<th>( E_{CT} ) [eV]</th>
<th>( D_{it} ) [cm(^{-2} \text{eV}^{-1} )]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>5610</td>
<td>0.57</td>
<td>( 2.38 \times 10^{12} )</td>
</tr>
<tr>
<td>0.5</td>
<td>1690</td>
<td>0.54</td>
<td>( 7.94 \times 10^{12} )</td>
</tr>
<tr>
<td>1.0</td>
<td>415</td>
<td>0.50</td>
<td>( 1.23 \times 10^{13} )</td>
</tr>
<tr>
<td>1.5</td>
<td>186</td>
<td>0.48</td>
<td>( 1.84 \times 10^{13} )</td>
</tr>
<tr>
<td>2.0</td>
<td>99.8</td>
<td>0.46</td>
<td>( 2.58 \times 10^{13} )</td>
</tr>
</tbody>
</table>
The extracted trap information using the capacitance and conductance method are plotted in Figure 30. Compared with the capacitance method, works [21, 22] have shown that the conductance method is more accurate for trap characterization for Si and GaN MOS structure. Besides, the conductance method extracts the trap density and time constant from the measurement result without using any additional physical constant, such as the electron capture cross section, resulting in a higher accuracy. However, trap energy level coverage is narrower for the conductance method since lower bias voltages were used during the Cf sweep to avoid gate oxide breakdown. Other techniques, such as the pulse method [23], can be used to probe a wider range of the bandgap with a high accuracy. Besides, since both the capacitance and the conductance methods rely on the gate capacitance measurement, only traps that located in the gate region can be detected and traps that located in the access region needed to be characterized by other methods.

![Figure 30 Comparison of the trap density extracted by using the capacitance and conductance methods.](image)

6.3 Pulse Measurement

We use pulse IV measurements to study the relationship between trapping and drain current transient effects. Compared with the conventional staircase IV sweep which measures all the bias points continuously, pulse measurement ensures the DUT returns to its initial state before another measurement point is taken. For a MOS-HEMT, since charges trapped below the gate and in the access region are most commonly reported, we characterized those traps by conducting gate and drain pulse measurements.

6.3.1 Zero Base Gate Pulse

Figure 31(a) shows the gate and drain voltage waveform of the gate pulse measurement with a zero base voltage. The DUT was pulsed from a zero gate bias (on-state) to a negative gate
voltage (off or semi-on state) where the drain current measurement was taken. The recovery time between each pulse is long enough, e.g. 10 minutes, to allow the device to recover to its initial state.

Figure 31 (a) Voltage waveform applied to DUT’s gate and drain terminal, drain current is measured at the end of each gate pulses. (b) Pulsed transfer characteristic with various pulse width and a zero base gate voltage, the green dash line indicates the current level used for threshold voltage extraction.

The pulse measurement result is shown in Figure 31(b), on-state drain current was extracted at $V_G = 0 \, V$ and threshold voltage was extracted using the constant current method with $I_{D,\text{th}} = 50 \, nA$. As can be seen from Figure 32, the threshold voltage is lower when a longer pulse width is used because the negative gate bias detraps electrons in the gate region; furthermore, the maximum drain current remains the same, which implies there is no change in the access region during this measurement.

Figure 32 Extracted threshold voltage from the zero base voltage gate pulse sweep. Inset: extracted maximum drain current at $V_G = 0 \, V$. 

33
6.3.2 Negative Base Gate Pulse

Figure 33(a) shows the gate and drain voltage waveform of the gate pulse sweep with negative base voltages. The DUT is pulsed from a given negative gate bias to an off or semi-on state for the drain current measurement. The recovery time between each pulse and hold time before the entire sweep is long enough, e.g. 10 minutes, to allow the device to return to its original state.

Figure 33(b) shows the measured transfer characteristic with different negative gate base voltages. All the transfer curves with negative base voltages show an around -0.5 V threshold voltage shift. This is consistent with the result from the zero base gate pulse measurement, which implies that reverse gate bias helps detraping in the gate region. Besides, lowered the base voltage also caused the maximum drain current to drop. This indicated that more electrons were trapped in the access region with lower base voltage. It is possible that -2 V gate bias is enough to detrap most of the traps in the gate region since the threshold voltage shift almost remains unchanged as the base voltage decreases further. Drain current drop and threshold voltage shift are also reported in [24] where a packaged MOS-HEMT was used for the pulse measurement. By pulsing the device from $V_G = -10 \, V, V_D = 400 \, V$ with $5 \, \mu s$ pulse width, an around -1 V threshold voltage shift and 20% drain current drop was observed.

![Figure 33 (a) Voltage waveform applied to the DUT’s gate and drain terminal (gate base voltage is -6 V), drain current is measured at the end of each gate pulses. (b) Pulsed transfer characteristic with various base gate voltages.](image)

6.3.3 Zero Base Drain Pulse

Figure 34(a) shows the gate and drain voltage waveform for the drain pulse measurement. The drain voltage of the DUT is pulsed from zero (no channel current) to a given value (current flows through the channel) for the drain current measurement. The recovery time between each
pulse is long enough, e.g. 10 minutes, to allow the device to return to its original state. Drain current increases with longer pulse width indicates that the device is not sensitive to the self-heating effect when it is dissipating power. Instead, this effect is caused by detrapping in the access region, which also creates the kinks and NDR in the output characteristic.

Compared with the measurement result from others, however, our data shows the opposite trend as the pulse width increases. In [10], 0.2 μs to 100 μs pulse widths were used and the drain current decreased for more than 25% as the pulse width increased [10]. Difference of the trap distribution in the gate and the access region between our MOS-HEMTs and the devices used in [10] could cause this discrepancy. Moreover, the pulse widths that we used in our measurements were much larger than the ones used in [10]; and the traps which were detected by the pulse signal could be different.

![Figure 34](image.png)

**Figure 34** (a) Voltage waveform applied to the DUT’s gate and drain terminal, the drain current is measured at the end of each gate pulses. (b) Pulsed output characteristic with a zero base drain voltage.

Although the pulse measurements could not provide any quantitative result of the trap distribution in a GaN MOS-HEMT as the capacitance measurements do, they could predict the device’s response to a given circuit stress. Experiments in which the gate voltage is pulsed from a zero base voltage showed that biasing the transistor in the linear region with a negative gate voltage induces a negative threshold voltage shift which results in an increase of the on-state drain current. Experiments in which the gate voltage is pulsed from negative base voltages showed that the drain bias causes severe trapping effect in the access region which increases the on-state resistance ($R_{on}$) when the device is in the off or semi-on state. Drain pulse measurements with a zero drain base voltage have the drain voltage and pulse width dependency since several curvature changes were found from the pulsed $I_D-V_D$ curves. This implies that the drain current
transient waveform may not be monotonic for an on-state stress due to the existence of multiple (de)trapping mechanisms and the detailed characterization should be done in the future.

6.4 Transient Degradation

Although pulse measurements can provide information about trapping mechanisms for a given condition, it cannot predict the exact transient behavior of a MOS-HEMT in a real circuit state, such as a constant voltage state or a switching state. This section discusses the result of transient degradation using DC and AC stresses.

6.4.1 Constant Voltage Stress

When a constant drain and gate voltage is applied to a GaN MOS-HEMT and bias it in the on- or semi-on state, its drain current may change with time as the result of trapping and/or detrapping. Figure 35(a) compares the drain current transient waveform of different gate biases in the linear region, a monotonic drain current increase can be observed for all curves with non-zero gate voltages. Although a higher reverse gate bias reduces the drain current as it depletes the 2DEG, it increases the rate of drain current increase which corresponds to the slope \( \frac{dI_D}{d(\log t)} \) of the \( I_D \)-time curve, e.g. the drain current increases faster with a lower gate bias. Since the drain bias is low (device in linear region) and the rate of drain current increase is proportional to the reverse gate bias voltage, this effect is the result of a negative threshold voltage shift induced by the detrapping effect in the gate region. This observation is similar to the threshold voltage recovery after a forward gate stress reported in [19], where the rate of the threshold voltage recovery is nearly constant in the first 1k seconds of the measurement.

Figure 35(b) compares the drain current transient waveform with different applied drain bias voltages. For low drain voltages such as 1 V, the drain current almost remains constant since the (de)trapping effect is negligible. For moderate drain voltages, the drain current first slightly increases in the first few seconds of stress and then starts to drop. This change of the curvature appears earlier for a higher drain voltage. With a high drain voltage between 10 and 20 V, the curvature change happens even earlier and the drain current keeps increasing at the end of stress which makes it exceed the initial value. This phenomenon shows that there are multiple (de)trapping mechanisms taking place during the drain stress and the bias voltage may be able to change the time constant of those effects. This drain current transient phenomenon cannot be explained by the “current collapse” which corresponds to drain current reduction that results from the application of a drain-source bias [25]. A similar drain current transient waveform is also reported in [26], that a HEMT was biased in on-state with \( V_D = 0.5 \) V, an around 7% drain
current fluctuation can be seen and the corresponding time constant changes with the bias and temperature applied.

![Graphs showing drain current transient waveform with various gate voltages and drain voltages.](image)

Figure 35 (a) Drain current transient waveform with a fixed drain bias and various gate voltages. (b) Drain current transient waveform with a fixed gate bias and various drain voltages.

### 6.4.2 Off-State Stress

Compared with on-state stress, monitoring the device state is more difficult during off-state stressing since one cannot extract a device’s performance when it is off. Therefore, we developed a stress-measure loop to monitor device degradation during the off-state stress and the recovery after the stress is removed. The bias condition during the stress and recovery are shown in Figure 36. Device parameters such as the threshold voltage and maximum drain current are extracted from the fast IV sweep.
Figure 36 Flow chart of the sweep-stress and recovery-sweep loop used to monitor device degradation during the off-state stress and post-stress recovery. Device was characterized by the Fast IV sweep, which ramps $V_G$ from -8 V to 0 V with $V_D$=1 V at a ramp-rate of 3 kV/s. All instruments were controlled automatically by the software.

Figure 37 shows the extracted maximum on-state drain current of the DUT during off-state stress and recovery. During the stress, the maximum drain current drops as a function of time implies that electrons are trapped in the access region. During the recovery, the extracted on-state drain current shows opposite behavior as the stress indicates the access region detrapping. Slow drain current degradation and recovery are ascribed to the long time constants, e.g. several hundred seconds, of the traps which are located deeply in the bandgap. Extracted threshold voltage is not shown since the change is negligible.
The device in the off-state stress exhibits a more than 80% on-state drain current drop while the device in the on-state stress barely sees any change. Thus, the off-state stress brings more degradation to the device. This observation is consistent with the result reported in [27] where a HEMT was stressed at off-state with $V_G = -9 \, V$. The stress caused an around 50% recoverable drain current drop, and the time constant of the corresponding traps are between 100 second and 1000 second [27].

6.4.3 Device in Circuit

Although the on- and off-state stress tests provide some insight about the degradation mechanisms in GaN MOS-HEMTs, we are unable to predict the device’s behavior during the switching operation. To study the transient degradation when a MOS-HEMT is in a switching state, we applied a constant drain voltage to the DUT and drive the gate voltage to toggle the device on and off. Figure 38(a) shows the drain and gate voltage waveforms, a 10 Hz switching frequency was chosen to ensure the accuracy of the drain current measurement while the switching frequency of a typical power circuit is around 50 kHz. Figure 38(b) shows the normalized drain current versus time with various duty cycles. Clearly devices operating at a lower duty cycle shows a higher drain current drop. This observation proves that the off-state stress which causes $R_{on}$ to increase dominates the device’s performance during normal operation.

The switching state stress is a combination of on-state and off-state stresses; their bias conditions were also used in the DC stress tests. Therefore, we compared the results of the switching state stresses and DC stresses by comparing the total drain current drop. For a 100 second switching state stress with 10% duty cycle, for which the transistor is biased in the off-state for a total of 90 seconds and biased in the on-state for a total of 10 seconds, a 22% drain
current drop was observed. However, the corresponding off-state DC stress only has an 11% drain current drop while the drain current degradation is negligible for the on-state DC stress. Similarly, the drain current drop for a 100 second switching state stress with 50% duty cycle is 2.7% but a 50 second off-state DC stress degrades the drain current by more than 5%. Clearly, whether AC stress or DC stress causes more device degradation depends on the AC waveform duty cycle, and thus the correlation factor between the switching state (AC) stress and the DC stress is complicated, which needs more investigation in the future. Therefore, the device degradation in the switching state cannot be accurately predicted based on the results of the DC stress experiments. It is also worth mentioning that the amount of $R_{on}$ increase during the switching state is not a linear function of the duty cycle and this can be studied in the future.

![Figure 38](image)

**Figure 38** (a) Voltage waveform applied to the DUT’s gate and drain terminal, the drain current is measured at the end of each gate pulses. (b) Measured on-state drain current (normalized) from each stress cycles.

We have found that increasing the switching frequency reduces the rate of drain current drop since the time of off-state stress during each switching cycle is reduced, e.g. the rate of drain current decrease with 200 Hz switching frequency is lower than with 10 Hz. Besides, the drain voltage of a switching power transistor in the off-state is much higher than 1 V, thus the device will likely have a much higher drain current drop in that condition. To have a more accurate prediction about the device’s behavior, future study should be done by pulsing the gate and drain terminal simultaneously with various switching frequencies to emulate the real bias condition of a switching operation.
7. Conclusion

In this thesis, we have quantitatively evaluated the performance and reliability of GaN MOS-HEMTs fabricated at the University of Illinois for power switching applications, including the DC characteristic, gate oxide quality and trap-related effects. Customized measurement setups were designed and used. We have shown that the performance of GaN devices is mostly limited by trap-related effects. Trap distribution was estimated using the capacitance and conductance methods while trapping effects were illustrated by pulse measurements and stress tests. We have also shown that the performance of GaN MOS-HEMT in a switching power circuit is limited by the access region trapping which results from the application of a drain-source bias. High-quality gate oxide is needed for enhancement mode MOS-HEMTs to handle forward gate bias.

Although several aspects of the GaN MOS-HEMT have been investigated in this thesis, details of the degradation mechanisms and the drain current transient effects should be studied in the future. Extracting the trap distribution with different methods and using the result for a device simulation could provide more insight about the degradation mechanisms. Performing pulse measurements with a wider range of the pulse width, bias level and temperature could provide more information about the drain current transient effect during DC stress tests. Finding the correlation between the drain current degradation and the switching frequency, duty cycle and drain voltage waveform for a device in a switching state stress can help us to establish an aging model for GaN MOS-HEMTs.
References


