ASYNCHRONOUS DIFFERENTIAL POWER PROCESSING FOR TRUE MAXIMUM POWER POINT TRACKING OF PHOTOVOLTAIC SUB-MODULES

BY

FELIX ZEPHYR HSIAO

THESIS

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Adviser:

Assistant Professor Robert Carl Nikolai Pilawa-Podgurski
Abstract

This thesis examines maximum power point tracking (MPPT) at the photovoltaic (PV) sub-module level, but in the context of large arrays. Central communication carries large overheads, and neighbor-to-neighbor communication can have long propagation times in large arrays, so a communication-less solution was explored. An MPPT algorithm that could be run asynchronously was developed, and simulations confirmed its viability. Simulated tracking efficiencies of 99.977% and above were attained at steady-state.

Next, a power electronics hardware prototype was designed to implement the MPPT algorithm. A differential power processing (DPP) architecture was used to achieve high system efficiencies. The efficiency of a single DPP converter reached a peak of 94.0%. In the laboratory tests performed, an increase in PV module power of up to 29.7% was observed using the proposed method when compared to no sub-module MPPT.

Additionally, a long-term measurement system for a 12-module PV array was constructed. The system provided a safe, durable, and weatherproof mounting scheme for the power electronics and related circuitry. Furthermore, the setup allowed communication with the power electronics, so sub-module data could be collected and analyzed to determine the performance of the MPPT.

Possible future work includes gathering more results, revising the circuit board, and simplifying the measurement system.
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<tr>
<td>AC</td>
<td>Alternating Current</td>
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<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
</tr>
<tr>
<td>BBB</td>
<td>BeagleBone Black</td>
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<tr>
<td>DC</td>
<td>Direct Current</td>
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<td>DMM</td>
<td>Digital MultiMeter</td>
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<tr>
<td>DPP</td>
<td>Differential Power Processing</td>
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<tr>
<td>EMI</td>
<td>ElectroMagnetic Interference</td>
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<tr>
<td>ESR</td>
<td>Equivalent Series Resistance</td>
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<tr>
<td>FET</td>
<td>Field-Effect Transistor</td>
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<tr>
<td>I²C</td>
<td>Inter-Integrated Circuit</td>
</tr>
<tr>
<td>LDO</td>
<td>Low-DropOut (linear voltage regulator)</td>
</tr>
<tr>
<td>MCU</td>
<td>MicroController Unit</td>
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<tr>
<td>MPP</td>
<td>Maximum Power Point</td>
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<tr>
<td>MPPT</td>
<td>Maximum Power Point Tracking</td>
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<tr>
<td>Op amp</td>
<td>Operational amplifier</td>
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<tr>
<td>PC</td>
<td>Personal Computer</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
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<tr>
<td>PoE</td>
<td>Power over Ethernet</td>
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<tr>
<td>PV</td>
<td>PhotoVoltaic</td>
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<tr>
<td>PWM</td>
<td>Pulse-Width Modulation/Modulated (signal)</td>
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<tr>
<td>P&amp;O</td>
<td>Perturb and Observe</td>
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<td>TI</td>
<td>Texas Instruments</td>
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List of Symbols

Symbols for units are omitted.

- $C$: Capacitance
- $D$: Duty ratio/cycle
- $f$: Frequency
- GaN: Gallium nitride
- $I$: Current
- $k$: Boltzmann constant
- $L$: Inductance
- $n$: Ideality factor
- $P$: Power
- $q$: Electric charge
- $R$: Resistance
- $T$: Temperature
- $t$: Time
- $V$: Voltage
- $\phi$: Magnetic flux
1.1 Solar Power

Solar power is an attractive form of clean, renewable energy. It produces no greenhouse gases, and we need not worry about the source of power running out. Additionally, more and more solar generation is being added every year while the price is steadily decreasing. Even small-scale, residential rooftop installations are becoming cost-effective, especially if there are government incentives.

Solar power has much potential, but many factors need to be considered to ensure that the most power is being harvested. There are numerous areas of ongoing research related to solar power, ranging from solar cell fabrication to system-level integration. This thesis focuses on solar panel operation in a multi-panel system, rather than on solar panel design.

1.2 Power Electronics

Power electronics are circuits that perform power conversion in a controllable manner. Power may be converted from AC to DC (rectifier), DC to AC (inverter), or DC to DC. Direct AC to AC conversion is also possible, but uncommon; power is usually converted to DC as an intermediate step.

The applications of power electronics are essentially limitless: Solar panels produce DC power, which needs to be converted to AC power via an inverter if the panels are connected to the power grid. Conversely, a computer charger converts AC power from the outlet to DC power the computer can use. DC-DC converters produce different voltage levels within the computer.

As mentioned, the power electronics need to be controllable. They should
be able to adjust for changes in the load or input source. In motor drives, the output may have to change dynamically, whether it be the frequency or voltage level, to achieve desired motor behavior.

Nearly all of the electronics used in our daily lives contain some power electronics, even if we are not mindful of them. Given the omnipresence of power electronics, advancements in this field can yield significant benefits. Major topics of focus include efficiency, physical size, weight, waveform quality, cost, reliability, thermal management, and electromagnetic interference. It should be noted that for a given technology and architecture, there is generally a trade-off between these categories; one aspect can be improved by sacrificing others.

For this thesis, a buck-boost DC-DC converter was designed for power conversion within a solar panel as well as between panels. The objective was, naturally, to increase the total power generated by compensating for power mismatches while performing a process called maximum power point tracking. The power converters were intended to be installed on a small array of 12 solar panels with a nominal total power output of 2.94 kW. Inverter design was not the focus of this project, so a commercial inverter was used to connect the array to the grid as well as perform array-level maximum power point tracking.

A thorough explanation of relevant, fundamental principles will be given in Chapter 2. Detailed specifications and converter design will be discussed in Chapter 4.
Chapter 2

Background Theory

In this chapter, basic theory surrounding solar power and related power electronics will be covered. See Chapter [4] for a detailed discussion about the design of the power converter used for this thesis. The reader is expected to already understand the concepts of voltage, current, and power; be familiar with fundamental circuit elements such as resistors, capacitors, inductors, diodes, and switches; as well as be able to perform simple circuit analysis. The equations will be reviewed, and the analysis guided, but it is assumed that this is not the first time the reader has encountered these topics.

2.1 Theory of Photovoltaics

Devices that can produce voltage (and power) from electromagnetic radiation (or light, but not necessarily visible) are collectively called photovoltaics (PV). In this text, the term PV module is used interchangeably with solar panel. Device physics is not the main focus of this thesis, so the working principle of a conventional solar cell is very concisely as follows: A solar cell consists of positively-doped and negatively-doped semiconductor, usually silicon, joined together. A depletion region forms at the junction due to diffusion, and an electric field is established. Free charge carriers generated by incident electromagnetic radiation can then flow against the direction of external voltage polarity. Thus, power is generated as current flows out of the positive voltage terminal.

2.1.1 I–V Characteristic

Again, the underlying physics is not of primary concern here, but its effects will now be examined more rigorously from a circuits point of view. Many
electrical elements are often characterized by their I–V, or current–voltage, characteristic. In other words, the current is expressed as a function of voltage. This is a line in the case of a resistor, for example. For a diode, which is fundamentally no different from a solar cell, the relationship is exponential, and the Shockley ideal diode equation is given in Equation 2.1:

\[ I_D = I_0(e^{V_D/V_T} - 1) \]  

(2.1)

Here, \( V_D \) is the diode voltage from anode to cathode, \( I_D \) is the current into the anode, and \( I_0 \) is the reverse saturation current, which depends on device characteristics. The thermal voltage \( V_T \) is explicated in Equation 2.2, where \( k \) is the Boltzmann constant, \( T \) is the absolute temperature, and \( q \) is the elementary charge:

\[ V_T = \frac{kT}{q} \]  

(2.2)

For non-ideal diodes, an additional ideality factor \( n \) is introduced, and is unity only in the ideal case. Also, in PV systems, we are interested in the power produced, so the current is taken to be in the opposite direction by convention. Finally, the term \( I_{ph} \) is added to represent the photocurrent, or current generated by incident sunlight, thereby yielding Equation 2.3, the equation for a solar cell:

\[ I_{PV} = I_{ph} - I_0(e^{V_{PV}/nV_T} - 1) \]  

(2.3)

To account for losses as well as the dynamic response of the PV, resistors and capacitors can be included in the circuit model of a PV cell, as depicted in Fig. 2.1. At DC steady state, the capacitor will not have any effect on the circuit. The augmented equation for a solar cell then becomes Equation 2.4:

\[ I_{PV} = I_{ph} - I_0(e^{(V_{PV}+I_{PV}R_s)/nV_T} - 1) - \frac{V_{PV} + I_{PV}R_s}{R_p} \]  

(2.4)

Equation 2.4 is implicit and difficult to work with, but a well-designed PV cell will have \( R_s \) small enough and \( R_p \) large enough such that their effects are minor. Therefore, it is sufficient to perform an initial analysis using just Equation 2.3. Equation 2.4 can be easily incorporated in a computer simulation if deemed necessary.
2.1.2 Maximum Power Point Tracking

In practice, solar cells generate low voltages and high currents. To simplify wiring, reduce losses due to high current, and ease voltage conversion, cells are typically connected in series to form a string. Many series-connected cells make up a solar panel, and panels are further connected in series to form an array. This series connection presents additional challenges when there are mismatches, as will be covered in Section 2.1.3, but for simplicity, first consider the case where all the PV cells are equal. Their voltages sum, and the same current passes through all cells. Thus, the PV module will have the same characteristics as a single cell except with a multiplied voltage.

A sample I–V characteristic similar to that of the actual panel used in this project is plotted in Fig. 2.2a. Quantities of interest include the current at zero voltage, or short-circuit current $I_{\text{SC}}$, and the voltage at zero current, or open-circuit voltage $V_{\text{OC}}$. Power is voltage times current, and it is reasonable that there is one unique point on the I–V curve that corresponds to the highest power. This is called the maximum power point (MPP). For illustration, the power versus voltage (P–V) curve for the same I–V characteristic is plotted in Fig. 2.2b.

Ideally, we want the PV module to always operate at the MPP. In fact, at an arbitrary voltage that happens to be negative or greater than $V_{\text{OC}}$, the PV just behaves like a diode and becomes a load instead of a source. As such, maximum power point tracking (MPPT) is necessary. Moreover, the MPP changes with the amount of incident sunlight (also termed insolation or solar irradiance), so MPPT must be actively performed to track dynamic changes. It should be emphasized that MPPT is different from solar tracking, which is the physical movement of PV panels to maximize insolation. MPPT is the process of biasing PV modules with the correct voltage (and current) such that the maximum power is extracted for a given irradiance.

The actual operating point of a PV module is determined by the intersection of its I–V curve with the I–V curve of the load. It is unlikely that an arbitrary load will bias the PV at exactly its MPP, and typically the load cannot be controlled at will. Also, the MPP changes dynamically, as just discussed. Hence, power electronics are used to interface the PV module with the load. Power electronics are also responsible for executing the MPPT, making them indispensable in PV systems. To reiterate, there are two roles...
for the power electronics: perform MPPT to determine how the PV module must be biased, and convert the generated power to a form the load can use.

### 2.1.3 Mismatches

A major problem with the series connection of PV cells and modules arises when there are mismatches between them. These mismatches may be caused by differences in manufacturing, aging, temperature, or shading. In particular, partial shading of a PV module is commonly encountered and can have very significant effects. Since the PV cells are connected in series, they must all share the same current. Then if one cell is shaded, it will limit the current through the whole string. The system becomes inhibited by the weakest-performing cell. This implies that shading a single solar cell could compromise an entire array, even if the system contains numerous cells. Furthermore, the shaded cell becomes a load and creates a hotspot in the solar panel, degrading panel lifetime [1,2].

To mitigate the effects of partial shading, a simple and inexpensive solution commonly used in industry is the addition of bypass diodes. The cells in a PV module may be grouped into multiple sub-modules, with a bypass diode connected in parallel across each, cathode at the positive terminal. Under normal operation, the bypass diodes have no effect. However, when the voltage across a sub-module becomes negative (it has been shaded became a load), the bypass diode becomes active and essentially short-circuits the sub-module. The power produced by the sub-module is still lost, but the rest of the string remains relatively unaffected. Alternatively, the use of more sophisticated power electronics at the sub-module level allows the power produced by the shaded sub-module to be extracted, while keeping the other sub-modules at their optimal bias points. In other words, MPPT can be implemented at the sub-module level.

### 2.1.4 Differential Power Processing

In traditional PV systems, panels are connected in series and then tied to a central inverter, which converts the power to AC power for the grid as well as performing array-level MPPT. There is no module- nor sub-module-level
MPPT, potentially resulting in significant power loss. Distributed power electronics architectures that address this problem are presented in Fig. 2.3.

Firstly, DC-DC converters, also called DC optimizers in this context, may be connected in parallel with each PV module, and then connected in series before feeding to the central inverter. Figure 2.3a illustrates the arrangement. This method can also be extended to the sub-module level. The drawback to this approach is that all of the power is processed twice by the power electronics. Overall efficiency becomes prorated by the efficiency of the DC-DC converters. Work done in the area of DC optimizers include [3–6].

The next approach, depicted in Fig. 2.3b, uses micro-inverters; each PV module has its power directly converted to AC. Unfortunately, micro-inverters are seldom used at the sub-module level due to their high cost and low efficiency [7, 8]. The architecture employed in this project is called differential power processing (DPP), and is portrayed in Fig. 2.3c.

In DPP, only the differences in (sub-)module powers are processed, rather than the full system power. Nominally, all of the power flows through the string of PV modules to the central inverter, as if the distributed converters were not present. Only when there is a mismatch in power do the DPP converters shuffle this differential power around the modules. Since the power processed is usually low compared to the full system power, very high system efficiencies can be achieved. For instance, if the DPP converters are 90\% efficient, but only process 20\% of the total system power, overall system efficiency is 100\% \times (100\% - 90\%) \times 20\% = 98\%.

DPP is further motivated in [9–12]. Additionally, DPP has been investigated extensively in works such as [7, 8, 13–16], which were particularly similar to this thesis. More works using DPP for PVs include [17–24]. DPP can also be applied to other series-stacked systems, such as servers in data centers [25–30].

2.1.5 MPPT Algorithms

Devising good MPPT algorithms is an area of ongoing research. Many algorithms have been proposed, although most can be considered variations or sub-classes of established techniques. Some examples of MPPT algorithms used in similar work can be found in Chapter 3. For a more comprehensive
comparison of different MPPT techniques, the reader may refer to [31]. Here, a few relevant MPPT algorithms will be explored.

One of the simplest and most commonly used MPPT algorithms is perturb and observe (P&O), which is a hill-climbing algorithm. As the name suggests, the system is first perturbed and the resulting change in power is observed. If the power increased, then the system continues to be perturbed in the same direction. Otherwise, the system is perturbed in the reverse direction.

The main drawbacks of P&O include oscillation around the MPP as well as a slow rate of convergence, assuming the amount of perturbation, or step size, is constant. In fact, whenever a constant step size is used, there is always an inherent trade-off between convergence rate and steady-state accuracy. Additionally, the effect of noise must be considered when choosing the step size [32]. Furthermore, as a hill-climbing algorithm, P&O suffers from the possibility of tracking a local maximum rather than the true MPP. In the theoretical case, with no bypass diodes, PV modules will fortunately have only one maximum, although practical non-idealities may engender more [33]. Nevertheless, the simplicity of P&O makes it very popular. The proposed MPPT algorithm of this thesis is a variation of P&O.

An even simpler MPPT algorithm than P&O is virtual parallel. For this method, all of the PV modules are regulated to the same voltage, as if they were connected in parallel. The reasoning is that the voltage at the MPP does not vary much with insolation. In other words, even with mismatches in irradiance, the MPP voltages of the PV modules will be about the same. Equalizing all module voltages will then bias each of them at approximately their MPP. It should be emphasized that this is an approximate technique, and not true MPPT. However, the algorithm is very simple, and can even be implemented without feedback, as was done for part of this project. A more in-depth analysis of virtual parallel can be found in [34].

2.2 Power Electronics Theory

The following theory will be covered rather concisely, and the reader may wish to consult [35] for a more thorough analysis.

To reiterate, power electronics are circuits that convert power from one form to another. The conversion may be between DC and AC, as in recti-
Power conversion relies on the principles of temporary energy storage and switching. The energy storage devices, namely capacitors and inductors, act as buffers between the input and output, storing and releasing energy during different switching states. The desired result can then be achieved through calculated switching and filtering.

### 2.2.1 Power Electronics Fundamentals

Capacitors store energy using electric charge, while inductors store energy in a magnetic field. Equations 2.5 and 2.6 define capacitance and inductance, respectively:

\[
C = \frac{q}{V_C} \quad \text{(2.5)}
\]

\[
L = \frac{\phi}{I_L} \quad \text{(2.6)}
\]

The charge on each conductor of the capacitor is \( q_C \), and the total magnetic flux through the coils of the inductor is \( \phi_L \). In power electronics, the equivalent differential equations are more useful, and are given by Equations 2.7 and 2.8:

\[
I_C = C \frac{dV_C}{dt} \quad \text{(2.7)}
\]

\[
V_L = L \frac{dI_L}{dt} \quad \text{(2.8)}
\]

Since currents cannot be infinite, capacitor voltages cannot change instantaneously. Similarly, inductor currents must be continuous. Capacitors and inductors can thus be regarded as temporary voltage and current sources, respectively. In addition, the average of the time derivatives must eventually go to zero, or else the voltages and currents will increase or decrease without bound. This implies that there is a periodic sequence of switching, and a periodic steady state will be reached. By setting the derivative terms to zero, Equations 2.9 and 2.10 are obtained:
These equations must always be true at periodic steady state. However, capacitor currents and inductor voltages are normally not equivalently zero; only their averages are. This means that the energy storage devices are constantly being charged and discharged, producing a ripple component in the capacitor voltages and inductor currents. Generally, this ripple is undesirable, and can be reduced by increasing capacitance/inductance, or increasing the switching frequency (decreasing $\Delta t$). From another perspective, this means that increasing frequency decreases the required amount of capacitance and inductance. This is noteworthy, as energy storage devices often make up the bulk of the volume, weight, and cost of power electronics. In the ideal scenario, frequency can be made arbitrarily high without penalty, but practical limitations prevent this, as will be discussed in Section 2.2.3. First, a concrete example may provide some more insight into the ideas just explored.

2.2.2 The Buck-Boost Converter

A buck-boost converter, the DC-DC converter used in this project, will now be analyzed. A schematic diagram of the converter is shown in Fig. 2.4. For the project, a synchronous buck-boost was actually used, in which the diode is replaced with a switch, to allow for bidirectional power flow. Nonetheless, the analyses are essentially the same, especially since the switches will be assumed ideal, for simplicity. Ideal switches behave like open circuits when they are open (off), and like short circuits when closed (on). The same are true for ideal diodes, but they cannot be turned on or off at will, being passive devices. Voltage is only blocked from cathode to anode, and current only flows from anode to cathode.

The high-level operation of a buck-boost converter is as follows: The switches are switched complementary to each other (as is the case for virtually all power electronics), meaning when one switch is on, the other is off, and vice versa. This occurs automatically if a diode is used. When the
active switch is on, the inductor is charged by the input power source. Then, the switch turns off, and the inductor discharges into the output through the diode. The output capacitor is sized large enough such that the outgoing (diode) current is filtered through the charging and discharging of the capacitor, and DC is achieved at the load. Note that the output voltage and current are negative.

The input–output voltage relationship can be derived by performing voltage balance on the inductor (Equation 2.10). Let the active switch be toggled on and off at a constant frequency, and be on for a fraction \( D \) of the switching period. \( D \) is called the duty ratio or duty cycle, and is often expressed as a percentage. Applying this to Equation 2.10 yields Equation 2.11. The equation can then be rearranged to obtain the input–output relationship, shown in Equation 2.12.

\[
DV_{\text{in}} + (1 - D)V_{\text{out}} = 0 \quad (2.11)
\]

\[
\frac{V_{\text{out}}}{V_{\text{in}}} = \frac{-D}{1 - D} \quad (2.12)
\]

In an ideal power converter, there is no power loss, so the input and output powers must be equal: \( P_{\text{out}}/P_{\text{in}} = 1 \). The input–output current relationship is therefore just the inverse of Equation 2.12. Alternatively, the same result can be derived by performing charge balance on the capacitors (Equation 2.9), although this will require solving for the inductor current first. The more roundabout derivation is omitted, and just the solution is presented in Equation 2.13.

\[
\frac{I_{\text{out}}}{I_{\text{in}}} = \frac{- (1 - D)}{D} \quad (2.13)
\]

The output current and average inductor current are related by Equation 2.14 as can be easily reasoned by examining the circuit schematic. Rearranging gives an expression for inductor current in terms of output current, as shown in Equation 2.15. Knowledge of the inductor current will be necessary for proper product selection.

\[
I_{\text{out}} = -(1 - D) \langle I_L \rangle \quad (2.14)
\]

\[
\langle I_L \rangle = \frac{-I_{\text{out}}}{1 - D} \quad (2.15)
\]
The current *ripple* in the inductor can be derived by using Equation 2.8 and making the approximation that the input and output capacitors maintain constant voltages. For a switching frequency $f$, the peak-to-peak current ripple is given by Equation 2.16:

$$\Delta I_{L,pp} = \frac{V_{in}D}{L} = -\frac{V_{out}(1 - D)}{Lf}$$  \hspace{1cm} (2.16)

Observe that if a diode is used, Equation 2.16 holds only if the peak-to-peak ripple is no more than twice the average value. Otherwise, the inductor current will become negative, which is allowable in a synchronous buck-boost converter, but not in the diode case.

The output voltage ripple be found in terms of the inductor or output current. Again, first approximate the capacitors as having constant voltages, so that the inductor current is piecewise linear and the output current purely DC. Note that since the inductor current is linear during a given switching state, the average current in either state is equal to the average over the whole switching period. This means the average current flowing to the output capacitor during the charging state is equal to the average inductor current. (Remember that the load is still drawing current, however.) By applying this to Equation 2.7, the peak-to-peak output voltage ripple is obtained as in Equation 2.17:

$$\Delta V_{out,pp} = \frac{\langle I_L + I_{out}\rangle(1 - D)}{C_{out}f} = \frac{\langle I_L \rangle D(1 - D)}{C_{out}f} = -\frac{I_{out}D}{C_{out}f}$$  \hspace{1cm} (2.17)

Finally, notice that if a diode is used, the buck-boost converter must be operated with a load connected. Otherwise, the output capacitor will have no way to discharge, while current is continually supplied by the inductor. This will lead to voltage runaway, and most likely device failure. On the other hand, this is not a concern in a synchronous buck-boost converter, since the output capacitor will simply discharge back into the inductor ($\langle I_L \rangle = 0$, so inductor current goes negative) through the switch, whereas a diode would have blocked this current.
2.2.3 Practical Considerations

In practice, there are many non-idealities associated with power electronics that can complicate their implementation considerably. Firstly, all active switches need a gate signal to turn them on and off. In the case of field-effect transistors (FETs), the dominant type of switches used in power electronics today, this is a voltage signal relative to the source of the switch. Since an ideal gate signal is either high or low, it should consist of a series of square pulses, the widths of which can be varied by the logic circuitry generating them. This process is called pulse-width modulation (PWM), although such modulated signals are sometimes also referred to as PWM. The problem is that the source of a switch might not be at the “ground” (may or may not be true earth ground) of the logic circuitry generating the PWM. Moreover, when there are multiple switches, it is possible that each will require a gate signal relative to a different ground. Level shifters will thus be necessary for each of these signals.

Furthermore, high-power switches are physically large, and require significant electric charge to charge the gate capacitance. Naturally, it is desirable for the switch transitions to be as fast as possible, but the logic output from, for instance, a microcontroller unit (MCU) generally cannot supply enough current to accomplish this. Hence, a specialized gate driver will be necessary to drive (that is, turn on and off) the switch quickly. Modern gate drivers may be packaged together with level shifters in a single chip. The design of level shifters and gate drivers is not the main focus of this thesis, so they will not be further discussed here. A simple level shifter used in this project will be presented in Section 4.2.2.

As just alluded to, FETs require their gates to be charged before turning on and discharged before turning off. Therefore, they do not have instantaneous switch transitions. During transition periods, neither the switch’s voltage nor current are zero, so power is dissipated in the switch. As this occurs during every switch transition, it is an example of switching loss, which is proportional to switching frequency. This is in contrast with conduction loss, which occurs only when the switch is on and arises from non-zero on-state resistance. Also part of switching loss is the power used to charge and discharge the gate capacitance of the FET. Switching loss is one major reason why it is impractical to increase switching frequency indefinitely.
Another practical consideration is dead-time. In many circuits, having two complementary switches on at the same time could result in short-circuiting the input source to ground, the output to ground, two different voltage sources, etc. and produce catastrophic results. Therefore, a short dead-time is introduced where both complementary switches are off. If an inductor is present, current will forcibly flow through one of the switches via reverse conduction during this time. Reverse conduction is current flow from the source to the drain of the FET, and results in power loss as voltage drop will be present. Dead-time should also be kept short compared to the switching period because this is clearly not a nominal state of the power converter, and could affect performance. The minimum dead-time should account for switch transitioning times, but may be foremost limited by the clocking abilities of the logic controller. This is yet another factor that may limit switching frequency.

Next, parasitic elements will be discussed. Real components are not purely capacitive, inductive, etc. and will exhibit slight, undesirable behaviors of other elements. For example, switches have parasitic capacitances and finite on-state resistances, as mentioned above. Similarly, inductors have non-zero resistances in their coils, and their winding configurations create parasitic capacitances. Ohmic losses and leakages in capacitors are modeled with a single equivalent series resistance (ESR). The leads of the capacitors also have parasitic inductance. In fact, all conductors in the circuit include parasitic elements, making it paramount to have a proper physical layout of the circuit.

The most straightforward effect of parasitic elements is power loss caused by parasitic resistances. In addition to lowering efficiency, this limits the amount of current that can flow through an element due to thermal considerations. Switches, inductors, and conductors must be properly sized to handle the current. For magnetic-core inductors, there is the additional problem of magnetic saturation, where the inductance drops as the magnetic field, which depends on current, increases. Therefore, the current must also be limited to preserve inductive capabilities. Furthermore, there is magnetic-core loss that increases with the amplitude of the AC magnetic field.

For switches and capacitors, there is already a finite voltage that the devices can support, but the ESR imposes an additional AC current rating in capacitors. Moreover, ESR causes voltage jumps (discontinuities) in a capacitor if the current through it is discontinuous. This occurs during switch
transitions in certain converter topologies, including the buck-boost. The ESR voltage jump can be much larger than the nominal voltage ripple, and may present a problem if DC is expected.

The parasitic capacitances and inductances are usually small compared to the components used, but they are difficult to model and become significant at high frequencies. In fact, past their resonance frequencies, capacitors start behaving like inductors, and inductors like capacitors. Resonance frequencies are typically on the order of many megahertz.

These parasitic elements also cause ringing at switch transitions. During transitions, the current through a switch changes rapidly, resulting in large voltages across parasitic inductances. This means that the peak voltage experienced by the switch can be much larger than the expected value, possibly more than twice as much in a poor design. The voltage then oscillates due to the presence of parasitic capacitors, generating loss and electromagnetic interference (EMI). EMI can couple to and corrupt other signals, making it detrimental both the power converter and other electronics.

To mitigate ringing, switch transitions are often intentionally slowed down through the use of gate resistors. The slower transitions mean more switching losses, but they are generally necessary to limit the amount of ringing. Other techniques also exist, such as the use of snubbers or soft-switching. The reader is referred to [35] for more information.

In the preceding discussions, various forms power loss were mentioned, and these are all dissipated in the form of heat. Thermal management may thus be necessary to prevent devices from overheating. In particular, switches and inductors are typically the dominant heat generators. Physically spreading out the hot elements might be beneficial, but this is not always feasible in light of other design considerations. One of the simplest solutions is the use of heat sinks. These are thermally conductive structures that have a large surface area, allowing for fast heat transfer to the ambient air. If heat sinks are not sufficient, then forced-air or water cooling may be necessary, but these methods have significant overheads. As the physical sizes of power electronics shrink, thermal management becomes increasingly challenging.

Lastly, it is of course important to ensure that all device ratings are respected.
2.3 Figures

Figure 2.1: Solar cell equivalent circuit

(a) I–V characteristic

(b) P–V characteristic

Figure 2.2: Electrical characteristics of a typical PV module
Figure 2.3: Distributed power electronics architectures for PV

(a) DC optimizers
(b) Micro-inverters
(c) DPP

Figure 2.4: A buck-boost converter
Chapter 3

Literature Search

Several classes of MPPT algorithms that have been developed in the past were compared in [31]. Virtual parallel, which was used in this project as a comparative standard, was analyzed in [34]. The proposed MPPT algorithm was also previously used in [36], except it relied on central communication and tests were only performed on a single, emulated module.

The work in [37, 38] presented PV power data over long periods of time, and compared the trade-offs of tracking speed and accuracy. It was shown that high power capture could be attained even at MPPT frequencies as low as tens of millihertz so long as the steady-state tracking accuracy was high.

Work done on the more conventional DC optimizers includes [3–6]. Additionally, Stauth et al. designed resonant switched-capacitor converters of varying architectures in [20–24], and very high efficiencies were achieved.

Krein et al. performed several analyses on the performance of DPP. Motivations for sub-module-level MPPT and DPP were presented in [1, 12, 19], and different DPP architectures were evaluated in [9, 11, 17, 18].

DPP applied to a non-PV application, namely servers in data centers, was studied in [25–30].

The work done in [7, 8] was similar to that of this thesis, but approximate MPPT methods were used, and the power converters were only tested on a single PV module. Some related, earlier works include [13–15]. Asynchronous DPP for PV applications was also examined in [16, 39], but a different DPP architecture was employed and the converter prototype was not adequately designed to be mounted on the back of a panel.

A simple method for emulating PV modules in the lab was investigated in [40, 41]. These emulated modules were also used in this project for easy and reliable testing.

In addition, this thesis incorporated the windowing technique discussed in [42–45] to increase the resolution of current sensing.
Chapter 4

Design and Implementation

4.1 Power Converter Design

4.1.1 Problem Statement

The goal of this project was to design power converters to perform submodule-level MPPT on an array of solar panels. The converters were to implement DPP to achieve high efficiency. Our test system consisted of an array of 12 PV modules, each with three sub-modules, and was connected to the power grid through a Sunny Boy 3000HF-US inverter by SMA Solar Technology AG. The inverter provided array-level MPPT, which used a step size of about 4 V and operated at a frequency of about 0.5 Hz.

As an additional goal, it was desired for the converters to run MPPT algorithms asynchronously, that is, without communication. A system having central communication would require extra wiring to every power converter, voltage isolation, as well as other overheads. Alternatively, neighbor-to-neighbor communication could be used, but the propagation times would become unacceptably slow for MPPT in large systems. Thus, it would be beneficial if the power converters could run their MPPT algorithms independently, yet not conflict with each other. This potential conflict comes from the fact that each sub-module (except for the two at the ends of the string) will have two DPP converters interfacing it. The converters may attempt to drive the voltage of the sub-module in different directions if there is no communication.

Finally, this project needed a system for mounting the power electronics on the back of solar panels as well as acquiring data. The setup was meant for long-term use, and therefore had to be designed with safety and weather considerations in mind. Additionally, diagnostic information about
the power electronics and the PV panels should be readable by a personal
computer (PC). The PC could then perform actions such as shutting off a
power converter in case of a failure, or analyzing and displaying data like
power over time.

4.1.2 MPPT Algorithm

To attempt to achieve high efficiency, a true MPPT algorithm (as opposed to
an approximate algorithm) was implemented. The MPPT method is a vari-
ation on P&O. It is still a hill-climbing algorithm, and observations are still
made during system perturbation. However, the criterion for the direction
of perturbation is not the measured power, but the slopes of the P–V curves
of adjacent PV sub-modules. Figure 4.1 will help illustrate the concepts to
be discussed.

Consider when the slope of a P–V curve is positive. Then of course the
voltage should be increased to increase power. Conversely, if the slope is
negative, the voltage is too high and should be decreased. When the slopes
of two adjacent sub-modules have opposite signs, then either bringing their
voltages closer together or making them further apart is sure to increase
system power. For example, if the first PV sub-module has a positive slope
and the second a negative slope, then the voltage of the first should be
increased and the second decreased. In this case, the voltages are brought
closer together. This way of thinking is most similar to how power electronics
operate. Only the voltage ratio is truly controllable; actual voltage values
will depend on the input (and “output,” in bidirectional converters). Hence,
voltages can be either brought together or separated. More concisely, the
voltage difference, $\Delta V$, can be decreased or increased.

The MPPT algorithm implemented in each DPP converter is as follows:
First, measure the voltages and powers of the PV sub-modules. Perturb the
system, then measure again. Determine the signs of the slopes of the P–V
curves using the measured data. Now, let $\Delta V \equiv V_2 - V_1$, and change $\Delta V$
depending on the signs of the slopes: If the slope of the first sub-module is
positive and the second negative, decrease $\Delta V$. If the slope of the first is
negative and the second positive, increase $\Delta V$. Do nothing if the slopes have
the same sign.
The algorithm is also presented in flowchart form in Fig. 4.2.

When the P–V slopes have the same sign, changing $\Delta V$ will cause the power of one sub-module to increase and the other to decrease, leaving the net effect on system power ambiguous. Therefore, no action is taken until the circumstances are changed by the MPPT of adjacent DPP converters or the central inverter. Since no converter will attempt to decrease the power of any PV sub-module, it seems reasonable that this algorithm will not cause any conflicts.

However, it is still possible that the system is altered by other converters between the time measurements are taken and MPPT is performed. In other words, the DPP converter uses outdated measurements that do not reflect the present system. This can be easily remedied by slowing down the MPPT rate, such that there is a long idle time compared to the time required for perturbation, measurement, MPPT execution, and system settling. The probability of an inaccurate measurement can thus be made small, and an occasional incorrect step will not hinder the overall MPPT significantly. Simulations have been performed to verify this MPPT strategy, and the results will be presented and analyzed in Section 5.1. It was desired for the sub-module-level MPPT to be at least an order of magnitude faster than that at the array level, so it was decided that the DPP converters would run their MPPT algorithms at a frequency of 10 Hz. With typical MCU clock frequencies on the order of tens of megahertz, and switching frequencies (which affect settling time) on the order of hundreds of kilohertz, there would be plenty of idle time.

4.1.3 DPP Method

A synchronous buck-boost converter was used to perform DPP. The converter was synchronous so that there could be bidirectional power flow, and the buck-boost topology was selected as it is a relatively simple converter that can both step up and step down voltage. A schematic of how it connects to the PV sub-modules is shown in Fig. 4.3. As can be seen in the figure, the converter topology is essentially the simplest possible; only a minimal number of charge storage devices and switches are used.

However, there are some other complications. Firstly, the MPPT algorithm
requires voltages and powers to be measured, or to the same effect, voltages and currents. Voltage measurements are typically quite straightforward; the measurements are made in parallel and can be performed directly by an analog-to-digital converter (ADC). On the other hand, current must usually be measured by measuring the voltage across a sense resistor inserted into the current path. It is possible to directly measure current without breaking connections by using hall sensors, but these have drawbacks such as cost and accuracy, and are much less common. Disadvantages of current-sense resistors include a small but non-negligible power loss, especially at high currents, as well as necessary access to the current path.

Physical implementation of the power converters requires having a separate circuit board, in this project a printed circuit board (PCB), for every PV panel. Each PCB needs to have three DPP converters (except for the PCB at the top of the PV string, which only needs two) as well as its own set of logic circuitry. Since there is no communication, the logic circuitry will only have information about the currents measured on its own board. As such, each PCB will have to make one string-current measurement using a sense resistor.

However, for other currents, it is possible to perform “lossless” current sensing by taking advantage of the parasitic series resistance in the inductors. This technique was used in [46,47]. The method is not truly lossless, but since the inductors are already part of the design, no additional loss is incurred through current sensing. Unfortunately, the series resistance is not physically accessible, so the voltage across the inductor terminals must be measured. As the average voltage across an ideal inductor is zero at periodic steady state (Equation 2.10), any DC voltage at the inductor terminals must be due to the series resistance. Averaging the voltage across the inductor will thus produce a value proportional to the average inductor current. This averaging can be accomplished with simple RC filters, as depicted in Fig. 4.4. One drawback to this technique is that the series resistance of an inductor is imprecise and may not be well matched to those of other inductors. However, recall that the MPPT algorithm only uses the changes in powers to determine the next action. Therefore, it is not necessary to obtain accurate measurements of the exact current value; only the way the value changes is important.

There is one more high-level problem related to the current sensing. Even with the string current and all the inductor currents, there is not enough
information to determine the currents through all the sub-modules. This is because some DPP converters will interface sub-modules on two different panels, with a differential wire connecting to the adjacent panel. The PCB with the DPP converter will not have information about the other panel, and the adjacent PCB will not have information about the current through the differential wire. Thus, two additional current measurements are needed on each PCB (except for those at the ends of the string, which only need one): one for each neighbor. Since the DPP converters usually process a small amount of power compared to the full system power, the currents through the differential wires will likely be much smaller than the string current. Therefore, the additional current measurements should be sensed through differential wires to reduce power loss. A block diagram of the architecture with all the necessary current sensing is illustrated in Fig. 4.5.

Observe that this architecture requires an additional differential wire, for a total of two, to be connected between adjacent panels. This is an added complexity, but in return, it enables true MPPT as well as the possibility of two-way neighbor-to-neighbor communication of diagnostics. The two-way communication can reduce message propagation times in large systems, and may be useful to, for example, quickly shut off a power converter. Keep in mind that this is only for the communication of diagnostic information, and that the MPPT can operate asynchronously. Table 4.1 summarizes the overheads and capabilities of different distributed DC-DC power electronics architectures.

4.2 Power Converter Implementation

An annotated photograph of the PCB is shown in Fig. 4.6. The main sections of the circuit will now be discussed in turn. A complete bill of materials for the PCB is provided in Appendix A.

4.2.1 Power Stage

The PV modules used in our system were by Mage Solar, and had a nominal power output of 245 W, an open-circuit voltage of 37.46 V, and a short-circuit current of 8.57 A. Complete specifications are provided in Table 4.2. However,
before sizing components, it was necessary to determine the worst-case duty ratios. Extreme duty ratios (near 0 or 1) cause practical problems, so it was decided that the duty ratio would be restricted to a certain range for safety. Moreover, MPP voltages typically do not vary much, so the duty ratios were expected to be around to 50%, corresponding to voltage equalization. Restricting the duty ratio range thus aided debugging as well. In fact, the gate drivers required power at 5 V, which was provided by the sub-modules through linear regulators, so DPP converters would shut off at extreme duty ratios anyway. Assuming identical PV sub-modules, the open-circuit voltage of a sub-module is simply 

\[ V_{oc} = 37.46 \div 3 = 12.49 \text{ V} \]

Then, the ratio of this voltage to 5 V corresponds to the duty ratios given in Equations 4.1 and 4.2:

\[ D_1 = \frac{V_1}{V_2} \left(\frac{1}{1 + V_1/V_2}\right) = \frac{5/(1.1 \times 12.49)}{1 + 5/(1.1 \times 12.49)} = 26.68\% \] (4.1)

\[ D_2 = \frac{V_2}{V_1} \left(\frac{1}{1 + V_2/V_1}\right) = \frac{(1.1 \times 12.49)/5}{1 + (1.1 \times 12.49)/5} = 73.32\% = 1 - D_1 \] (4.2)

This means that a duty ratio outside of this range would certainly cause a DPP converter to shut off, so using such a value would yield no benefits. Note that a 10% safety margin was applied to the open-circuit voltage, as will be done for all PV parameters from now on. For good measure, it was decided that the duty ratios would be restricted between 25% and 75%, corresponding to conversion ratios between 1/3 and 3.

The DPP converters were designed to handle half of the short-circuit current, or \(8.57 \div 2 = 4.29\) A, through their inductors, just as a proof of concept. The SER1360-103KL inductor by Coilcraft was selected as it had a good balance of inductance, current rating, series resistance, and physical size. The inductance was 10.\(\mu\)H ± 10% and it could carry a current of 7.5 A, at which point the inductance drops by 30% of its nominal value. In the worst-case scenario, the minimum switching frequency required to prevent the peak inductor current from exceeding 7.5 A is calculated in Equation 4.3:

\[ f_{min} = \frac{V_L}{L} \frac{D}{\Delta I_{L,pp}} = \frac{1.1 \times 12.49}{0.7 \times 0.9 \times 10 \times 10^{-6}} \times \frac{0.75}{2(7.5 - 1.1 \times 4.29)} = 293 \text{ kHz} \] (4.3)

The input/output capacitances were sized such that the voltage ripples would be at most ±0.5% of the sub-module open-circuit voltage. The com-
putations are shown in Equation 4.4:

\[ C_{\text{min}} = I_C \frac{D}{f_{\text{min}} \Delta V_{C,pp}} = 1.1 \times 4.29 \times \frac{0.75}{293 \times 10^3 \times 12.49/100} = 96.5 \mu F \]  

(4.4)

In the end, a switching frequency of 300 kHz was chosen for good measure. Three 47 \( \mu \)F ± 20% ceramic capacitors from TDK were used in parallel to meet the capacitance requirement. As ceramic capacitors, these had low ESR, and this model also had good capacitance per area.

Gallium nitride (GaN) switches were used for this project. In addition to having several advantages over conventional silicon switches, such as lower on-state resistance, faster switch transitions, and smaller physical size, GaN is a relatively new technology. Successful application of these devices can provide helpful information to the research community. More details about the advantages of GaN can be found in [48].

The current ratings of the switches had to be at least the maximum inductor current (7.5 A), and the necessary voltage ratings were equal to the voltage across two PV sub-modules, the worst case being \(2 \times 1.1 \times 12.49 = 27.5\) V. The EPC2014C GaN FET by EPC was selected as the switch. It was rated for 40 V and 10 A, and was the smallest product that met the voltage and current requirements.

The LM5113TM GaN gate driver by Texas Instruments (TI) was used to drive the switches. This gate driver supported voltages up to 100 V and was able to drive both of the switches in a DPP converter at the same time, with an internal level shifter for the high-side switch. However, the driver still needed to have the same ground as the low-side switch, and thus additional level shifters were required for two of the DPP converters on each PCB. The level shifters will be discussed in more detail in Section 4.2.2.

To ease prototyping, modular design was adopted for this project. If a switch fails while running high power, it is likely that the PCB will be permanently damaged. To avoid having to reassemble another entire PCB in case of such an event, a switching-cell module was developed. The switching cell was a small “daughter board” consisting of two GaN switches, a gate driver, and supporting circuitry such as decoupling capacitors and gate resistors. Daughter boards could be soldered onto the main “mother board,” and replaced as necessary. They can be seen in Fig. 4.6 as the red PCBs. The
compact layout of the switching cell also ensured low parasitic inductances, reducing ringing. Lastly, by keeping the switching cell footprint (how it interfaces the mother board) the same, cells can be shared or redesigned by fellow research group members, and then used with any mother board that supports the footprint. As such, developments in one research project can aid many others.

4.2.2 Logic Circuitry

The logic circuitry consisted of five main parts: level shifters, logic power, current-sense amplifiers, windowing circuitry, and the MCU. There was also circuitry for inter-integrated circuit (I2C) communication, but this was only used for testing purposes. The final intended form of communication is through the differential wires.

Four custom level shifters were used for shifting PWMs to the grounds of the upper two DPP converters. A schematic of the level shifter is depicted in Fig. 4.7. First consider operation while disregarding the resistors ($R_{\text{limit}}$ short and $R_{\text{large}}$ open). The diode charges the capacitor to the higher-voltage ground. Then, when the PWM toggles, the gate signal changes in the same manner, but will have the correct DC offset due to the capacitor. However, the voltage of the high ground may drop, in which case the capacitor will need a discharge path. Therefore, a resistor is placed in parallel with the diode. In addition, to prevent inrush current from damaging the MCU during start-up, a current-limiting resistor $R_{\text{limit}}$ is placed in the current path. However, the circuit operation now changes slightly, and requires reanalysis.

At steady state, no net current flows to the capacitor, so the DC voltage drop across the limiting resistor must be zero, meaning the average voltage at the anode of the diode must equal high ground. When the PWM goes high, the diode is off, and the voltage at the anode will be determined by the resistor divider formed by $R_{\text{large}}$ and $R_{\text{limit}}$. As this voltage is greater than high ground, the anode voltage must drop below the ground when the PWM goes low. Since the diode turns on at this time, it means the gate signal will also be too low. To mitigate this problem, $R_{\text{large}}$ is made much larger than $R_{\text{limit}}$, so that the “AC waveform” at the anode has a small amplitude, and the gate signal is referenced close to the high ground.
Logic power was provided by low-dropout (LDO) linear voltage regulators, or simply LDOs, that tapped into power from the PV module. Analog circuitry such as current-sense amplifiers and operation amplifiers (op amps) required 5 V and 3.3 V power, while only 3.3 V digital power was needed. Two LDOs were used to provide the analog and digital 3.3 V separately. These voltage rails were not shared in order to prevent digital noise from coupling to the analog components. Similarly, the analog and digital grounds were separated for noise immunity, and then connected at a single point to make them an equipotential. The 3.3 V LDOs derived their power from the analog 5 V to reduce the necessary device ratings, and the 5 V LDO was in turn powered by one PV sub-module.

It was also attempted to have a higher-rated, less efficient 5 V LDO be powered by the entire panel and then connected to the 5 V rail through a diode (cathode at the rail). This way, the logic circuitry would still have power even if the voltage of one sub-module becomes too low. On the other hand, the diode is normally off, so the more efficient LDO is used under nominal conditions. Unfortunately, this part of the circuit did not function properly, and future work is necessary for debugging and evaluating new components.

To reduce losses, low values of sense resistors were used, and thus current-sense amplification was necessary. The selected sense resistors had a resistance of 3 mΩ, so even 1 A of current would only result in a 3 mV of voltage drop. This would be very difficult for an ADC to measure accurately. Therefore, the LMP8602 current-sense amplifier by TI was used. These amplifiers amplify the differential voltage (in this case, the sense resistor voltage drop) by a factor of 50, and then generate an output relative to a specified reference. In this project, bidirectional current sensing was necessary, so the reference was set to half of the 3.3 V ADC range. This halving was done internally by the LMP8602, so no precision resistor divider was necessary.

On the topic of resistor dividers, the current-sense amplifiers in this application needed to handle high common-mode voltages up to the voltage of one PV module, since all the logic devices shared the same ground. If resistor dividers were used to step down this voltage, two would be necessary because the voltage of interest was differential. However, slight mismatches in the resistor dividers would cause large skews in the differential voltage, since the common-mode voltage was comparatively much larger. With the
differential voltage on the order of millivolts and the common-mode voltage on the order of tens of volts, the resistor dividers would need precisions on the order of hundredths of a percent for any reasonable measurement. It was thus more feasible to use a current-sense amplifier with a high common-mode voltage rating. The maximum common-mode voltage equaled the open-circuit voltage of the PV module, and factoring in a 10% safety margin yielded \(37.46 \times 1.1 = 41.21\) V. The LMP8602 could handle up to 60 V, well above the minimum requirement.

It was desired to further enhance the resolution of the current measurements. The problem was that the average inductor current may have been a substantial value, but the MPPT algorithm was interested in small changes in this current. Too much amplification would saturate, or exceed the range of, the ADC due to the sizable average value. Therefore, the windowing technique used in [42–45] was employed. This method subtracted out most of the average value and then amplifies the signal, effectively centering the ADC range, or “window,” at the average value while magnifying the resolution.

The actual implementation was simply op amps configured as a voltage subtractors. A schematic is provided in Fig. 4.8 for reference, but it is assumed that the reader already understands how such a circuit works. \(V_{\text{sense}}\) denotes the output of the current sense amplifier. \(R_1\) and \(R_3\) had the same value, as did \(R_f\) and \(R_4\), in order to match the impedances seen by the input voltages. The output of this circuit is then given by Equation 4.5:

\[
V_{\text{out}} = \frac{R_f}{R_1}(V_{\text{sense}} - V_{\text{bias}}) = \frac{R_4}{R_3}(V_{\text{sense}} - V_{\text{bias}}) \quad \text{(4.5)}
\]

The subtrahend voltage, also termed the bias voltage, was generated by averaging a PWM signal with an RC filter. The magnitude of the bias could then be controlled by adjusting the duty ratio. Window adjustment was performed at a frequency of 100 Hz, an order of magnitude faster than the MPPT. The RC filters on the PCB were then sized to have time constants of 1 ms, and the switching frequencies of the bias voltages were selected to be 100 kHz.

It was observed that at unity gain, the digital noise of a 12-bit ADC reading was about 3 peak-to-peak. The windowing gains were then chosen such that 0.1% of the short-circuit current corresponded to 32 in digital, for a good signal-to-noise ratio. However, a differential resistor divider may have been
necessary at the input of the current-sense amplifier to prevent saturation.
The scaling factor would have depended on the value of the sense resistance
and the maximum current desired to be sensed. For brevity, just one sample
calculation is given in Equation 4.6 for the case of 3 mΩ of sense resistance
and no resistor divider:

\[
\text{Gain} = \frac{R_f}{R_4} = \frac{R_4}{R_3} = \frac{32}{8.57/1000} \div \frac{2^{12}}{3.3} \div 50 \div (3 \times 10^{-3}) = 20.1 \quad (4.6)
\]

The MCU used was the TMS320F28030PN, part of the C2000 Piccolo
series by TI. It featured 14 PWM channels, 12-bit ADCs with a total of
16 channels, and a clock frequency of 60 MHz. Comparators and a capture
module were also included, which allowed for neighbor-to-neighbor commu-
nication. Recalling that there were three DPP converters, four voltage mea-
surements, and six current measurements per PCB, the numerous channels
were indeed necessary. The gate signals plus bias voltages required 12 PWM
signals, and at least 10 ADC channels were needed. The selected model was
the least expensive in the series that supported the project requirements.

4.3 System Implementation

In addition to the power electronics themselves, a system needed to be de-
veloped to connect them to the PV array and monitor performance. It was
also preferable for the system to be able to run over long periods of time,
and without the need of human intervention.

Since communication was not ready at the time of system implementation,
central communication was used for gathering diagnostic data. The PCBs
supported the I^2C communication protocol. To talk to the PCBs, BeagleBone
Blacks (BBBs) were used. These were commercially available, miniature,
low-cost Linux computers with various peripherals, including I^2C ports. The
BBBs could connect to a central PC over Ethernet, and thus functioned as
intermediaries between the PC and the PCBs. Python code was run on the
BBBs to send commands to the PCBs over I^2C. Capabilities included turning
on or off MPPT and measuring PV data.

However, the BBBs also needed power. To avoid the addition of more
wires, power over Ethernet (PoE) was used. With an appropriate Ethernet hub, power as well as data can be transferred over a single Ethernet cable. A commercial 24-port Ethernet hub from TP-Link was used to provide PoE. Then, PoE splitters, also from TP-Link, were used to separate the power and data lines, which were then connected to the BBBs.

At the heart of the system, a PC collected measurements from the PCBs as well as two digital multimeters (DMMs) monitoring the voltage and current of the array. As such, information was available at both the sub-module level as well as the array level. The PC could then control when to perform MPPT, save results, plot data, and compare performance. Internet access was not available at the time, but if set up, the PC could be accessed remotely, and an operator would not need to be on-site to run the system. A block diagram of the overall system architecture is portrayed in Fig. 4.9.

A PCB, BBB, and Ethernet splitter were required for each PV module. This could not all fit in the junction box on the back of the solar panel, so additional enclosures were necessary. The containers needed to be weatherproof and safe, while allowing wires to reach the inside. Polycarbonate boxes from Bud Industries, with custom modifications, were used for this project. The boxes measured 171.0 mm × 121.0 mm × 41.66 mm (length × width × height) and included removable, watertight covers secured by screws. Custom openings with waterproof seals were built into the containers to allow wires to pass through. To fit all of the components, two enclosures were used per panel, and were permanently adhered to the lids of the junction boxes. The lids were removable, so the enclosures could be swapped with the original lids as needed.
4.4 Tables

Table 4.1: Comparison of Distributed Architectures

<table>
<thead>
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<th>DC Optimizer</th>
<th>Standard DPP</th>
<th>Proposed</th>
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<tbody>
<tr>
<td>Differential Wires</td>
<td>0</td>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>Power Processed</td>
<td>Full</td>
<td>Differential</td>
<td>Differential</td>
</tr>
<tr>
<td>MPPT</td>
<td>True</td>
<td>Approximate</td>
<td>True</td>
</tr>
<tr>
<td>Communication(^a)</td>
<td>Impossible</td>
<td>One-way</td>
<td>Two-way</td>
</tr>
</tbody>
</table>

\(^a\) Neighbor-to-neighbor

Table 4.2: PV Specifications

<table>
<thead>
<tr>
<th>Model Name</th>
<th>MAGE POWERTEC PLUS 245/6 PL</th>
</tr>
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<tr>
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</tr>
<tr>
<td>Weight</td>
<td>19.0 kg</td>
</tr>
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<td>Polycrystalline</td>
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<tr>
<td>Sub-Modules</td>
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</tr>
<tr>
<td>(V_{OC})</td>
<td>37.46 V</td>
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<tr>
<td>(I_{SC})</td>
<td>8.57 A</td>
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<tr>
<td>(P_{max})</td>
<td>245 W</td>
</tr>
<tr>
<td>(V_{mpp})</td>
<td>30.91 V</td>
</tr>
<tr>
<td>(I_{mpp})</td>
<td>7.93 A</td>
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</table>
4.5 Figures

Figure 4.1: Reasoning behind the MPPT algorithm
Figure 4.2: Flowchart of the MPPT algorithm
Figure 4.3: Synchronous buck-boost converter for DPP

Figure 4.4: Lossless current sensing
Figure 4.5: Proposed DPP architecture; lossy current senses are circled
Figure 4.6: Photo of the PCB; the small, red PCBs are switching cells
Figure 4.7: The custom level shifter

Figure 4.8: Windowing circuit; RC filters are omitted for clarity
Figure 4.9: The measurement system (diagram courtesy of Andrew Stillwell)
Chapter 5

Results

5.1 MPPT Simulations

The MPPT algorithm was simulated on a test system consisting of four PV panels to verify its functionality. The simulated MPPT was technically performed at the module level, but this would be indistinguishable from a four-sub-module simulation with different PV parameters. In the following simulations, PV modules 1–4 have insolation levels (corresponding to short-circuit currents) of 100%, 80%, 60%, and 80%, respectively, but are otherwise identical. The initial operating point of the system was chosen arbitrarily, but is the same in all simulations. Also, the axes (power and time) are in arbitrary units since these are independent of the qualities of interest, namely convergence and tracking accuracy. The average MPPT period is 30 units, although all the DPP converters have slightly different rates.

Recall that a potential problem with asynchronous MPPT is that DPP converters may conflict with each other, in which case MPPT would fail entirely. Another problem is that a DPP converter may use outdated measurements after the system is changed by another DPP converter. This will be dubbed as “interference.”

First, to confirm that the algorithm causes no conflicts between converters, a simulation was performed of an ideal scenario where each DPP converter always has up-to-date system information, corresponding to having central communication. The system power over time is plotted in Fig. 5.1a and powers produced by each of the panels are shown in Fig. 5.1b. There is an initial decrease in system power as power is shifted through the string of PV modules. However, it is clear that the algorithm is performing MPPT, as the system eventually reaches the MPP and remains there.

Next, the algorithm was simulated with 5 units of delay between measure-
ment and MPPT execution. This corresponds to a 1/6 chance of interference, which is very exaggerated. The final frequencies turned out to be 10 Hz for MPPT, 60 MHz for the MCU clock, and 300 kHz for switching. Even taking into account settling time, with four orders of magnitude of difference between frequencies, the chances of interference would be exceedingly slim. Furthermore, the MPPT executions were modeled as instantaneous, resulting in discrete jumps. In contrast, a real system would change slowly and not differ from the measured state as much. Thus, this is a simulation of a worst-case scenario. The results of the simulation are presented in Fig. 5.2. Compared to the ideal case, the system takes slightly longer to converge to the MPP. Otherwise, the results are similar, and the algorithm performs MPPT successfully.

Figure 5.3 shows the system power after running the algorithm until steady state was reached. The tracking efficiency was averaged over the last 10 MPPT iterations, and the proposed MPPT algorithm achieved a theoretical steady-state tracking efficiency of 99.977%.

5.2 Efficiency Measurements

The efficiency of a single DPP converter was measured over a range of currents. The DPP was connected as a buck-boost converter with a constant input voltage on the low side, and an electronic load in constant current mode on the high side. Power meters were connected to measure the power in and out of the buck-boost converter. The input voltage was set to 10.3 V, the nominal MPP voltage of the PV sub-module. The control was set to equalize the input and output voltages. The efficiency test thus represented a situation where the DPP converter interfaces two PV sub-modules operating at their nominal MPP voltages, although the current flow would be different in reality. The efficiency of the power converter was recorded as the load current was increased in increments of about 0.25 A up to about 2.25 A. The theoretical duty cycle was 50%, meaning the theoretical average inductor current was twice the load current. Going higher than 2.25 A would then exceed the current the converter was designed for.

A plot of efficiency versus load current is provided in Fig. 5.4. As expected, the efficiency dropped with load current due to factors such as conduction
losses, increased ringing, and increased temperature. A peak efficiency of 94.0% was achieved at 0.497 A of load current, corresponding to 0.994 A of theoretical average inductor current. It should be mentioned that the efficiency measurements included gate driver power consumption, but not other logic power. However, with three DPP converters running in the nominal situation, this power will only have one third of the effect.

5.3 Laboratory Testing

5.3.1 Emulated PV

To facilitate testing, emulated PV modules were used. When testing on real PV modules, there are many uncertainties in the weather, and it could be difficult just to get a stable measurement. Even if weather conditions are favorable, it is unlikely that the circumstances will match that of a previous test, making it difficult to compare results. Use of an emulated module can produce consistent, repeatable, and customizable test conditions, all performable in the lab without needing to depend on the weather.

A schematic of the emulated PV used in this project is shown in Fig. 5.5. The reasoning is that the series resistance in PV model will not very significant, and will thus be ignored. An external current source will then play the same role as photocurrent generated by the panel. By shading the panel so that the actual photocurrent is zero, the external source can emulate the photocurrent, and it is now entirely controllable. Additionally, since all other panel parameters are the same, the behavior of the emulated panel will hopefully match that of an actual illuminated panel.

5.3.2 Steady-State Performance

A single-panel laboratory test was performed to determine the performance of the proposed converter and MPPT algorithm. Three DC power supplies were used to emulate the short-circuit currents of the sub-modules. A DC electronic load was connected to the panel terminals and simple module-level MPPT was performed. The power output from the panel was also monitored with a power meter. Next, two of the DPP converters on the
PCB were connected to the sub-modules, and the system was tested with the proposed MPPT, virtual parallel, and no DPP. This was repeated for various permutations of short-circuit currents, representing different partial-shading scenarios. The steady-state power outputs of the PV module were recorded for each of these cases, and the results are compiled in Table 5.1.

Upon comparing the data, it can be seen that DPP can offer significant gains over no DPP, especially in heavy partial-shading scenarios. For example, when two sub-modules have 5 A of short-circuit current and the last only has 3 A, the proposed method increased power by 29.7% in the best case and by an average of 28% over the three scenarios. However, in the proposed algorithm, the power fluctuated more than in virtual parallel, so less precise measurements could be taken. Since the powers were already similar, this made it difficult to perform a rigorous comparison. The power under the proposed MPPT would typically oscillate above that of virtual parallel, but the average value showed little to no improvement over virtual parallel. It becomes questionable whether the proposed method can offset its added complexity and cost.

5.3.3 Dynamic Performance

The single-panel test was repeated with changing shading scenarios to observe the dynamic responses of the MPPT algorithms. An electronic load was programmed to perform a simple P&O MPPT at the module level. The MPPT rate was approximately 0.5 Hz and step size was 0.333 V. These parameters matched that of the commercial inverter, except the step size was divided by 12 to suit a single panel rather than the array. At the same time, a power meter was used to sample power data at a rate of about 10 Hz. DPP was turned on at sample zero, and step changes were applied to one of the short-circuit currents at samples 300 and 500. The resulting responses for the proposed MPPT, virtual parallel, and no DPP are plotted in Fig. 5.6.

It can be seen that at steady-state, DPP generated significantly more power than without DPP, as expected. Additionally, aside from the initial start-up, the sub-module MPPT reached steady-state very quickly, confirming that the MPP voltage does not vary much with different shading scenarios. Also observe that with DPP turned off (at sample zero), the power was slightly
less than not having DPP at all. This matches expectations since there are some static losses (such as gate driver power) just by having the converters connected.

Unfortunately, the proposed MPPT algorithm performed noticeably worse than virtual parallel. Since the power waveform was relatively steady, it suggests that the algorithm was tracking, but not the correct point. This may be due to skewed ADC readings or an error in the code. More testing is necessary to determine the cause of this inaccurate tracking.

5.4 Initial Field Test

Testing on a full PV array, along with the added complexities of the mounting communication and data acquisition setup, can present many unforeseen challenges. Therefore, a preliminary field test was performed with simple MPPT and verified power converters. The converter presented in [7, 8] was used, and ran open-loop (50% duty cycle) virtual parallel. The PV array at the test site is pictured in Fig. 5.7. Note that multiple arrays are included in the picture; the system tested only consisted of 12 panels. Figure 5.8 shows the PCB, bypass diodes, BBB, and PoE splitter mounted on the back of a solar panel using the custom enclosures.

Some practical challenges faced included physical challenges of working under the array, safety precautions, installation, wire management, and difficulty establishing Ethernet connections. However, one of the most significant challenges was that the PV modules were always live, with no way of stopping power flow (short of covering the entire array). Obviously, this also made physical access to the PCBs impossible after setup. As such, when failures occurred, there was nothing that could be done until the system was dismantled, at which point the converter was most likely unusable. Failures thus resulted in costly replacements, in turn requiring frequent trips back to the laboratory.

In the tests performed, MPPT was toggled on and off approximately every 10 s to determine the effect of the DPP converters. Some results from the tests of a single PCB (three DPP converters) are presented in Fig. 5.9a and Fig. 5.9b, corresponding to approximately 10% and 25% shading of a single cell, respectively. The sunlight was not very steady that day, so it is hard to decide
whether the power variations were due to MPPT or reduced insolation. Some seemingly stable intervals are circled in Fig. 5.9a and suggest slight power benefits from having the DPP converters on, but more data are required for a solid conclusion. Regrettably, a system-level failure occurred when a full-array test was attempted.

The cause of failure was insufficient voltage isolation. Digital isolators were used for I²C communication, and were sufficiently rated. However, recall that the DPP converters derived logic power from the PV sub-modules. To avoid potential problems due insufficient sub-module voltages, the PCBs were powered by the BBBs, but isolation was overlooked. Therefore, the power provided by PoE became non-isolated from the panels. The PoE hub was unable to provide the voltage isolation necessary for the entire PV array, resulting in a ground fault.

The fault caused several converters, BBBs, PoE splitters, and most of the PoE ports on the hub to fail. The fault also prompted the inverter to forcibly shut down for safety. Hence, even if the components survived, further data acquisition needed to be suspended while steps were taken to determine how to clear the error in the inverter and restart it. Luckily, no permanent damage was done to the array or the inverter, which has been successfully restarted after replacing a fuse. This incident is also a valuable lesson for future PV array tests.
# 5.5 Tables

Table 5.1: Steady-State Power Test

<table>
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<tr>
<th>$I_{SC}$ (A)</th>
<th>No DPP</th>
<th>Virtual Parallel</th>
<th>Proposed MPPT</th>
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<td>1, 1.5, 1</td>
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<td>137 W</td>
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<td>5, 3, 5</td>
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<td>5, 5, 3</td>
<td>97.9 W</td>
<td>126.7 W</td>
<td>127 W</td>
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</table>

* Ordered topmost sub-module to bottommost
Figure 5.1: Ideal simulation; dotted lines show maximum possible powers; colors represent MPPT execution by different DPP converters.
Figure 5.2: Simulation with interference; dotted lines show maximum possible powers; colors represent MPPT execution by different DPP converters, where black denotes interference; symbols show the directions of perturbation (for debugging purposes)
Figure 5.3: MPPT simulation at steady state
Figure 5.4: Buck-boost efficiency versus load current

Figure 5.5: An emulated PV module
Figure 5.6: Dynamic power test; sample rate was about 10 Hz

Figure 5.7: PV array at the test site (photo courtesy of Andrew Stillwell)
Figure 5.8: Mounting enclosure
Figure 5.9: Preliminary array measurements (graphs courtesy of Andrew Stillwell)

(a) 10% shading; intervals of stable insolation are circled

(b) 25% shading
Chapter 6

Conclusion

6.1 Summary

In this thesis, a new MPPT algorithm and DPP architecture were explored. The MPPT algorithm could be run asynchronously without causing conflicts between DPP converters, and chances of interference could be made slim by incorporating sufficient idle time. Furthermore, the algorithm performed true MPPT, at the cost of current sensing and related logic circuitry as well as an additional differential wire between PV modules. However, the extra differential wire could also be used for two-way communication of diagnostics. Simulations showed steady-state tracking efficiencies of 99.977% and greater.

To verify the proposed strategy, a hardware prototype was designed. A single DPP stage achieved a peak efficiency of 94.0%. Preliminary laboratory results also showed significant gains in using DPP compared with no submodule MPPT. However, limited improvement could be demonstrated over the simpler virtual parallel algorithm.

In preparation for field testing, a long-term measurement setup for the PV array was developed. The setup was safe, weatherproof, durable, and also allowed communication with the power electronics mounted on the array. Data could thus be collected to analyze the performance of the MPPT.

6.2 Future Work

There is still plenty of future work that can be done. Firstly, the proposed converter has yet to be tested on the actual PV array. More array data are also necessary to make quantitative statements about the effect of submodule MPPT at the array scale.
Next, demonstration of neighbor-to-neighbor communication would provide more concrete justification for the additional differential wire. The communication method could be simply modulating the switching frequency to represent binary. Currently, implementing the communication would require a PCB revision, but the MCU fully supports it.

Should the PCB be revised, it could also be modified to be physically smaller. In particular, for ease of testing, substantial PCB area was allocated for an additional model of current-sense amplifier as well as potentiometers, which can all be removed in the final design. Ideally, the PCB should be reduced to a size that fits inside the PV junction box, so that no additional enclosures will be necessary for the final implementation. Another minor refinement would be the option of deriving logic power from the whole PV module, as discussed in Section 4.2.2.

Steps can also be taken to simplify the array measurement setup. If a communication protocol other than I²C is used, such as the serial peripheral interface (SPI), it may be possible to talk over Ethernet directly. The BBs and hence PoE splitters would then be unnecessary. To reiterate, central communication was only used for ease of data acquisition and debugging, but a simplified setup could still save significant time.

In addition, the reliability of the proposed architecture can be investigated. The effect on the system due to the failure of a single DPP converter could be shown with simulation as well as real-time measurements.

Lastly, more analysis can be done to examine why the proposed MPPT did not perform as well as expected.

6.3 Concluding Remarks

Solar power is a promising source of clean, renewable energy. Efficient MPPT algorithms and power electronics can help maximize the potential of solar power. Hopefully, developments in power electronics in this field will also be of use for other applications. If anything, this project has been a valuable learning experience that provided insight into both the underlying theory and practical challenges.
## Appendix A

### PCB Bill of Materials

**Table A.1: PCB Bill of Materials**

<table>
<thead>
<tr>
<th>Product Description</th>
<th>Manufacturer</th>
<th>Part Number</th>
<th>Quantity per PCB</th>
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<tbody>
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<td>Phoenix Contact</td>
<td>1755736</td>
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<tr>
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<td>Phoenix Contact</td>
<td>1792249</td>
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<td>Phoenix Contact</td>
<td>1755752</td>
<td>3</td>
</tr>
<tr>
<td>4x1, 200 mil Plug</td>
<td>Phoenix Contact</td>
<td>1792265</td>
<td>3</td>
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<td>6x1, 100 mil Header</td>
<td>TE Connectivity</td>
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<td>TMS320F2830PNT</td>
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References


