INVESTIGATION OF SYSTEM-LEVEL ESD-INDUCED FAILURES

BY

SANDEEP GAUTAM VORA

DISSERTATION

Submitted in partial fulfillment of the requirements
for the degree of Doctor of Philosophy in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2020

Urbana, Illinois

Doctoral Committee:

Professor Elyse Rosenbaum, Chair
Professor Pavan Kumar Hanumolu
Professor José Schutt-Ainé
Assistant Professor Jin Zhou

ABSTRACT

Electrostatic discharge (ESD) is a phenomenon that can adversely impact the operation of systems. ESD is a short duration, high current stress which can cause the permanent failure of a system or temporary glitches in a system. Soft failures include any recoverable system malfunction, from resets to loss of stored data. They can be caused by noise entering signal pins or by supply voltage fluctuations. Soft failures have previously been studied by using test structures to identify failure mechanisms or actual products to identify the types of soft failures that occur. These models are either simplified or offer little to no insight into the cause of the soft failures. The first part of this dissertation addresses soft failures within a fully functional semi-custom microcontroller. This allows for both an understanding into the exact causes of soft failures as well as testing for effects of soft failures from ESD on operating software.

The second part of this work focuses on latch-up in reverse body biased core circuitry. Latch-up is a phenomenon where parasitic devices within a CMOS structure turn on and stay on, shunting current from power to ground, often causing permanent failure. Latch-up has often been looked at from a substrate current injection point of view, however, measurement of a reverse body biased chip, shows that latch-up can occur due to supply bounce. An analytic model and SPICE simulation verify the phenomenon, and with the help of simulation, methods of increasing robustness are discussed.

ACKNOWLEDGMENTS

I would like to thank my advisor, Professor Elyse Rosenbaum, without whom I would not be at this point in my life today. Through her mentorship, I have become a better researcher and writer.

A special thanks goes out to both past and present colleagues, Chloe Reiman, Nick Thomson, Yang Xiu, Zaichen Chen, Jie Xiong, Alec Wasowicz, Milan Shah, Alex Ayling, Rui Jiang and Prajwal Mysore Vijayaraj. Their technical knowledge, insight, and friendship have enabled me to perform my best during these last few years.

I would like to thank Michi Stockinger of NXP for providing technical guidance for the work presented in Chapter 5.

Finally, I would like to thank my family who pushed me towards pursuing a Ph.D. and have supported me throughout this journey.

TABLE OF CONTENTS

LIST OF ABBREVIATIONS

ADC	Analog to Digital Converter
ALU	Arithmetic Logic Unit
APD	Anti-Parallel Diode
BER	Bit Error Rate
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide-Semiconductor
DB	Down-Bond
DECAP	Decoupling Capacitor
DFT	Design for Test
DMEM	Data Memory
ESD	Electrostatic Discharge
EM	Electromagnetic
EUT	Equipment Under Test
FDTD	Finite Difference Time Domain
ggNMOS	grounded-gate N-type Metal-Oxide Semiconductor Transistor
GPR	General Purpose Register
HBM	Human Body Model
HCP	Horizontal Coupling Plane
IC	Integrated Circuit
IEC	International Electrotechnical Commission

IO	Input/Output
IR	Infrared
LDO	Low-Dropout
MCU	Microcontroller Unit
MOSCAP	Metal-Oxide-Semiconductor Capacitor
MUX	Multiplexer
NMI	Non-Maskable Interrupt
NMOSFET	N-type Metal-Oxide-Semiconductor Field-Effect Transistor
ORID	Out of Range Input Detector
OV	Over-Voltage
PCB	Printed Circuit Board
PDK	Process Design Kit
PDN	Power Delivery Network
PESD	Power-on Electrostatic Discharge
PMC	Power Management Controller
PMEM	Program Memory
PMOSFET	P-type Metal-Oxide-Semiconductor Field-Effect Transistor
RBB	Reverse Body Bias
SFR	Special Function Register
SRAM	Static Random Access Memory
TRX	Tristate Buffer
TVS	Transient Voltage Supressor
UART	Universal Asynchronous Receive Transmit
UV	Under-Voltage
VCP	Vertical Coupling Plane
VFTLP	Very-Fast Transmission Line Pulse

CHAPTER 1

INTRODUCTION

Semiconductor devices may be subjected to electrostatic discharge (ESD) throughout their life cycle (manufacture, handling, packaging, and use). These ESD events occur when the charge on an object, built up through triboelectric charging, is shared with another object [1]. This brief stress can result in ones to tens of amps of current and can last hundreds of nanoseconds. If a semiconductor device is subjected to these stresses, it may be permanently damaged due to heating or high electric-fields.

In order to mitigate the potential damage from these events, several committees have released design guidelines and test procedures to qualify an integrated circuit (IC) or an electrical system against ESD. Each of these standards cover various scenarios that may occur throughout a product's life. Two types of failures can result from inadequate ESD design: hard failure and soft failure. Hard failure refers to the permanent damage of an IC. Soft failure refers to the temporary, incorrect, operation of a system.

Typically, hard failures result from large amplitude stresses impinging directly on an IC pin. Often times, these hard failures occur directly on the discharge path. For this reason, hard failures have traditionally been studied at the component level. Testing can be performed by directly probing unpackaged wafers and injecting ESD current or by injecting current into the leads of a packaged part. When doing component level ESD testing, the device is typically powered off. Standards such as the Human-Body Model

(HBM) [2], and the Charged-Device Model (CDM) [3] specify how to characterize the hard failure of components resulting from ESD. However, hard failure may also occur from the turn-on of parasitic devices. This mode of failure, i.e., latch-up, occurs when the device is powered on. This necessitates testing via a power-on standard like the International Electrotechnical Commission (IEC) 61000-4-2 test [4].

The IEC 61000-4-2 test is a system-level test standard. Here, the system refers to one or more packaged ICs, a PCB, and any other components necessary for the operation of the main IC. Because the tested system should be operational, testing is performed with the system powered-on which allows testing for soft failures in addition to latch-up. Example of soft failures include loss of data in latches or RAM, corrupted input values, and crashes.

Many modify this test procedure to perform pseudo-component level testing. Here, a test board with the bare minimum of extra components needed to operate the IC being tested is used. This test board includes, direct, often unrealistic, traces to the IC's pins to allow for the injection of ESD current into a pin of the IC. This allows for the IC to be on and operational, while targeting only it with ESD instead of the entire system.

In order to pass the IEC test, in most cases, dedicated ESD protection devices must be added to a system. These protection devices are placed within an IC, on a printed circuit-board (PCB), or both. Deciding where and which type of ESD protection device(s) to use can often be difficult. ESD devices need to be large enough to handle the current levels seen during ESD events while also keeping the voltage levels within specification. Due to the nature of the ESD stress, these devices tend to be large. If placed on a chip, they eat up large amounts of chip area. On the other hand, if these protection devices are placed on the board, they often take up large amounts

of board area. In addition, regardless of which method is used, these devices often decrease the performance of what they are protecting. This leads to difficult decisions when trying to minimize cost and area while maximizing performance and still trying to meet specifications. Therefore, understanding how to best design against ESD induced failures is important to optimizing a design.

This work seeks to understand failures that occur when a device is powered on. Two main topics are studied: soft failures in a microcontroller and latch-up within a core with reverse body bias (RBB) capabilities.

Soft failures have become more and more important as technology has advanced, leading to more complicated chips and smaller supply voltages. Add to that, the increased use of electronics in our daily lives to mission critical applications like autonomous vehicles, and the need to minimize soft failure occurrence becomes clear. Soft failures in ICs with computational capabilities can be monitored through software by running program suites that test the functionality of the IC; this approach works in all but the most severe of cases, i.e., those in which system resets or hangs occur. This study looks to systematically and pro-actively address soft failures as opposed to the more common "trial and error" method used.

Latch-up can result in the permanent failure of a customer's system, and at that point, the only recourse is to replace, at the very least, the damaged IC. If this failure occurs often in a product, customers will switch to competing products, subsequently resulting in a loss of revenue. Therefore, it is important to ensure these events do not occur. The latch-up studied in this work was first observed in a commercial microcontroller. Simulation is used to analyze the latch-up as well as model potential fixes.

Chapter 2 provides a detailed explanation of the system-level ESD (or

powered ESD — PESD) test procedure which is used as a basis for testing throughout the dissertation. Chapter 3 provides the details of the test vehicle used to understand soft failures. In order to ensure reasonable complexity and applicability to real world products, a fully functional 32-bit microcontroller was fabricated. Chapter 4 provides a more complete picture of soft failures within an IC through a combination of hardware and software detection. Chapter 5 details experimental observations of latch-up and provides an analytical model to explain said observations. Measurement shows that latch-up can occur from supply fluctuations. Simulation is used to validate the analysis and expand upon the measurement data. Via simulation, evaluation of potential mitigation strategies can be performed.

CHAPTER 2

SYSTEM LEVEL ESD TESTING

Chapter 1 explained the use of system-level testing for ESD failure analysis. As mentioned, latch-up requires the device to be powered-on and can culminate in hard failure. Soft failures are interruptions in the normal operation of a system and likewise require the device to be powered-on. While there have been several standards developed for system-level ESD testing, one of the more wide spread ones is the IEC 61000-4-2 test standard. This work will use this standard as a basis for all tests performed.

2.1 IEC 61000-4-2 Test Setup

The IEC 61000-4-2 test setup is shown in Figure 2.1. The test setup includes a horizontal coupling plane (HCP) placed on a non-conducting table above a ground plane. The HCP is connected to the ground plane via two 470 kΩ resistors in series. These resistors provide a bleed path for the charge stored on the HCP after the ESD event. An insulating sheet is placed on the HCP upon which the equipment under test (EUT) is placed. There is no requirement for the height of the EUT above the HCP, other than emulating a real-life scenario [4].

The EUT can be tested in two configurations. The mobile configuration electrically isolates the EUT from any other large conducting object, but places two bleed resistors of 470 kΩ in series between the EUT and the HCP.

In a tethered configuration, the EUT is connected to earth ground, or some large conducting shape through a relatively low impedance path.

Placing the EUT on an insulating sheet ensures that no shorts exist between it and other conducting objects (the HCP). An EUT should be tested in all of its standard use cases. This mean, that should an EUT be battery operated, it should be tested in a mobile configuration. Likewise, if it can be used while plugged in to the wall, tests should be performed while it is tethered. A mobile setup removes slow transients from the discharge current waveform. The difference in the ESD discharge waveform between mobile and tethered scenarios is explained in more detail in [5].

Figure 2.2 shows a lumped schematic of the ESD gun's internals. The gun is discharged into the EUT after first being charged using a separate high voltage (HV) generator. During charging, the discrete capacitor, C_{slow}, and a parasitic capacitor formed between the gun and surround objects, C_{fast}, will be charged. Discharge is initiated by actuating an internal relay which connects the tip of the gun to the charged components inside. The inductance at the tip of the gun shapes the current pulse and ensures it meets specifications. The ground strap, represented as an inductor, is a long metal line that connects the gun to earth ground.

Several different testing methods are specified in [4]. Contact discharges are performed by placing the tip of the gun in contact with the EUT before actuation of the gun. This is the most severe testing method as all the current from the gun directly enters the EUT. The second test method is an air discharge. Here, the ESD gun is actuated before the gun tip is in contact with the EUT. The gun is then brought toward the EUT until a discharge occurs. Discharges often occur before contact with the EUT is made as the air ionizes [6]. The third type of test is an indirect discharge. In this test, the

ESD gun is discharged onto either the HCP or the vertical coupling plane (VCP, not shown in Figure 2.1). The VCP is an isolated conductor mounted vertically and placed near the HCP.

Since contact discharges tend to be the the harshest form of stress and better controlled than air discharges [6], in this work, they are the primary test event used. Contact discharges also give the opportunity to inject current directly into IC pins. Precharge levels were increased until failures were observed.

The ESD waveform is specified using a 2 Ω target. These specifications can be seen in Table 2.1. The waveform's parameters (I_p, t_r, I_{30}, and I_{60}) are marked in Figure 2.3 along with its overall shape. Note that at time zero, the waveform has reached 10% of its peak value. General rules of thumb are as follows:

First Peak Rise Time:

$$t(I = 90\%I_{peak}) - t(I = 10\%I_{peak}) = t_r = 800ps$$

First Peak Maximum:

$$\frac{I_P}{V_{pre}} = 3.75\frac{A}{kV}$$

Current at 30 ns:

$$\frac{I_{30}}{V_{pre}} = 2(\frac{A}{kV})$$

Current at 60 ns:

$$\frac{I_{60}}{V_{pre}} = 1(\frac{A}{kV})$$

2.2 Figures and Table

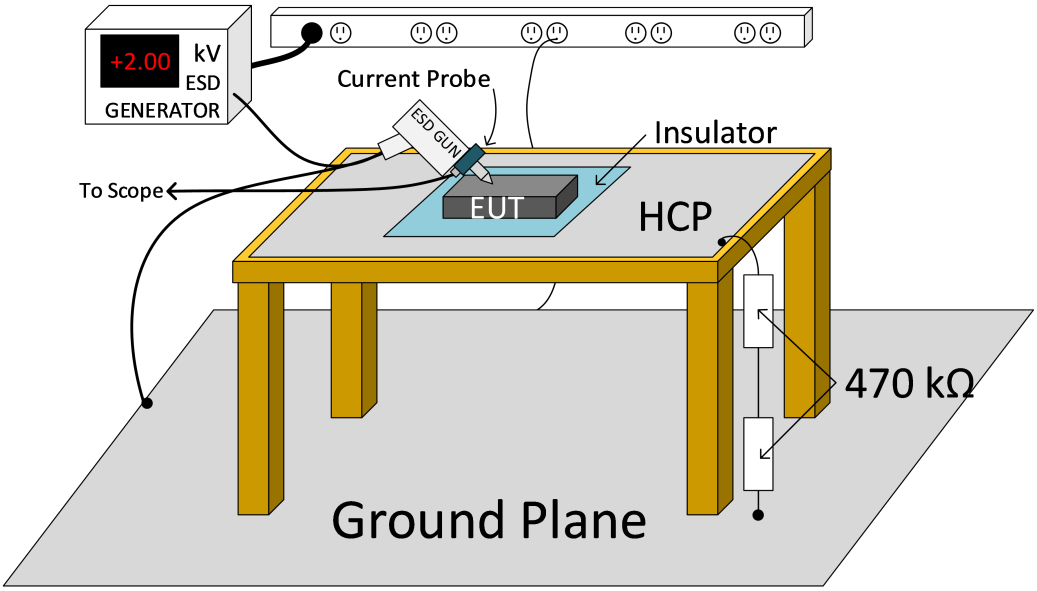


Figure 2.1: Test setup for the IEC 61000-4-2 test standard [4]. The HCP is elevated above the ground plane, connected only via two 470 kΩ resistors in series. On the HCP an insulating sheet is placed, upon which, the EUT is placed. An ESD gun is used to generate the ESD event and is tied to the ground plane via a thick metal line. Figure courtesy of N. Thomson.

Table 2.1: IEC ESD waveform parameters for contact discharge into a 2 Ω target.

Level	**Precharge Voltage** V_{pre} (kV)	**First Peak Current** I_P (A), ±15%	**Rise time** t_r (ns) ±25%	**Current at 30 ns** I_{30} (A) ±30%	**Current at 60 ns** I_{60} (A) ±30%
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

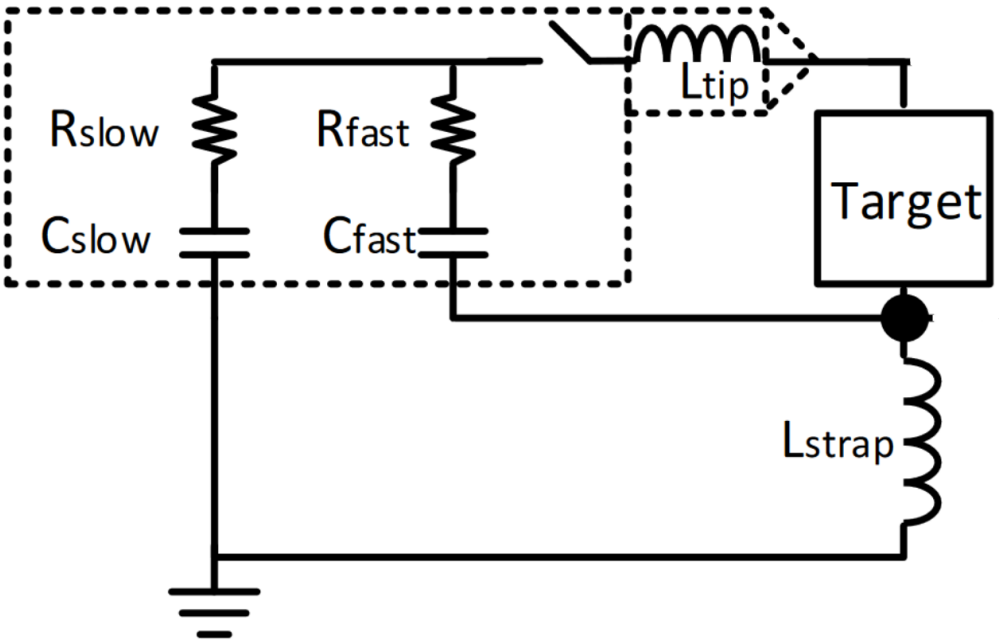


Figure 2.2: Lumped model of the ESD gun. Figure courtesy of [7].

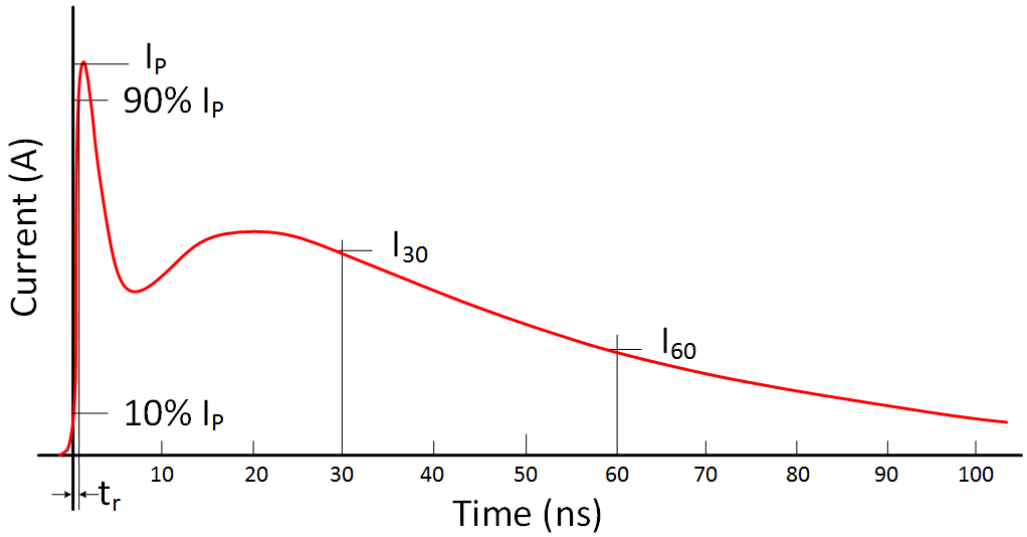


Figure 2.3: Sample waveform of current discharge from the ESD gun into a 2 Ω target. Figure courtesy of N. Thomson.

CHAPTER 3

TEST SYSTEM FOR SOFT FAILURE ANALYSIS

In order to understand how soft failures manifest in a large system during system-level ESD, a representative system must be acquired. While it is possible to purchase an off-the-shelf consumer device and subject it to ESD stresses, very little insight can be gleaned by using such devices. Oftentimes, these systems are black boxes [8]. Without detailed knowledge of the inner workings of these systems, identifying the source of soft failures often proves a difficult and sometimes fruitless endeavor. Additionally, many of these systems are exceedingly complicated, e.g., cell phones, laptops, etc. As complexity of a device increases, the likelihood of concurrent soft failures increases, making it increasingly difficult to isolate cause and effect. Unfortunately, in order to run software and understand how it is affected by ESD, a certain degree of complexity is required.

Current state-of-the-art literature has looked at test structures and simplified testchips [9], [10], [11] or at board level noise coupling [12], [13], [14]. In order to minimize complexity, yet fulfill the goal of this work, a semi-custom microcontroller was fabricated in a 130-nm CMOS technology [15], [16]. Additionally, in order to operate the chip, a printed circuit board was fabricated. The EUT used for investigations includes a chip, a printed circuit-board, and all the components necessary to operate the chip.

3.1 OpenMSP430 Test Chip Overview

The layout of the test chip is shown in Figure 3.1. There is 3.3 V supplied to the input/output (IO) circuitry (VDDIO), while the core circuitry is connected to a 1.2 V supply (VDD). This 40 pin chip includes a microcontroller core, stand-alone test structures and banks of supply voltage monitoring circuits.

3.1.1 Synthesis and Core Design

The chip's core was designed using the OpenMSP430 [17], an open-source microcontroller core that runs the same instruction set architecture as Texas Instruments' MSP430 microcontroller. A block diagram of the OpenMSP430 is shown in Figure 3.2 and includes the following.

- **Frontend**: This contains the execution state machine and performs the fetch and decode operations.
- **Execution unit**: This unit executes the decoded instruction and include the arithmetic logic unit (ALU) and register file.
- **Serial debug interface**: This unit contains all of the required logic to communicate with the host device. It uses a standard two-wire signal interface following the universal asynchronous receive transmit (UART) protocol. Initialization of a program can be performed through this interface.
- **Memory backbone**: This unit facilitates communication between the frontend, execution unit, serial debug interface, data memory (DMEM) and program memory (PMEM).

- **Basic clock module**: This generates the main clock (MCLK) and manages the lower power modes.
- **Special function registers (SFRs)**: These configuration registers store information for special core functions such as the non-maskable interrupt (NMI), watch-dog timer, etc.
- **Program memory (PMEM)**: A configurable memory space from 1 kB to 59 kB for the designer's needs. This chip sports a 4 kB sized PMEM.
- **Data memory (DMEM)**: A configurable memory space from 128 B to 32 kB. This chip includes 1 kB.
- **Peripheral memory**: This memory is used to support the functions of various peripheral components. One kilobyte was used in this chip.

All components of the core were synthesized using Synopsis Design Compiler using ARM standard cells. During synthesis, a scan chain was inserted using the design for test (DFT) compiler integrated with Design Compiler. The scan chain, shown in Figure 3.3, allows better insight into what is happening in the core. When the scan chain is enabled on the core, the data stored in the core registers can be directly read out. The scan chain provides an additional benefit; it allows programming of the core registers while the system is off-line. The ability to read data into the scan chain gives knowledge of the register states before a zap is applied to the system. Bit flips can be monitored by reading out the data after the ESD zap and comparing the result with the known input.

The core was placed and routed using Cadence Encounter and designed for a main clock frequency of 100 MHz.

3.1.2 Noise Monitors

Supply noise is monitored because that noise is a potential cause of soft failures. Supply noise can cause glitches at IO pins [7] and may upset stored data by exceeding the storage element's noise margins. Figure 3.4 shows the on-chip portion of the ESD current path. The current returns to the circuit board primarily via the VDDIO and VSSIO pins. Due to the package inductance, this causes noise on the IO supply. Bounce on the IO ground is transmitted to the core supply domain through the anti-parallel diodes (APD).

Two types of supply voltage monitors [11] are included on this test chip. The over-voltage (OV) monitor measures the peak positive excursion on a supply rail and the under-voltage (UV) monitor measures the peak negative excursion. Those monitors store the measured voltage for a time interval that exceeds the duration of an ESD event. The stored value is sampled by a 2 bit asynchronous analog to digital converter (ADC) and saved in latches for later readout; a larger output code indicates a larger voltage excursion. A supply voltage monitor connected to the IO supply is denoted as HV and a monitor circuit for the core supply is denoted as LV. Four supply voltage monitors — HVOV, HVUV, LVOV and LVUV — were placed in each of two monitor banks (MB0 and MB1), which were then put roughly on opposite sides of the chip (Figure 3.1). The over-voltage monitors have only three output states while the under-voltage monitors have four output states.

Standalone versions of the supply voltage monitors were placed on the chip for calibration purposes. The supply voltage monitor test circuits are calibrated using a very-fast transmission line pulse (VFTLP) testing setup. The current pulses have a 200 ps rise-time and a 2 ns pulse width. A bias-tee

is used to inject the pulse onto the powered-up supply bus, and the supply bus voltage waveform is recorded.

On the basis of those measurements, Table 3.1 is constructed to provide the mapping from a monitor circuit's output code to the peak amplitude of the supply noise. However, if the supply disturbance is of much shorter duration than the pulse used in this experiment, then a larger disturbance than indicated in the table is needed to achieve a given output due to the limited bandwidth of the voltage monitors. Voltage monitor readings simulated across different pulse widths can be found in [18].

A second type of monitor circuit called an out of range input detector (ORID) [19] was placed on chip. ORIDs were placed on two pins within the circuit, GPIO 4 and I2C_IO. An ORID detects if a signal pin experiences a voltage excursion above the chip's V_{DDIO} or below the chip's V_{SSIO}. Such a voltage excursion can occur due to board-level noise on a signal trace, or due to common-mode noise on the on-chip supply, which shifts the input circuit's logic threshold relative to board ground. The monitor circuits' outputs can be transmitted through a GPIO pin for read-out by the external computer. Due to pin number constraints only half of each monitor circuit was wired for read-out. The input high read-out was monitored in the I2C_IO cell while the input low read-out was monitored in the GPIO 4 cell.

3.1.3 I/O Design

All signal IOs were designed using the same protection scheme. Each IO includes primary and secondary ESD protection. Primary protection is created using dual diodes while secondary protection uses a series resistor along with a grounded gate NMOS (ggNMOS). Each IO was designed to

handle 8 kV HBM stresses.

There are three IO pins for each supply — V_{DDIO}, V_{SSIO}, V_{DD}, and V_{SS}. Each VDD[IO] IO cell contains a one stage active rail clamp designed for power-on ESD [20]. The VDDIO rail clamps use a pass transistor of 5.5 mm while the VDD rail clamps' pass transistors is 2 mm. Each VSSIO cell contains APD, where each diode has a perimeter of approximately 500 μm.

Signal IOs each include a Schmitt trigger for glitch rejection. The noise monitor reset signal includes a 10 ns RC filter on chip to minimize the potential for noise monitor data loss during testing. The function of each IO is shown in Table 3.2. All signal IOs included a tristate buffer (TRX), however, if an IO did not need the full functionality, the TRX control signal was tied to the appropriate power or ground rail.

3.2 Package

The test chip is packaged in a 5 mm by 5 mm, 40 pin QFN package. Bond-wires connect the test chip to the package. Two separate assemblies of the parts were tested. In the first, all chip pins were connected to package pins. In the second assembly, the chip ground pins were down-bonded ("db").

Down-bonding is a method of reducing the bond-wire inductance on the ground nets. Figure 3.5 shows that instead of a bond-wire connecting a chip bond-pad to a package lead, the bond-wire may connect the chip bond-pad to the die pad of the package. The package die pad will be strongly tied to the board ground.

In this work, the chips with down-bonds have all three VSSIO pins and all three VSS pins down-bonded. Measurement results are for parts without down-bonds unless otherwise indicated.

3.3 Board Design

The test system is a four-layer FR-4 circuit board, shown in Figure 3.6. The test system was set up to be powered only by a DC power supply. Independent low-dropout (LDO) regulators were used to supply each of the power domains: IO (3.3 V) and core (1.2 V). Adequate decoupling capacitance was placed on-board following best practices. Each chip supply pin has a set of three decoupling capacitors — 100 pF (0402 packaging), 10 nF (0603 packaging), and 1 μF (0603 packaging) — placed as near to the test chip as possible. Additional 10 μF tank capacitors were placed at the voltage regulators' outputs.

Since the chip contains IOs intended for ESD testing, the board includes traces out to the edge. This is where the tip of the ESD gun is placed for a contact discharge to a signal line. Some on-board pulse shaping of the incident noise due to the length of the traces is expected. Likewise, board-level coupling to signal traces does occur.

For ease of testing, most control and data signals are routed through USB connectors (not using the USB protocol) to an external computer. All DC control signals had 2200 pF capacitors placed on their lines to help mitigate any board level coupled noise. Due to lack of board real-estate and control pins, control signals and data signals that did not need to be supplied simultaneously, e.g., dbg_en, scan_mode, sensor read, etc., were tied to an appropriate default state and were routed through an on-board multiplexer (MUX).

Both clocks are generated on-board by crystal oscillators and are placed as close to the chip as possible to minimize noise coupled to the clock line. In scan mode, for synchronous data readout, a user-defined clock is used as the

main clock instead of the on-board crystal oscillator. Therefore, a mechanical relay is used to switch between the user-defined clock and the crystal. A mechanical relay was used as it is one of the few on-board switches that would not significantly alter the clock signal going into the chip. However, it should be noted that due to the size of the relay (and the fact that it is a leaded part), the crystal oscillators had to be placed further away from the chip than would be seen in a commercial design.

3.4 Figures and Tables

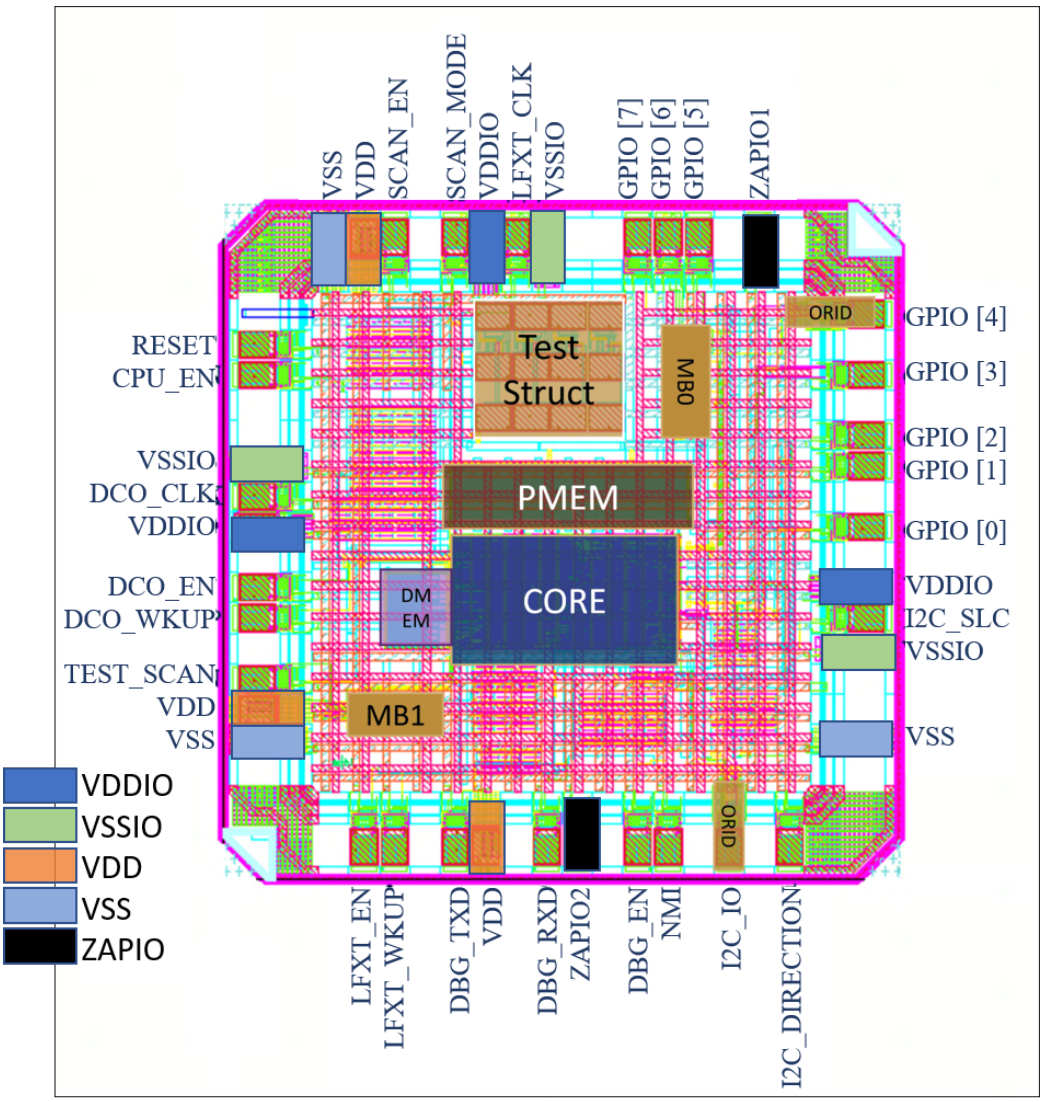


Figure 3.1: Layout of the OpenMSP430 test chip.

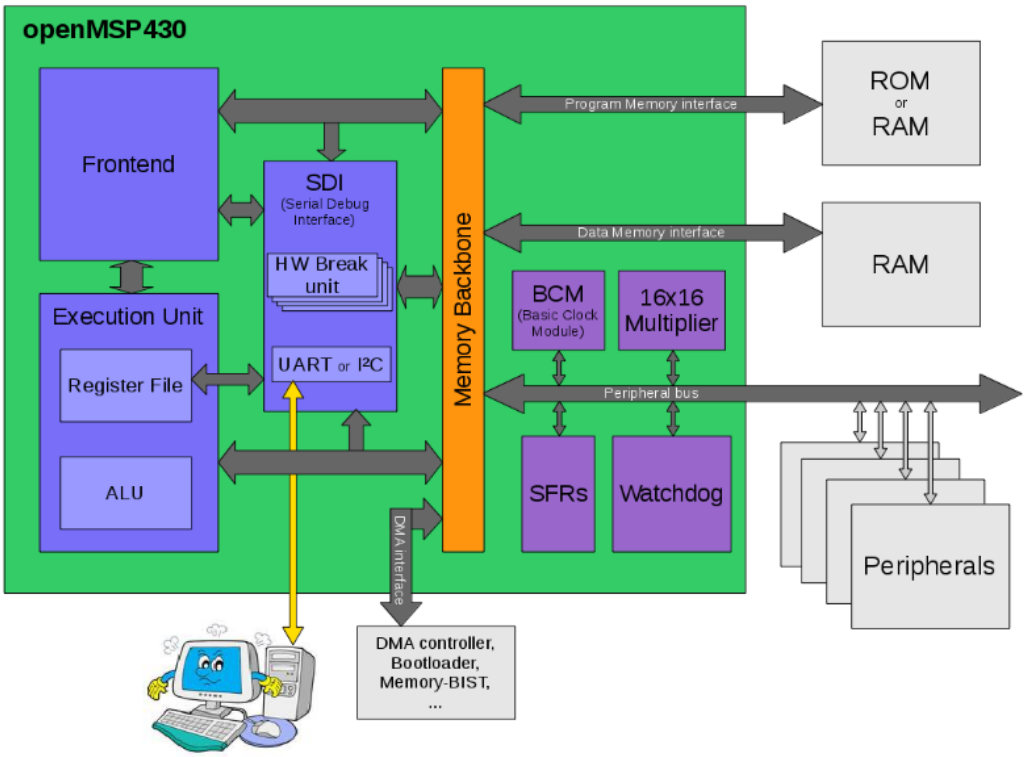


Figure 3.2: Block diagram of the OpenMSP430. Figure from [17].

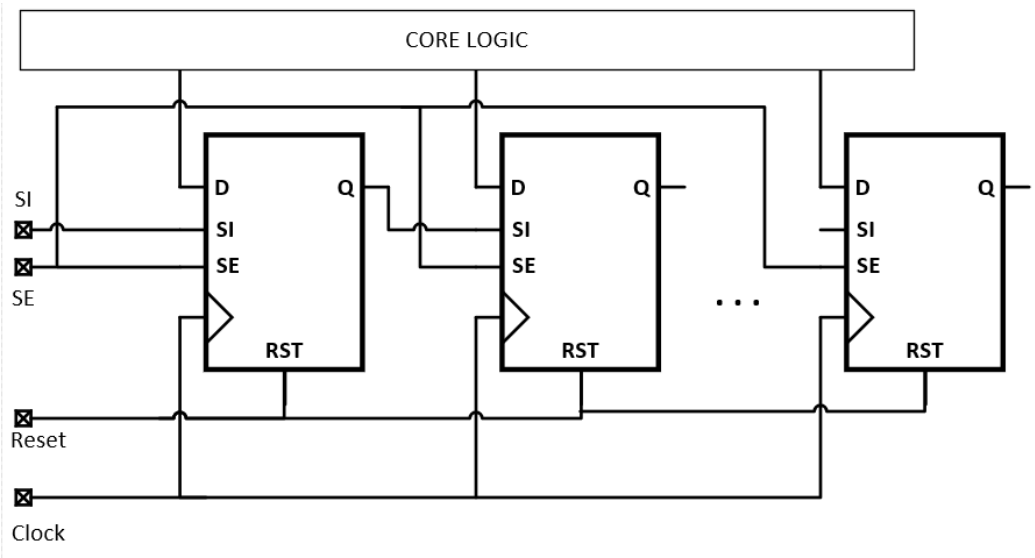


Figure 3.3: Diagram of a scan chain. Here, by toggling the SE signal, the functional core registers will be switched into a single large shift register.

Table 3.1: LV [HV] monitor calibration results. A supply voltage monitor's output code increases as a function of the magnitude of the supply voltage noise. The nominal value of V_{DD} is 1.2 V [3.3 V]. VMIN denotes the lowest value of $V_{DD[IO]}$ (under-voltage) and VMAX denotes the highest values of $V_{DD[IO]}$ (over-voltage). Calibration is performed using a 2 ns VFTLP.

LVUV VMIN (V)	Output Code	HVUV VMIN (V)
0.87 <VMIN <1.2	00 (0)	2.64 <VMIN <3.3
0.48 <VMIN <0.87	01 (1)	1.56 <VMIN <2.64
0.12 <VMIN <0.48	10 (2)	0.48 <VMIN <1.56
VMIN <0.12	11 (3)	VMIN <0.48
LVOV VMAX (V)	**Output Code**	**HVOV VMAX (V)**
1.2 <VMAX <1.61	00 (0)	3.3 <VMAX <3.57
1.61 <VMAX <1.72	10 (1)	3.57 <VMAX <4.51
VMAX >1.72	11 (3)	4.51 <VMAX

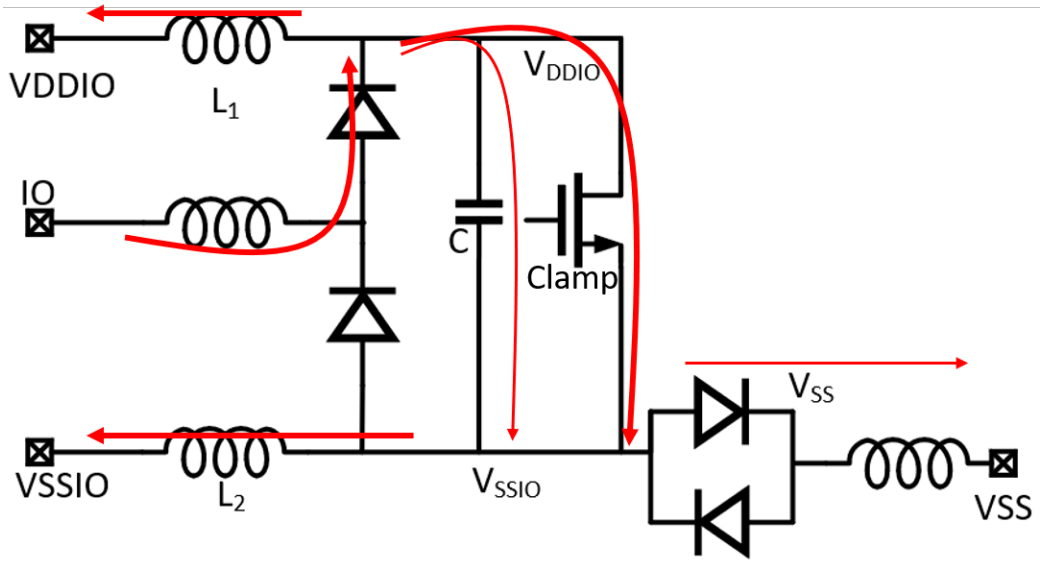


Figure 3.4: ESD current path for a positive discharge to an IO. All diodes shown in the schematic are ESD protection devices. The bond-wires are represented as inductors. The capacitor C represents the on-chip decoupling capacitance. The MOSFET labeled "Clamp" is an ESD protection device that gets turned on by an ESD-detection circuit (not shown).

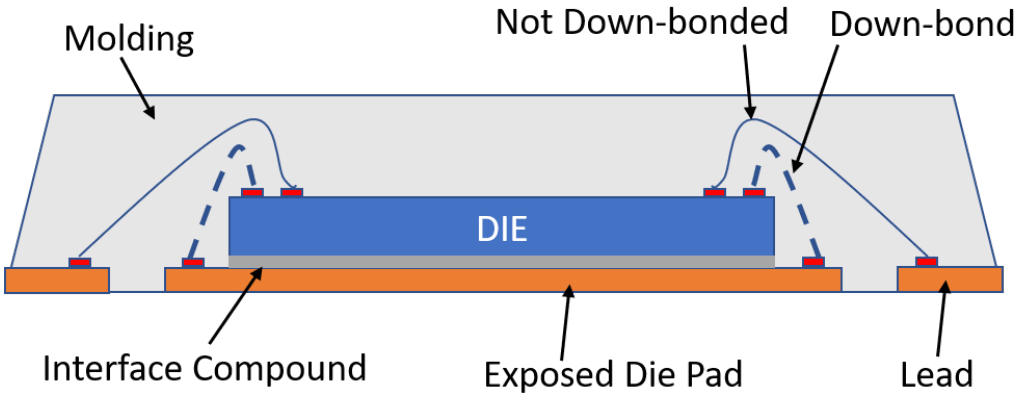


Figure 3.5: Inside view of a package, illustrating the down-bond assembly option. Down-bonding reduces bond-wire length (and inductance) for ground connections. The package used in this work has a copper die pad.

Table 3.2: List of pins and functionality for the test chip.

Pin #	Pin List	Direction	Use Cases
1	RESET_N	Input	Global reset to MCU
2	CPU_EN	Input	Enable CPU
4	DCO_CLK	Input	System clock
6	DCO_ENABLE	Output	Control signal for crystal
7	DCO_WKUP	Output	Control signal for crystal
8	TEST_SCAN	Input	Input of scan_chain shift signal
11	LFXT_ENABLE	Output	Control signal for crystal
12	LFXT_WKUP	Output	Control signal for crystal
13	DBG_UART_TXD	Output	UART transmit port
15	DBG_UART_RXD	Input	UART read port
17	DGB_EN	Input	Enables debug/allow programming
18	NMI	Input	Non maskable interrupt
19	I2C_SDA	I/O	I2C input and output
20	I2C_DIRECTION	Input	Select I2C IO direction
23	I2C_SLC	Input	I2C clock signal
25	GPIO_PIN[0]	Input	MUX shift clock for sensor readout
26	GPIO_PIN[1]	Input	MUX reset signal
27	GPIO_PIN[2]	Input	MUX address input
28	GPIO_PIN[3]	I/O	General purpose IO
29	GPIO_PIN[4]	I/O	General purpose IO
31	GPIO_PIN[5]	Input	MUX select for GPIOs 0, 1, and 2
32	GPIO_PIN[6]	Output	Error detector output 1
33	GPIO_PIN[7]	Output	Error detector output 2
35	LFXT_CLK	Input	Low Frequency clock for GPIO, etc
37	SCAN_ENABLE	Input	Enables scan chain
38	SCAN_MODE	Input	Sets scan chain mode
14,30	ZAP_IO	X	Dedicated zap IO
10,21,40	VSS	Ground	Core ground
3,22,34	VSSIO	Ground	IO ground
9,13,39	VDD	Power	Core power
5,24,36	VDDIO	Power	IO power

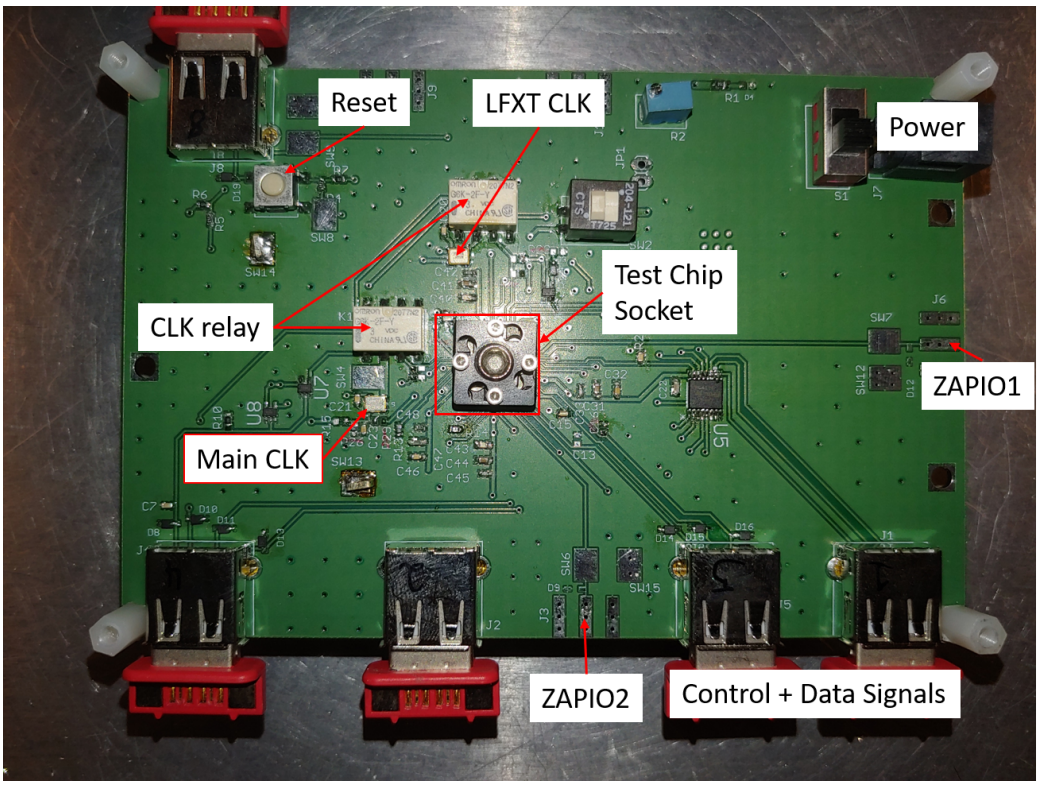


Figure 3.6: Photograph of the board serving as the EUT.

CHAPTER 4

SOFT FAILURES

4.1 Simulation Setups

Simulations allow for further analysis and understanding of soft failures from ESD. While the effect of the ESD noise can be seen during measurement, in order to figure out the root cause, simulations were used. Two types of simulation are performed in this work. The first is a SPICE-type circuit simulation, henceforth referred to as "SPICE sim," and the second is mixed-mode full-wave EM/SPICE simulation, henceforth referred to as "EM sim."

4.1.1 SPICE Simulation

A SPICE simulation deck allows for a qualitative understanding of what happens in the core. Because board effects are neglected and board impedances estimated, trends can be found, however, quantitative accuracy cannot be maintained. On the other hand, a SPICE-only simulation does allow one to isolate chip-only affects.

The model used for the SPICE sim represents the IO ring and power delivery network (PDN), including all decoupling capacitors (decaps) and primary ESD protection devices (dual diodes, rail clamp and APD). Figure 4.1 presents a schematic representation of the simulation netlist. The I-V characteristics for the ESD diodes are matched to 1-ns pulse I-V mea-

surements. The IO decoupling capacitors are left as nonlinear (MOSCAP) elements, while the core decaps are represented as ideal capacitors. No significant simulation error is introduced by the ideal capacitors. The on-chip power and ground routing is represented by a resistive network.

The package model consists of bond-wires that are modeled as shown in Figure 4.2. The L, R, and C values were calculated by approximating the bond-wire as a straight wire above a ground plane, yielding L = 1.8 nH, R = 92.5 mΩ, and C = 48.5 fF. In actuality, all the bond-wires do not have precisely the same impedance because the lengths differ by about 10% based on the location around the chip, but this does not have a significant effect on the simulation results. For the down-bonded components, the bond-wires from VSSIO or VSS to the grounded die pad have L = 0.4 nH, R = 22 mΩ, and C = 11 fF. The ESD gun model is described in Chapter 2.

4.1.2 Electromagnetic/SPICE Combined Simulations

An electromagnetic simulation allows for accurate modeling of the board PDN and any board-level coupling that might be seen. In order to perform these simulations and have any measurable accuracy, it is important that the terminations of the chip are properly represented. Recall that the chip has ESD protection devices, resulting a highly nonlinear input impedance during an ESD event.

The EM sims use Speed2000, a 2D/2.5D full-wave EM solver based on the finite difference time domain (FDTD) method. It has the ability to interface with SPICE circuit elements, allowing for accurate simulation at the board, package and chip levels. Using the FDTD method, the electric and magnetic fields of the simulated structure are found. The SPICE models act as sources

for the solver and are solved along with the EM fields. This allows for a much more accurate simulation that can capture board-chip interactions.

Figure 4.3 shows the testbench used for the EM simulation. The 3D, computer aided design (CAD) model of the board is an input into Speed2000. Excitations were placed at their appropriate location on the board (i.e., voltage sources where the LDOs and control signals enter the EUT). Manufacturer-provided SPICE models were used for all the passive components on the circuit board. The test chip was placed on a new layer 200 μm above the top layer of the board. Since a majority of the package parasitics come from the bond-wires, those are modeled by the EM sim. The QFN package pad parasitics and on-chip bond-pad parasitics were ignored for simplification purposes as these parasitics are small enough that they do not change the simulation results. For the EM sims, it was necessary to further limit the complexity of the chip model, so all of the on-chip decoupling capacitors were replaced with their ideal counterparts.

4.2 Supply Noise and Bit Flips in Registers

ESDs were applied to the powered-on system following the IEC 61000-4-2 standard. The system was connected in a tethered configuration (i.e. powered from a grounded DC supply). Contact discharges were applied to the two dedicated ZAPIOs.

In the first set of experiments, the ESD gun was discharged into the ZAPIO1 and ZAPIO2 signal lines at precharge voltages ranging from -4 kV to $+4$ kV. A minimum of 100 discharges, to each ZAPIO, at each precharge voltage, was performed on at least three different test chips. After each discharge (or "zap"), the voltage monitor outputs are read by the external

computer. The scan chain is also read out to determine if any of its 1535 registers changed state. This experiment is intended to show if there is a correlation between the amplitude of the supply noise and bit flips in registers. In these experiments, the chip's clock pin is tied low through an on-board resistor.

4.2.1 Voltage Monitor Readings

Table 4.1 and Table 4.2 list the mode — value that occurs most often — of the noise readings from the supply voltage monitors at a given precharge voltage. The data shown in those tables were collected from the under-voltage and over-voltage monitors located in both monitor bank 0 (MB0) and monitor bank 1 (MB1). The data indicate that discharges to ZAPIO2 result in larger amplitude noise on the IO supply near MB1 than do discharges to ZAPIO1, while discharges to ZAPIO1 cause more noise on the IO supply nearby to MB0. These results are attributed to a proximity effect — ZAPIO1 is significantly closer to MB0 and ZAPIO2 is closer to MB1.

However, the LV monitors indicate that discharges to ZAPIO2 cause more noise on V_{DD} near both monitor banks. This is attributed to ZAPIO2's proximity to a VDD pin. Noise can be transmitted to the core supply through the APD or by magnetic coupling to a VDD bond-wire [21] and on-board trace. This was confirmed via EM sims. Figure 4.4 shows that for positive 4 kV discharges to ZAPIO1, the peak magnitude of the current on the VDD pin is 0.4 A smaller than for positive 4 kV discharges to ZAPIO2.

The LV monitors readings suggest that the core supply may be slightly noisier in the vicinity of MB0 than in the vicinity of MB1; see the results for -4 kV discharges to ZAPIO2. SPICE simulation is used to elucidate the

underlying reason. Figure 4.5 shows the simulated over-voltage on the core supply induced by a −4 kV discharge and measured at different spots in the pad ring. In simulation, the over-voltage on the core supply is larger near MB0 than near MB1. MB0 is closer to the VSSIO IO cell, which includes the APD that connect VSSIO to VSS and inject noise onto the core supply. Figure 4.6 shows the ESD current paths in the case of (a) a VSSIO cell and (b) a VSS cell. the VSS cell connects V_{SS} to board ground. The simulated overshoot on the core supply varies around the pad ring by only 133 mV, which explains why the voltage monitors, with their coarse sensitivity, detect the variation only under limited conditions, i.e., when the noise amplitude is very near the threshold for one of the monitor output levels.

4.2.2 Zap Polarity Dependence

The supply voltage monitors report overall higher amplitude noise in the IO domain for positive discharges. This polarity dependency was previously reported and analyzed [7], [18], and its cause is summarized below.

The ESD current pulse has a rising edge and a falling edge. It can be roughly approximated as a triangular pulse with a rise time of 1 ns and a fall time of 2 ns. The discharge current path for a positive discharge is given in Figure 3.4. Current enters the IO pin and flows through the top diode to the V_{DDIO} bus. From there, it splits, traveling through the VDDIO bond-wire, the IO rail clamps, the decoupling capacitors, and VSS/VSSIO bond-wires. During the leading edge of the current pulse, a positive voltage will be induced on the V_{DDIO} bus ($L\frac{di}{dt}$). This will cause an initial supply over-voltage. Current will also flow through the IO rail clamp as it turns on and through the VSSIO and VSS bond-wires.

For the leading edge of a negative discharge, current will initially flow through the V_{SSIO} and V_{SS} bond-wires from the board to the chip. This will lower the on-chip ground potential, also resulting in an initial over-voltage. A smaller over-voltage is seen during a negative discharge due to the decreased impedance to ground compared with the positive discharge path.

To understand why the under-voltage is smaller for a negative discharge, we must first look at the core voltage domain. Recall that the IO and core domains are connected via the APD. A positive discharge will cause current to flow out of the VSS bond-wire, raising V_{SS} above board ground and causing an initial under-voltage. This in turn means that the core rail clamp does not turn on. During the trailing edge of the positive current pulse, a negative $\frac{di}{dt}$ causes the voltages V_{DDIO} and V_{SSIO} and V_{SS} to decrease. Since the core rail clamp is initially off, all the ESD current must flow through the VSSIO, VDDIO and VSS bond-wires. On the other hand, the leading edge of the negative discharge causes current to flow into the VSS bond-wire, lowering V_{SS} and causing an initial over-voltage on the VDD supply. This initial over-voltage causes the rail-clamps in the core domain to turn on, providing an additional path for ESD current compared to a positive discharge. That is, during the trailing edge of the negative discharge, ESD current will flow through the VDDIO, VSSIO, VSS, and VDD bond-wires. The impedance to ground during a negative discharge is lower than for a positive discharge resulting in a smaller under-voltage on the IO supply [7].

A slightly different scenario plays out on the core power supply. Looking back at the noise monitor data for the LV domain (Table 4.2), it can be seen that the worst-case over-voltage is induced by a negative discharge. This is due to the slew rate of the current. Remember that the initial rising edge of the first peak of the IEC discharge has a faster rise time than the falling

edge's fall time. This, in turn, results in a larger initial peak ($L\frac{di}{dt}$) in the core domain, whether it be an under-voltage or an over-voltage. Since the first peak for a negative discharge is an over-voltage in the core domain, it is larger than the second peak (over-voltage) caused by a positive discharge. In turn, the positive discharge causes a larger under-voltage than a negative discharge. However, it must be noted that while all the LVUV data in Table 4.1 and Table 4.2 support the conclusion that a positive discharge causes a worse under-voltage than a negative discharge, the data for over-voltages are much more sparse. Another study [18], with a different test chip, show similar results. The data there show a strong correlation between positive discharges and worse under-voltages on the core supply while showing inconclusive results for the over-voltage.

4.3 Noise on Clock and Reset Lines

4.3.1 Scan Chain Test Setup

In conjunction with reading the voltage monitors, bit flips within the core were monitored. As mentioned in Chapter 3, the core included a scan chain, which allowed insight into bit flips in the core. The scan chain consists of a total of 1535 registers which can be programmed if the system is set to "scan chain mode." Using this capability, prior to each discharge, the scan chain registers were programmed to one of three initial states:

1. All zeros
2. All ones
3. A pseudo-random, replicable, bit sequence

The scan chain is read-out after each discharge. If any of the scan chain registers are observed to have changed state, this cannot be attributed to corrupted data having propagated from the peripheral inputs (excluding RESET and the clock inputs) because those inputs cannot be received when the chip is in scan mode. Instead, the possible causes of scan chain bit flips are as follows:

1. On-chip supply noise which exceeds the registers' noise margins.
2. Clock glitches that cause the shift register to advance.
3. Reset glitches caused by board-level coupling or chip-level supply noise.

Clock glitches may be caused by board-level coupling to the clock trace or by noise on the chip-level IO supply, which moves the switching threshold of the clock receiver circuit [10]. A negative discharge will cause the chip's common mode voltage to fall below that of the board. At the same time, the driver for a input signal will still be referenced to the board ground. As such, if the common mode noise on the IO supply from a negative discharge is large enough, a 0 will be read as a 1. A positive discharge will cause the common mode voltage of the chip's IO to rise relative to the board's common mode voltage. This will cause a 1 to be read as a 0.

Initial states 1 and 2 are intended to reveal whether the registers are more prone to flipping if initially set to 0 or 1. Additionally, tests performed with those initial states reveal the number of bit flips that occur without obfuscation from clock glitches.

Initial state 3 is used to detect if the ESD has induced any clock glitches. Should any number of glitches occur on the clock line, around one-half of the registers will have values differing from their expected values. By minimizing the count of differing values, the number of clock glitches and bit flips can

be determined. It should be noted, however, that should a full scan chain reset occur, the number of clock glitches cannot be determined.

4.3.2 Clock Glitches

Clock shifts were observed under two condition. When the chip is operated in scan chain mode, the clock is vulnerable to more board-level noise coupling than under normal operating conditions. A clock generated by the external computer was used during scan chain tests in order to synchronize the receiver and the transmitter. The board trace for the external clock is longer than that for the on-board clock because the former terminates at a connector at the board edge. Recall, bit flips due to clock noise are easily detected after a pseudo-random bit sequence (initial state 3) has been stored in the scan chain. Figure 4.7 shows the probability of a discharge onto ZAPIO1 causing between 1 and 11 clock glitches at each precharge voltage. As expected, the number of clock glitches increases with the precharge voltage. In the worst cases, 10 clock glitches were observed for a given ESD.

The reason that multiple clock glitches occur when the clock trace extends to the board edge can be understood by using EM simulations. Figure 4.8 plots the clock signal with respect to the on-chip VSSIO at the CLOCK IO as well as the quantity $V_{DDIO} - V_{SSIO}$, measured on-chip in proximity to the clock pin. The clock signal is nominally low (0 V), however, this figure shows the clock signal exceeding the switching threshold multiple times in a very short timespan, given a single ESD, thereby, causing multiple clock glitches. The simulation shows that the noise can last 10's of nanoseconds despite the fact that the initial current peak is on the order of 1 ns.

In contrast, during normal operation, the on-board clock generator was

placed as close to the chip as possible (Figure 3.6) to minimize coupled noise. Experiments for identifying clock glitches in this configuration required adding a pull-down resistor at the test chip's clock pin. ESD tests were performed at precharge voltages ranging from −4 kV to +4 kV. Figure 4.9 shows the number of measured clock glitches. For some of the chips, in 100% of trials performed at −4 kV, the scan chain experienced one clock shift, while discharges from −3 kV to +3 kV did not cause any clock glitches. For those same chips, the occurrence of clock glitches at +4 kV could not be verified due to the resetting of the scan chain.

The supply noise monitor circuits indicate larger magnitudes of on-chip noise for +3 kV discharges than for −4 kV discharges. However, clock glitches only occurred during −4 kV discharges. Table 4.3 shows that a lower positive precharge voltage is needed to cause a "1" to "0" glitch while a lower negative precharge is required to cause a "1" to "0" glitch. These data suggest that the clock glitch results from common mode noise at the input causing the input "0" to be read as a "1" resulting in a glitch. The scan chain results show that the discharge level at which a "0" to "1" glitch occurs is lower for negative discharges than for positive discharges, and this conjecture is corroborated by the ORIDs (Table 4.3) as well as the study in [5].

Since the RESET signal is transmitted from an off-board source, it is vulnerable to board-level noise coupling; however, large amounts of on-board filtering help to mitigate glitches on RESET. Full scan chain resets were only observed for discharges of +4 kV.

By comparing Figure 4.7 with Figure 4.9, it is clear that there is a significant reduction in clock glitches when a well placed, on-board, clock generator is used over an off-board clock. Clock glitches can be catastrophic to the operation of a chip, thus careful consideration should be made for clock routing.

4.3.3 Bit Flips in Registers

By adjusting for clock glitches and excluding trials in which the full scan chain was reset, the number of bit flips for a given ESD event could be found. Figure 4.10 shows the probability of a trial causing n bit flips, where n is an integer. The data are further organized by the precharge voltage at which the discharge occurred. It is observed that the number of bit flips is in the single digits for all precharge voltages other than +3 kV and +4 kV. The number of bit flips caused by discharges above +3 kV may vary by up to 50% depending on the chip tested; Figure 4.10 shows results for one chip.

These bit flips can be broken into two categories, random bit flips and bit flips caused by glitches on the RESET line. Depending on the chip tested, between 0% and 15% of bit flips at +4 kV were random. These bit flips would occur in the same registers for a given chip, but were not consistent across multiple chips. Also, these random bit flips did not follow any known pattern that would suggest that they result from an input glitch. That is, measurements without ESD while toggling combinations of inputs (e.g. CLOCK, SCAN_EN, SCAN_MODE, etc.) to simulate glitches, result in different bits changing state compared with the random ESD induced bit flips. A majority of the bit flips, however, could be attributed to resets. This was ascertained by comparing the flipped bits' states to the reset state; the latter is obtained by asserting RESET and then reading out the scan chain without a discharge event in-between.

The RESET signal is an asynchronous signal that is buffered and fanned out within the core. Figure 4.11 shows part of the on-chip path of the RESET signal. The RESET signal enters the chip via the RESET pin. It is then filtered by a Schmitt trigger and level-shifted down to the core voltage,

after which it is buffered and distributed through the core. Each connection between gates is a "circuit node." A circuit node's electrical distance from the RESET pin is determined by the number of logic elements, e.g. inverters and buffers, between that circuit node and the RESET pin. By using a directional graph, all registers could be associated with a circuit node along the RESET line. The number of bit flips per circuit node for a given trial could then be identified. The results of that analysis are shown in Figure 4.11, where the values in orange denote the percentage of registers at a given circuit node that get reset. The fraction of registers that experience a reset decreases as the circuit node becomes electrically farther from the RESET pin.

The EM simulation results in Figure 4.12 predict that the active-low RESET signal transitions briefly from high to low during a +4 kV discharge to ZAPIO1, consistent with the measurement results. In essence, the internal RESET signal has a glitch. In the figure, the voltage on RESET minus the common mode voltage is plotted along with the instantaneous supply voltage, $V_{DD} - V_{SS}$. It is observed that the supply voltage briefly drops below zero; this supply inversion is not unexpected and has been documented in the past [22]. When $V_{DD} - V_{SS}$ is larger than the threshold voltage (approximately 0.35 V), the register can respond to input signals. In the simulation, at $t \approx 3$ ns, the register is powered on and there is a glitch on RESET that pulls it low for about 0.5 ns after. In simulation, the register output flips to its reset state. Figure 4.13 shows EM simulation results of the reset signal at different points along its path to the core. While the glitch at the IO introduces noise on the reset line, the on-board and on-chip filtering help minimize the noise seen in the chip after the level-shifter. However, the on-chip core supply noise significantly degrades the quality of the reset signal

as it passes through the large buffers from the IO to the core. As the supply noise may be large enough to corrupt internal core signals by itself, all signals originating from the IO ring are highly susceptible to glitches.

4.4 Noise on Down-Bonded Chips

Table 4.4 show MB0 and MB1 voltage monitor readings following discharges to ZAPIO1 on a down-bonded chip, at levels ranging from −4 kV to +4 kV. When these results are compared to those obtained for chips without down-bonding (Table 4.1), two notable things were observed.

1. Significantly decreased noise on the core supply.

2. Little change in noise on the IO supply.

4.4.1 Decreased Noise on the Core Supply

The LVUV monitor on the down-bonded chips shows significantly reduced supply noise and the same is predicted by SPICE sim; see Figure 4.14. The down-bonds reduce the $L\frac{di}{dt}$ noise on V_{SSIO}. The amplitude of the noise transmitted by the APD to the core voltage supply is, therefore, reduced.

4.4.2 Noise on the IO Supply

The HV monitors on the down-bonded chips show roughly similar results to those on chips without down-bonds. Figure 4.15, created via SPICE simulation, confirms that the under-voltage on the IO supply should not significantly change when down-bonds are used. This finding may be understood with the aid of Figure 4.16, which provides a simplified representation of the ESD current injected into the chip and its return paths to the board ground.

In that figure, Z represents the impedance of the on-chip routing, the rail clamp, and the on-chip decoupling capacitors. If the rail clamp is triggered on, Z can be reasonably well modeled as purely real (Z = R).

Using the model of Figure 4.16, the magnitude of the noise on V_{DDIO} is found to be

$$V_{DDIO} = |I_{ESD}(\omega)| \frac{L_1 \omega \sqrt{L_2^2 \omega^2 + R^2}}{\sqrt{R^2 + \omega^2 (L_1 + L_2)^2}} \tag{4.1}$$

where $I_{ESD}(\omega)$ is the ESD current and ω is the frequency of the ESD current. Circuit analysis indicates that the noise on V_{SSIO} is a fraction of that on V_{DDIO}, with a magnitude given by

$$V_{SSIO} = V_{DDIO} \times \frac{\omega L_2}{\sqrt{R^2 + \omega^2 L_2^2}} \tag{4.2}$$

Equations (4.1) and (4.2) show that the down-bonded chips, with the smaller L_2, will have a reduced bounce on the V_{DDIO} and V_{SSIO} busses. To understand why the monitor circuit and the SPICE sim is not strongly affected by the down-bonding requires one to also consider the phase of the noise on V_{SSIO} relative to the noise on V_{DDIO}. To find the phase difference, one can set the phase of V_{DDIO} to 0 and calculate the phase difference as

$$\angle V_{SSIO} - \angle V_{DDIO} \;=\; tan^{-1}(\frac{R}{\omega L_2}) \tag{4.3}$$

The phase difference between V_{DDIO} and V_{SSIO} increases as the inductance of the VSSIO bond-wire decreases, and this tends to increase the maximum voltage excursion on the supply, i.e., the deviation from nominal $V_{DDIO} - V_{SSIO}$. Figure 4.17 shows the simulated current waveforms at a VDDIO and a VSSIO pin. This figure confirms that there will be a larger phase shift in the down-bonded chip.

Equations (4.1) and (4.2) as well as simulations establish that the bounce on VSSIO is reduced by the down-bonds and that, as a result, there is less noise on VSS and the core supply. The use of down-bonds is recommended.

4.4.3 Clock Glitch Comparison

No clock glitches are seen in down-bonded chips (Figure 4.18), during any scan-chain tests using a grounded clock pin, for discharges from +4 kV to −4 kV. In comparison, chips without down-bonds were observed to experience clock glitches at +4 kV and −4 kV. The only difference between the two test setups was the presence or absence of down-bonds on the test chip. A comparison of glitches occurring, during ESD, at other (non clock) pins will allow us to draw conclusions about clock glitch occurrence. Compare Table 4.5 (down-bonded ORID results) with Table 4.3 (not down-bonded ORID results). Notice the increased precharge voltage required to cause the ORID circuits to trigger in a down-bonded chip. Furthermore, the down-bonds reduce the common-mode noise on the IO supply, thereby requiring higher precharge levels to shift the input levels of the IO circuits enough to cause a glitch. Taken together, these observations indicate that clock glitches occur preferentially in chips with larger supply noise.

4.4.4 Scan Chain Program State Affects Peak Core and IO Supplies' Under-Voltages

As indicated in Table 4.6, if the scan chain was filled with 0's before the discharge event, the HVUV and LVUV monitors detected a smaller under-voltage than if the scan chain was filled with either all 1's or a pseudo-random pattern. The result is consistent between chips. SPICE simulation was used

to assess whether the core devices contribute significantly different capacitances when the registers are programmed to different states; the answer was negative, and this was ruled out as a cause of the unexpected findings. The supply current (I_{DD}) varies slightly (less than 10 mA) when the scan chain is programmed to different bit patterns, but the effect is too small to be a likely cause of the phenomenon. At this time, no explanation has been found for the results in Table 4.6. One possible hypothesis is that, as the control registers are set to different states, the configuration within the core may be different. Thus, if during the ESD events control signals are corrupted the core may instantaneously and for a short period of time draw a significantly higher current based on the programmed registers' states.

4.5 Operational Tests

In a second set of experiments, simple programs were executed by the microcontroller while it was subjected to static discharges. These experiments are designed to analyze the impact of ESD when the memory is being utilized. After each discharge, the contents of the SRAM were read via the universal asynchronous receive transmit (UART) debugger port by the external computer. Assessing memory robustness against ESD-induced errors allows assessment of the feasibility of initiating a software-controlled recovery after the ESD event. If the contents of the memory cannot be trusted, recovery techniques, e.g., checkpoint and rollback, will incur a significantly larger overhead.

In these experiments, glitches on the RESET signal line often caused parts of the chip, e.g., the debug unit, to stop communicating, compromising the functionality of any applications requiring user input or data input/output.

Luckily, the DBG_EN signal allows for resetting of the UART port (which allows data to be read from the debug unit) while maintaining SRAM data integrity, a fact that the test programs were written to take advantage of. Nevertheless, such interruptions greatly extended program run times and can look like system hangs to a user.

Three programs [23] were developed to exercise different parts of the on-chip circuitry and provide insight into ESD-induced soft failures:

- Program 1 sets every word of the DMEM to the value 0x1248. Afterwards, it infinitely loops to emulate a halted state during which a discharge is performed.

- Program 2 sets all of the DMEM to the value 0x1248. Next, the program repeatedly iterates through the DMEM, reading out one word at a time into a temporary register and then writing it back to its original location in DMEM. The discharge occurs during the read/write operations.

- Program 3 sets each general purpose register (GPR) to a distinct known value. Each register is then used as a source and destination register for idempotent arithmetic operations. The discharge occurs during the arithmetic operations. Periodically, the contents of the registers are written into SRAM to preserve the data against a potential reset.

A minimum of 100 discharges were performed per test case and ZAPIO on each of three chips. To ensure that each program has finished initializing before an ESD, the test chip and external computer are synchronized. Unfortunately, due to the design of the EUT, all results except for SRAM bit flips were obscured by resets.

4.6 Memory Tests

Programs 1 and 2 can reveal bit flips in the SRAM. No bit flips in the SRAM were observed at ESD precharge levels ranging from −5 kV to +4 kV. At +5 kV, bit flips in SRAM were observed, in contrast, some registers experienced upsets at +3 kV. This finding suggests that the SRAM is more immune to ESD-induced noise than are the registers.

Memory tests were performed when the chip V_{dd} was set to 1.5 V and 1.2 V. It was found that SRAM bit flips did not occur when the supply was at 1.5 V, however, did occur upon lowering the supply voltage was set to 1.2 V. This shows that low voltage ICs are more susceptible to ESD induced bit flips than ICs with a higher supply voltage. This is not surprising as higher supply voltages result in higher noise margins, and thus large amplitudes of noise are required to corrupt signals and data within the core.

Bit flips in SRAM occurred for +5 kV discharges to ZAPIO2 but not ZAPIO1. This finding is consistent with the voltage monitor readings in Table 4.1 and Table 4.2. The LVUV readings indicate that discharges at ZAPIO2 cause more supply droop that those at ZAPIO1.

There is no direct path from the IC's external pins to the SRAM; therefore, SRAM bit flips could be attributed to core supply noise upsetting memory cells. Specifically, bit flips are attributed to the undershoot on the core supply that occurs at high positive precharge levels. EM sims, Figure 4.14, show supply inversion occurring in the core. This may lead to charge loss at the storage nodes of an SRAM cell and the cell may flip its state as the power supply is restored, especially if the cross-coupled inverters are asymmetrical due to process variation. For a given chip, 95% of bit flips occurred in the same SRAM cells, trial after trial, while the remaining 5%

were at random locations. The SRAM cells that get upset consistently by ESD noise are referred to as "weak" cells, and the location of those "weak" cells differ between chips. The "weakness" is attributed to process variation. For example, a mismatch between the transistors in a SRAM cell will reduce its noise margin, making the cell more vulnerable to supply variations. The fraction of cells in the memory array that are "weak" is estimated to be about 0.025% in this study. It is likely that the random bit flips reported in Section 4.3.3 occur in registers that have a reduced noise margin due to process variations, i.e., "weak" registers.

Bit flips are also observed in PMEM. Approximately 0.02% of cells experienced bit flips, a similar quantity to that in DMEM, but there are some notable differences between the findings for DMEM and PMEM. PMEM cells that get disturbed are not randomly distributed throughout the memory array; they are clustered in one physical region and that region is consistent across different chips. If those cells were being accessed by the system, it could explain their heightened sensitivity to ESD. Or, perhaps, the supply noise has its maximal amplitude where the PMEM upsets occur. Those hypotheses cannot be confirmed for the following reasons. (1) The ESD event is triggered manually during testing and cannot be precisely aligned to a given clock cycle (or even within 1000's of clock cycles). In order to verify which instruction is being executed and which stage of execution the EUT is on requires the aforementioned lacking accuracy. (2) The simulation test-bench required to verify which PMEM cells get upset requires a level of complexity that will require excessive amounts of time along with convergence issues. Finally, finding the exact location of a bit within a synthesized block of memory also tends to be excessively time consuming.

An experiment was conducted in which the PMEM was restored to its

original state only once every 10 trials. Figure 4.19 shows that the erroneous bits are retained until the PMEM is refreshed, i.e., the stored data do not flip back and forth between 0 and 1. A storage cell may have a preferred state, 0 or 1, either due to process variations or due to an asymmetric noise environment, e.g. on the word lines or bit lines. Once a SRAM cell gets disturbed due to noise, it may enter a preferred state, after which the probability of it switching in the opposite direction is low. The measurement results in Figure 4.19 support the hypothesis that the memory cells that get disturbed have a preferred state. Interestingly, every set of 10 trials had at most a single discharge that caused bit flips. However, with 6 kV discharges, multiple discharges in a sequence of 10 cause bit flips, and like the 5 kV results, once a memory cell flips states, it does not flip back.

4.7 Suggestions on the Mitigation of Soft-Failures

Soft failures can be a significant problem for the operation of ICs. While there are many methods to help reduce the bit error rate (BER) from the computer architecture side, e.g. triple modular redundancy, error correcting codes, etc., ESD poses another challenge entirely. ESD events can cause catastrophic noise on the ICs power supplies which affects the entire chip. Additionally, recovery techniques like checkpoint and rollback cannot be reliably used with SRAM as the SRAM experiences soft failures. It was observed that on average, 0.0025% of SRAM cells were weak. For our memory size (5 kB) this amounts to around three cells, however, in many modern products, it is not unusual to have 1,000 times as many memory cells as on our test chip. Thus, for more complex chips, the quantity of SRAM bit flips likewise increases.

Soft failures need a full system design strategy in order to mitigate them. Board design should be executed carefully. Core supply pins and critical signals, e.g., clock, should be placed away from signal lines that may experience ESD. Using on-board elements that shunt ESD current to board ground, e.g. transient voltage suppressors (TVS), will reduce glitches on the signal lines and supply fluctuations [24]. However, just doing this may not be enough [7]. Down-bonding significantly reduces the differential noise seen on the core supply and should be used whenever possible. Down-bonding has the additional benefit of reducing the common mode noise through reduction of bond-wire inductance. Designing a chip such that sensitive core circuitry is located closer to VSS bond-wires and as far away from the APD as possible will also help improve soft failure immunity.

The number of bit flips in registers increases as the precharge voltage increases (Figure 4.10), until all the registers are reset. Both under-voltage monitors track this increasing trend (Table 4.1 and Table 4.2) but the 2-bit outputs of the monitors do not provide sufficient sensitivity for the monitors to achieve precise tracking with the bit flip trend. For example, the MB0 LVUV reads the same value for a +2 kV discharge to ZAPIO2 and a +3 kV discharge to ZAPIO1, however, bit flips are only seen in the latter case. Careful placement of these monitors within the chip and tuning of the voltage reference levels might allow the monitors' output bits to change at noise levels where bit flips start occurring. These monitor outputs can be used to determine if computations can be trusted. If a monitor triggers, steps can be taken to verify or re-compute suspect outputs. However, just supply noise monitors may not be enough; common mode supply bounce can potentially cause or exacerbate the glitch likelihood and requires detectors like the ORID circuit to monitor.

4.8 Figures and Tables

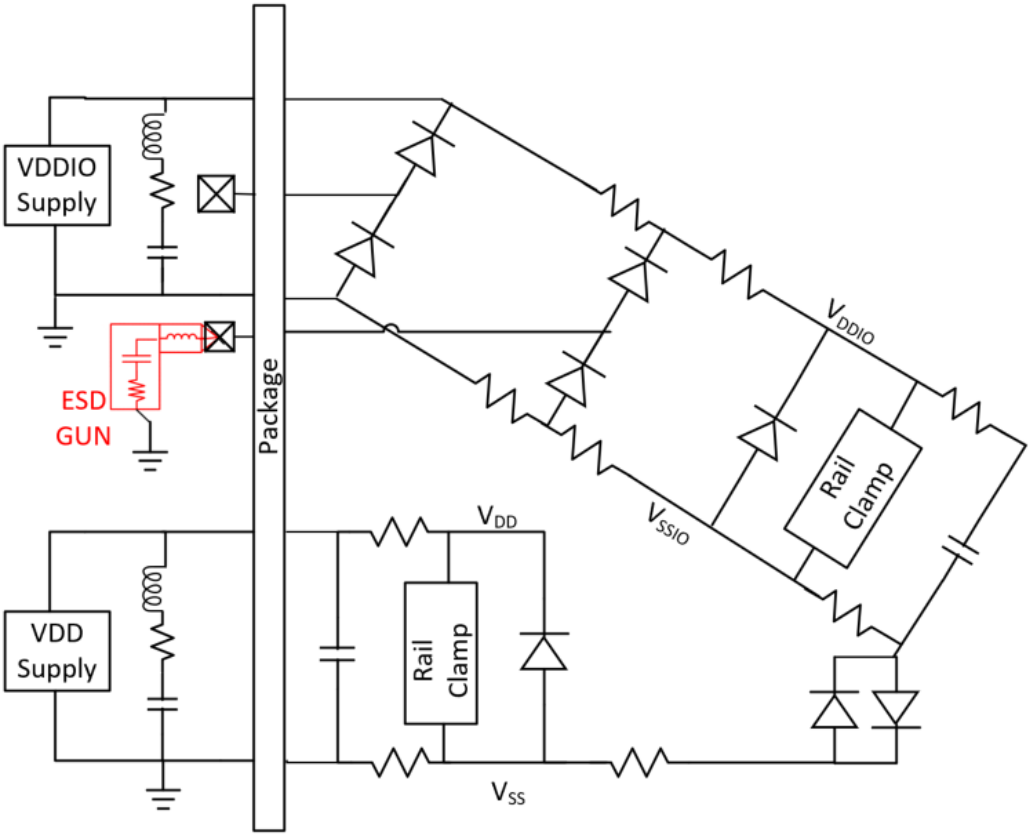


Figure 4.1: Schematic of the SPICE sim netlist. The same chip-level schematic is used for EM sims. The ESD gun is connected to an IO protected by dual diodes. A rail clamp connects V_{DDIO} to V_{SSIO} and V_{DD} to V_{SS}. APD connect V_{SSIO} to V_{SS}. A diode is used to prevent supply inversions above approximately 0.7 V.

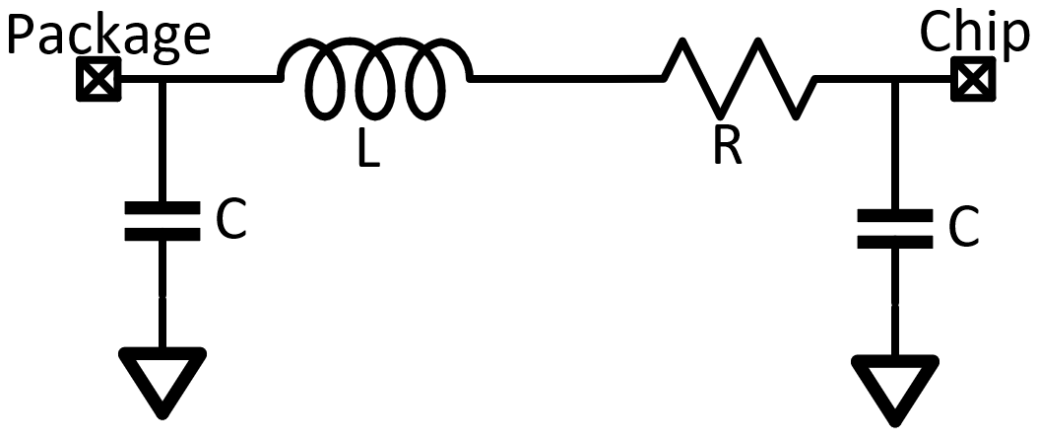


Figure 4.2: Lumped, LRC model of a bond-wire. Values are calculated for a 25 μm bond-wire, modeled as a straight line, 200 μm above a ground plane. Down-bonds have L = 0.4 nH, R = 22 mΩ, and C = 11 fF. Otherwise, L = 1.8 nH, R = 92.5 mΩ, and C = 48.5 fF.

Table 4.1: The response of voltage monitor circuits in MB0 and MB1 to ESD applied to ZAPIO1. The mode values are listed; 100 discharges for each precharge voltage were used to calculate that quantity. V_{pre} is the ESD gun precharge voltage. Monitor output codes randge from 0 to 3, with larger values denoting a larger amplitude voltage disturbance.

Vpre [kV]	MB0				MBI			
	HVOV	HVUV	LVOV	LVUV	HVOV	HVUV	LVOV	LVUV
-4	3	2	0	0	1	1	0	0
-3	3	1	0	0	1	1	0	0
-2	3	0	0	0	1	0	0	0
2	3	2	0	1	3	2	0	1
3	3	2	0	2	3	2	0	2
4	3	3	0	3	3	2	0	3

Table 4.2: Response of voltage monitor circuits in MB0 and MB1 to ESD applied to ZAPIO2. The mode values are listed.

Vpre [kV]	MB0				MB1			
	HVOV	HVUV	LVOV	LVUV	HVOV	HVUV	LVOV	LVUV
-4	1	1	1	2	3	1	0	1
-3	1	1	0	1	3	1	0	1
-2	1	0	0	1	3	0	0	1
2	3	2	0	2	3	2	0	2
3	3	2	0	3	3	2	0	3
4	3	2	0	3	3	3	0	3

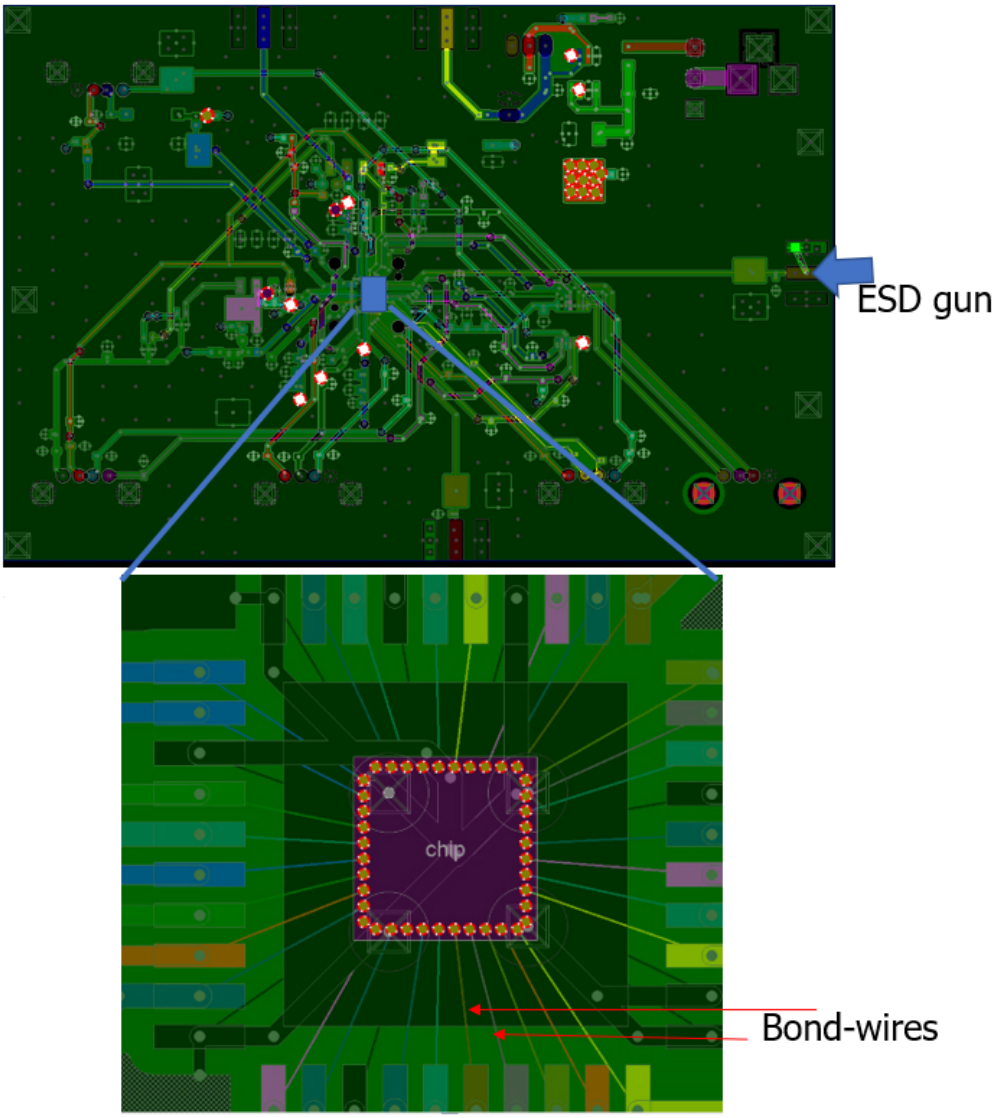


Figure 4.3: The top image shows the EUT (PCB) translated into Speed2000. The bottom image shows a zoomed in figure of the area around the chip. The chip is in the middle with bond-wires, indicated, connecting it to the board mounting pads.

Table 4.3: ORID readings for discharges from +4 kV to −4 kV. An input glitch is partially dependent on the polarity of the discharge.

Vpre	GPIO ORIDL	I2C ORIDH
-4	1	1
-3	1	1
-2	0	1
2	1	0
3	1	1
4	1	1

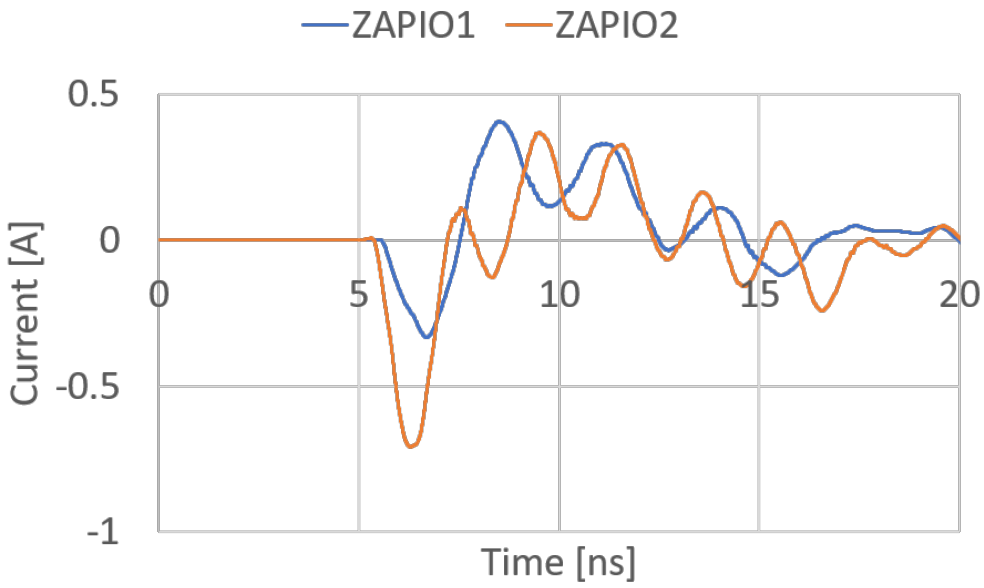


Figure 4.4: EM simulation of the current into a VDD pin located near ZAPIO2 given a +4 kV discharge to ZAPIO1 (blue) and ZAPIO2 (orange). ZAPIO1 does not have a VDD pin located nearby. Notice the higher amplitude current for a discharge to ZAPIO2.

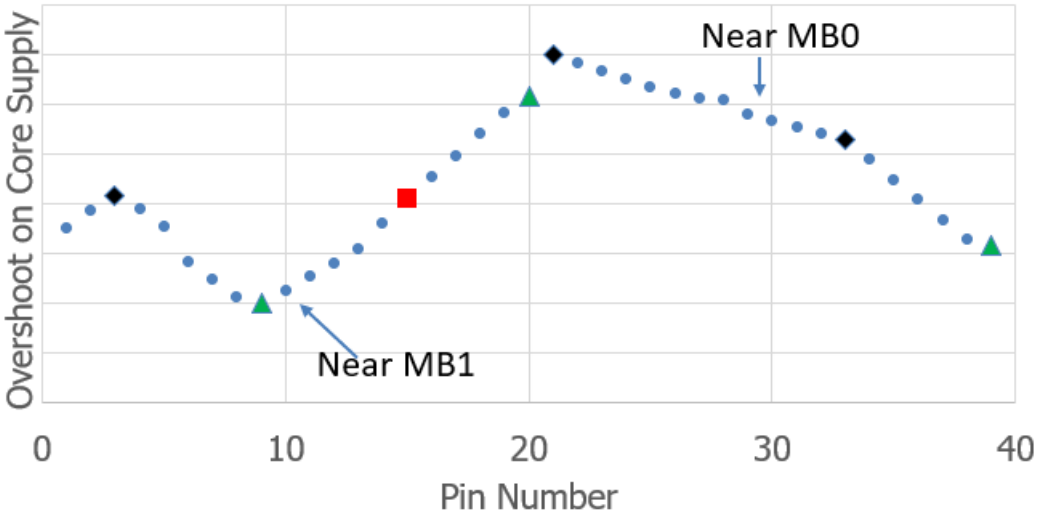


Figure 4.5: SPICE sim of the overshoot voltage on the core supply from a −4 kV discharge to ZAPIO2 as a function of the location on the chip. VSS bond-pads emphasized (green triangle). VSSIO bond-pads (black diamond) and ZAPIO in red. Values are normalized.

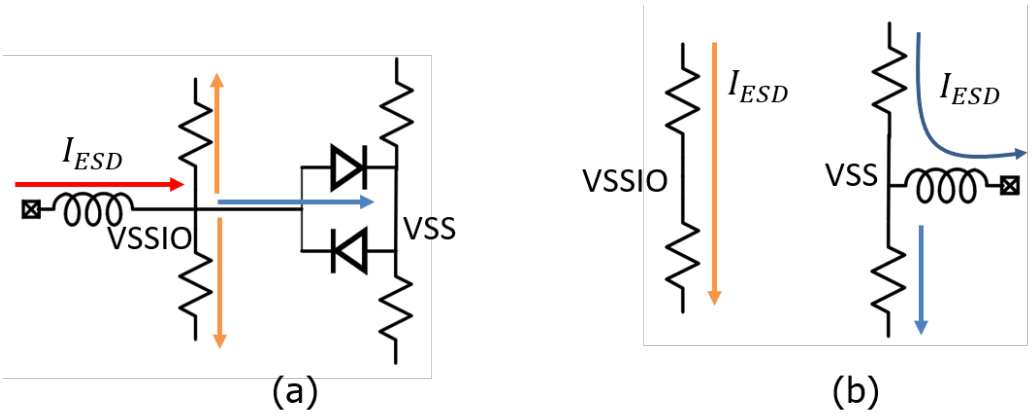


Figure 4.6: (a) Representative figure of a VSSIO IO cell. Current enters the VSSIO bond-wire and couples to VSS through the APD. (b) Representative figure of a VSS IO cell. Current travels within the VSS power grid and exits the chip at the VSS bond-wire.

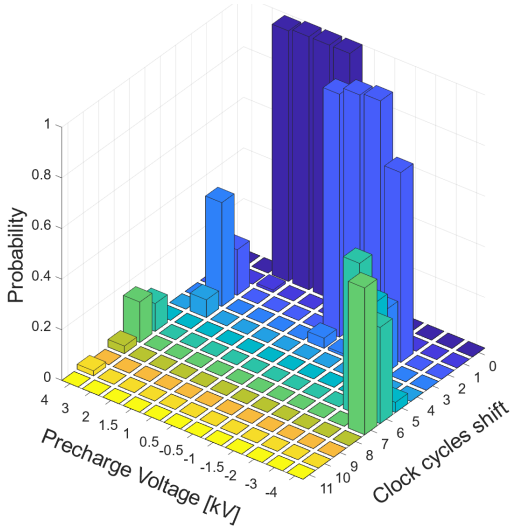


Figure 4.7: Probability of a discharge causing N clock shifts when board was set to use the external clock. Discharges performed to ZAPIO1 with the scan chain initialized with a PRBS pattern. Clock cycles shift refers to how many clock cycles were needed to shift the data to match the expected values.

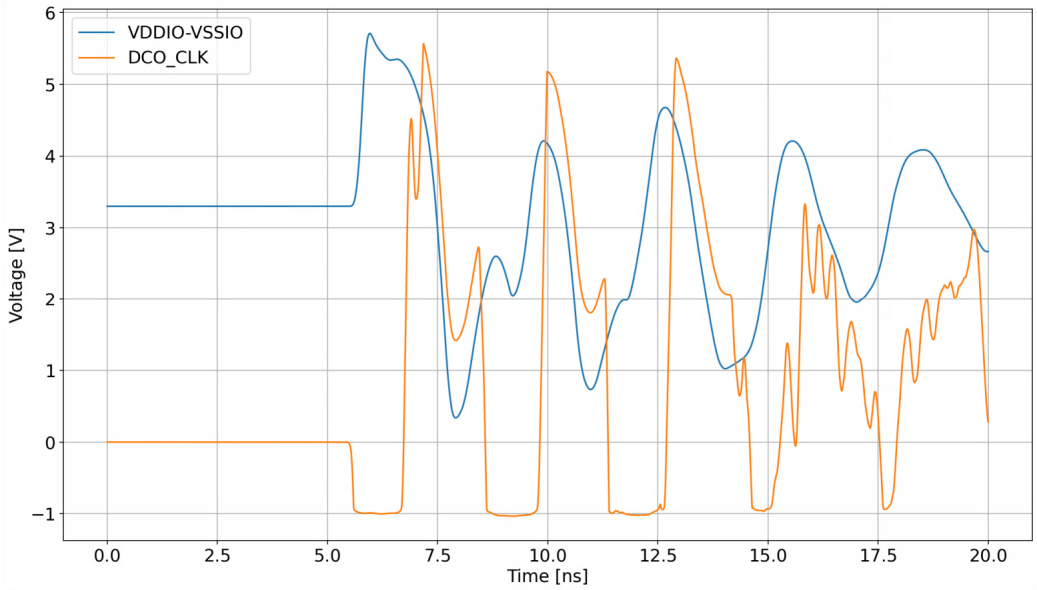


Figure 4.8: EM simulation results of the differential mode noise seen on the chip given a positive 4 kV discharge. DCO_CLK minus the local VSSIO at the input IO is plotted in orange. The local VDDIO−VSSIO is plotted in blue. The clock signal is driven from the edge of the board in the external clock setup. Notice that DCO_CLK exceeds VDDIO multiple times during a single ESD event, which will cause multiple clock glitches.

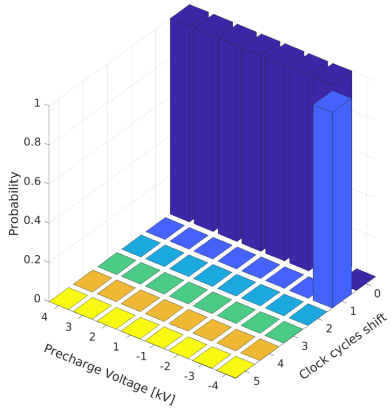


Figure 4.9: Probability of a discharge causing N clock shifts when the board was set to use the internal clock. Discharges performed to ZAPIO1 with the scan chain initialized with a PRBS pattern. Clock cycles shift refers to how many clock cycles were needed to shift the data to match the expected values.

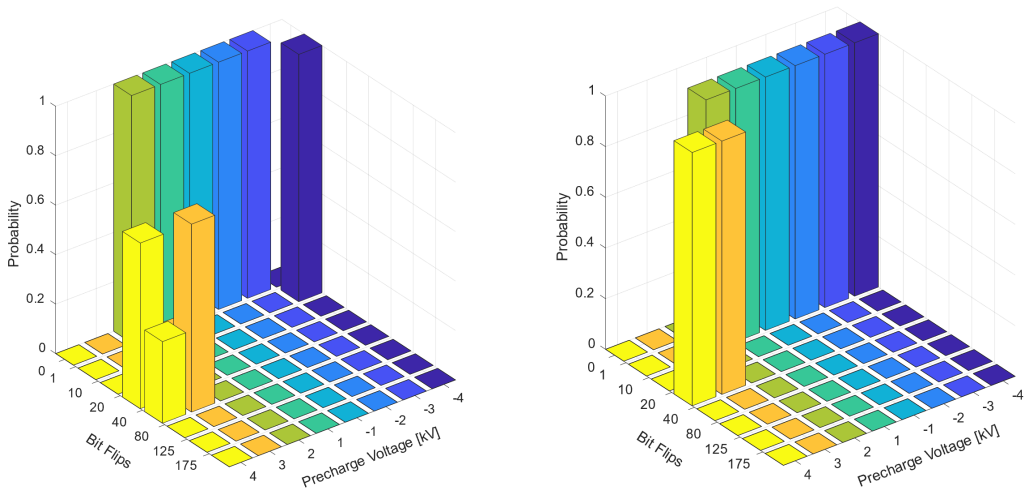


Figure 4.10: Probability that a discharge at a given precharge voltage will result in a number of bit flips, after adjusting for clock glitches and removing trials where resets occurred, given an initial state of 0 for all registers in the scan chain. The number of bit flips were grouped in increasing large bins. The left-hand side shows bit flips caused by discharges to ZAPIO1. The right-hand side shows bit flips caused by discharges to ZAPIO2. Values shown are for a single chip and upwards of a 50% variation is seen across different chips.

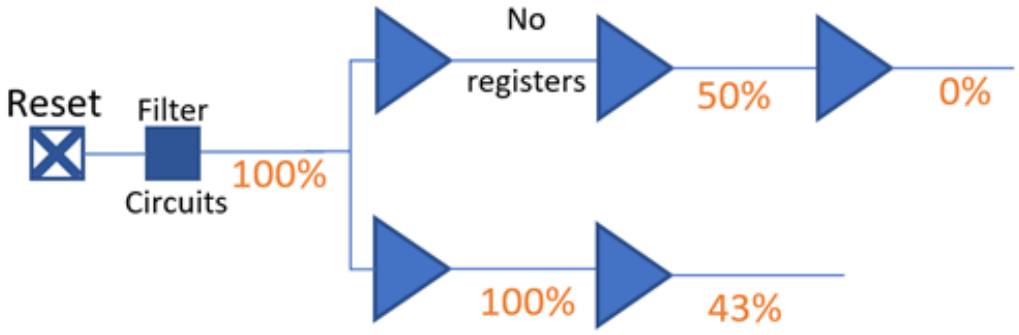


Figure 4.11: Percentage of registers that flip at a specific electrical distance from the RESET pin in response to a +4 kV discharge. The triangles signify combinational logic blocks which feed the RESET signal to banks of registers. The block denoted "filter circuits" includes a Schmitt trigger, level shifters and super buffers.

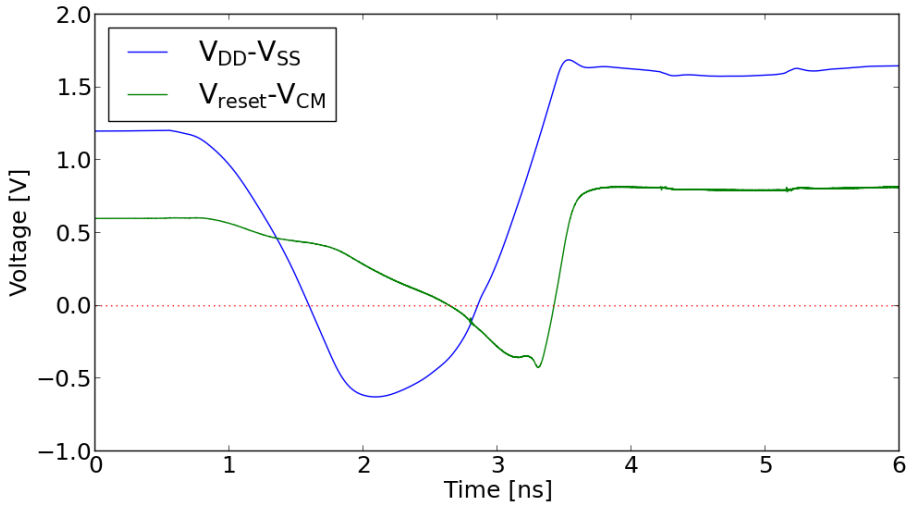


Figure 4.12: EM simulation of the core supply voltage (blue) and the voltage at the reset pin of the register minus the common mode core supply voltage (green). The nominal reading of $V_{reset} - V_{CM}$ is 0.6 V. Notice that even after the supply voltage has risen above a threshold voltage (approximately 0.35 V), $V_{reset} - V_{CM}$ is below 0 for approximately 0.5 ns.

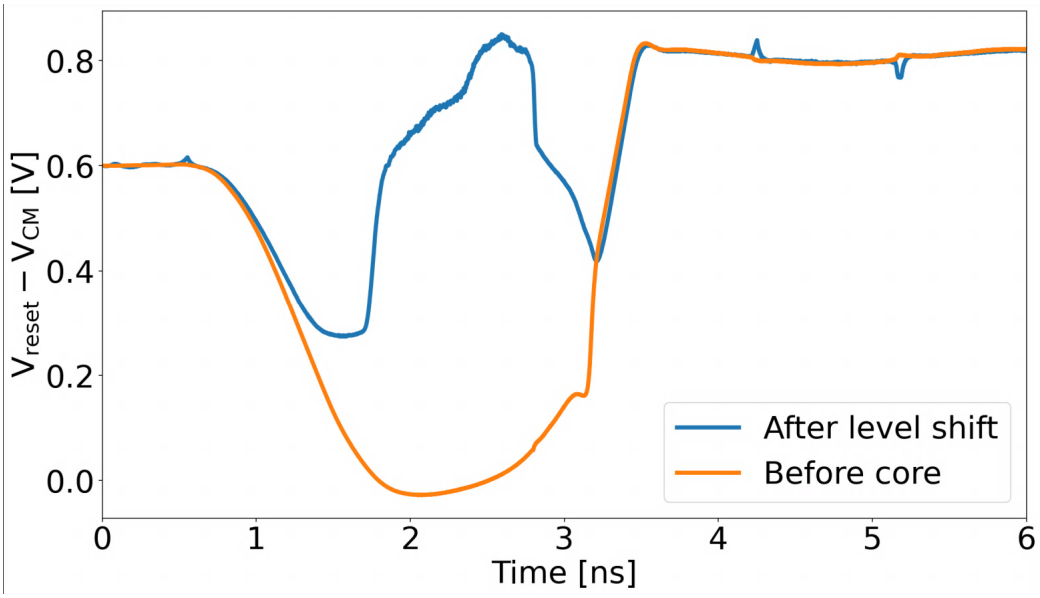


Figure 4.13: EM simulation of the reset signal at the output of the level shifter in the IO minus the common mode core supply voltage (blue) and the voltage at the input to the first buffer in the synthesized core minus the common mode core supply voltage (orange). The nominal reading of $V_{reset} - V_{CM}$ is 0.6 V. Notice the noise at the IO is then worsened by the core supply noise before entering the core. In fact, the main contributor to the noise on RESET is the on-chip supply noise.

Table 4.4: Response of voltage monitor circuits in MB0 and MB1 to ESD applied to ZAPIO1 of a down-bonded chip. The mode values are listed.

Vpre [kV]	MB0				MB1			
	HVOV	HVUV	LVOV	LVUV	HVOV	HVUV	LVOV	LVUV
-4	3	1	0	0	1	1	0	0
-3	3	1	0	0	1	0	0	0
-2	3	0	0	0	1	0	0	0
2	3	2	0	0	3	2	0	0
3	3	3	0	1	3	2	0	1
4	3	3	0	1	3	3	0	1

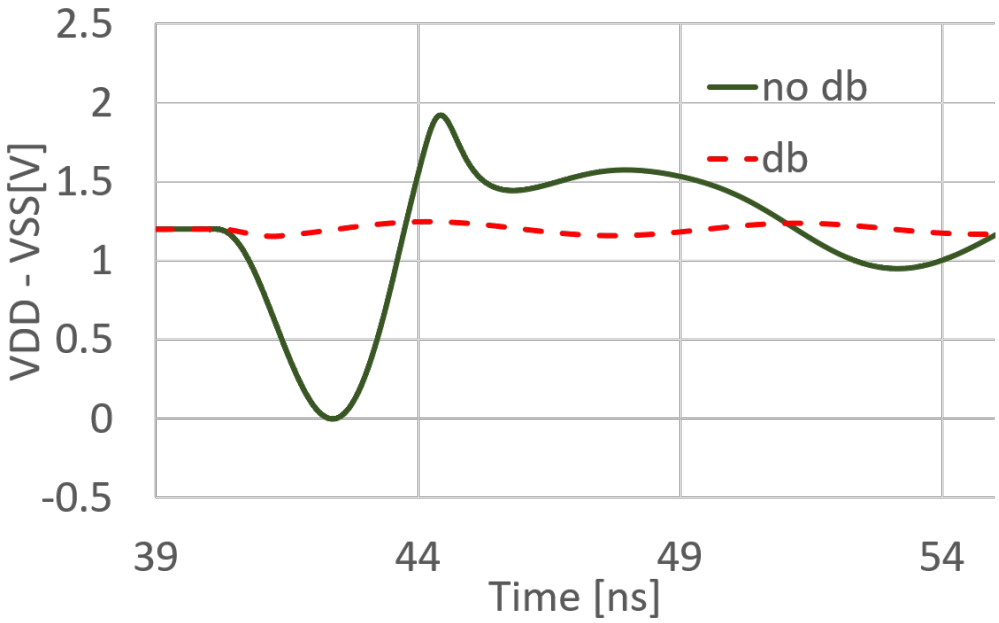


Figure 4.14: SPICE sim of noise on the core supply for a non-db chip (green) and a db chip (red).

Table 4.5: ORID readings for discharges from +4 kV to −4 kV in a down-bonded chip. An input glitch is partially dependent on the polarity of the discharge.

Vpre	GPIO ORIDL	I2C ORIDH
-4	1	1
-3	0	1
-2	0	1
2	1	0
3	1	0
4	1	1

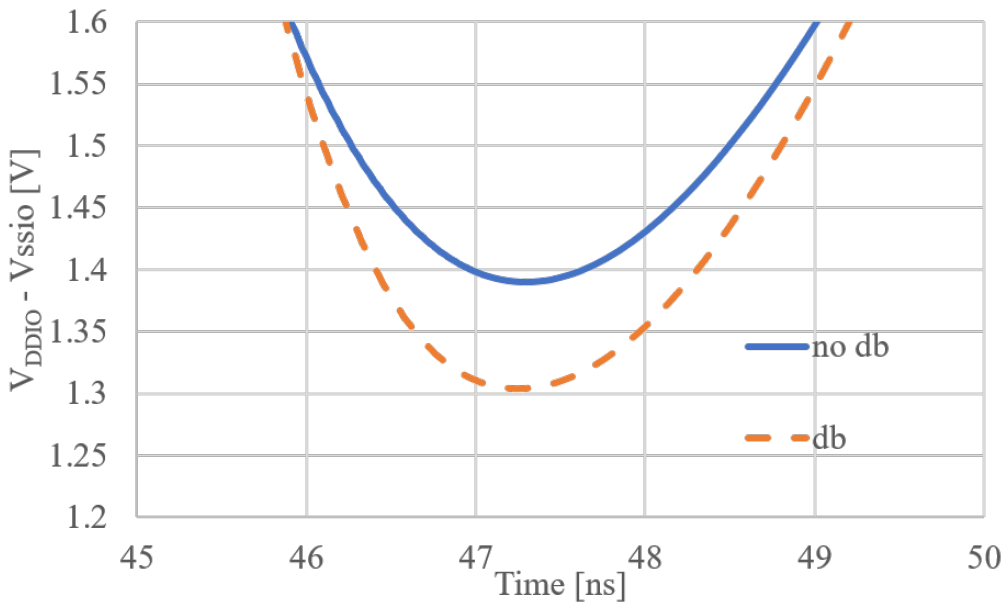


Figure 4.15: Simulated under-voltage on the IO supply; +4 kV discharge to ZAPIO1. $V_{DDIO} - V_{SSIO}$ is plotted; it is nominally 3.3 V. The dashed orange line is for a db chip; solid blue is no db. The peak difference between the two traces is 80 mV.

Table 4.6: Down-bonded chip data from MB1 across the three different scan chain patterns. Aggregate data from three chips. Notice the bolded cells. MB0 shows a similar difference between STATE0 and the other states.

Vpre [kV]	PATTERN		STATE0		STATE1	
	HVUV	LVUV	HVUV	LVUV	HVUV	LVUV
-4	1	0	1	0	1	0
-3	0	0	0	0	0	0
-2	0	0	0	0	0	0
2	2	0	2	0	2	0
3	2	1	2	**0**	2	1
4	3	1	**2**	1	3	1

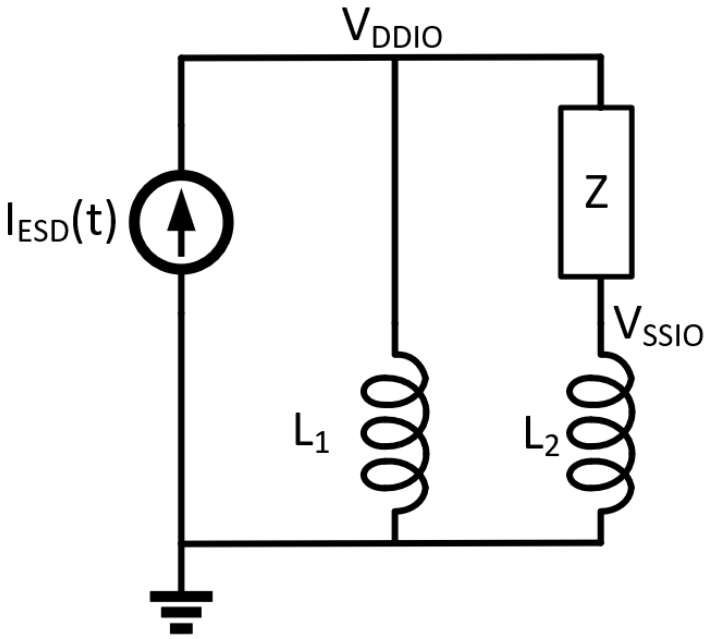


Figure 4.16: Simplified version of the circuit shown in Figure 3.4. $I_{ESD}(t)$ represents the ESD current injected into the IO pin and shunted to the power bus by the IO protection diode. L_1 represents the VDDIO bond-wire and L_2 is the VSSIO bond-wire. The APD and VSS bond-wire are not included in the schematic because significantly less current flows through the VSS bond-wires than the VSSIO bond-wires.

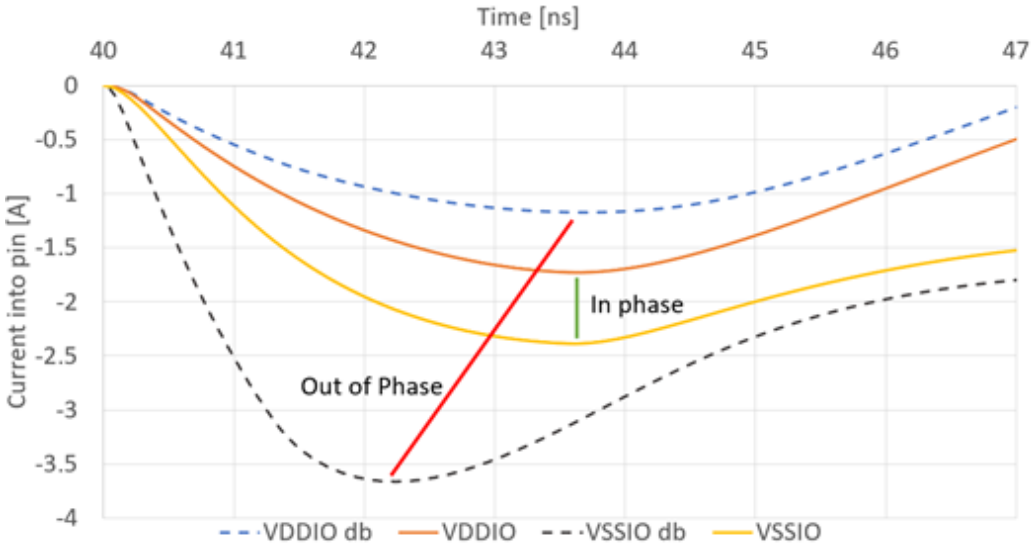


Figure 4.17: Current of a VDDIO pin and a VSSIO pin for both down-bonded (dashed) and non down-bonded (solid) simulations. Notice the phase shift of the two currents for each case.

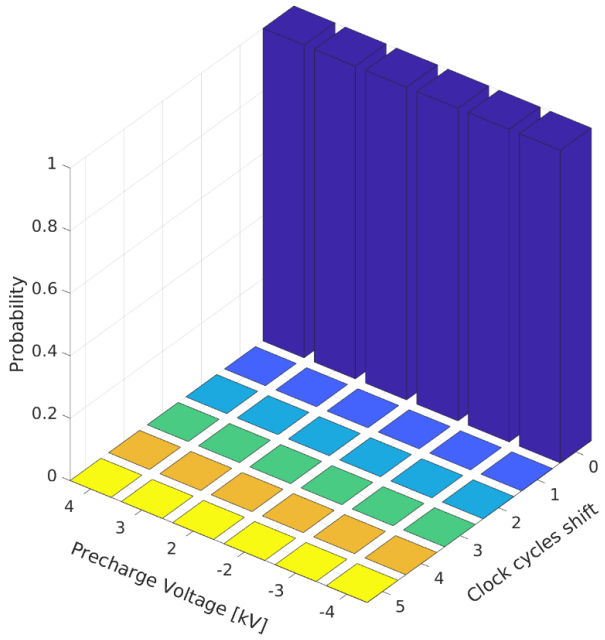


Figure 4.18: Down-bonded clock shift data for discharges to ZAPIO1. Aggregate data across three chips.

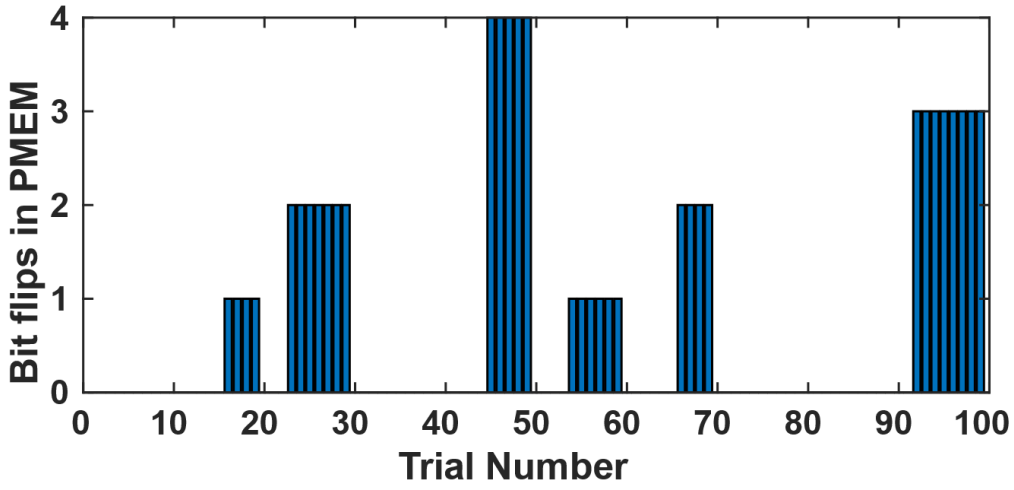


Figure 4.19: Positive 5 kV discharges onto ZAPIO2. The PMEM was reprogrammed every 10 trials. The bit flips in PMEM are retained until it is reprogrammed. The zaps were performed in increasing order of trial number.

CHAPTER 5

TRANSIENT LATCH-UP IN REVERSE BODY BIASED CORE CIRCUITRY

5.1 Latch-Up

The negative effects of system-level ESD, or powered ESD more generally, are not limited the soft failures described previously. Powered ESD may also trigger latch-up. Figure 5.1 shows a cross section of an inverter, including the parasitic devices. Figure 5.2 shows a schematic of the latch-up structure, a PNPN. Latch-up may be triggered by a voltage perturbation on one of the terminals of the parasitic PNPN [25] or by nearby current injection that affects the potential of the N-well and/or P-well that comprise the central regions of the structure [26], [27], [28], [29], [30]. If the holding voltage of the PNPN is less than the supply voltage [25], [31], latch-up will be sustained after the disturbance has subsided.

Previous latch-up studies [28], [29], [30] have looked at latch-up caused by an aggressor, usually an ESD protection device, that injects carriers into the substrate. These carriers can then be picked up by victim circuits, causing the parasitic PNPN to latch. Usual methods to avoid latch-up include increased aggressor to victim spacing, guard rings and isolated wells. However, as will be shown, even with these precautions, latch-up can occur due to an entirely different mechanism.

This work focuses on a latch-up phenomenon that was not detected by the standard JEDEC latch-up tests [32]. Instead, latch-up occurred during

power-on ESD (PESD) testing, which is used to assess a chip's resilience to system-level ESD. PESD testing was performed using a custom test procedure based on the IEC 61000-4-2 standard [4]. All the designs that suffered from latch-up use reverse body bias (RBB) in the digital core of the chip that was provided by a sponsor. These designs were production chips, and this work will focus on measurement data and design details for one of these chips [33]. When a circuit is in a low-power mode, a standby mode or exceeding its power budget, the application of RBB raises the magnitude of the transistors' threshold voltages, thereby reducing leakage current and power dissipation.

5.2 Reverse Body Bias

Reverse body bias is used to reduce the leakage of transistors by raising the magnitude of the threshold voltage, V_{TH}. This is done by raising the voltage of the bodies of PMOSFETs above their source potentials and/or decreasing body potential of NMOSFETs below that of their sources. While RBB can be used in chips with two power modes, normal and sleep, it can also be used in a more complex adaptive body bias scheme. Adaptive body bias is used to adjust the power consumption and performance of an IC such that all produced ICs meet power and performance specifications. In adaptive body biasing, body biasing will be enabled at all times. Figure 5.3 shows the difference between a normal biasing scheme and a body biasing scheme. The bodies of the transistors are separated from their sources and driven to different potentials. Here, the expectation is for increased latch-up immunity by adding a reverse bias across the base-emitter junctions of the latch-up structure, pulling the potential further away from the necessary 0.7 V (i.e.,

requiring more current injected into the substrate to forward bias the PN junctions). However, measurement shows that latch-up still occurs.

5.3 JEDEC Latch-Up Test

The JEDEC latch-up test [32] is designed to capture most latch-up vulnerabilities before products enter the field. Two tests, an I-test (current injection) and a supply over-voltage test are specified. In the I-test, both positive and negative polarity injections are performed, and a device passes the test if no latch-up was observed with injected current levels of up to 100 mA. Latch-up is observed by measuring supply current before and after the test event. Should the current increase by more than 10 mA (if the nominal supply current is less than 25 mA) or increase by a factor of more than 1.4 (if the nominal supply current is more than 25 mA), latch-up has occurred. A supply over-voltage test is performed by raising the supply voltage to 1.5 times the nominal supply voltage and observing for any latch-up phenomena. The current and voltages pulses are trapezoidal with the characteristics presented in Table 5.1 and Table 5.2. The pulse width can be up to one second long to allow enough time such that sufficient substrate current can be injected and collected to cause latch-up. Notice that the current injected via these tests is much less than the current levels seen for the IEC testing as described in Chapter 2.

5.4 Experiment

A commercial microcontroller was fabricated in a 90 nm CMOS technology. The floorplan is shown in Figure 5.4. The digital core is shown in teal. The

core MOSFETs have their bodies and sources connected to separate supply nets. The power management controller (PMC), in the bottom right, controls the power supply voltages and well bias voltages for the core. Figure 5.5 illustrates the basic design of the PMC. Except for the $V_{ss_{bulk}}$ net, which connects to the chip substrate and provides the NMOSFETs' body biases, all core supply nets are regulated by the PMC and are not bonded out from the chip. The chip has two modes of operation: low-power/standby mode, for which RBB is enabled, and normal mode, with no RBB. In low-power/standby mode, the control signal SC is high, VREG2 regulates $V_{dd_{nwell}}$ to a higher value than V_{dd}, which is regulated by VREG1. VREG3 regulates V_{ss_s} above $V_{ss_{bulk}}$. In normal mode, SC is low, $V_{dd_{nwell}} \cong V_{dd}$, and VREG3 is switched to set $V_{ss_s} \cong V_{ss_{bulk}}$. The chip uses the distributed ESD protection scheme described in [34], [35], i.e., dual-diode IO protection with distributed RC rail clamps (Figure 5.6). The rail clamp design uses an special floating bus for the ESD current which results in all the ESD current exiting the chip through the $V_{ss_{bulk}}$ net. This microcontroller passed all standard JEDEC latch-up tests [32], but it latched-up during PESD tests that were conducted while the chip was in the normal operation mode.

Contact PESD testing was performed using an IEC 61000-4-2 compliant ESD gun and test bed [24]. The microcontroller was mounted on a custom test board, similar to the one shown in Figure 5.7. A test board is used because the microcontroller product is integrated into a variety of customer systems. Only a subset of the IO pins was tested due to the time-consuming nature of the test. The set of test pins includes samples based on each of the following categories: (1) pad cell type; (2) pin function (including "special" pins, e.g., USB or reset); (3) pad placement (e.g., proximity to a corner, the PMC, an IO segment break, or a region where the chip core extends to the

IO region). Discharges were performed by placing the ESD gun tip onto the exposed chip pins located on the chip-side of the board. No on-board protection, e.g., TVS, was provided. Digital IO pins were configured in the tri-state mode and were alternatingly tied-off to board-level VDD or VSS using 10 kΩ resistors. Adequate decoupling capacitors (100 nF) were placed close to the chip, near each VDD supply pin.

ESD tests were performed while the microcontroller was running a program that performs basic read/write operations with the memory and that assesses the health of various sub-modules. Two blinking LEDs were used to indicate if the code was running properly or if certain types of resets or code exceptions had occurred. For each discharge to a pin that caused latch-up during testing, the lowest ESD level at which latch-up occurred is indicated in Figure 5.8, along with the value of the sustained current drawn from the chip's power supply following the conclusion of the ESD event. Subsequently, emission microscopy was used to identify the locations of the latched-on PNPNs. The arrows in Figure 5.4 identify the IO pins from which latch-up was triggered at ESD magnitudes below 6 kV; the lowest ESD level at which latch-up was observed is marked adjacent to the arrows. The locations of the latched-on PNPNs are circled in the figure, and the dashed lines show the mapping from the light emitting region to the IO pin that was zapped. The "X" in the IO ring denotes bonded VSS pads. The PMC is placed in the bottom right of the chip. The following was observed:

(A) Positive discharges cause latch-up to occur near the zapped pin.

(B) Negative discharges cause latch-up to occur far from the zapped pin.

(C) Negative discharges to pins nearby the PMC are more likely to cause latch-up than negative discharges to pins far from the PMC.

(D) Positive discharges to pins far from the PMC are more likely to cause latch-up than positive discharges to pins near the PMC.

(E) Positive discharges cause latch-up to occur at lower ESD voltages than do negative discharges.

It should be mentioned that a significant number of the tested IO pins saw latch-up resulting from -6 kV discharges (Figure 5.8); however, as emission microscopy was not performed for zaps over 6 kV, it is impossible to form a hypothesis on the root-cause of these latch-up events.

5.5 Analysis

PESD testing of IO pins injects current to the chip substrate, a known cause of latch-up [26]-[32]. However, the latch-up reported in Section 5.4 is not attributed to substrate current injection because best practices for well tap spacing and guard rings were followed, and, furthermore, the experimental findings are not consistent with that latch-up mechanism. In particular, observation B runs directly contrary to the expectations from substrate current injection. In addition, the pins where zaps resulted in latch-up, observations C and D, are unexpected results if substrate current was the cause. Instead, the latch-up susceptibility is a consequence of the core biasing scheme (Figure 5.5). The parasitic NPNs associated with each of the core NMOSFETs experience a base-emitter bias, V_{BE}, equal to $V_{ss_{bulk}} - V_{ss_s}$. If V_{BE} is sufficiently large (e.g., 0.7 V), the NPN turns on and may kickstart the latch-up process. Likewise, latch-up may occur if the V_{EB} applied to the PMOSFETs' parasitic PNPs is sufficiently large; V_{EB} is equal to the potential difference $V_{dd} - V_{dd_{nwell}}$.

During ESD stress, each core NMOSFET receives a regulated V_{ss_s} from the PMC and a $V_{ss_{bulk}}$ from the bonded VSS pads. The $V_{ss_{bulk}}$ distribution is determined by the ESD current flow from the zapped IO pad to the VSS pads via the resistive ground supply grid, which includes the ground bus in the IO ring. Voltage excursions are measured relative to the $V_{ss_{bulk}}$ potential at the PMC. The V_{ss_s} potential is assumed to be uniform throughout the chip even during ESD because the associated supply grid carries no significant ESD current. The physical separation between the PMC, which regulates V_{ss_s}, and the various points in the $V_{ss_{bulk}}$ grid allows there to be a significant voltage difference between V_{ss_s} and the local $V_{ss_{bulk}}$. In contrast, the V_{dd} and $V_{dd_{nwell}}$ nets are both regulated by the PMC; thus, ESD is not expected to induce a large voltage difference between V_{dd} and $V_{dd_{nwell}}$ at any core PMOSFET. Therefore, the following analysis focuses only on the NMOSFETs' source and body voltages, V_{ss_s} and $V_{ss_{bulk}}$, respectively. Additionally, the analysis primarily focuses on the case that the core is in its normal operation mode (no RBB).

The ESD current induces large potential gradients on the $V_{ss_{bulk}}$ net; ultimately, the current exits the chip via the ground pins. While this production chip's ESD design conduct all ESD current to the chip ground ($V_{ss_{bulk}}$ net), many designs split this current to both the $V_{ss_{bulk}}$ and V_{dd33} nets. Figure 3.4 shows one such design, where a portion of the postive ESD current is directed to a power net. However, in either case, ESD causes significant current to pass through the $V_{ss_{bulk}}$ net before exiting the chip. The following analysis is valid for both cases, however, the latch-up robustness for each design will differ.

Figure 5.9 shows a simplified model of the ground supply routing, which suffices for discussion purposes. The bus resistances, R_{bus_1} through R_{bus_7},

each represent the net resistance between two points in the PDN, which includes the core mesh and the bus in the IO ring and, where applicable, bond wire resistance to board ground. In the model, the V_{ss_s} net is represented as an equipotential. $I_{esd}(+)$ and $I_{esd}(-)$ represent a positive and a negative ESD current, respectively. Only one of those ESD current sources is active at a time; the other is set to zero. $I_{esd}(+)$ and $I_{esd}(-)$ are modeled as pulse current sources. For an IEC 61000-4-2 discharge, one may assume that the second current peak (which has a roughly 50-ns pulse width [34]) is the cause of the latch-up, and that assumption underlies the analyses in this work. The assumption arises from two observations. First, the duration of the first current peak is too short to cause latch-up [36], and second, in many systems, the first current peak is filtered.

The ESD current induced by a positive PESD to an IO pin will be shunted to the $V_{ss_{bulk}}$ net by the on-chip protection. Figure 5.9 shows a current, $I_{esd}(+)$, entering the $V_{ss_{bulk}}$ net at the node labeled with V_b. The $V_{ss_{bulk}}$ net is tethered to the board ground via multiple ground pins and a body diode at node a sees an induced voltage of

$$V_a = \frac{(R_{bus_1} + R_{bus_4}) \times R_{bus_2}}{(R_{bus_1} + R_{bus_2} + R_{bus_3} + R_{bus_4})} \times I_{esd}(+) \tag{5.1}$$

Since V_{ss_s} is referenced to V_1,

$$V_{ss_s} \cong V_1 = \frac{(R_{bus_2} + R_{bus_3}) \times R_{bus_1}}{R_{bus_1} + R_{bus_2} + R_{bus_3} + R_{bus_4}} \times I_{esd}(+) \tag{5.2}$$

Equation (5.1) assumes that $R_{bus_5} + R_{bus_6} + R_{bus_7} \gg R_{bus_1}$. From (5.1) and (5.2), one finds that the voltage difference between $V_{ss_{bulk}}$ and V_{ss_s} at node a

is

$$V_{BE} = \frac{R_{bus_4} \times R_{bus_2} - R_{bus_1} \times R_{bus_3}}{R_{bus_1} + R_{bus_2} + R_{bus_3} + R_{bus_4}} \times I_{esd}(+) \tag{5.3}$$

An analysis of (5.3) indicates that for positive discharges:

1. Zaps to pins located far from the PMC (large R_{bus_4}) are most likely to cause latch-up.

2. Logic circuits close to the zap pin (small R_{bus_3}) are most susceptible to latch-up.

3. Placing the PMC very close to one or more ground pins (small R_{bus_1}) will increase the latch-up susceptibility.

4. Logic located close to a ground pin (small R_{bus_2}) has a reduced latch-up susceptibility.

The first and second of those conclusions are supported by experimental observations D and A, respectively.

A negative PESD to an IO pin will direct a negative current, $I_{esd}(-)$, to the $V_{ss_{bulk}}$ net. The voltage difference between $V_{ss_{bulk}}$ and V_{ss_s} is largest near node d of Figure 5.9, and the corresponding forward bias on the body diodes, assuming that $R_{bus_2} + R_{bus_3} + R_{bus_4} \gg R_{bus_1}$, is

$$V_{BE} = \frac{R_{bus_1} \times R_{bus_6} - R_{bus_5} \times R_{bus_7}}{R_{bus_1} + R_{bus_5} + R_{bus_6} + R_{bus_7}} \times I_{esd}(-) \tag{5.4}$$

An analysis of (5.4) indicates that for negative discharges:

1. Zaps to pins located close to the PMC (small R_{bus_5}) are most likely to cause latch-up.

2. Logic circuits far from the zap pin are most likely to latch-up (large R_{bus_6}).

3. Placing the PMC very close to one or more ground pins improves the latch-up resilience (small R_{bus_1}).

4. Logic located close to a ground pin is more likely to latch-up (small R_{bus_7}).

The first and second of those conclusions are supported by experimental observations C and B, respectively.

5.5.1 Rail Clamp Design and Placement

In Figure 5.9, node a denotes the chip location at which the forward bias on the NMOS body diodes is largest, which is where latch-up will occur. The rail clamp design in the product chip tested shunts all the ESD current to the $V_{ss_{bulk}}$ net. This higher current flow in the ground net, for a given ESD discharge voltage, based on the analysis in this chapter, will result in a lower robustness compared to a design without a floating ESD bus design.

The topology of the on-chip protection network will also affect the location of node a and, therefore, the latch-up location. Notably, a distributed rail clamp scheme [34] and a non-distributed rail clamp scheme, with large spot clamps, provide different avenues of current injection into the $V_{ss_{bulk}}$ net for positive discharges.

A distributed rail clamp scheme places a rail clamp in every IO cell, such that relatively small spacing between each rail clamp is maintained. Figure 5.10(a) shows the placement of distributed rail clamps in a chip. This allows for smaller individual clamps compared with a non-distributed rail clamp scheme. It can be expected that all of the ESD current does not flow through a single rail clamp, rather, the ESD current is split among multiple clamps. On the other hand, for a non-distributed rail clamp scheme, rail

clamps will be placed more sparsely in the IO region. This results in a larger separation between each rail clamp, as shown in Figure 5.10(b), necessitating larger rail clamps as the increased net resistance from rail clamp to rail clamp results in a majority of the ESD current passing through a single clamp.

5.5.2 Non-Distributed Rail Clamp Latch-Up Analysis

For a distributed rail clamp design, the worst-case node a is located close to a zap IO pin that itself is far from any bonded VSS cells, while also being far from the PMC — this provides maximal R_{bus_2} and R_{bus_4}. The worst-case node a is located near the zap pin described above, because that placement minimizes R_{bus_3}. The distributed nature of the protection causes node a to be slightly offset from the pin, which will be addressed further in Section 5.6.

In contrast, for a non-distributed rail clamp design, the current does not enter the $V_{ss_{bulk}}$ net within the zapped IO cell, and the worst-case node a is located right next to the rail clamp — this minimizes R_{bus_3}. If all the rail clamps are equidistant from their nearest ground pins, then node a will be close to whichever rail clamp is farthest from the PMC and conducts significant ESD current. Otherwise, the relative distance of each rail clamp from the ground pins will also play a role. In a non-distributed design, the rail clamps are placed typically in either the VSS cells or the VDD cells, or in both. In the MCU design studied here, each VDD cell is adjacent to a bonded VSS cell, a usual practice for many commercial products. If that practice is followed in a design with non-distributed rail clamps, the positive ESD current will exit the chip close to the point at which it enters the $V_{ss_{bulk}}$ net, resulting in a small R_{bus_2} and a potentially high latch-up resilience. However, it must be acknowledged that a particular chip design may be assembled in

a variety of packages, some of which might not have enough pins to bond-out all VSS cells, causing some of the rail clamps to be located far from a bonded VSS cell. Additionally, more rail clamps may be needed than exist VSS cells, leading to an increased R_{bus_2} and a potentially increased latch-up susceptibility.

5.6 Simulation

5.6.1 Setup

A simulation test-bench, Figure 5.11, was constructed to confirm the analysis in Section 5.5. The test-bench provides a somewhat simplified representation of the product chip and is intended to be used to examine, qualitatively, the trends observed in measurement. The test-bench contains an RC model of the microcontroller's PDN, including the chip's core supply mesh and the supply buses in the IO ring. The supply routing within the core is non-uniform, therefore, approximations were made to limit the complexity of the model. Specifically, the core is represented by a 20 by 24 array of 100 μm $\times$100 μm squares. This results in a rectangular core, which, while not perfectly representing the shape of the core in the chip of Figure 5.4, provides a sufficiently good test case to validate the analysis. It should be noted that reducing the block size further results in equivalent results. While the resolution is increased, the results are qualitatively equivalent. Similarly, a simplified model of the PMC circuit is used, but care was taken to ensure that the response time of the control loop is roughly the same as in the complete design (on the order of 1 μs). Two types of ground straps connect the $V_{ss_{bulk}}$ mesh of the chip core to the $V_{ss_{bulk}}$ bus in the IO region. The first

type of strap uses wide, top-level (thick) metal to connect the core region directly to VSS pad cells; those straps are shown in grey. The second type uses thinner metal to connect the core region to the IO ground bus; those straps are shown in red. In the model, the $V_{ss_{bulk}}$ net along the core periphery is strapped to the IO region every 100 μm, which mimics the strap placement in the actual microcontroller.

The simulation test-bench includes the ESD devices, their routing, and their placement — all of which were matched to the actual chip. Standard process design kit (PDK) models were used for all devices, including the protection devices. Using special ESD compact models does not significantly change the simulated values of $V_{ss_{bulk}}$ and V_{ss_s} and therefore, they are not needed for latch-up simulation. IO cells are placed in the simulation test-bench as per the chip's design.

In order to model the current injected into the bases of the parasitic NPNs, an N+/P-well diode (i.e., a NMOSFET body diode) was placed between V_{ss_s} and $V_{ss_{bulk}}$ for each of the 480 core sub-blocks; the diode size roughly matches the cumulative size of the body diodes in the sub-block. A 50 ns current pulse with a 10 ns rise time was used as the stimulus for simulating the circuit's ESD response. As noted earlier, this current pulse emulates the second peak of an IEC discharge, and simulations using an IEC ESD gun model provide a similar prediction of the latch-up trigger level. The current pulse in the simulation is matched to the maximum of the IEC discharge's second peak. The pulse characteristics are such that the interconnect inductance has a negligible effect on the simulation results, which is why the PDN is represented by an RC model. The simulated currents within the core were sampled during the last 10 ns of the pulse, at which time the circuit is in a quasi-steady-state.

5.6.2 Results

Four simulations are presented:

1. Positive current injection far from the PMC.
2. Positive current injection near to the PMC.
3. Negative current injection far from the PMC.
4. Negative current injection near to the PMC.

The "far" location corresponds to a pin that caused latch-up at +3 kV in measurement and is marked with the arrow on the left side of the chip in Figure 5.4, while the "near" location corresponds to the location marked with the arrow on the bottom side of the chip. Current was stepped in 1.5 A increments until significant core current was observed or until a magnitude of 12 A was reached. The test setup used in this work produced a 1.5 $\frac{A}{kV}$ second peak [34], and 12 A corresponds to the 8 kV upper limit of the PESD testing.

Figure 5.12 shows the simulated result of a positive 4.5 A discharge (3 kV ESD gun stress equivalent) to a pin located far from the PMC, and Figure 5.13 shows the result for a positive 12 A discharge to a pin located close to the PMC. Figure 5.14 shows the result for a negative 12 A discharge to a pin far from the PMC, and Figure 5.15 shows the result for a negative 7.5 A discharge to a pin that is near to the PMC. In those plots, the X- and Y-axes denote the physical location within the core. The PMC is located at the lower right corner of the plots' X-Y planes and is marked by an orange asterisk. In each figure, a lightning bolt denotes the location of the current injection, and the bonded VSS pads are marked GND. The diode current is plotted in the vertical direction (Z-direction); notice the Z-axis scale differs

from plot to plot. The current that flows through an individual base-emitter diode is only a small fraction of the total ESD current, but it has been shown that mA-scale base current can be sufficient to trigger latch-up [36].

As shown in Figure 5.12, the core current resulting from a positive current injection far from the PMC is highest near the zapped pin. However, the largest core current is not found immediately adjacent to the zap pin. That finding is explained by referring to the example presented in Figure 5.16. As shown in the figure, in a distributed clamp design, multiple rail clamps each conduct part of the ESD current into the $V_{ss_{bulk}}$ net. In this example, the zap pin is close to one ground pin ($V_{ss_{bulk}}$ pin), so the current flow is rightward in the $V_{ss_{bulk}}$ net. Assume that a majority of the ESD current flows through the three clamps depicted. In this case, the potential at node z is $V_z = R \times I_{esd}$. It follows that $V_y > V_z$, and $V_x > V_y$.

In the example, even though node y is electrically closer to the discharge pin, node x is at a higher potential and thus larger core currents will be induced in the vicinity of x. However, as one moves progressively farther from the zap pin, e.g., to node w, the potential starts to decrease (i.e., $V_w < V_x$), In regions where there is little to no current injection to $V_{ss_{bulk}}$, the potential decreases as the distance to the injection point(s) increases (increasing R_{bus_3}). Figure 5.13 shows the results for a larger positive current injection than in Figure 5.12, but for a discharge point (zap pin) much closer to the PMC. A marked reduction in the induced core current is observed — notice that the current values plotted in Figure 5.13 are much less than 1 μA. Figure 5.13 confirms that a positive injection near to the PMC should not cause latch-up within the core.

In simulation, opposite trends are observed for negative discharges, as predicted by the analysis of Section 5.5. Specifically, as shown in Figure 5.14

and Figure 5.13, negative discharges to pins far from the PMC are unlikely to cause latch-up (note that the currents plotted in Figure 5.14 are less than 1 μA), while discharges to pins near the PMC can induce significant core currents, especially at locations far from the PMC. In Figure 5.15, the largest core current occurs at a spot adjacent to a VSS cell because that is where the voltage on the $V_{ss_{bulk}}$ net is highest. V_{ss_s} is pulled to $V_{ss_{bulk}}$ near the PMC, and $V_{ss_{bulk}}$ at locations far from the PMC may be significantly higher, creating a forward bias on the NMOSFET body diodes and producing the core currents plotted in Figure 5.15. These simulations predict higher latch-up robustness to negative discharges than to positive discharges, in accordance with experimental observation E.

All of the simulation results are qualitatively consistent with the data in Figure 5.4 and match the experimental observations. One can argue further that the quantitative agreement is good, in light of the 1 kV step size in measurement and the corresponding 1.5 A step size in simulation. The granularity of the data is such that the precise latch up trigger point is not identified in either measurement or simulation. Denote the ESD level at which latch up is observed as $V_{esd,fail}$; those values are shown in Figure 5.4. Denote the actual latch-up trigger level as V_f. V_f is related to $V_{esd,fail}$ by the inequality $|V_{esd,fail}| - 1kV < V_f < |V_{esd,fail}|$. A 1 kV uncertainty in the precise value of V_f corresponds to a 1.5 A uncertainty in the value of the ESD current needed to trigger latch up. The simulation results of Figure 5.12 and Figure 5.15 confirm that at current levels matched to the measured $V_{esd,fail}$, a significant current is induced in the core at locations near to where latch-up was observed.

5.6.3 Rail Clamp Proximity to Board Ground

A "toy example" is created to investigate designs with non-distributed rail clamps and, most importantly, confirm the earlier assertion (Section 5.5) that the rail clamp proximity to a grounded VSS cell strongly affects the latch-up robustness. This is not an important consideration for designs with distributed clamps because in those designs, there will always be some rail clamps that are not adjacent to ground pins. The simulation test-bench for the toy design maintains identical net resistances to those on the product chip used in this study. Rail clamps were placed adjacent to bonded VSS cells, which provide a path to ground. In simulation, positive PESD current is injected adjacent to the rail clamp farthest from the PMC to ensure a majority of the ESD current will flow through just one rail clamp — a worst-case scenario. The ESD level at which the maximum core current reaches roughly 1.25 mA (similar to the peak current value in Figure 5.12) is recorded; presumably, this provides a good estimate of the latch-up threshold for the toy chip. Next, the test-bench was modified such that the rail clamp that carries the ESD current is separated from the nearest bonded VSS cell by an IO cell, and the PESD simulation was repeated. Simulation indicates that this seemingly minor change to the chip floorplan worsens the latch-up threshold by about 30% (i.e., latch-up occurs at an injection level that is 0.7 times (7.5 A down from 10.5 A) that of the first case. These simulations confirm the analysis in Section 5.5.2. For completeness, negative PESD simulations are carried-out as well, and, as expected, the thresholds of the original and the slightly changed floorplan cases are identical. This is not surprising because ESD current from negative discharges enters the V_{ssbulk} net via the bottom diode and is not dependent on rail clamp location.

5.6.4 IO to Core Strapping

It is reasonable to consider whether the number and placement of the ground straps affect the latch-up susceptibility. The test-bench for the production chip is modified such that most of the thin straps are removed from the design. There remains only one thin strap at each corner of the chip, along with all of the original thick straps. An ESD simulation is subsequently performed under the same configuration as for Figure 5.12. The results are shown in Figure 5.17. The core current is observed to be highest near the (thick) ground strap closest to the zap point. Since there are few ground straps, the ESD current must travel significantly farther before it can enter the core. This results in a lower amplitude current passing through the core because the core to discharge location resistance — R_{bus_3} in (5.3) — has increased significantly.

On the other hand, for the "weakly strapped" test case, if a strap is added nearby the zap pin, the peak current into the core increases to 1.8 mA in simulation (Figure 5.18) for the same positive 4.5 A discharge. Compare this to the peak current of 1.25 mA in Figure 5.12, and it is concluded that, on balance, weak strapping increases latch-up susceptibility. This results from an increase in the resistance to ground — R_{bus_2} in (5.3) — for the design with the weakly strapped core. In addition, the increased resistance from "weak strapping" will negatively affect CDM robustness [37]. This come as a consequence of the increased bus resistance, once again, resulting in higher IR drops across the chip.

5.6.5 Enabled RBB

So far, this work has focused on the normal operation of a chip designed with a reverse body bias capability, for which V_{ss_s} is strongly pulled to $V_{ss_{bulk}}$ at the PMC. Reverse body bias is activated for the low power mode, which for this chip corresponds to the core being in sleep mode. To assess latch-up susceptibility when the RBB is activated, the PESD simulations are repeated with the RBB set to 0.3 V, which places the chip in sleep mode. The gates of the pass transistors inside the voltage regulators are controlled by a two-stage amplifier. The loop bandwidth of the system is roughly 120 kHz, resulting in a response time in excess of a microsecond. The control loop will not respond to an ESD disturbance of 50 ns. Since the core is in sleep mode, 480 2-nA current sources, spread across the core for a total of approximately 1 μA of current, were used to model the leakage current of the core. This leakage current is necessary for the regulator to raise V_{ss_s} above $V_{ss_{bulk}}$.

Table 5.3 compares the PESD levels at which latch-up occurs for normal operation and sleep mode. The latch-up thresholds are significantly higher when the chip is in sleep mode. The increase results from the necessity to overcome the additional -0.3 V applied across the body diodes. Since a chip must be latch-up robust in all its operating states, it is recommended to perform PESD testing with RBB disabled (normal operation mode) if limited resources impede a thorough characterization of the chip in all of its operation modes.

5.7 Increasing Design Robustness

The analysis in Section 5.5 shows that latch-up robustness to negative discharges is roughly inversely proportional to R_{bus_1}, of which a significant por-

tion comes from the packaging. The analysis is valid regardless of packaging type, e.g. BGA and QFN. Table 5.4 lists the negative ESD current needed to cause latch-up for two different values of the package resistance. Those ESD current values were obtained by assuming that latch-up occurs when the core current reaches roughly 180 μA, but the relative increase of the latch-up threshold with decreasing package resistance is insensitive to the assumed value of the core current. For negative discharges, a reduction in the package resistance increases the latch-up robustness. In contrast, the package resistance has a negligible effect on the robustness against positive discharges because, in that case, the on-chip net resistance dominates the resistance to ground. Given that a reduced package resistance will improve latch-up resilience to only negative ESD and that the latch-up threshold is lower for positive ESD, reducing the package resistance may not be a worthwhile avenue to pursue because the overall latch-up susceptibility of an IC will not be decreased.

5.7.1 Split the Voltage Regulator

One method to increase latch-up resiliency is to split the pass transistor of the V_{ss_s} voltage regulator. For example, as illustrated in Figure 5.19, the one large pass transistor may be broken into four quarter-size devices, each placed in a different corner of the die and connected to a bonded-out VSS cell. In the actual design, the (one large) pass transistor is placed in the PMC block.

The design of Figure 5.19 was simulated; the simulation setup ensures that proper biasing of the four pass transistors is maintained during PESD. This should not pose a problem during normal operation of the microcontroller.

During normal operation, the pass transistors' gates will be tied high, and it can be expected that there will be, at most, low millivolt scale voltage gradients across any supply net. This will not be enough to endanger the normal operation of the core. In low power mode, with RBB enabled, there will be no voltage gradients across the chip's core supplies as micro-amps to nano-amps of current will be consumed. The slow response time of the control logic and the high gate impedance should ensure that the voltage seen at the gate of each pass transistor will be identical. Issues, however, may arise in attempting to maintain proper operation during power surges, e.g., ESD events. Each pass transistor will have a different V_{gs} based on their physical locations if enough current is flowing through the chip's ground net. If the pass transistors do not have the same impedance to system ground, some may temporarily turn off. This will result in a change in voltage seen on the core transistors, which may then result in timing violations, and in the worst cases, corruption of data or hangs.

The modified simulation test bench ensured proper operation of the pass transistors, even during ESD events, by including bonded ground pads near each pass transistor. Table 5.5 summarizes the results; there is a significant increase in latch-up robustness for both positive and negative discharges if a split pass transistor design is implemented. That finding is expected based on the observations made in Section 5.5, specifically, the observation (1) for positive discharges, and observations (1) and (2) for negative discharges.

5.7.2 Add Current Shunting Diodes

A second method to increase latch-up robustness is to insert ESD diodes from $V_{ss_{bulk}}$ to V_{ss_s}. For a given ESD current level, those diodes will reduce the

forward bias on the core body diodes, thereby reducing the current that enters the core. To examine the prospective efficacy of this solution in simulation, a diode was inserted into the IO ring roughly every 100 μm (for a total of 88 inserted diodes). Figure 5.20 shows the ESD current levels necessary to induce the same peak core current seen in the "no diode" cases (Figure 5.12 and Figure 5.15) as a function of diode perimeter. A diode with a perimeter of at least 50 μm provides significant improvement in latch-up robustness for both positive and negative discharges.

An examination of the simulation results reveals that it is the clamping diodes located closest to where the core current takes on its peak value that provide most of the benefit. Therefore, one may achieve a similar effect at a lower area cost by inserting diodes non-uniformly into the pad ring, guided by circuit simulation. Figure 5.21 shows the core current given a positive 5 A current injection after the placement of three diodes, near the location of the core current peak, each with a perimeter of 20 μm. Compare this result with that shown in Figure 5.12 for a 4.5 A current injection to a design without the current shunting diodes. One can conclude that inserting just three diodes would increase the latch-up robustness of this product chip. However, the analysis of Figure 5.20 needs to be repeated for all pins that may cause latch-up. If the chip has latch-up susceptibility in widely spaced regions, multiple sets of diodes may need to be inserted, reducing the area savings.

5.7.3 RBB via Charge Pumps

Thus far, the analysis has focused on designs that apply RBB to the core NMOSFETs by regulating their source potentials. An alternative method to generate a reverse body bias is to pull the bodies of the NMOSFETs

below 0 V using a charge pump circuit [38]. In bulk Si, that approach requires the use of junction-isolated p-wells, i.e., triple well technology. The latch-up susceptibility is a strong function of the triple well implementation; merged triple well structures have been shown to contain latch-up hazards [39]. Figure 5.22 shows a cross section of a merged triple well structure including the parasitic PNPN. A complete analysis of designs that use the alternative method for applying RBB would require the physical hardware and thus is outside the scope of this work. However, a preliminary analysis suggests that depending on the design specifics, latch-up can be induced during PESD.

Analysis predicts a latch-up scenario opposite to that in Section 5.5, where the analysis based observations for positive discharges now apply to negative discharges and visa-versa. Figure 5.23 presents a schematic of the PMC and bus network in the case of a charge pump based RBB design. VREG refers to the charge pump which regulates the body net. Here current is injected into the chip ground, to which the sources of the NMOSFETs are tied and from which the body net is regulated. The following can be gleaned from a similar analysis as performed in Section 5.5.

For positive zaps, assuming that $R_{bus_2} + R_{bus_3} + R_{bus_4} \gg R_{bus_1}$,

$$V_{BE} = \frac{R_{bus_1} \times R_{bus_6} - R_{bus_5} \times R_{bus_7}}{R_{bus_1} + R_{bus_5} + R_{bus_6} + R_{bus_7}} \times I_{esd}(+) \tag{5.5}$$

Following from Equation 5.5:

1. Zaps to pins located close to the PMC (small R_{bus_5}) are most likely to cause latch-up.

2. Logic circuits far from the zap pin are most likely to latch-up (large R_{bus_6}).

3. Placing the PMC very close to one or more ground pins improves the latch-up resilience (small R_{bus_1}).

4. Logic located close to a ground pin is more likely to latch-up (small R_{bus_7}).

For negative zaps, assuming that $R_{bus_5} + R_{bus_6} + R_{bus_7} \gg R_{bus_1}$,

$$V_{BE} = \frac{R_{bus_4} \times R_{bus_2} - R_{bus_1} \times R_{bus_3}}{R_{bus_1} + R_{bus_2} + R_{bus_3} + R_{bus_4}} \times I_{esd}(-) \tag{5.6}$$

Following from Equation 5.6:

1. Zaps to pins located far from the PMC (large R_{bus_4}) are most likely to cause latch-up.

2. Logic circuits close to the zap pin (small R_{bus_3}) are most susceptible to latch-up.

3. Placing the PMC very close to one or more ground pins (small R_{bus_1}) will increase the latch-up susceptibility.

4. Logic located close to a ground pin (small R_{bus_2}) has a reduced latch-up susceptibility.

In order for current to flow through the NMOS body diode, a closed current loop (i.e., Kirchoff's current law — KCL) must exist. Thus, current must flow through VREG, the charge pump, in Figure 5.23. However, charge pump based designs do not need to drive large currents as the bodies of MOSFETs are high impedance. Typically, charge pumps are designed to drive less than 10 μA of current [38], [40], [41], a value much too low to initiate latch-up. However, RBB may not always be enabled, thus requiring a pass transistor to

tie the body of the MOSFET to its source. In this case, this pass transistor may be large enough for milliamp scale current to pass through it, thereby resulting in a latch-up hazard.

The parasitic capacitance between the deep N-well and isolated P-well will also provide a path for current to flow through the NMOS body diodes. This capacitance may be large enough for milliamp scale current to flow through it during an ESD event. In this case, a charge pump based RBB design will be more latch-up susceptible than the preceding analysis may suggest. Figure 5.24, Figure 5.25, and Figure 5.26 present three different schemes for power delivery along with the ESD current path for a positive discharge: (a) externally regulated core voltage, (b) internally regulated core voltage, (c) internally regulated core voltage with a floating ESD bus which prevents ESD current from entering or exiting via the V_{dd33} net, respectively. Each of these designs will have a different amount of differential noise between the V_{dd} and V_{ss_s} voltages. This differential noise will determine the $\frac{dV}{dt}$ across the parasitic capacitance, $C_{parasitic}$, and therefore, in part, the current that will flow through that capacitance.

The parasitic capacitance per unit area between the deep N-well and isolated P-well in a 130 nm production PDK is roughly $1\frac{fF}{\mu m^2}$. For a 1 mm^2 core, with 50% of the core area taken by isolated P-well, this results in around 500 pF of parasitic capacitance. Simulations were performed to assess if that quantity of parasitic capacitance per unit area would be sufficient for latch-up to occur. Simulations were performed using a nearly identical simulation test bench to the one described in Section 5.6.1. The pass transistor in the PMC was disabled such that no current flowed through it. The capacitance ($C_{parasitic}$) between V_{dd} and $V_{ss_{bulk}}$ (the regulated net for this scenario) was varied. When $C_{parasitic}$ reached a value of $0.5\frac{fF}{um^2}$, milliamp scale current was

induced in the body diodes within the core; a threshold for latch-up to likely occur.

5.8 Figures and Tables

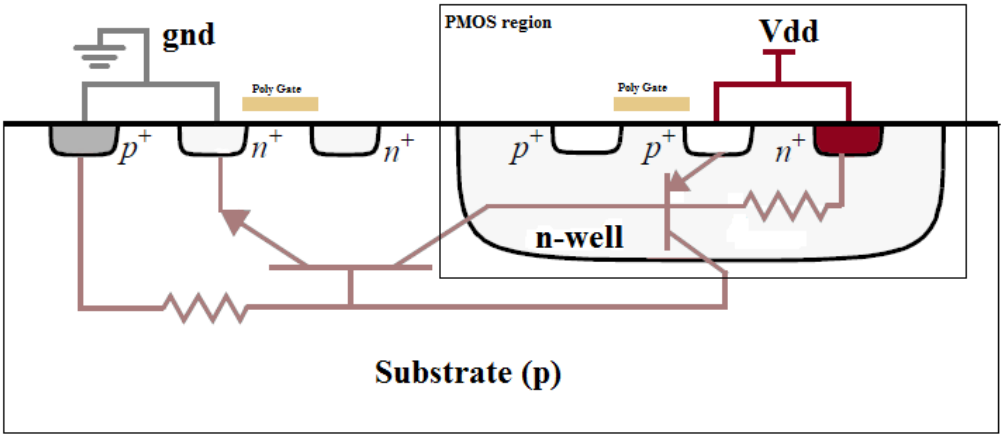


Figure 5.1: Cross section of a CMOS inverter. The parasitic PNPN structure is shown. Figure courtesy of Wikipedia.

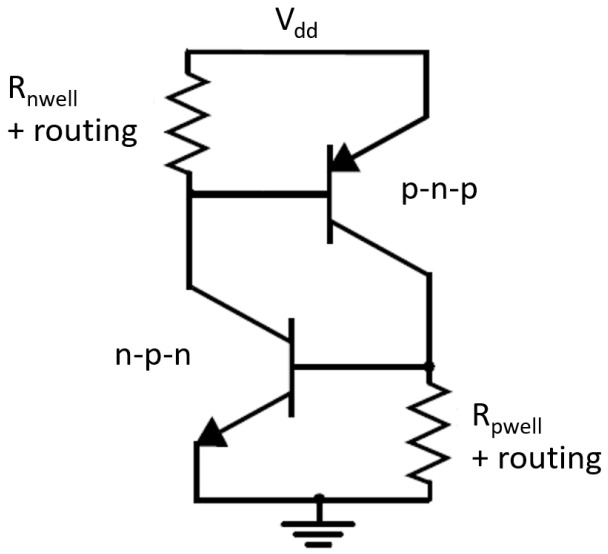


Figure 5.2: Standard latch-up structure. If the resistance between the base and emitter regions of the BJTs is large enough, current injected into the bases can cause large enough voltage differences to forward bias the base-emitter junctions and potentially initiate latch-up.

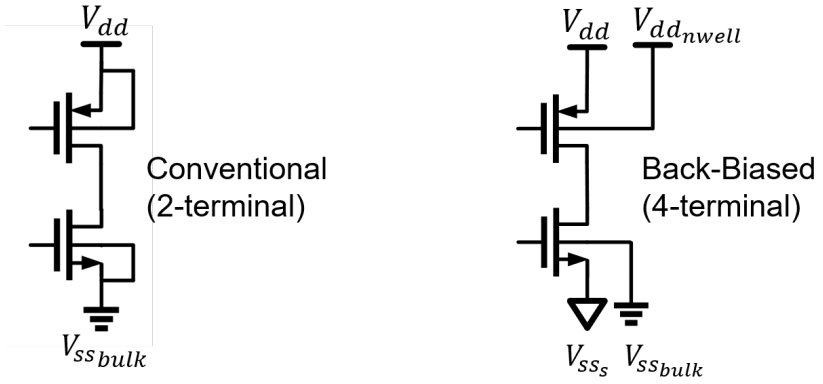


Figure 5.3: Conventional biasing of an inverter is shown on the left. There is one power and one ground with the bodies of the devices connected to the appropriate potentials. On the right is a body bias scheme. There are two powers and two grounds. This separation of nets allows for larger voltage differences to develop during an ESD event.

Table 5.1: Current injection waveform parameters for the JEDEC latch-up standard [32]. Waveform pertains to both positive and negative discharges and current injection levels should reach at least 100 mA unless the resulting voltage would be over the designed hard failure specifications of a given chip.

Symbol	Parameter	Limits	
		MIN	MAX
t_r	Rise Time	1 μs	5 ms
t_{width}	Pulse Duration	$2 \times t_r$	1 s
t_f	Fall Time	1 μs	5 ms

Table 5.2: Supply voltage pulse waveform parameters for the JEDEC latch-up standard [32]. The voltage pulse should increase the supply voltage by 50% that of the nominal supply voltage.

Symbol	Parameter	Limits	
		MIN	MAX
t_r	Rise Time	5 μs	100 ms
t_{width}	Pulse Duration	$2 \times t_r$	1 ms
t_f	Fall Time	5 μs	100 ms

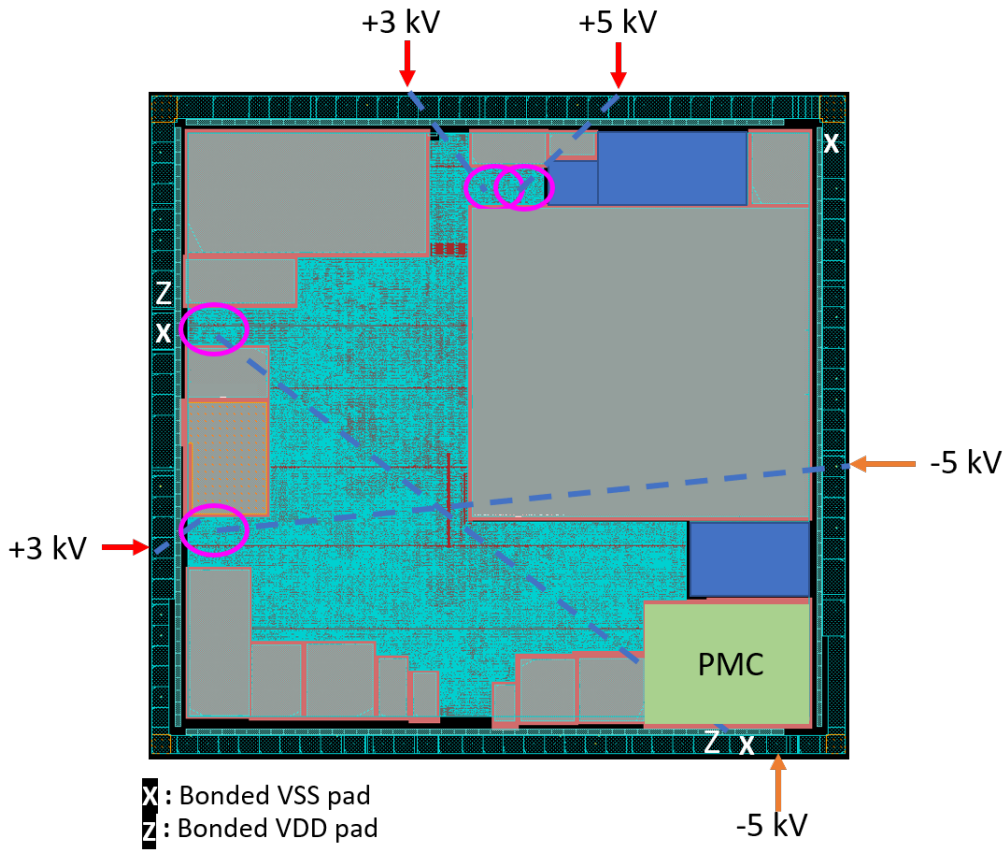


Figure 5.4: Measured latch-up in a RBB chip. Latch-up location was determined by using an infrared (IR) camera. Chip floorplan including locations where ESD discharges caused latch-up within the core. Circled locations denote observed latch-up locations within the CMOS core. The tested IO pad locations are indicated by arrows labeled with the zap level at which latch-up occurred. The dashed lines link the latch-up locations to the corresponding IO pad. The "X" in the IO ring denotes bonded VSS pads. The "Z" denotes the bonded VDD pads. Positive discharges cause latch-up with lower precharge voltage and close to the discharge location.

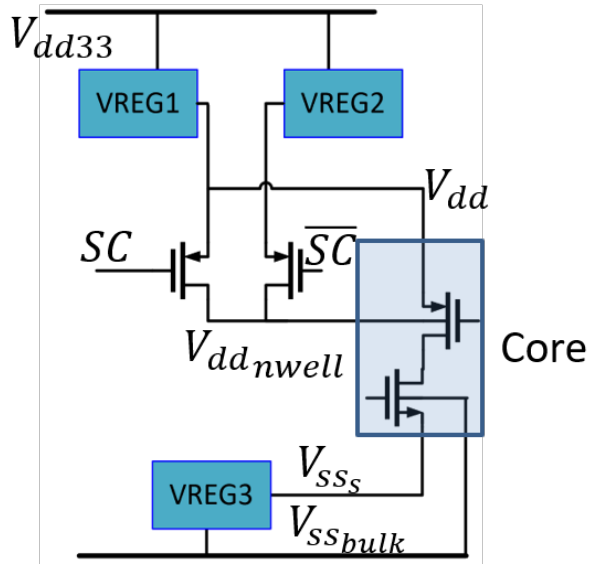


Figure 5.5: Block diagram of biasing scheme used for the RBB core. During normal operation, V_{SS_S} is tied to $V_{SS_{bulk}}$ and V_{dd} is tied to $V_{dd_{nwell}}$. $SC = 0$ for normal operation and $SC = 1$ for low power/standby.

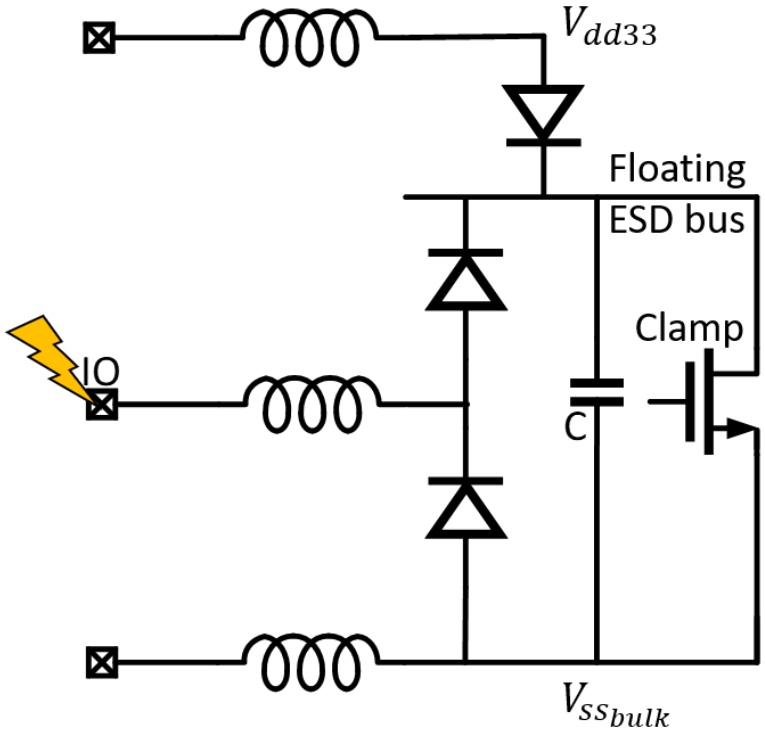


Figure 5.6: Schematic of the ESD network. Positive ESD current entering an IO pin is directed to a floating ESD bus which is then clamped to the $V_{ss_{bulk}}$ net. This results in all of the ESD current exiting the chip via ground.

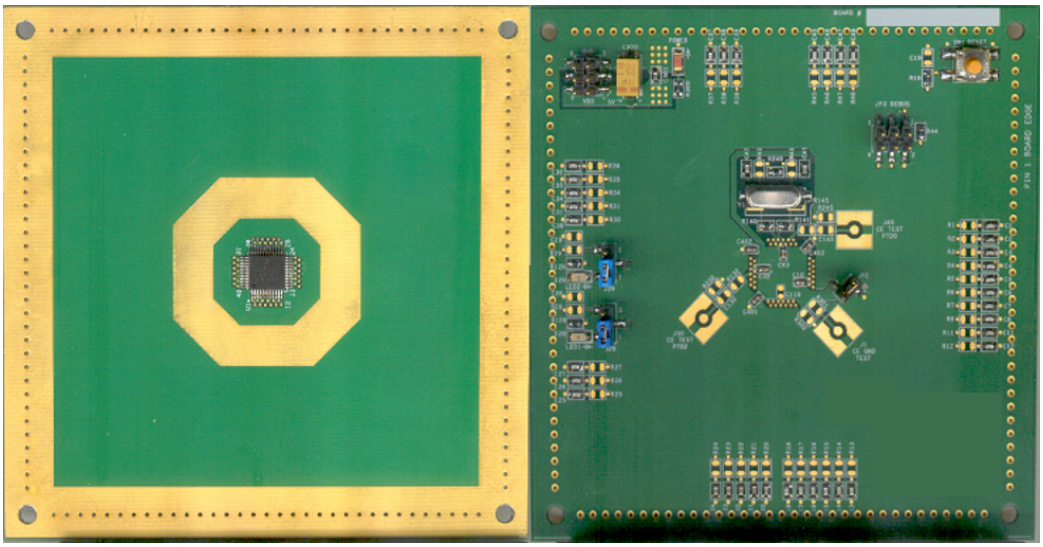


Figure 5.7: Sample of a custom test board used for powered-on ESD testing. Both sides are shown. The microcontroller chip can be seen on the left, all other peripheral components on the right. Testing is performed by placing the ESD gun directly on the chip pins.

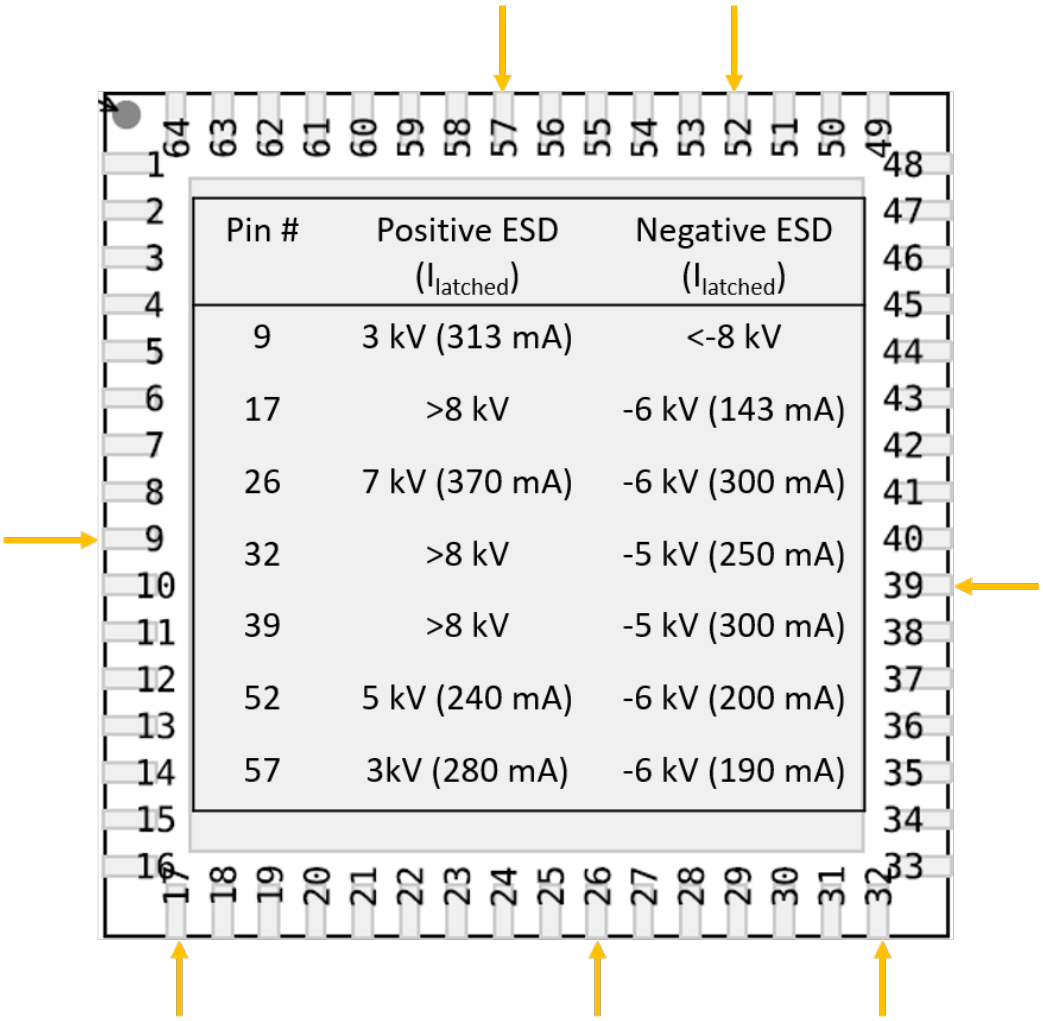


Figure 5.8: Arrows indicate the pins where discharges were observed to cause latch-up during PESD testing at levels up to 8 kV. The corresponding latch-up current for each pin is listed on the figure. Nominal supply current is roughly 30 mA.

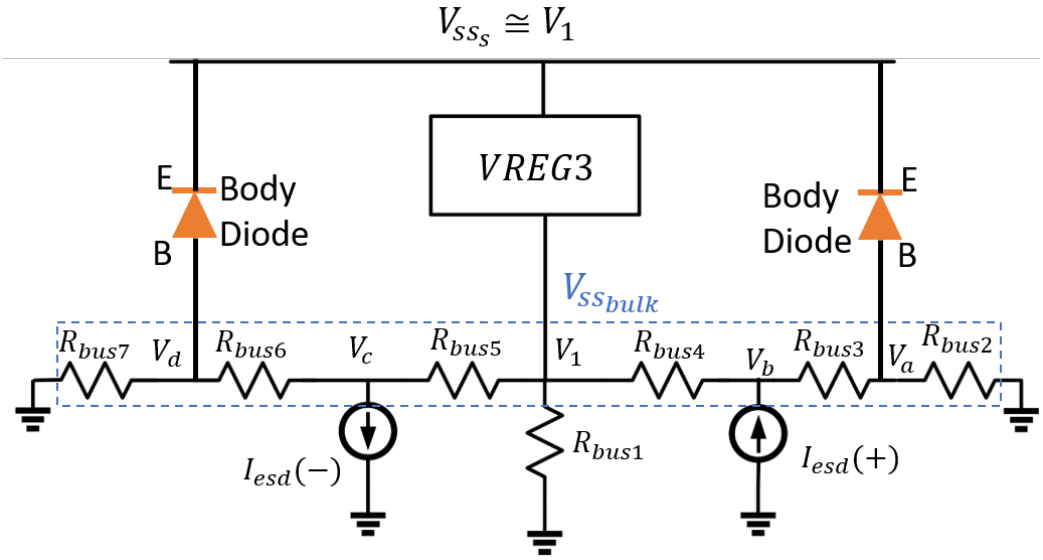
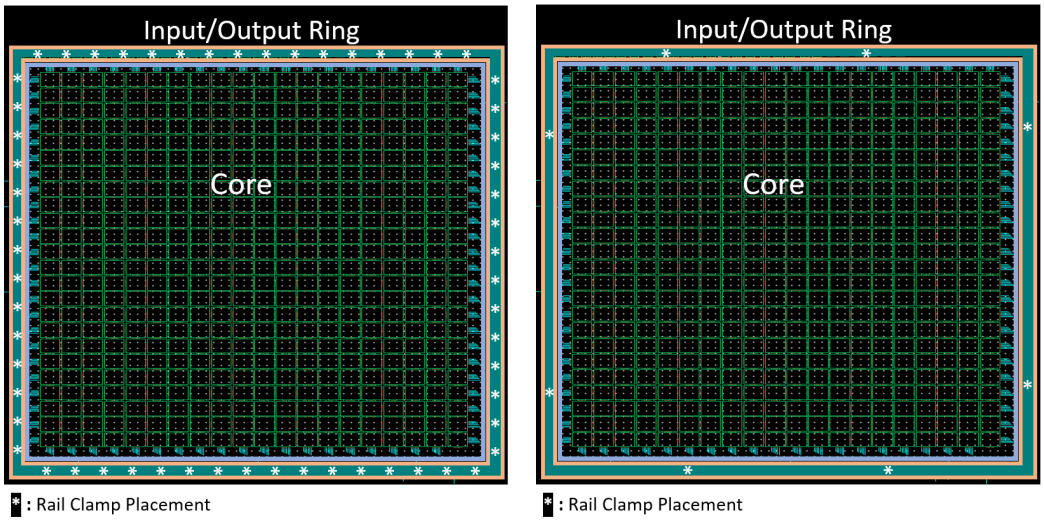


Figure 5.9: Resistive model of the V_{ss_s} and $V_{ss_{bulk}}$ nets. V_{ss_s} is approximately equal to V_1 when the voltage regulator ($VREG3$) is configured as a pass through device (normal operation). NMOSFET body diodes are depicted in orange.



(a) (b)

Figure 5.10: Chip layouts highlighting the rail clamp placement in (a) a distributed rail clamp design, and (b) a non-distributed design. The smaller spacing of each rail clamp in a distributed rail clamp scheme allows for smaller clamps compared to a non-distributed rail clamp design given equivalent ESD specifications. As a distributed rail clamp is in each IO cell, ESD current during a positive zap will flow to the $V_{ss_{bulk}}$ net at the zapped IO. In contrast, for the non-distributed rail clamp, the same current will flow into the $V_{ss_{bulk}}$ net relatively far from the zapped IO, where the closest rail clamp was placed.

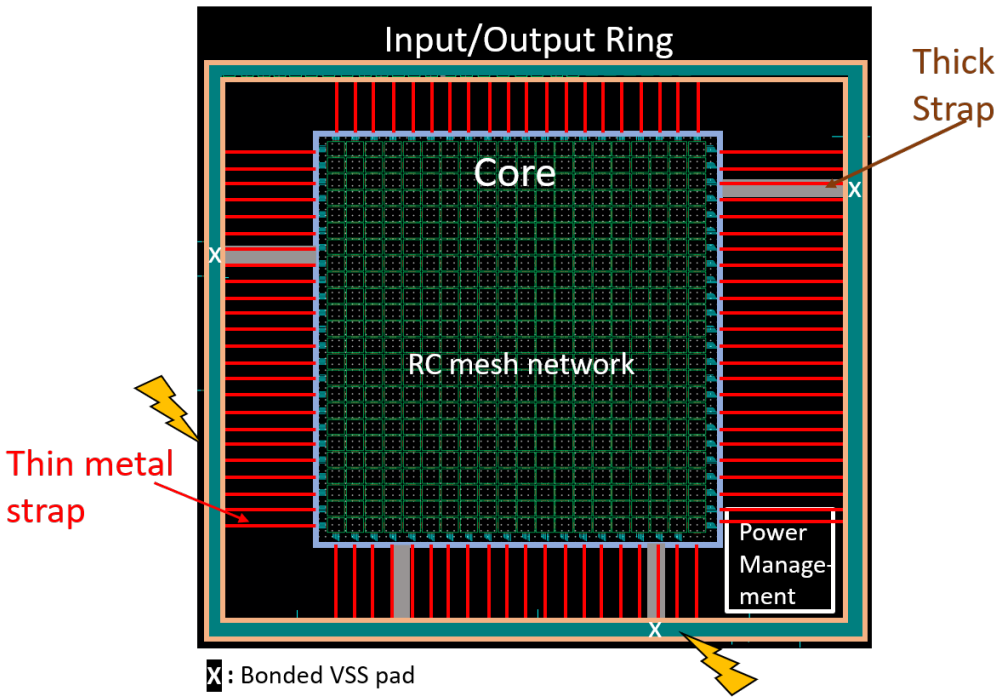


Figure 5.11: Simulation test-bench including the chip core, IO ring, power management and routing. All straps shown are $V_{ss_{bulk}}$ connections. The zapped IO locations are indicated by lightning bolts. The core is broken up into 100 μm by 100 μm squares where the decoupling and parasitic capacitances and PDN resistances are lumped. Four, fixed, ground straps (grey) are shown connecting the core to the $V_{ss_{bulk}}$ IO cells. The straps shown in red are additional straps added wherever possible to create a more robust ground network for the core. Bottom right of the figure shows the power management unit. Note, that in reality, the PMC is placed within the core, which is not a perfect rectangle.

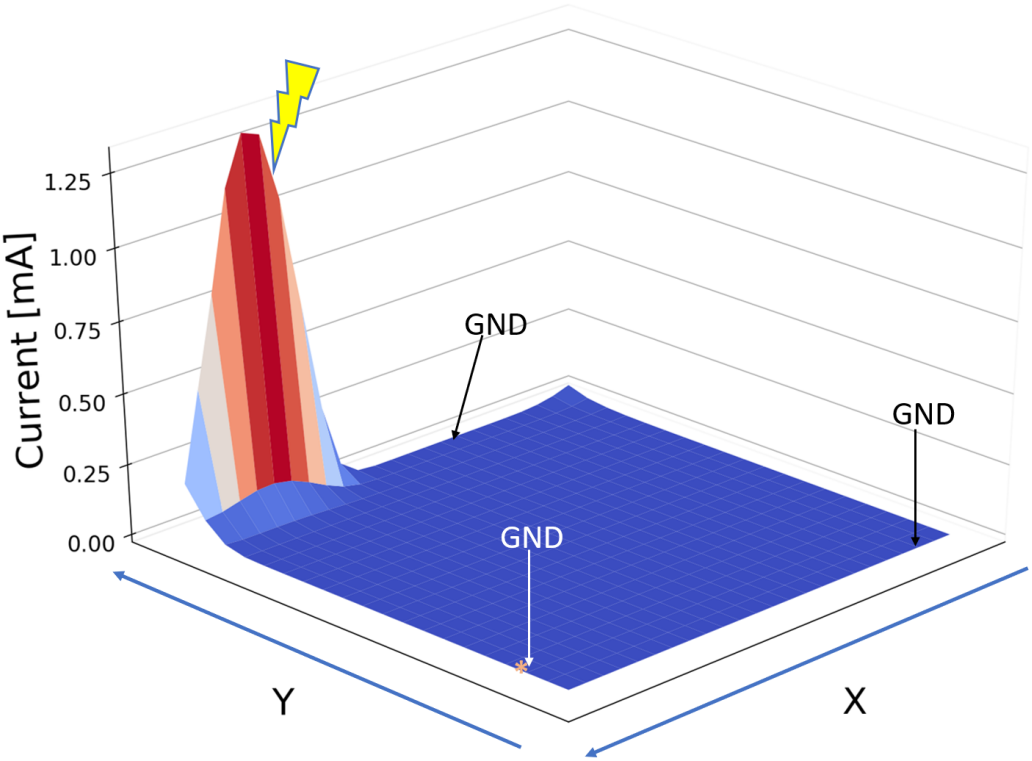


Figure 5.12: Plot of the voltage seen in a RBB core every 100 μm. A positive, 4.5 A, 50 ns current injection, to an IC pin far from the PMC, was used as the stimulus. Ground straps were placed every 100 μm around the periphery of the core. Notice the peak current is in the milliamps and adjacent to the zapped pin.

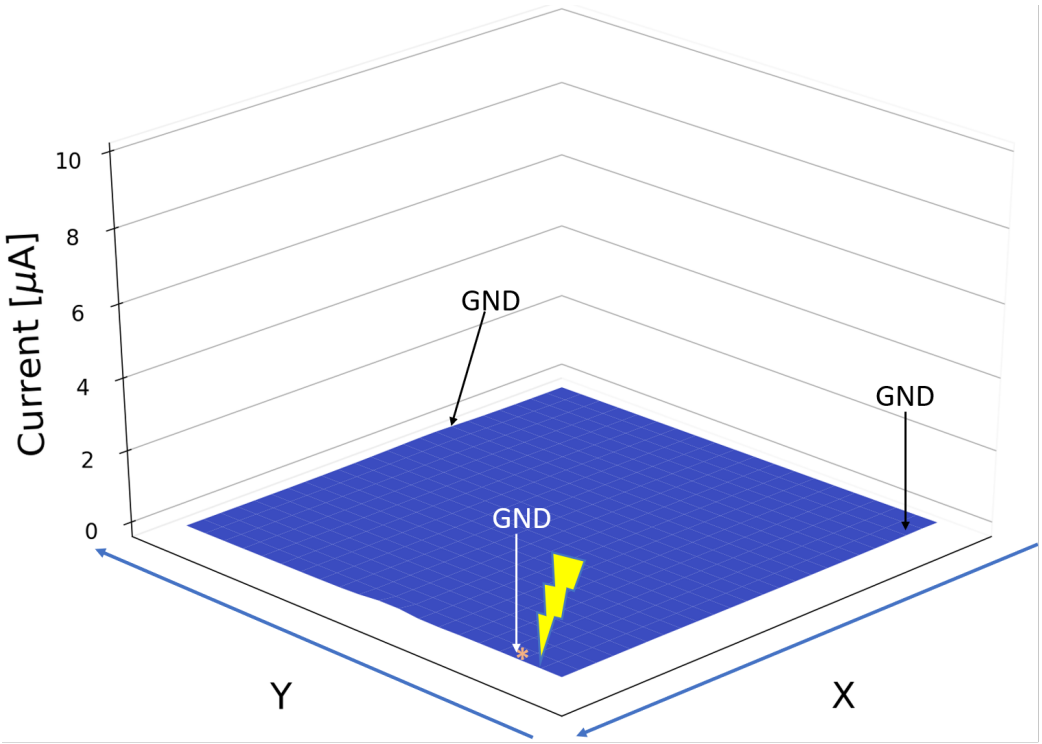


Figure 5.13: Plot of the voltage seen in a RBB core every 100 μm. A positive 12 A, 50 ns, current injection, to an IC pin near to the PMC, was used as the stimulus. Ground straps were placed every 100 μm around the periphery of the core. Less than 1 μA of current is seen within the core.

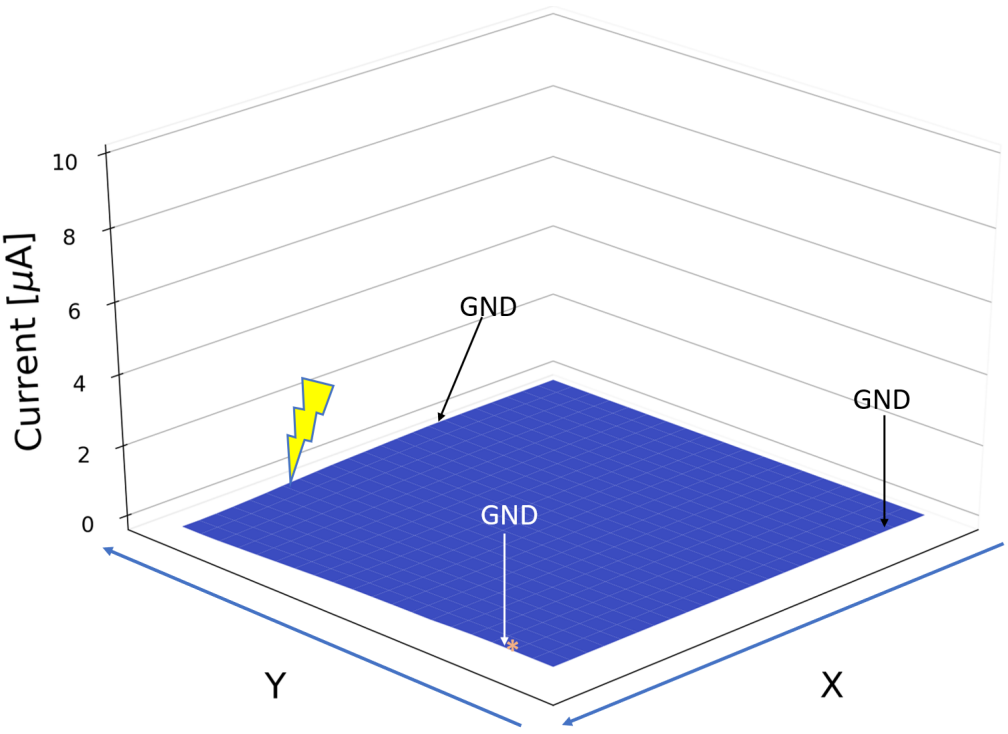


Figure 5.14: Plot of the voltage seen in a RBB core every 100 μm. A negative 12 A, 50 ns, current injection, to an IC pin far from the PMC, was used as the stimulus. Ground straps were placed every 100 μm around the periphery of the core. Less than 1 μA of current is seen within the core.

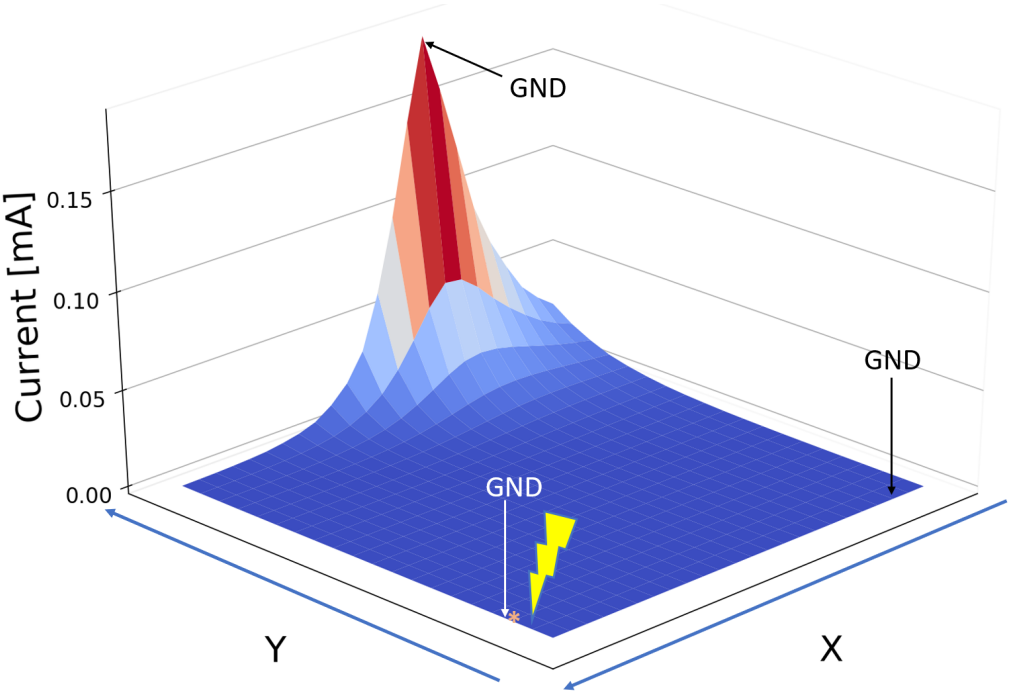


Figure 5.15: Plot of the voltage seen in a RBB core every 100 μm. A negative 7.5 A, 50 ns, current injection, to an IC pin near to the PMC, was used as the stimulus. Ground straps were placed every 100 μm around the periphery of the core. Peak current is observed far from the discharge location and near to a ground pin.

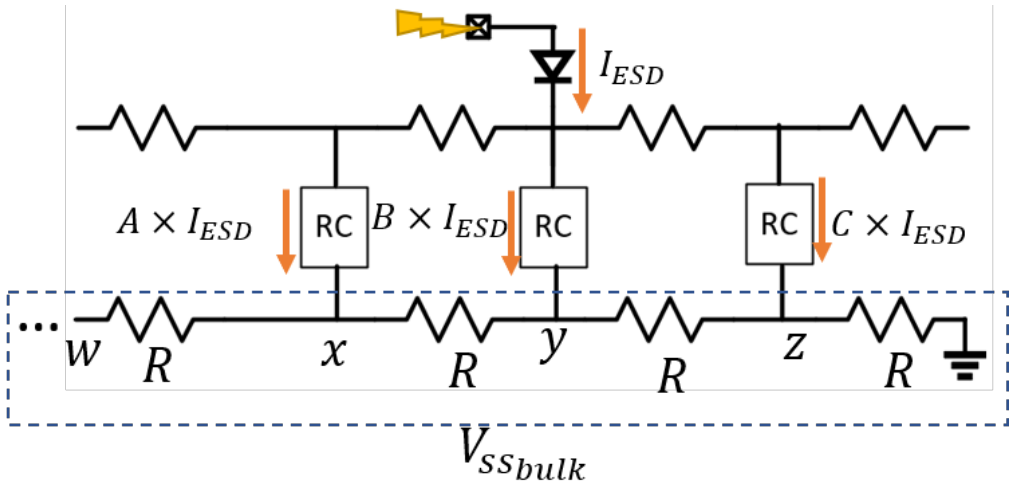


Figure 5.16: ESD current splitting across multiple rail clamps (RC) in a distributed rail clamp scheme. A, B, and C are fractions less than 1. The sum of A, B, and C is less than or equal to 1 such that the total current through the shown rail clamps is less than or equal to the injected ESD current. The lightning bolt represents the discharge location.

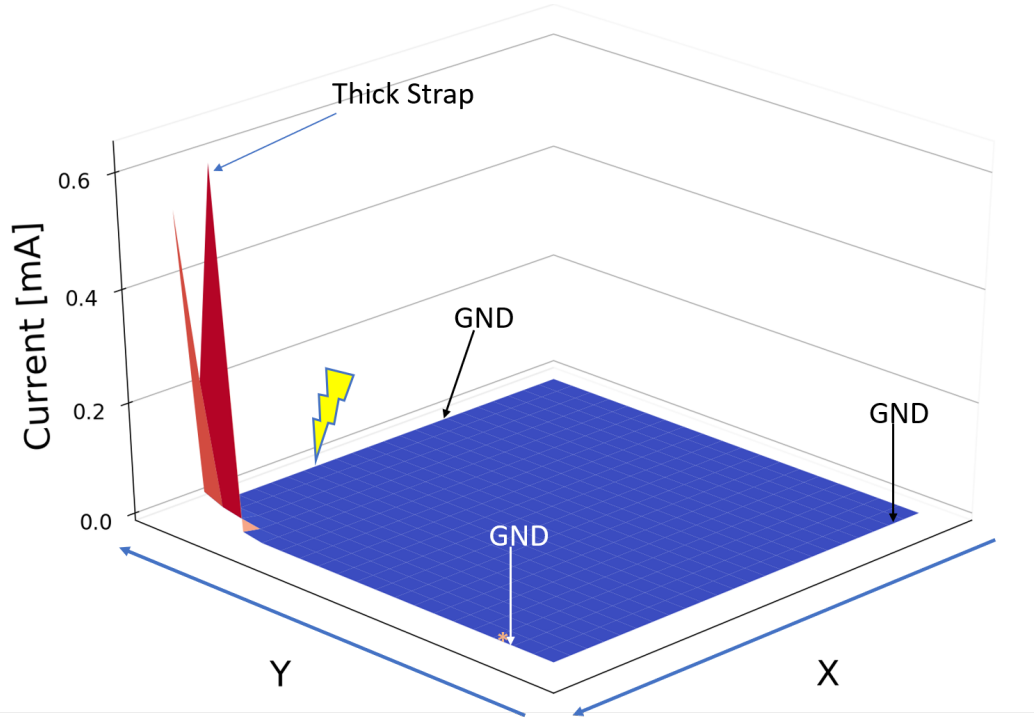


Figure 5.17: Plot of the voltage seen in a RBB core every 100 μm. A positive 4.5 A, 50 ns, current injection, to an IC pin far from the PMC, was used as the stimulus. Ground straps were placed at each of the four corners of the chip in addition to the thick straps. Notice the shift in location of peak current relative to Figure 5.12.

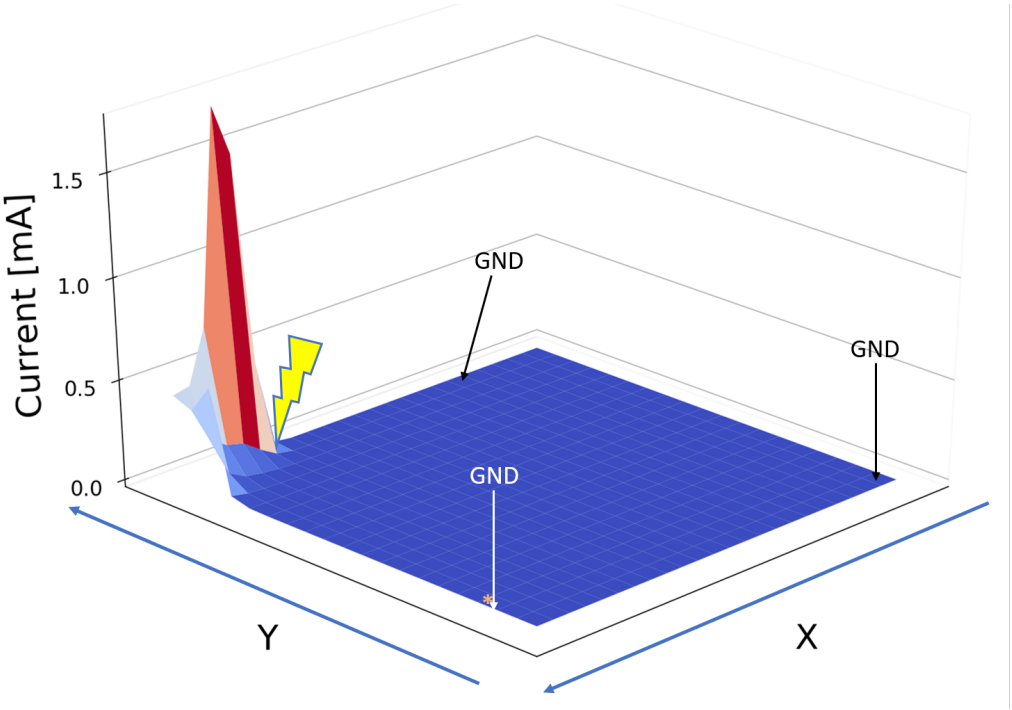


Figure 5.18: Plot of the voltage seen in a RBB core every 100 μm. A positive 4.5 A, 50 ns, current injection, to an IC pin far from the PMC, was used as the stimulus. Ground straps were placed at each of the four corners of the chip in addition to the thick straps. A strap was placed adjacent to the discharge location. Notice the higher peak current relative to Figure 5.12.

Table 5.3: Simulation data. Latch-up threshold both with RBB disabled and with RBB enabled. When RBB is enabled, the latch-up thresholds increase for both positive and negative discharges. Testing should be performed for the worst-case scenario, which is when RBB is disabled.

Current Polarity	RBB Disabled	RBB Enabled
Positive	4.5 A	7.5 A
Negative	-7.5 A	<-12 A

Table 5.4: ESD current necessary to cause latch-up given various package resistances (simulation) for ground connections. Package resistance refers to the resistance from the chip bond pad to board ground.

Package Resistance	90 mΩ	10 mΩ
ESD current to latch-up	-7.5 A	<-12 A

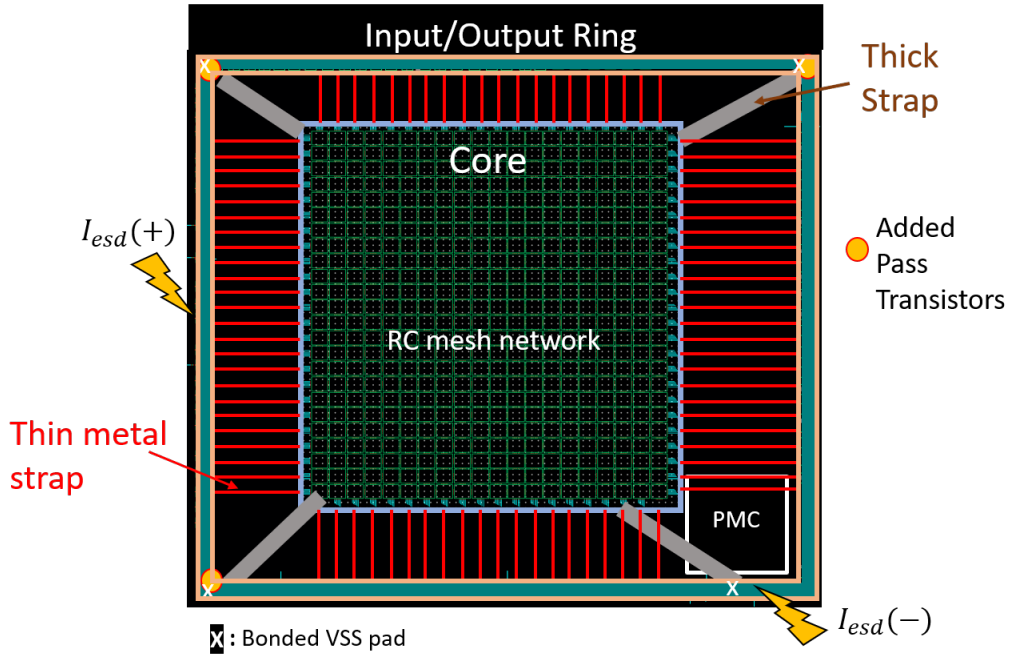


Figure 5.19: Test-bench schematic for splitting the pass transistor. The red and yellow circles mark the locations of the additional pass transistors. Discharge locations are marked with a lightning bolt and the polarity.

Table 5.5: Simulation data. Latch-up thresholds of the original design and a design with split pass transistors.

Current Polarity	Base Design	4 Pass Transistor Design
Positive	4.5 A	7.5 A
Negative	-7.5 A	<-12 A

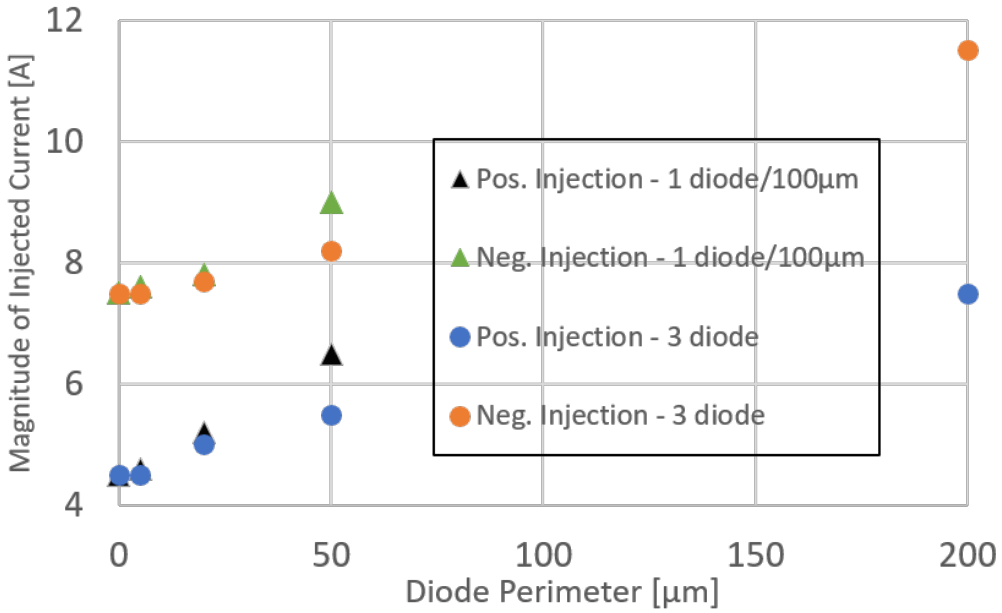


Figure 5.20: Simulated current injection levels necessary to match the values seen in Figure 5.12 and Figure 5.15, given clamping diode of various sizes. Triangle markers: a diode is placed every 100 μm. Circle markers: three diodes in total are inserted near to the peak core current. Positive current injection is in blue/black and negative in orange/green.

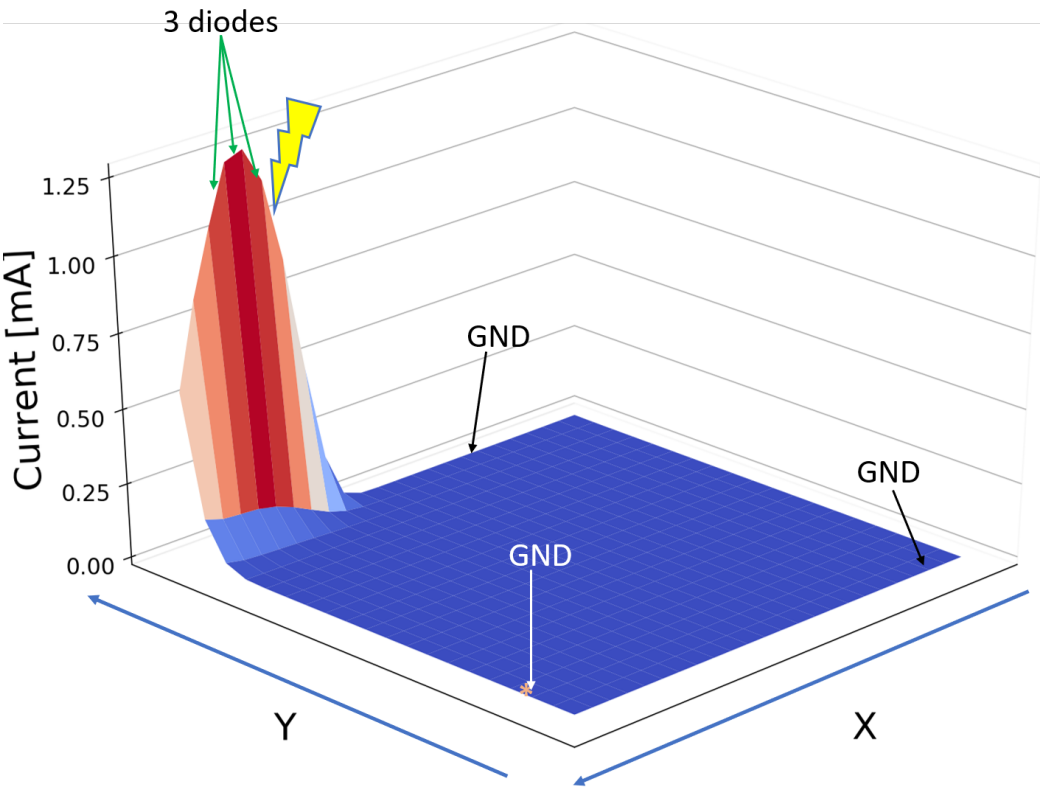


Figure 5.21: Simulation of a positive 5 A discharge. Green arrows indicate the placement of the three inserted diodes.

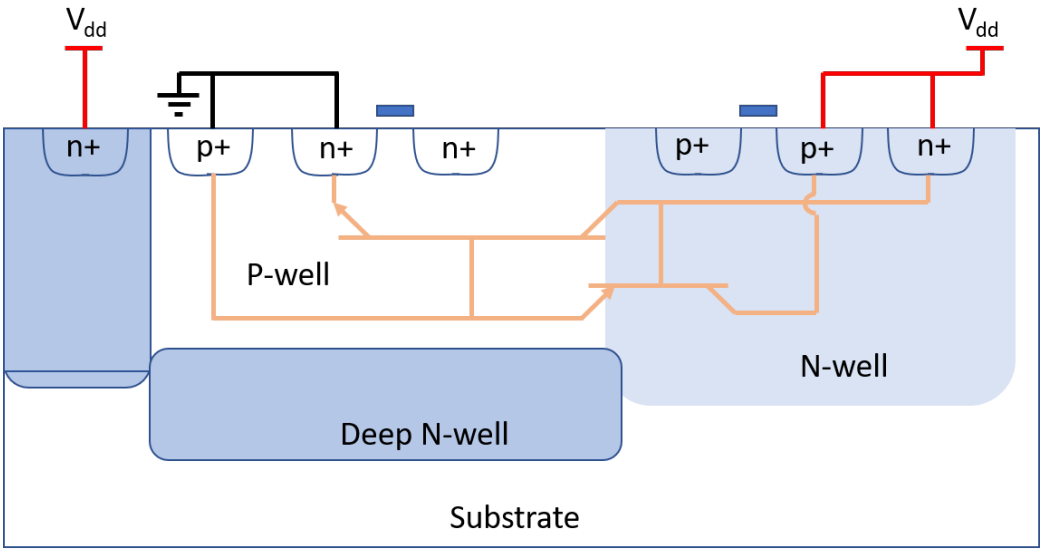


Figure 5.22: Cross-section of a CMOS inverter in a merged triple well layout. Observe the parasitic PNPN that is formed.

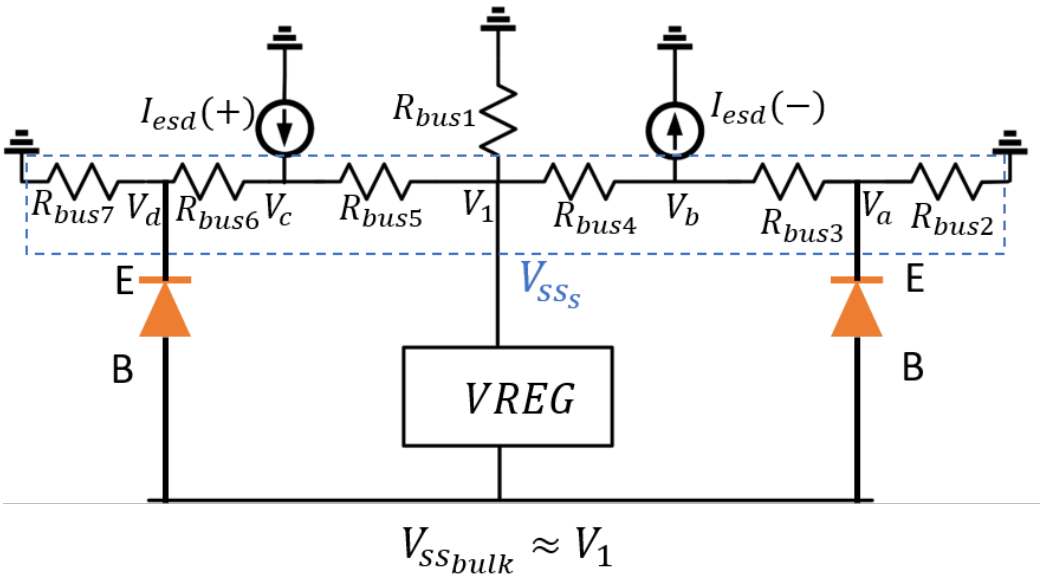


Figure 5.23: Resistive model of the V_{ss_s} and $V_{ss_{bulk}}$ nets. $V_{ss_{bulk}}$ is approximately equal to V_1 when the voltage regulator ($VREG$) is configured as a pass through device (normal operation). NMOSFET body diodes are depicted in orange.

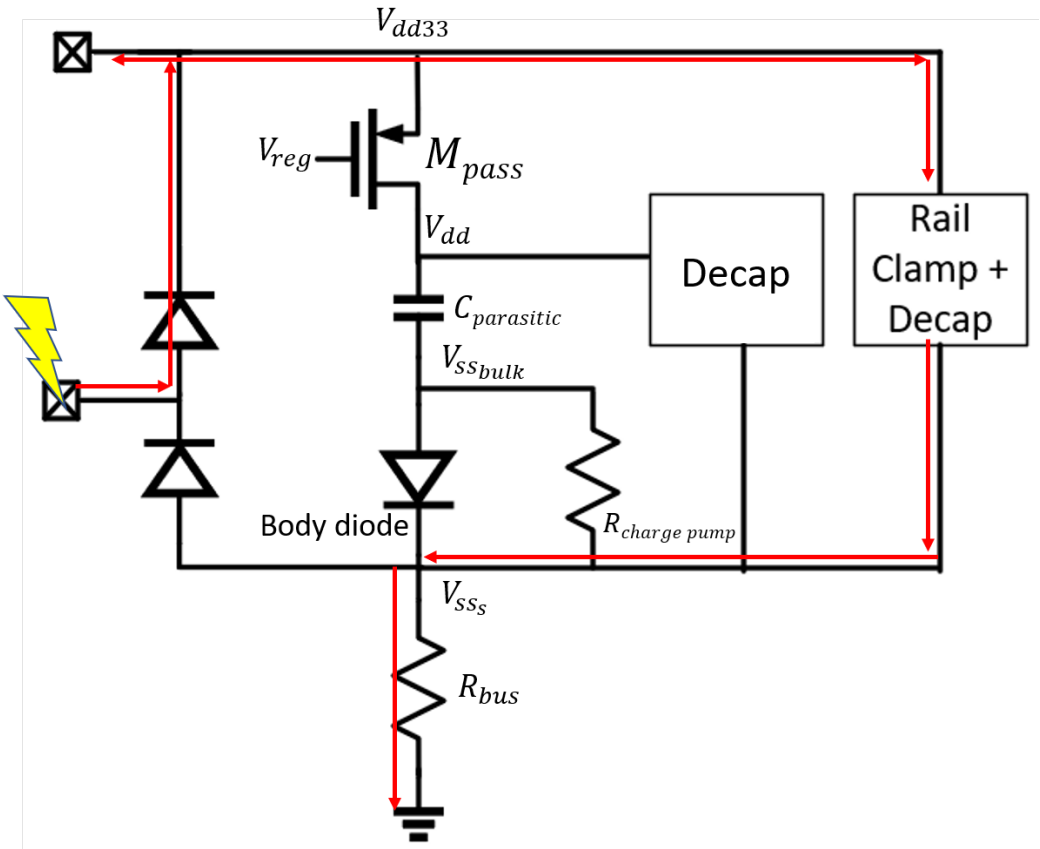


Figure 5.24: Simplified schematics of ESD and power delivery design. The core V_{dd} is driven internally by a regulator connected to the V_{dd33} net. The positive ESD current flows into the V_{dd33} net resulting in a $\frac{dV}{dt}$. This $\frac{dV}{dt}$ is attenuated by M_{pass} resulting in a smaller $\frac{dV}{dt}$ on V_{dd}.

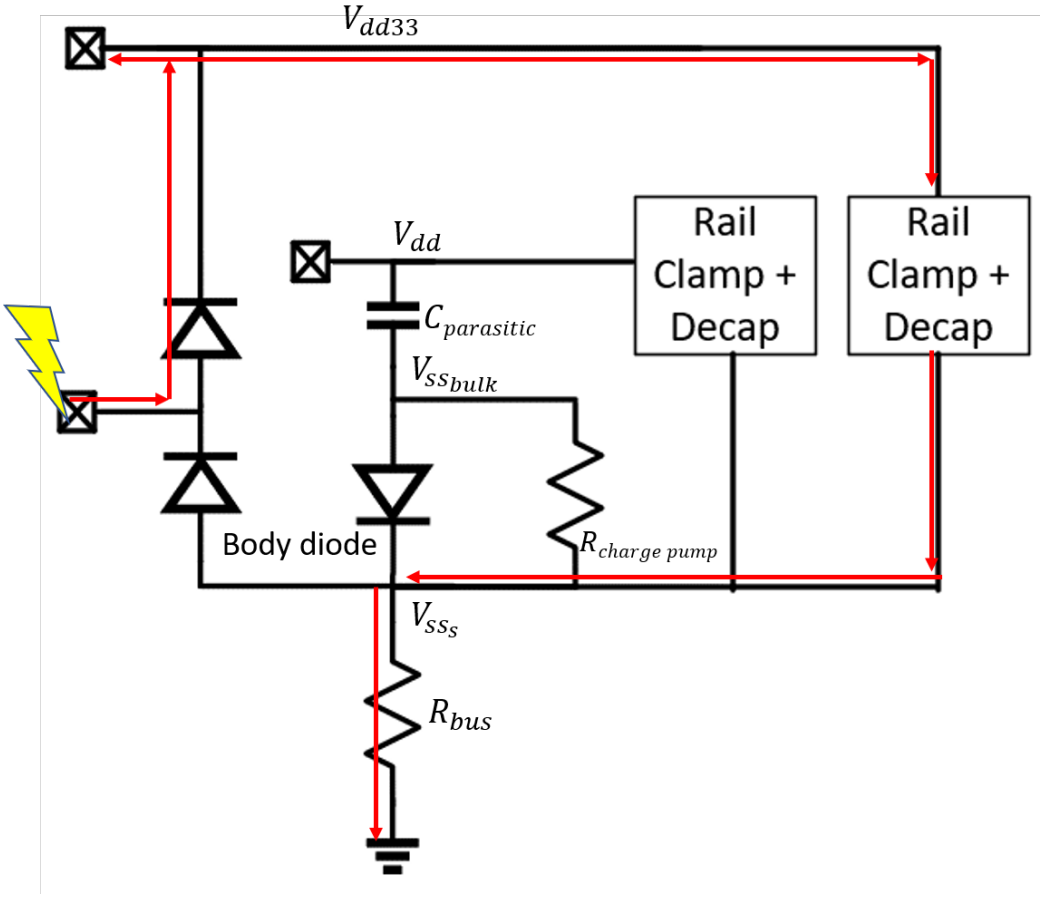


Figure 5.25: Simplified schematics of ESD and power delivery design. V_{dd} is regulated off chip.

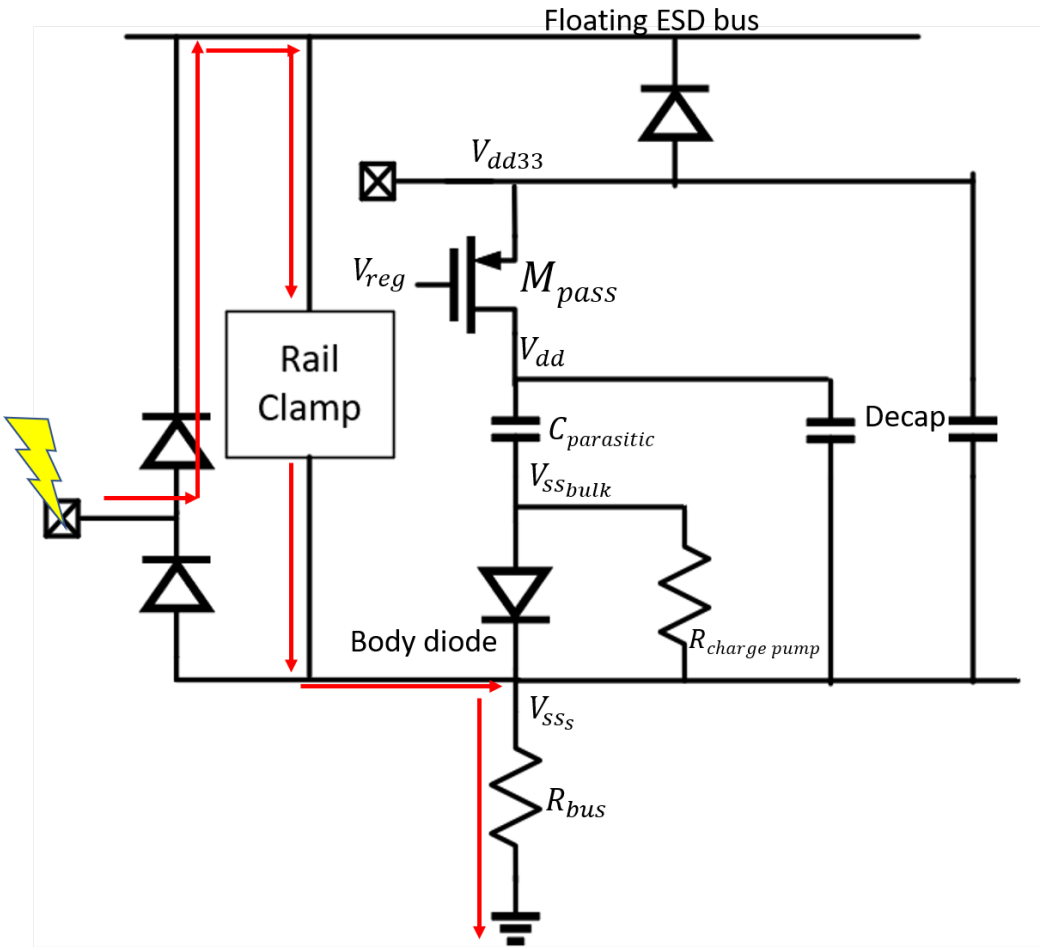


Figure 5.26: Simplified schematics of ESD and power delivery design. A floating ESD bus is used to prevent ESD current from entering the V_{dd33} which in turn eliminates any $\frac{dV}{dt}$ on the V_{dd} net as well.

CHAPTER 6

CONCLUSION

In Chapter 3, a system for testing for soft failures was presented, designed to allow significant diagnostic capabilities, including a scan chain, supply voltage monitors, and noise monitors. In addition, the use of a fully operational microcontroller provides a sufficiently complex system for a larger variety of ESD induced soft failures to manifest.

In Chapter 4, soft failures were categorized and analyzed for two different packaging solutions, not down-bonded and down-bonded chips. The on-chip supply noise monitor circuits recorded that positive discharge events resulted in larger under-voltages than negative discharge events. Soft failures were observed in both registers and SRAM, however, it was noted that a majority of bit flips in the registers could be attributed to glitches on the reset signal. The combined use of SPICE and EM simulation allowed for further investigation and confirmation of the reset glitches. Down-bonding was found to significantly decrease differential noise on the un-zapped supply domain on the chip while resulting in little change for the zapped supply domain.

In Chapter 5, a cause of latch-up that stems from a chip design's support for reverse body bias was described. Separate drivers are used to bias the sources and bodies of core NMOSFETs, and the electrical separation between those drivers increased the chip's latch-up susceptibility. This latch-up phenomenon may not be detected during standard latch-up testing; however,

it can be triggered during system-level ESD testing due to the higher incident current. Any body-biasing scheme runs the risk of increasing latch-up susceptibility. However, this work focuses on a chip with RBB generated by tying an NMOSFET's body to chip ground and elevating its source potential.

The latch-up susceptibility is affected, significantly, by the on-chip bus resistances and package resistance. For the chip studied in this chapter, positive discharges to IO pins far from both the PMC and bonded ground pins are most likely to trigger latch-up. This latch-up will occur close to the zap pin. On the other hand, negative discharges to pins near to the PMC will result in latch-up far from the zap pin and near to a bonded ground pin. For non-distributed rail clamp designs, an increased distance from a rail clamp to the nearest grounded VSS cell will significantly negatively impact latch-up immunity.

Splitting of the pass transistor which regulates the core NMOSFETs' source potentials with respect to chip ground, $V_{ss_{bulk}}$, can increase latch-up robustness. Inserting diodes between $V_{ss_{bulk}}$ and V_{ss_s} can also improve the latch-up robustness. Circuit simulation is demonstrated to correctly identify the latch-up susceptible portions of the design and can be used to optimize the design for latch-up robustness and area minimization.

However, the simulations presented in this dissertation include several simplifications that reduce the accuracy of the modeling. Care must be taken to accurately model the PDN, and ideally, core shape should be maintained to further improve accuracy. The core supply network in the real product chip was highly asymmetric, and the regularization of the supply network for simulation results in a loss in accuracy. Rather than the full PNPN latch-up structure, NMOS body diodes were used, which does not provide for any time dependencies in latching-up. Furthermore, diode sizes were estimated

to match the sizes of the parasitic devices within the core, however, lack of measurement data does not allow for high confidence in the sizings used. These sources of error and along with process variation likely explain why negative discharge location on the right-hand side of Figure 5.4 does not cause latch-up exactly at the bonded VSS pin farthest from the PMC, as would be expected based on the analysis. Slight variations in latch-up trigger levels for latch-up structures throughout the chip may result from process variation and core shape.

6.1 Future Work

Further refinement and understanding of the latch-up phenomenon presented in this dissertation will require physical hardware. To that end, careful design of a new test vehicle must be performed. The following presents a high level overview of a test vehicle that may be used for analysis of a RBB design using a charge pump and triple well structures.

6.1.1 IO Design and Floorplanning

A technology that offers merged triple well structures that have the potential to latch-up must be selected. Figure 6.1 provides a block diagram of a test chip for measuring latch-up. All IO cells are non-operational as there is no actively running logic. The test chip may be small (1 mm by 1 mm), however, analysis must be performed to verify adequate bus resistance for significant voltage gradients. Larger chips may be mimicked by increasing the bus resistance, as if the metal was of a longer run. ESD design can be simple, dual diodes and a distributed rail clamp. Distributed rail clamps will provide a higher granularity of potential latch-up locations. ESD protection

should be designed to provide a large overhead before physical failure. Best practices (guard rings, spacing) should be followed to remove potential for latch-up via substrate current injection.

6.1.2 Core Design and Test Structures

The core should consist of standard cell arrays of inverters (latch-up structures) with the maximum well tap spacing allowed within the PDK. Approximately 1 nF of decoupling capacitance between the core power net and chip ground net should be evenly spread throughout the core. Merged triple well devices should be used. Regular, high level metal meshes should be used for all supply routing as any asymmetry will add additional variables to the design and further complicate analysis. This design ensures that the core will be representative of a real production chip in terms of resistance and capacitance.

A cutout, centered within the core, will be necessary for the placement of isolated test structures. Two test structures should be placed. One will consist solely of an inverter with an adjacent well tap for characterization. The second test structure should consist of a small isolated section of the mock core. Figure 6.2 shows a test structure which will allow for characterization of a latch-up structure likely to be found within a core. These structures will allow for measuring latch-up time, current, and voltage, thus allowing for an increase in modeling accuracy.

6.2 Figures

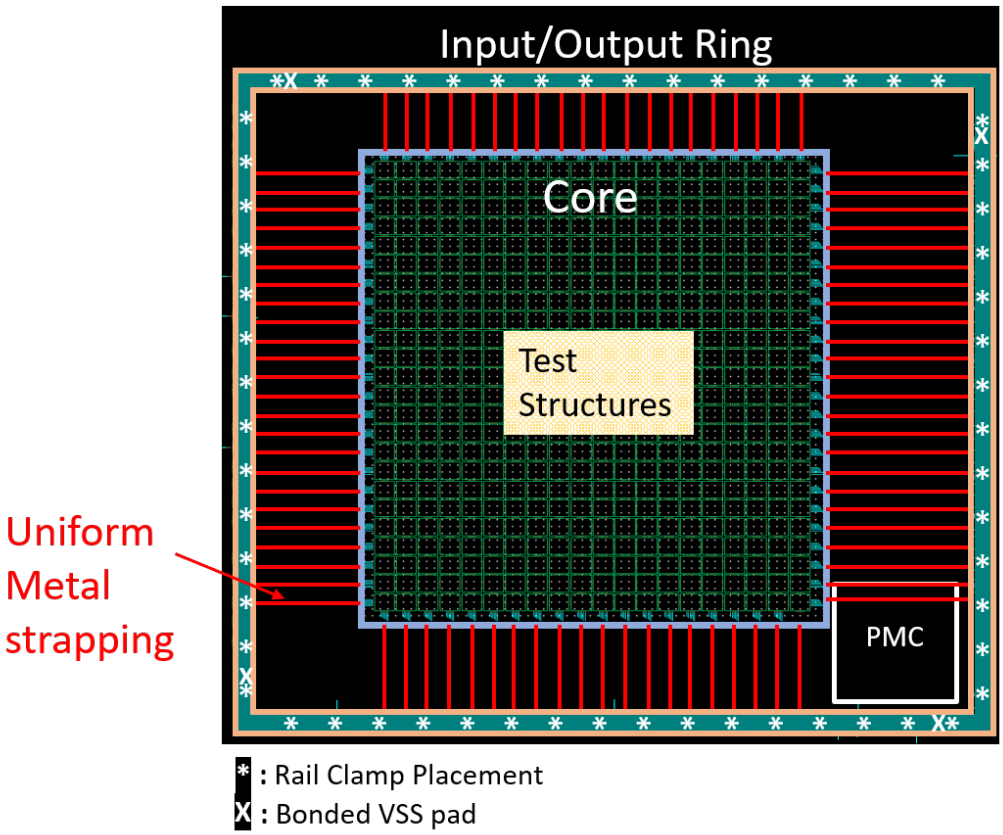


Figure 6.1: Block level floorplan of a test chip designed to measure latch-up in a RBB core using a charge pump power delivery design.

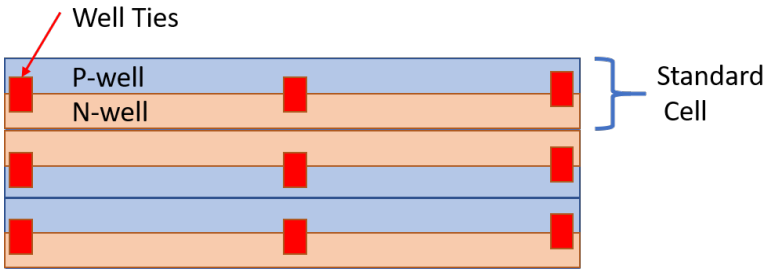


Figure 6.2: Layout of a latch-up test structure for characterization. Well ties are marked as red boxes. the standard cell P-well and N-well are in blue and orange, respectively. Each standard cell should array latch-up structures as well as decoupling capacitors.

REFERENCES

[1] E. Association, "Fundamentals of electrostatic discharge, part one: An introduction to ESD," ESD Association, Rome, NY, 2013.

[2] *For Electrostatic discharge sensitivy testing human body model (HBM) - device level*, ANSI/ESDA/JEDEC Std. JS-001-2014, 2014.

[3] *For Electrostatic discharge sensitivy testing charge device model (CDM) - device level*, ANSI/ESDA/JEDEC Std. JS-001-2014, 2014.

[4] *Electromagnetic compatibility (EMC) – Part 4-2: Testing and Measurement Discharge Immunity Test*, IEC Std. IEC-61 000-4-2, 2009.

[5] N. A. Thomson, Y. Xiu, and E. Rosenbaum, "Soft-failures induced by system-level ESD," *IEEE Trans. Device Mater. Rel.*, vol. 17, no. 1, pp. 90–98, Mar. 2017.

[6] Y. Xiu, S. Sagan, A. Battini, X. Ma, M. Raginsky, and E. Rosenbaum, "Stochastic modeling of air electrostatic discharge parameters," in *IEEE International Reliability Physics Symposium (IRPS)*, Mar. 2018, pp. 2C.2–1–2C.2–10.

[7] Y. Xiu, "Failures caused by supply fluctuations during system-level ESD in integrated circuits," Ph.D. dissertation, Univ. of Illinois at Urbana-Champaign, Urbana, IL, Dec. 2018.

[8] S. Vora, R. Jiang, S. Vasudevan, and E. Rosenbaum, "Application level investigation of systemlevel ESD-induced soft failures," in *EOS/ESD Symposium Proc.*, Sep. 2016, pp. 1–10.

[9] Y. Xiu, N. Thomson, R. Mertens, C. Reiman, and E. Rosenbaum, "Chip-level ESD-induced noise on internally and externally regulated power supplies," in *EOS/ESD Symposium Proc.*, Sep. 2017, pp. 1–10.

[10] N. Thomson, Y. Xiu, R. Mertens, M. Keel, and E. Rosenbaum, "Custom test chip for system-level ESD investigations," in *EOS/ESD Symposium Proc.*, Sep. 2014, pp. 1–10.

[11] N. Thomson, C. Reiman, Y. Xiu, and E. Rosenbaum, "On-chip monitors of supply noise generated by system-level ESD," in *EOS/ESD Symposium Proc.*, Sep. 2017, pp. 1–10.

[12] A. Patnaik, W. Zhang, R. Hua, L. Chuang, A. Huang, H. Lin, B. Tseng, and D. Pommerenke, "Systematic evaluation of soft failures in system-level ESD transient events," *IEEE Trans. Electrom. Compat.*, vol. 60, no. 5, pp. 1263–1269, Oct. 2018.

[13] S. Yang, B. Orr, Y. Guo, Y. Zhang, D. Pommerenke, H. Shumiya, J. Maeshima, T. Sekine, Y. Takita, and K. Araki, "Measurement techniques to predict the soft failure susceptibility of an IC without the aid of a complete software stack," in *IEEE International Symposium on Electromagnetic Compatibility (EMC)*, Jul. 2016, pp. 41–45.

[14] A. Hosseinbeig, O. H. Izadi, S. Solanki, T. D. Lingayat, B. P. Subramanya, A. K. Vaidhyanathan, J. Zhou, and D. Pommerenke, "Methodology for analyzing ESD-induced soft failure using full-wave simulation and measurement," *IEEE Trans. Electrom. Compat.*, vol. 61, no. 1, pp. 11–19, Feb. 2019.

[15] S. Vora, R. Jiang, P. M. Vijayaraj, K. Feng, Y. Xiu, S. Vasudevan, and E. Rosenbaum, "Hardware and software combined detection of system-level ESD-induced soft failures," in *EOS/ESD Symposium Proc.*, Sep. 2018, pp. 1–10.

[16] S. Vora and E. Rosenbaum, "Analysis of system-level ESD-induced soft failures in a CMOS microcontroller," *IEEE Trans. Electrom. Compat.*, pp. 1–10, 2020.

[17] O. Girard, "Openmsp430," 2009. [Online]. Available: https://opencores.org/websvn/filedetails?repname=openmsp430&path=%2Fopenmsp430%2Ftrunk%2Fdoc%2FopenMSP430.pdf

[18] Y. Xiu, N. Thomson, and E. Rosenbaum, "Measurement and simulation of on-chip supply noise induced by system-level ESD," *IEEE Trans. Device Mater. Rel.*, vol. 19, no. 1, pp. 211–220, Mar. 2019.

[19] R. Mertens, "Understanding, modeling and mitigating system-level ESD in integrated circuits," Ph.D. dissertation, Univ. of Illinois at Urbana-Champaign, Urbana, IL, May 2015.

[20] R. Merrill and E. Issaw, "ESD design methodology," in *EOS/ESD Symposium Proc.*, 1993.

[21] J. Flucke, F. Schnieder, F. Schmückle, W. Heinrich, and M. Rudolph, "On the magnetic coupling between bondwires in power-transistor packages," in *German Microwave Conference Digest of Papers*, Mar. 2010, pp. 90–93.

[22] R. Mertens, N. Thomson, Y. Xiu, and E. Rosenbaum, "Analysis of active-clamp response to power-on ESD: Power supply integrity and performance tradeoffs," *IEEE Trans. Device Mater. Rel.*, vol. 15, no. 3, pp. 263–271, Sep. 2015.

[23] K. Feng, S. Vora, R. Jiang, E. Rosenbaum, and S. Vasudevan, "Guilty as charged: Computational reliability threats posed by electrostatic discharge-induced soft errors," in *2019 Design, Automation Test in Europe Conference Exhibition (DATE)*, 2019, pp. 156–161.

[24] *System level ESD part 1: Common misconceptions and recommended basic approaches*, JEDEC Std. JEP161, 2011.

[25] R. R. Troutman, "Latchup in CMOS technologies," *IEEE Circuits and Devices Magazine*, vol. 3, no. 3, pp. 15–21, May 1987.

[26] C. Chen and M. Ker, "Investigation on latch-up path between I/O PMOS and core PMOS in a 0.18-um CMOS process," in *IEEE International Reliability Physics Symposium (IRPS) Proceedings*, 2019, pp. 1–4.

[27] K. Domanski, "Latch-up in FinFET technologies," in *IEEE International Reliability Physics Symposium (IRPS) Proceedings*, 2018, pp. 2C.4–1–2C.4–5.

[28] F. Farbiz and E. Rosenbaum, "Modeling and understanding of external latchup in CMOS technologies—part i: Modeling latchup trigger current," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 3, pp. 417–425, Sep. 2011.

[29] F. Farbiz and E. Rosenbaum, "Modeling and understanding of external latchup in CMOS technologies—part ii: Minority carrier collection efficiency," *IEEE Trans. Device Mater. Rel.*, vol. 11, no. 3, pp. 426–432, Sep. 2011.

[30] W. Liang, R. Gauthier, S. Mitra, and H. Lai, "External latchup risks and prevention solutions in advanced bulk FinFET technology," in *EOS/ESD Symposium Proc.*, Sep. 2019, pp. 1–9.

[31] S. Voldman, *Latchup*. U.K.: Wiley, 2007.

[32] *IC Latch-Up Test*, JEDEC Std. JESD78E, 2016.

[33] S. Vora, M. Stockinger, and E. Rosenbaum, "Increased latch-up susceptibility of ICs using reverse body bias," in *EOS/ESD Symposium Proc.*, Sep. 2020, pp. 1–10.

[34] M. Stockinger, W. Zhang, K. Mason, and J. Feddeler, "An active MOSFET rail clamp network for component and system level protection," in *EOS/ESD Symposium Proc.*, 2013, pp. 1–10.

[35] M. Stockinger, J. W. Miller, M. G. Khazhinsky, C. A. Torres, J. C. Weldon, B. D. Preble, M. J. Bayer, M. Akers, and V. G. Kamat, "Boosted and distributed rail clamp networks for ESD protection in advanced CMOS technologies," in *EOS/ESD Symposium Proc.*, 2003, pp. 1–10.

[36] F. Farbiz, "Modeling and suppression of latchup," Ph.D. dissertation, Univ. of Illinois at Urbana-Champaign, Urbana, IL, May 2010.

[37] M. Etherton, S. Ruth, J. W. Miller, R. Agarwal, R. Bhooshan, M. Ershov, M. Cadjan, Y. Feinberg, K. Srinivasan, N. Chang, and Youlin Liao, "A new full-chip verification methodology to prevent CDM oxide failures," in *EOS/ESD Symposium Proc.*, 2015, pp. 1–10.

[38] M. Blagojević, M. Cochet, B. Keller, P. Flatresse, A. Vladimirescu, and B. Nikolić, "A fast, flexible, positive and negative adaptive body-bias generator in 28nm FDSOI," in *IEEE Symposium on VLSI Circuits (VLSI-Circuits)*, 2016, pp. 1–2.

[39] D. Kontos, K. Domanski, R. Gauthier, K. Chatty, M. Muhammad, C. Seguin, R. Halbach, C. Russ, and D. Alvarez, "Investigation of external latchup robustness of dual and triple well designs in 65nm bulk CMOS technology," in *IEEE International Reliability Physics Symposium (IRPS) Proceedings*, 2006, pp. 145–150.

[40] L. Wang, C. Wu, L. Feng, A. Chang, and Y. Lian, "A low-power forward and reverse body bias generator in CMOS 40 nm," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 7, pp. 1403–1407, 2018.

[41] N. Kamae, A. Tsuchiya, and H. Onodera, "An area effective forward/reverse body bias generator for within-die variability compensation," in *IEEE Asian Solid-State Circuits Conference*, 2011, pp. 217–220.