ANTI-PHASE COATING FOR MODE CONTROL IN SINGLE-MODE OXIDE-CONFINED VERTICAL-CAVITY SURFACE-EMITTING LASERS

BY

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THESIS

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ABSTRACT

The prevalence of Vertical-Cavity Surface-Emitting Lasers (VCSELs) in the technological landscape has increased substantially recently due to many inherent and beneficial device characteristics. For emerging application such as 3D-sensing in smart phones and automobiles, light detection and ranging (LiDAR), and 4-level pulse amplitude modulation (PAM4), VCSELs present solutions not possible otherwise with edge-emitting lasers (EELs) or light-emitting diodes (LEDs). VCSELs inherently exhibit a circular, low-noise and low-dispersing emission beam, operate with low threshold currents, and can be packaged into high-power 2D-arrays because of their unique geometry. Moreover, VCSELs that operate with only a single-fundamental mode in the transverse direction have improvements in these lasing characteristics. Therefore, control of the lasing modes of a VCSEL is essential to meeting the demands of the applications aforementioned.

Single-transverse fundamental-mode operation can be achieved many ways, most readily by use of a semiconductor anti-phase coating. By depositing and patterning the coating spatially across the top surface of a VCSEL into the shape of an annulus, the threshold modal gain in the outer region can be selectively increased while minimizing the gain in the center of the device. This coating therefore suppresses the higher order transverse modes and fundamental-mode operation can be achieved.

This work explores the development process of 850 nm oxide-confined VCSELs. By first simulating the device structure, the coating can be designed with the appropriate parameters. This is followed up with the fabrication of the VCSEL structure concluding with the characterization of the device for various performance metrics. Thus, the effects of the anti-phase coating are illustrated and single-mode high-power VCSEL operation is realized.

To my parents, for their love and support.

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The close friends I made at community college, in classes, and in clubs on campus have taught me the true meaning of friendship. I am grateful to have you all in my life and have made my time on campus much more enjoyable.

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LIST OF ABBREVIATIONS

EEL	Edge-Emitting Laser
LED	Light-Emitting Diode
DBR	Distributed-Bragg Reflector
SNR	Signal-to-Noise Ratio
IILD	Impurity-Induced Layer Disordering
PVD	Physical Vapor Deposition
SEM	Scanning-Electron Microscope
FIB-SEM	Focused-Ion Beam Scanning-Electron Microscope
BCB	Benzocyclobutene
SMSR	Side-Mode Suppression Ratio

CHAPTER 1

INTRODUCTION

1.1 Motivation and Applications of VCSELs

The changing of the guard from traditional incandescent light bulb and copper interconnects in telecommunication systems to optoelectronic devices such as light-emitting didoes (LEDs) and edge-emitting lasers (EELs) transformed the technological landscape forever. These modern devices have numerous advantages over the previous eras, including lower energy requirements, capability for optical data transmission enabling high speed modulation for optical communication systems, and capability to aid in many material processing applications. However, the limitations of these devices prevent their range of applications from expanding, unlike VCSELs. Historically, VCSEL applications have been limited to optical mice and optical finger navigation [2], laser printers [3], and optical data communication systems [4]. As shown in Figure 1.1, data traffic is expected to increase drastically over

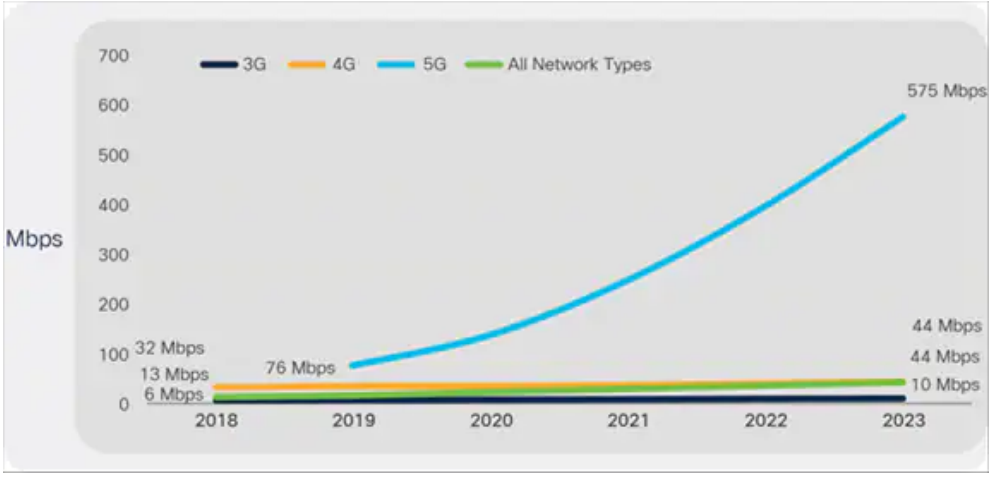

Figure 1.1: Average global mobile speeds from the years 2018-2023, where 5G speeds are expected to increase by over 700% [1] in that time period.

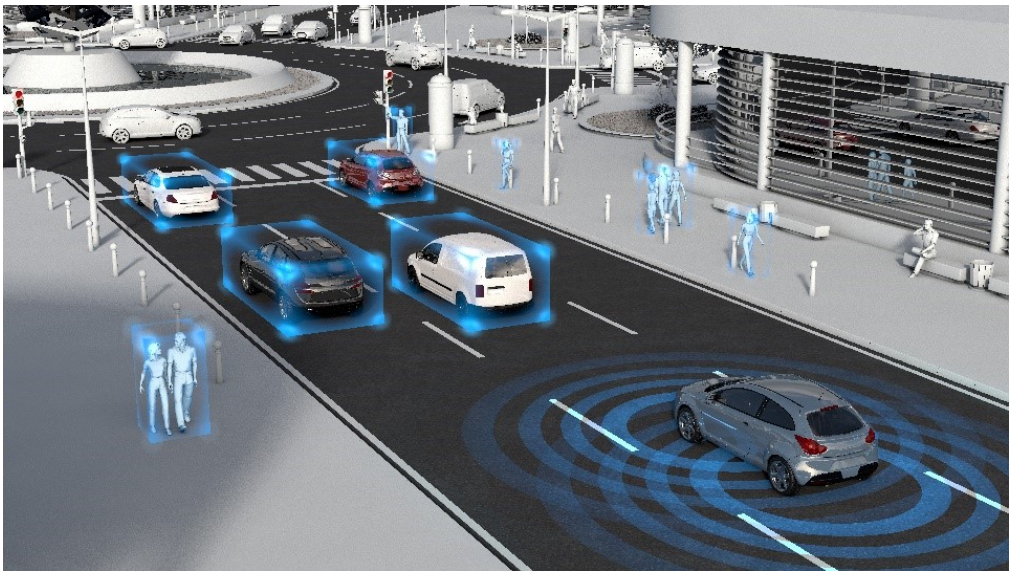

Figure 1.2: Depiction of LiDAR system utilizing short light pulses to map surrounding cars and people [7].

the next few years due to the advent of 5G communication and applications demanding higher data transmission, severely hindering the existing infrastructure. More recent interest into VCSEL technology has been garnered for several reasons. These reasons include the capability of VCSELs to be packaged into dense arrays enabling on-chip testing, energy-efficient operation due to low current thresholds [5], and high-speed operation [6] capable of meeting modern-data demands. Additionally, augmented reality and virtual reality (AR/VR) consumer applications require fine-linewidth and polarization-stable beams, making VCSELs a very suitable candidate for these applications as well.

Modern-day VCSELs are being pushed to their performance limits due to these emerging applications, necessitating research and development into accommodating these demands. Attractive solutions to these problems include increasing optical-power emission that allows for increased signal-to noise ratio (SNR), better single-transverse-mode operation which furthermore increases SNR, and ease-of-manufacturing allowing for easy implementation into standard commercial VCSEL process flows. This work explores an anti-phase coating that enables enhanced single-fundamental transverse-mode operation while maximizing beam output power.

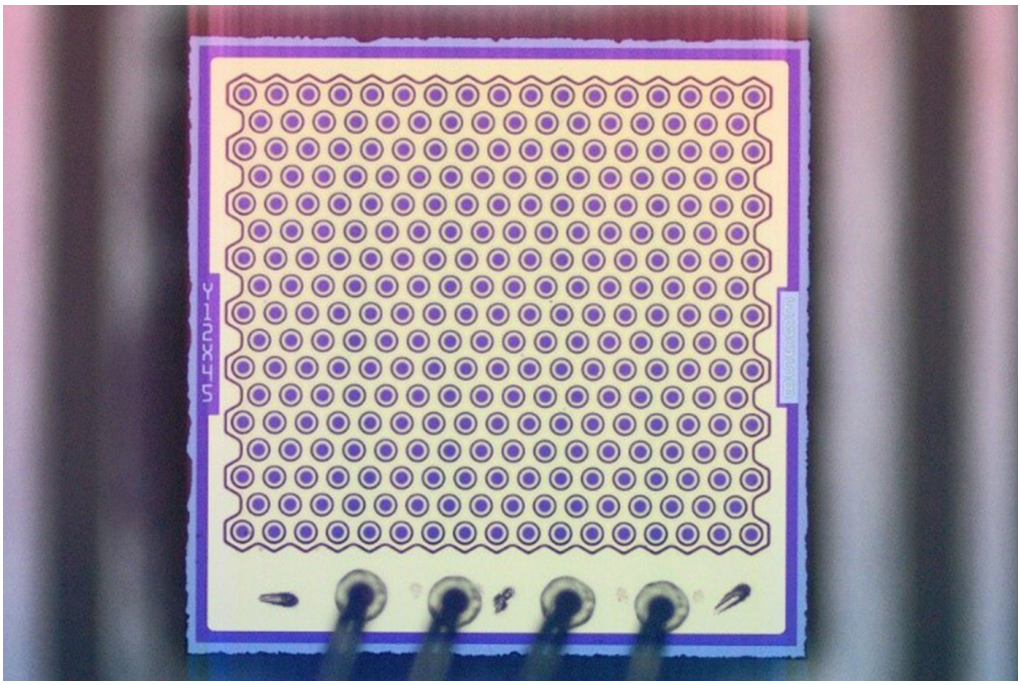

Figure 1.3: Commercial VCSEL array wire-bonded and used in automotive LiDAR applications [8].

1.2 History of Surface-Emitting Lasers

The first instance of a surface-emitting laser was in 1965 when Melngailis injected current and obtained coherent light emission along the longitudinal direction of an InSb n^+pp^+ structure [9]. The large device layers and poor facet reflectivities restricted this device in several ways, most notably a large threshold current and multimode operation. This was followed up by Soda and Iga in 1979 with the GaInAsP/InP surface-emitting laser that experienced similar difficulties [10]. Several technological breakthroughs were necessary to overcome these difficulties and transform these VCSELs into the modern day version capable of meeting the demands of modern day applications. One breakthrough included depositing Distributed-Bragg reflector (DBR) mirrors onto the facets, first realized and patented by Scifres and Burnham in 1975 [11]. Moreover, the discovery of native and stable oxide Al_xO_y growth in $Al_xGa_{1-x}As$ heterostructures by Dallesasse and Holonyak in 1989 [12] and subsequent application to VCSEL structures by Huffaker and Deppe in 1994 (Figure 1.4) [5] alleviated many of the issues aforementioned, leading to low threshold current and energy-efficient operation.

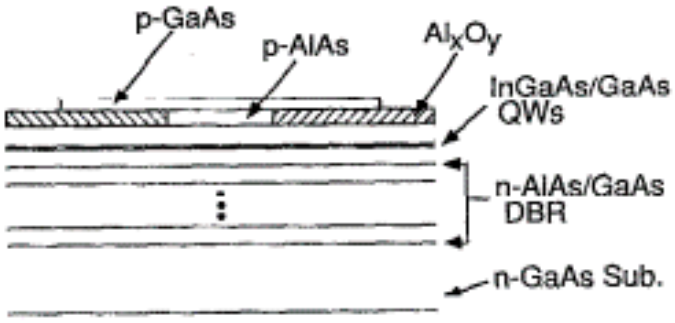

Figure 1.4: First Native Oxide-Aperture VCSEL by Huffaker and Deppe [5].

CHAPTER 2

VCSEL FUNDAMENTALS

2.1 Laser Diode Basics

The modern-day VCSEL has many unique characteristics both structurally and operationally to other lasers. Firstly, the structure consists of two p-type doped and n-type doped $Al_xGa_{1-x}As$/GaAs DBR pairs to create highly reflective mirrors, forming a Fabry-Pérot cavity. $Al_xGa_{1-x}As$/GaAs pairs are used due to their cost-efficient growth and also lattice-matched conditions with the other materials present. The operational principle behind a DBR (also referred to as a Bragg reflector) is that by depositing an integer number of layers with alternating low-and high-refractive index materials, electromagnetic waves can be reflected and transmitted in-phase at each interface. If there are enough pairs (~ 20), the mirror can become virtually lossless generating structure reflectivities of $\sim 99\%$ over a stop band ranging many 10's of nanometers. The equation governing the thickness of each

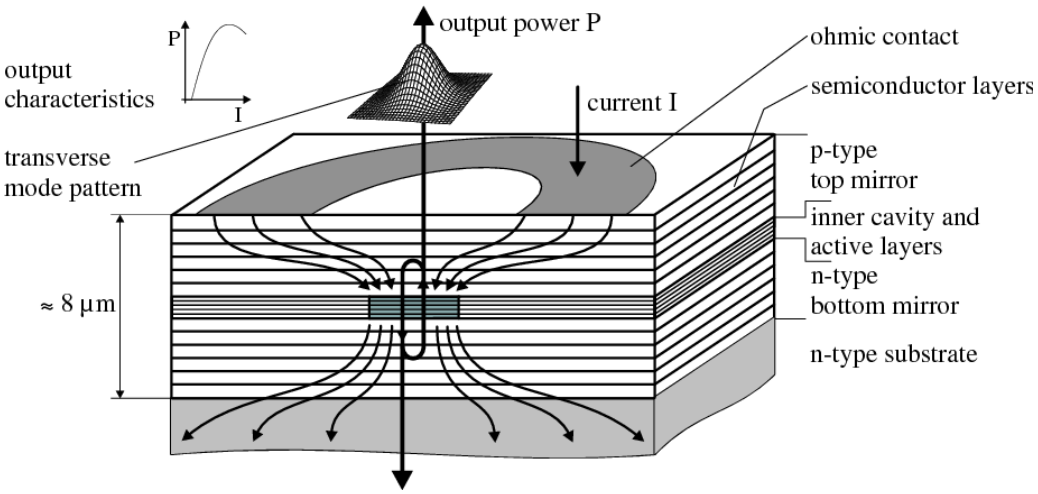

Figure 2.1: Cross sectional schematic of a modern-day VCSEL depicting the layer structure and operating characteristics [13].

layer is Eq. 2.1, where λ_b is the Bragg (or resonant) wavelength of the DBR structure

$$d = \frac{\lambda_b}{4n} \tag{2.1}$$

and n is the refractive index of the material [14]. The topic of DBR layers and in-phase reflections will be revisited later during the discussion of the anti-phase coating. In addition to DBR layers, VCSEL structures also contain an active region composed of multiple quantum wells surrounded by cladding layers in order to generate gain. The top of the p-type DBR includes a highly-doped GaAs cap layer in order to prevent natural oxidation of the top DBR and to aid in uniform current injection. Lastly, in order to operate with low current thresholds, the confinement of electric charge carriers is necessary. This can be accomplished with a ring-shaped oxide aperture [12] (lines converging at center of device in Figure 2.1) or proton-implantation [15]. This work focuses on an oxide aperture and the advantages over proton implantation, including the capability of optical-carrier confinement. The ring-shaped oxide-aperture layer is formed in an $Al_xGa_{1-x}As$ layer with sufficient enough aluminum content (>98%) placed a few layers above the active region.

2.2 Methods for Controlling Transverse Modes

Due to the size of the laser ($\sim$ 30 μm in the longitudinal direction and $\sim$ 8 μm in the transverse direction with an active region 10's of nm thick), VCSELs inherently operate with a single mode in the longitudinal direction and multiple modes in the transverse direction. Moreover, there are many advantages for operating with a single-fundamental transverse mode. For applications in 3D sensing and LiDAR, operating with a single-fundamental mode provides a very narrow linewidth beam that increases SNR [16]. Additionally, high-speed optical communications utilizing photodiodes suffer from various sources of noise including shot and thermal noise. Due to the lack of competition between the modes of single-mode VCSELs, they inherently operate with less noise compared to multimode devices, furthermore increasing SNR [17]. One method of limiting and controlling the transverse modes, which was mentioned in the previous section, is an oxide aperture.

By decreasing the active device size in the longitudinal direction, the num-

ber of supported optical modes can decrease to the point of operating with the desired single-fundamental mode [19]. However this comes as a trade-off with decreased optical power and more device self-heating, resulting in faster device rollover and decreased device operation lifetimes. This trade-off motivates the need for developing separate methods for optical confinement. One of these methods includes surface-etch relief [20] where 10's of nanometers in the outer radial regions of the top GaAs cap layer is etched away creating an out-of-phase optical wave that suppresses lasing. Another method utilizes impurity-induced layer-disordering (IILD) [21] where Zinc is selectively disordered into the top DBR, intermixing the $Al_xGa_{1-x}As$/GaAs layers and creating an IILD aperture. This annulus-shaped aperture spatially reduces the reflectivity of the top DBR of the VCSEL, suppressing higher-order modes [22–28]. These methods face their own difficulties, including controlling the etch depth in a dry etch system for the former and controlling the anisotropic shape of the IILD aperture for the latter. Because of these difficulties, it is behooving to explore a more controllable method for mode control in VCSELs.

On a side note, it is important to mention that mode-control techniques such as those mentioned here so far have only been applied to the top p-type DBR since these are top-emitting devices. If these were bottom-emitting

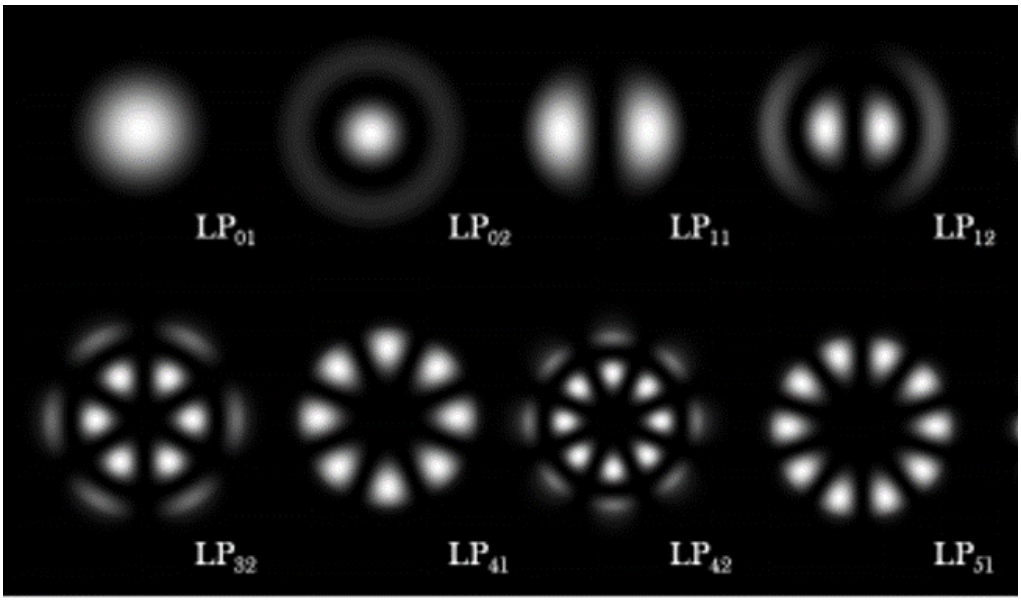

Figure 2.2: Transverse mode profiles of the first several modes supported in a cylindrical VCSEL cavity [18].

devices, the mode-control methods would instead be applied to the bottom n-type DBR. To understand and model the transverse optical modes of an oxide-confined VCSEL, various assumptions need to made. Firstly, the structure can be modeled as a two-layer inhomogeneous cylindrical waveguide, where the core is defined as the oxide-confined area and the cladding is the outer region containing the oxide [29]. Furthermore, by assuming a small difference in the refractive indices between the two regions, the weakly-guiding approximation [30] can be used and the resultant modes are modeled as linearly polarized (LP) modes and shown in Figure 2.2. The fundamental LP_{01} is maximized at the center of the device $\rho = 0$ and the higher-order modes (LP_{11},LP_{21},LP_{12}, etc.) reside spatially further away in the radial direction. The basis of any mode-control method is suppressing the lasing of the higher-order modes while maximizing the lasing of the fundamental mode by disrupting the outer regions of the VCSEL. This spatial discrimination is seen in the aforementioned surface-etch relief, oxide aperture, and IILD aperture. One method of mode control that does not face the problems previously mentioned due to its simplicity is the deposition of dielectric and semiconductor films capable of creating anti-phase (out-of-phase) optical waves that can suppress higher-order transverse modes. Previous multilayer filters [31–33] composed of the common dielectric materials Silicon Dioxide (SiO_2) and Titanium Dioxide (TiO_2) were used to create an in-phase fundamental mode and anti-phase higher-order modes, preferentially lasing the fundamental mode and impeding the lasing of the higher-order modes. The tedious nature of a multi-layer filter that requires multiple photolithography and deposition steps furthermore motivates the need for a single-layer anti-phase coating capable of ensuring fundamental-mode operation.

2.3 Threshold and Phase Condition of VCSELs

The basics for VCSEL operation [14] begin with the lasing equation (Equation 2.2)

$$r_1 r_2 e^{i2\beta L} = 1 \tag{2.2}$$

$$r_x = |r_x| e^{i\phi_x} \tag{2.3}$$

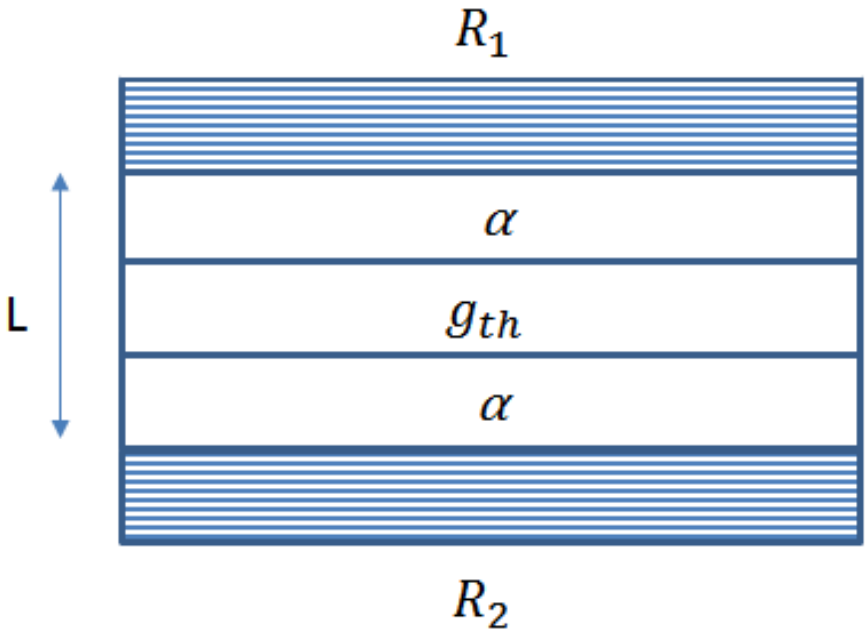

Figure 2.3: Schematic of VCSEL structure identifying terms used in threshold condition equation.

$$\beta = \beta_c + i\frac{\alpha - \Gamma g_{th}}{2} \tag{2.4}$$

$$R = |r_x|^2 \tag{2.5}$$

where r_1 and r_2 are the complex reflection coefficients shown in Equation 2.3, β is the propagation constant shown in Equation 2.4, and L is the length of the active gain region. Furthermore, β_c is the real propagation constant, α is the internal losses of the system including absorption and scattering, g_{th} is the threshold modal gain of the device, and Γ is the optical confinement factor. After plugging Equations 2.3 and 2.4 into 2.2, the resultant equation can be broken down into complex and real parts, where the phase (Equation 2.6) and threshold conditions (Equation 2.7) of the VCSEL can be obtained.

$$\phi_1 + \phi_2 + 2\beta_c L = 2m\pi \tag{2.6}$$

$$\Gamma g_{th} = \alpha_i + \alpha_m = \alpha_i + \frac{1}{2L} ln \frac{1}{R_1 R_2} \tag{2.7}$$

A basic analysis of these two important equations will conclude this section, while a detailed analysis of the device structure and anti-phase coating will occur in the next chapter once simulation data is obtained. The first of these two equations requires that the round-trip phase accumulated by the optical wave (left side) equals an integer number of 2π in order to maintain in-phase propagation everywhere in the structure. As mentioned earlier, the number of pairs in the DBR structure greatly influences the device operation. An increase in DBR pairs in general increases the power reflectance R (defined in 2.5) of the top DBR but not only is there a limit to gaining power reflectance per DBR pair added, adding half-DBR pairs creates an interesting phenomenon not discussed yet.

Firstly, it is important to mention a specific point regarding DBR layer ordering and the VCSEL epitaxial structure used in this work. An optical wave can experience two situations after leaving the active region: encounter a low-refractive index material followed by a high-refractive index material (low-high) or vice versa where the high-refractive index material is encountered first (high-low). Moreover, the situation determines whether an integer or half-integer number of DBR pairs are needed to generate an in-phase standing wave. In this work, a $Al_{.15}Ga_{0.85}As$ layer in the top DBR is seen first and the lower refractive index $Al_{0.9}Ga_{0.1}As$ follows, implying a half-integer number DBRs pairs is necessary and this is confirmed by an extra $Al_{0.15}Ga_{0.85}As$ half pair above the DBR (below the GaAs cap layer) in the epitaxial structure. With this high-low ordering and due to the half-wavelength length (λ / 2n) of the active region, the longitudinal standing wave pattern has an anti-node at the center of the device (maximizing electric field overlap with the active gain region). Furthermore, nodes are placed at the interface between the active region and first DBR layer due to the out-of-phase incident and transmitted waves (from Eq. 2.6, $\phi_1{=}\phi_2{=}\pi$), leading to destructive interference between the two waves. This is shown in Figure 2.4 where a longitudinal standing wave pattern is superimposed on a general VCSEL cavity.

Lastly, further analysis of the threshold condition in Equation 2.7 shows why the anti-phase coating can be so effective. The left side of the equation represents the gain of the system while the right side of the equation represents the internal losses α_i and mirror losses α_m. In order for the VCSEL to lase, the gain has to equal and exceed the losses. Since a basic understand-

ing of a DBR has been established, the full implications of an anti-phase coating can be realized. As described above, the addition and subtraction of top DBR pairs can greatly influence the phase of the optical wave and therefore, increase and decrease the top DBR power reflectance (R_1), respectively. Following this, if an extra half-DBR pair were etched away such as in surface-etch relief, the optical wave would then be out-of-phase generating a higher mirror loss due to a smaller R_1. However, rather than etching away a layer, depositing an additional quarter-wavelength thick layer accomplishes the same feat in a much more controlled way. Furthermore, if this quarter-wavelength layer is only deposited in the outer regions of the VCSEL in the

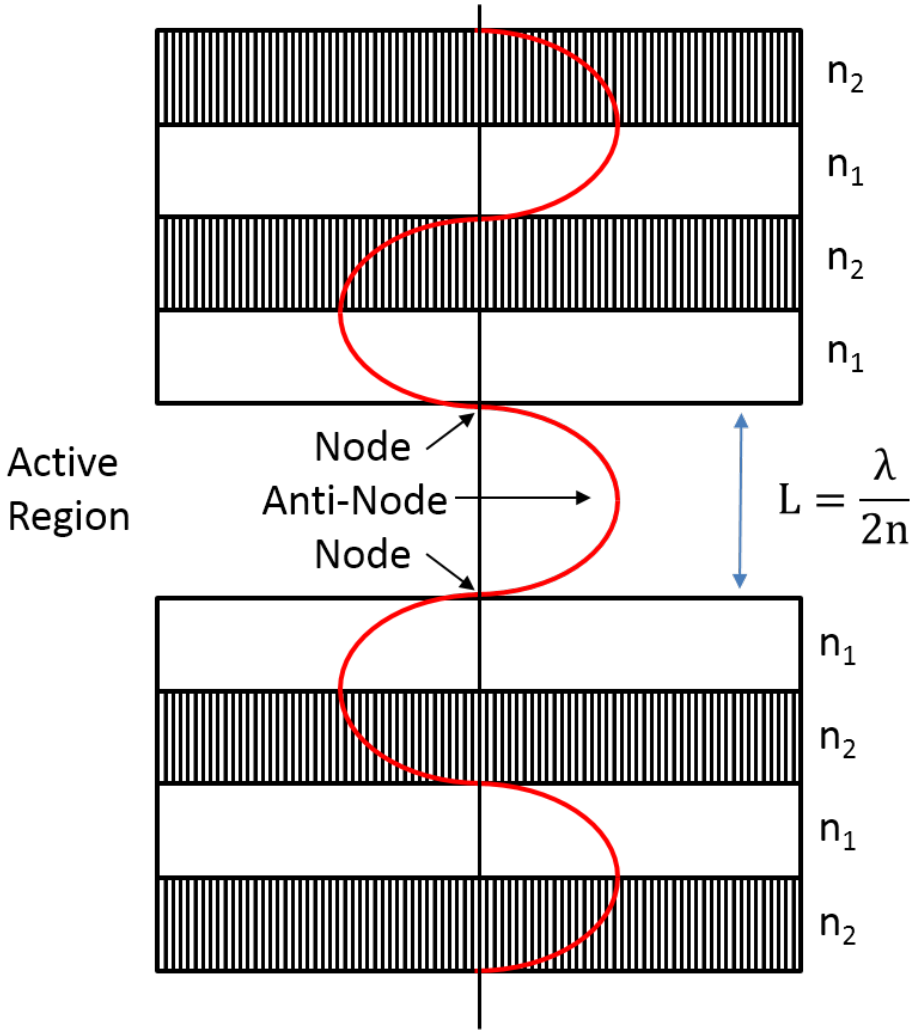

Figure 2.4: Longitudinal standing wave pattern (red line) in VCSEL structure ($n_1 > n_2$) with a optical cavity length of a half-wavelength [based on Figure 11.13.a in [14]].

shape of an annulus similar to that of the oxide aperture, the optical wave is anti-phase while the wave in the center of the device where the fundamental mode resides remains in-phase. Herein is the basis of the anti-phase coating. By creating this anti-phase wave, the confinement factor Γ decreases because of the reduced electric field overlap with the active region, raising the threshold modal gain g_{th} **only** for the higher order modes, suppressing their capability to lase. This is how single-fundamental-mode operation can be achieved in oxide-confined VCSELs and the remainder of this work explores the simulation, fabrication, and characterization of these devices.

CHAPTER 3

SIMULATION AND DESIGN OF MODE-CONTROLLED VCSELS

3.1 Modeling of Oxide-Confined VCSELs

In order to fully comprehend the effects of the anti-phase coating, several operational characteristics need to be observed including the power reflectance, phase of the optical wave, standing wave pattern, and finally the threshold modal gain of the optical modes. This can be accomplished by first modeling the device via the transfer-matrix method (TMM), where an incident wave E_0 is incident on an inhomogeneous medium such as a VCSEL DBR (Figure 3.1). By constructing matrices for each interface in the structure and taking the product of all the matrices, the reflection r and transmission t coefficients of the total field can be calculated. The simulated structure includes 20.5 DBR pairs of alternating $Al_{0.9}Ga_{0.1}As/Al_{0.15}Ga_{0.85}As$ layers capped with a GaAs current-spreading layer.

The derivation begins with a TE polarized incident wave and reflected wave [14]

$$E_i = \hat{y} E_0 e^{-ik_{0x}x + ik_{0z}z} \tag{3.1}$$

$$E_r = \hat{y} r E_0 e^{ik_{0x}x + ik_{0z}z} \tag{3.2}$$

In the l_{th} layer, the electric and magnetic fields are given by

$$E_y^l = \left[A_l e^{-ik_{lx}(x+d_l)} + B_l e^{ik_{lx}(x+d_l)} \right] e^{ik_{lz}z} \tag{3.3}$$

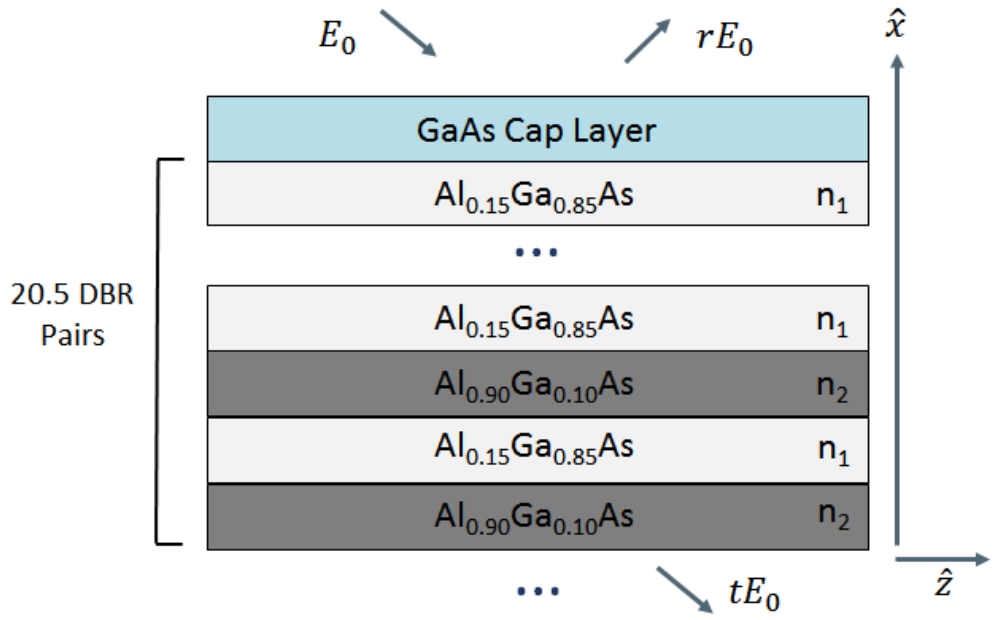

Figure 3.1: Model of top DBR in VCSEL structure.

Table 3.1: Refractive indices of DBR layers at 850 nm [34]

Material	Refractive Index
$Al_{0.9}Ga_{0.1}As$	3.06
$Al_{0.15}Ga_{0.85}As$	3.53
GaAs	3.60

$$H_z^l = \frac{-k_{lx}}{\omega\mu_l}\left[A_l e^{-ik_{lx}(x+d_l)} - B_l e^{ik_{lx}(x+d_l)}\right] e^{ik_{lz}z} \tag{3.4}$$

$$k_{lx} = \sqrt{\omega^2\mu_l\epsilon_l - k_{0z}^2}, k_{lz} = k_{0z} \tag{3.5}$$

where the first term in the bracket represents the transmitted wave and the second term represents the reflected wave. Next, the following term is defined

$$P_{l(l+1)} = \frac{\mu_l k_{(l+1)x}}{\mu_{l+1}k_{lx}} \tag{3.6}$$

and thickness h is given by

$$h_{l+1} = d_{l+1} - d_l \tag{3.7}$$

Once the boundary conditions of the electric and magnetic fields are met, the following matrix is formed

$$\begin{bmatrix} A_l \\ B_l \end{bmatrix} = \mathbf{B}_{l(l+1)} \begin{bmatrix} A_{l+1} \\ B_{l+1} \end{bmatrix} \tag{3.8}$$

where $\mathbf{B}_{l(l+1)}$ is defined as

$$\mathbf{B}_{l(l+1)} = \frac{1}{2} \begin{bmatrix} (1 + P_{l(l+1)})e^{-ik_{(l+1)x}h_{l+1}} & (1 - P_{l(l+1)})e^{ik_{(l+1)x}h_{l+1}} \\ (1 - P_{l(l+1)})e^{-ik_{(l+1)x}h_{l+1}} & (1 + P_{l(l+1)})e^{ik_{(l+1)x}h_{l+1}} \end{bmatrix} \tag{3.9}$$

By plugging this term into Equation 3.8 for each layer interface in the structure, the following matrix can be obtained

$$\begin{bmatrix} E_0 \\ rE_0 \end{bmatrix} = \mathbf{B}_{GaAs}\mathbf{B}_{Al_{0.15}Ga_{0.85}As}(\mathbf{B}_{Al_{0.90}Ga_{0.10}As}\mathbf{B}_{Al_{0.15}Ga_{0.85}As})^{\#DBR} \begin{bmatrix} A_{N+1} \\ B_{N+1} \end{bmatrix} \tag{3.10}$$

$$= \begin{bmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{bmatrix} \begin{bmatrix} tE_0 \\ 0 \end{bmatrix} \tag{3.11}$$

From this equation, the transmission and reflection coefficient of this structure, respectively, are

$$t = \frac{1}{b_{11}} \tag{3.12}$$

$$r = \frac{b_{21}}{b_{11}} \tag{3.13}$$

Now that the formulation for modeling the VCSEL structure has been established, various device characteristics for both the base and mode-controlled VCSEL can be explored.

3.2 Baseline VCSEL Device Characteristics

The unaltered VCSEL structure used in this work was designed such that the DBRs perform as complete mirrors capable of achieving power reflectances upwards of 99.51% at the operational wavelength of 850 nm, as shown in Figure 3.2. The stop band of this device spans roughly 70 nm. With power reflectances on this order, the mirror loss term α_m in Equation 2.7 is minimized, achieving minimized threshold modal gains for all modes. Due to the lack of modal discrimination however, this will result in operation with multiple-transverse modes and a single-longitudinal mode. Additionally, the normalized phase of the standing wave pattern in Figure 3.3 indicates resonant operation of the DBRs at 850 nm for a device with no mode-control techniques (as expected).

The meaning of complete mirrors is important to explore because it differentiates and motivates the single-layer coating used in this work against other multilayer coatings [23–25]. As previously mentioned, surface-etch relief is a commonly used mode-control technique despite its drawbacks. The

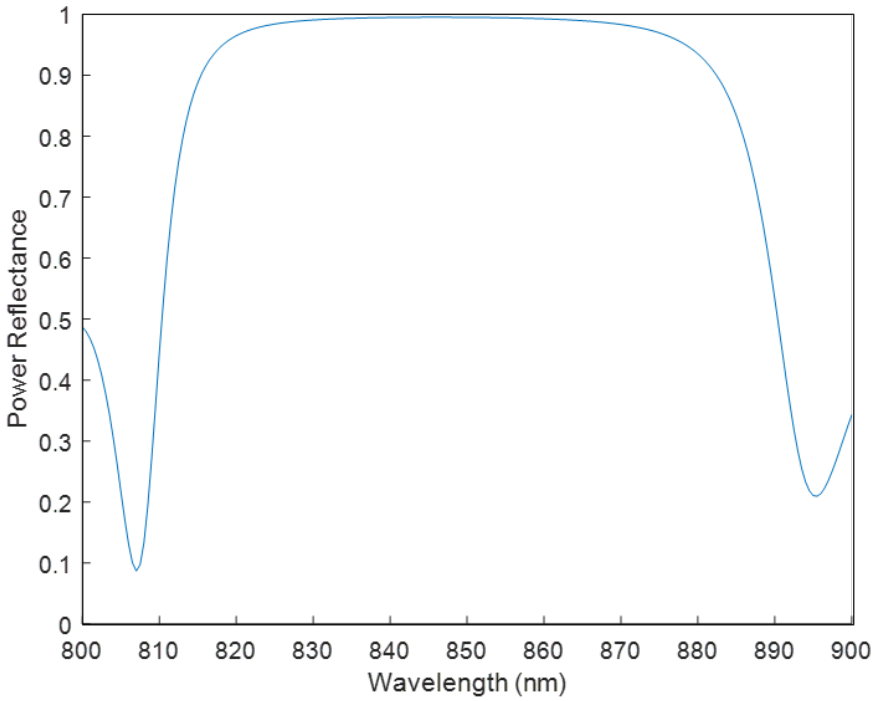

Figure 3.2: Power reflectance of top p-type DBR of VCSEL structure with no mode-control methods.

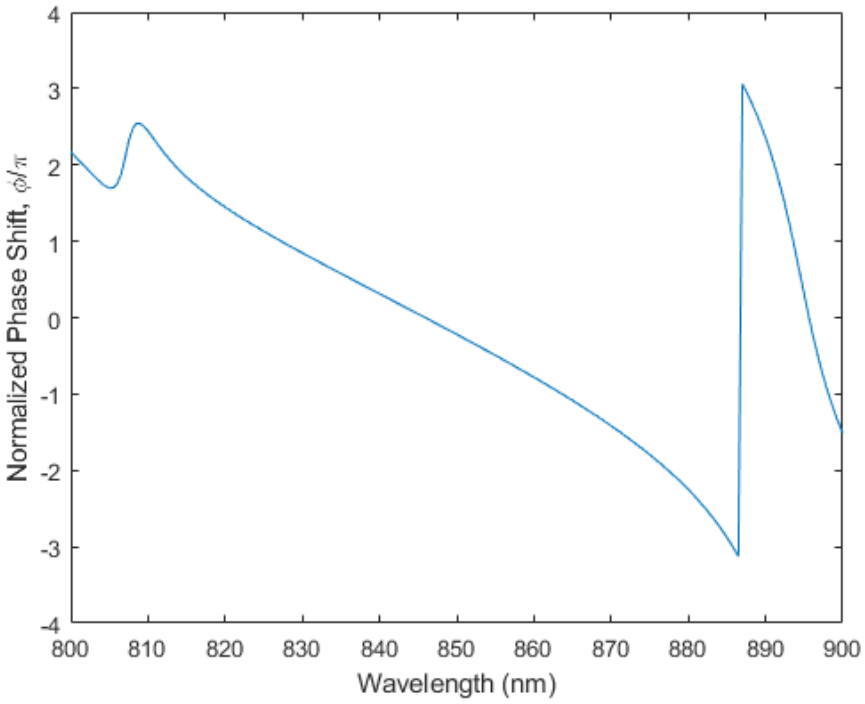

Figure 3.3: Normalized phase shift indicating zero phase shift at the operational wavelength 850 nm.

epitaxial material utilizing this technique purposely has a thicker GaAs cap layer capable of being etched back to create an in-phase fundamental mode while maintaining anti-phase higher-order modes. This thicker GaAs layer creates an incomplete mirror, where the round-trip phase is not equal to an integer number of 2π and therefore does not satisfy Equation 2.6. This leads to a threshold modal gain that is neither maximized nor minimized when the VCSEL is unaltered. The purpose of the multilayer filter is then clear: complete the mirror for the fundamental mode creating an in-phase wave while further disrupting the mirror for the higher-order modes creating an anti-phase wave. This is contrasted with the epitaxial material used in this work that was purposely designed with a complete mirror in order to be more flexible with other mode-control techniques (IILD, anti-phase coating). With this complete mirror, the round-trip phase condition is satisfied and the threshold modal gain is minimized for all modes. Furthermore this motivates the need for a mode-control method capable of only disrupting the higher-order transverse modes.

Simulating the standing wave pattern via the TMM method described in

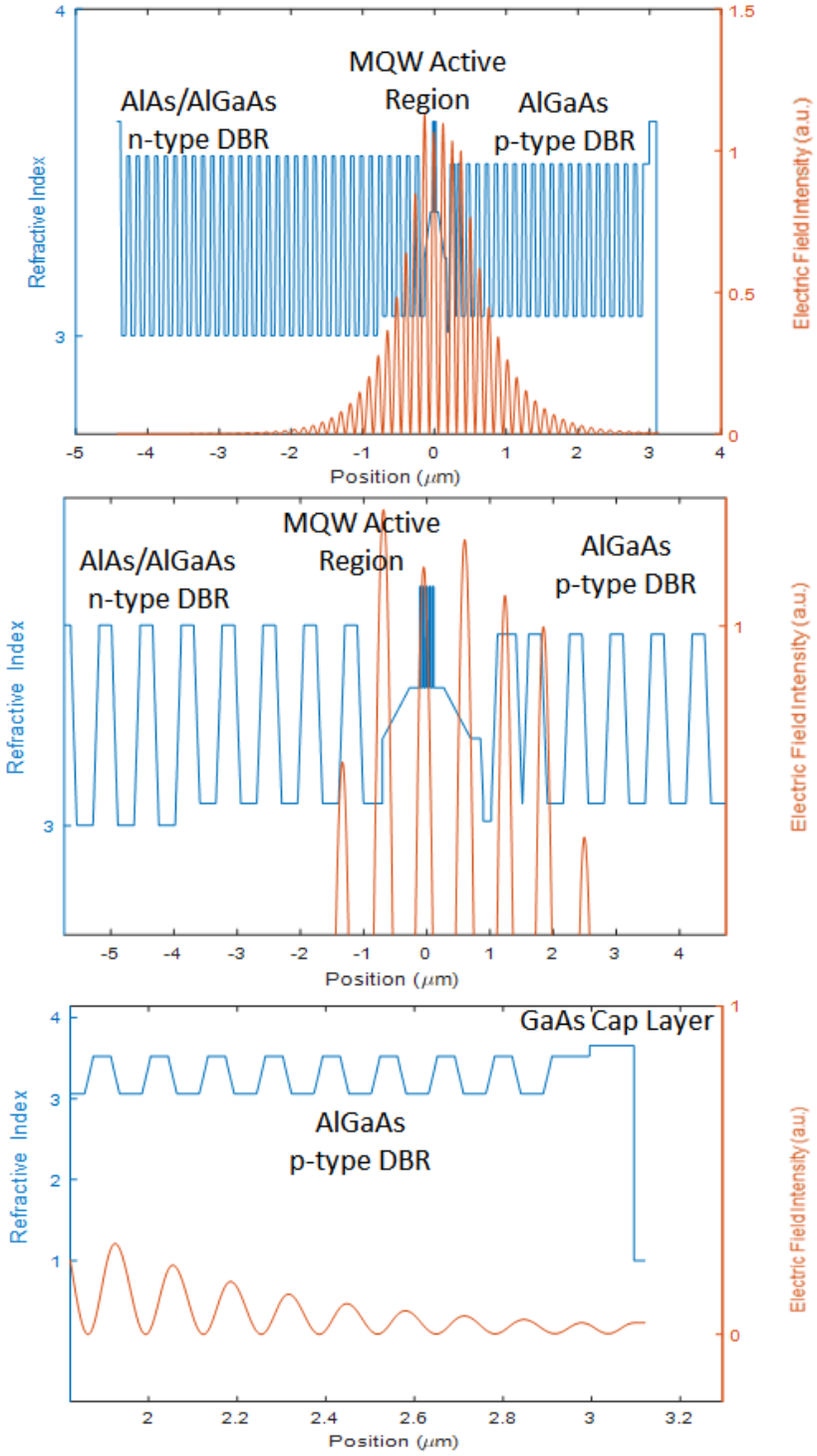

Figure 3.4: Standing wave pattern (orange) amplitude superimposed onto the refractive index profile (blue) of the entire VCSEL structure (top image), with focus on the multiquantum well active region (middle image), and with focus on the last several p-type DBR pairs and GaAs cap layer (bottom image).

the previous section is a very powerful and insightful tool into understanding the basic operation of a VCSEL and how it can be manipulated. Figure 3.4 illustrates the longitudinal standing wave of the VCSEL used in this work and superimposes it onto the refractive index profile of the structure in specific areas. As shown in the top image, the standing wave peaks in the center of the device and decays to a null at the edges of the device due to the high number of reflections concentrating the wave in the center of the device.

As mentioned before, the placement of nodes and antinodes is vital to correct and enhanced performance. Antinodes are meant to be placed in areas where good overlap and coupling of the material and wave are needed, such as the active region (middle image). This leads to a relatively high confinement factor leading to low threshold modal gains. Additionally, antinodes exist at the interfaces of high-to-low refractive index materials due to the constructive interference between the reflected and transmitted wave. This directly contrasts the placement of nodes that reside at the interfaces between low-to-high refractive index materials due to the destructive interference between the reflected and transmitted waves. The placement of a node at the oxide aperture is also vital to maintaining the weakly-guiding approximation used in simulating the device. The last image is the most telling and will be analyzed in more detail once the simulations of the anti-phase coating are completed. For now, it can be seen that due to the in-phase wave in the device, the wave decays and emits only a small portion of the standing wave out of the cavity, showing that the reflectivity of the DBR mirror is not 100%.

3.3 Simulation of Anti-Phase Coating on VCSEL Performance

The necessity for an anti-phase coating to suppress higher-order transverse modes of a VCSEL has been presented and is explored in this section. As previously mentioned, suppressing the lasing of higher-order modes while leaving the fundamental unaltered can be accomplished by patterning and depositing a radially dependent coating atop the p-type DBR. This can be done with a coating in the shape of an annulus which can be seen below in Figure 3.5. The fundamental LP_{01} mode is a smooth Gaussian beam that

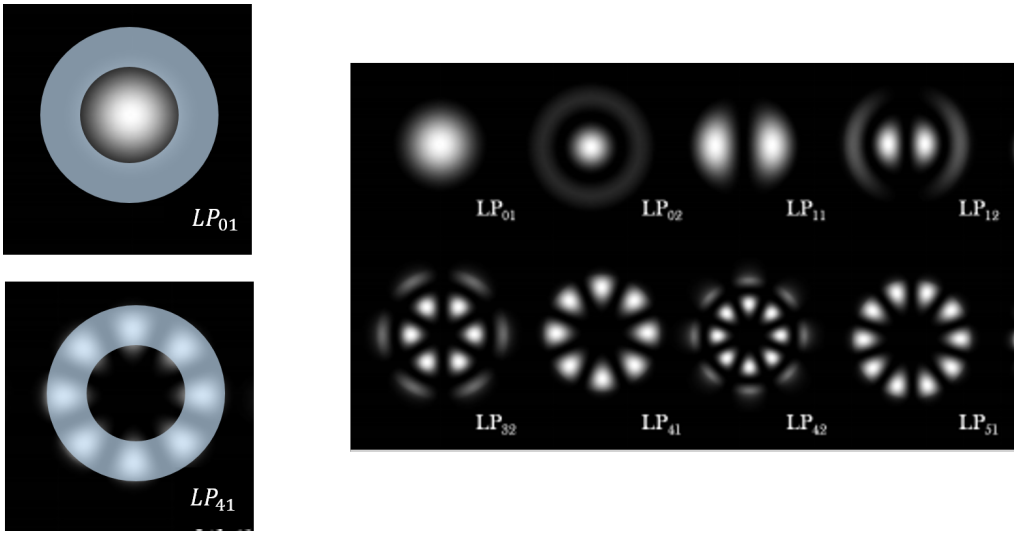

Figure 3.5: VCSEL transverse-mode profile overlaid with anti-phase coating shaped as an annulus, covering and disturbing the higher-order VCSEL modes (LP_{41}) while leaving the fundamental mode unaltered (LP_{01}).

is centered in the middle of the VCSEL while the higher-order modes reside radially further away. The annulus-shaped anti-phase coating overlaid with the VCSEL modes depicts the desired effects the anti-phase coating enacted on the VCSEL.

Now that the general shape of the coating has been established, several more factors are needed before a fabricated coating can be realized. These factors include thickness, material, and specific lengths of the inner aperture diameter of the annulus (the outer diameter is made large enough such that the entire mesa is covered). This last point is of particular importance because of the trade-off between higher-order mode suppression and single-mode optical power. While increasing the aperture size to the order of the oxide aperture may allow for increased optical power due to the increasing presence of supported higher-order modes, the presence of said modes will limit the single-mode operation of the device. However, apertures too small will allow for great single-mode operation while pinching-off the fundamental mode, hurting the maximum power output. The size of the annulus will be explored in greater detail in the following chapter.

The initial design steps for the anti-phase coating require determining suitable materials capable of performing well and achieving the desired results. Common dielectrics and semiconductor materials that can be easily deposited via electron-beam evaporation or physical vapor deposition (PVD) include

Table 3.2: Refractive indices of common dielectric and semiconductor materials at 850 nm [35–38]

Material	Refractive Index
TiO_2	2.5
SiO_2	1.45
Si	3.4-3.8
Air	1.0

TiO_2, SiO_2, or Si. In order to determine the best material, the refractive indices of the materials mentioned must be examined.

The range of the refractive index of silicon is due to the range of crystal qualities caused by various growth methods. Table 3.2 indicates that the lowest refractive index of the materials present is SiO_2 while silicon presents the highest refractive index. Picking the appropriate material requires revisiting the equations presented when discussing DBR reflectivities and introducing one that was implicit in those mentioned so far. Equation 3.14 below represents the reflection of a plane-wave incident on material with a refractive index of n_1 from a material with a refractive index of n_2.

$$R = (\frac{n_1 - n_2}{n_1 + n_2})^2 = (\frac{1 - n_2}{1 + n_2})^2 \tag{3.14}$$

This is the basis for the reflections present in a DBR material and the anti-phase coating. First off, the equation can be simplified by setting n_1=1 because for the coating, it is incident into air. With this simplification, it is next important to determine the appropriate value of R (different from the power reflectance R). Creating the maximum suppression of higher-order modes would mean creating the maximal destructive interference between transmitted and reflected waves. While the transmitted wave cannot be altered without changing the VCSEL structure, the reflected wave "incident" from the air can be influenced by the material forming the anti-phase coating. Maximizing destructive interference involves maximizing the amplitude of the reflected wave and therefore R. Therefore, the highest refractive index material available is used, in this case silicon.

Before moving forward, it is important to emphasize the mechanism justifying the operation of the anti-phase coating. As mentioned, maximizing the amplitude of the wave reflected from the coating/air interface creates the maximum destructive interference with the wave transmitted from the active

region. The effect of this interference is two-fold: the amplitude of the transmitted wave decreases over the whole structure which reduces the overlap of the standing wave with the active region. This in turn decreases the optical confinement factor Γ from Equation 2.7, necessitating an increase in the threshold modal gain g_{th}. If this increasing of g_{th} only happens in the outer portions of the VCSEL where the higher-order modes reside, these modes can selectively become more difficult to lase requiring a higher threshold current compared to the fundamental mode.

The other important design characteristic for the anti-phase coating is thickness of the silicon annulus. To first order, the thickness can be determined by 2.1, where λ_b is 850 nm and n is 3.4 (value used throughout the following simulations). However in reality, this value is slightly inaccurate due to the nonsymmetric and unique structure of the entire VCSEL. After several simulation iterations, it was determined that a thickness of 50 nm provides the best performance. It will become clear later in this section why this is the best performing thickness. Figure 3.6 below shows the affect of the coating on the power reflectance of the DBR structure. At the operational

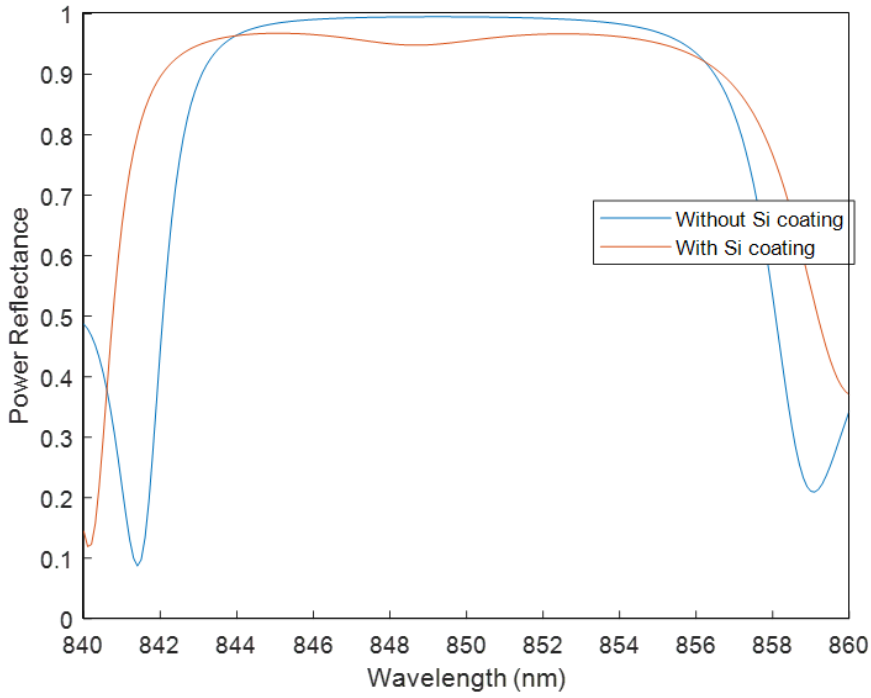

Figure 3.6: Power Reflectance of top DBR with and without the anti-phase coating.

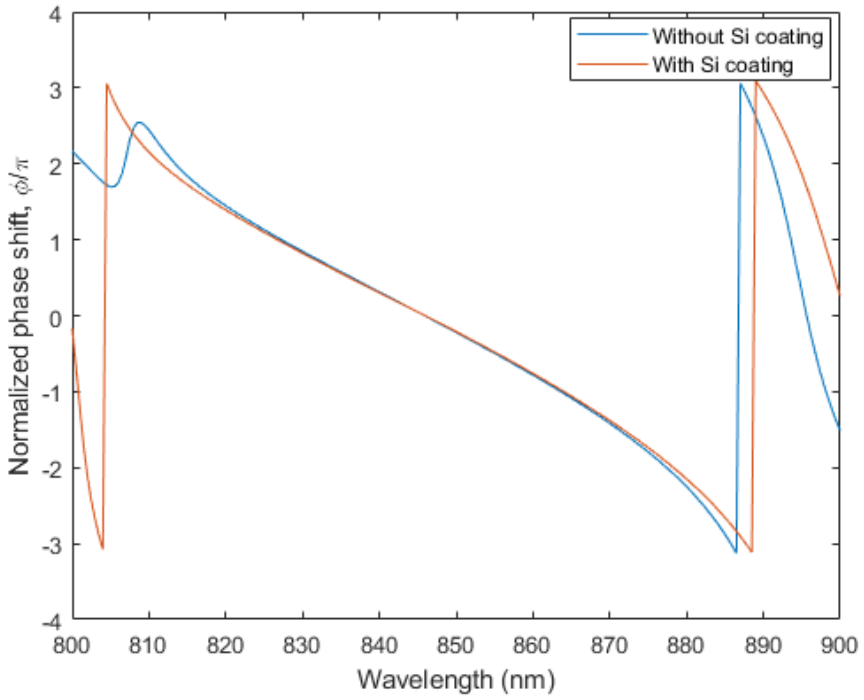

Figure 3.7: Normalized phase shift of longitudinal standing wave with and without the anti-phase coating.

wavelength of 850 nm, the power reflectance drops 4% from 99.5% to 95.5%. This is congruent with the increase in the mirror loss term due to the destructive interference caused by the anti-phase coating. An interesting note is how the anti-phase coating affects the phase of the standing wave insomuch as at 850 nm, the phase is not affected whatsoever. This is due to the fact that while the anti-phase wave does decrease the amplitude of the standing wave in the whole structure, it only affects the phase in the top-most DBR pairs (highlighted shortly) and not the whole device.

The standing waves shown in Figure 3.8 depict the importance of using the high refractive index silicon for the anti-phase coating. Compared to the bottom most image in Figure 3.4 where the standing wave is in-phase and decays to almost null at the surface, the effect of the anti-phase coating is apparent. The top image in 3.8 represents the standing wave of a VCSEL utilizing an anti-phase coating composed of TiO_2. The destructive interference caused by the coating manifests as "ripples" at the surface, where the standing wave is anti-phase and penetrates 2 DBR pairs into the structure before the phase is self-corrected. This point was introduced earlier that

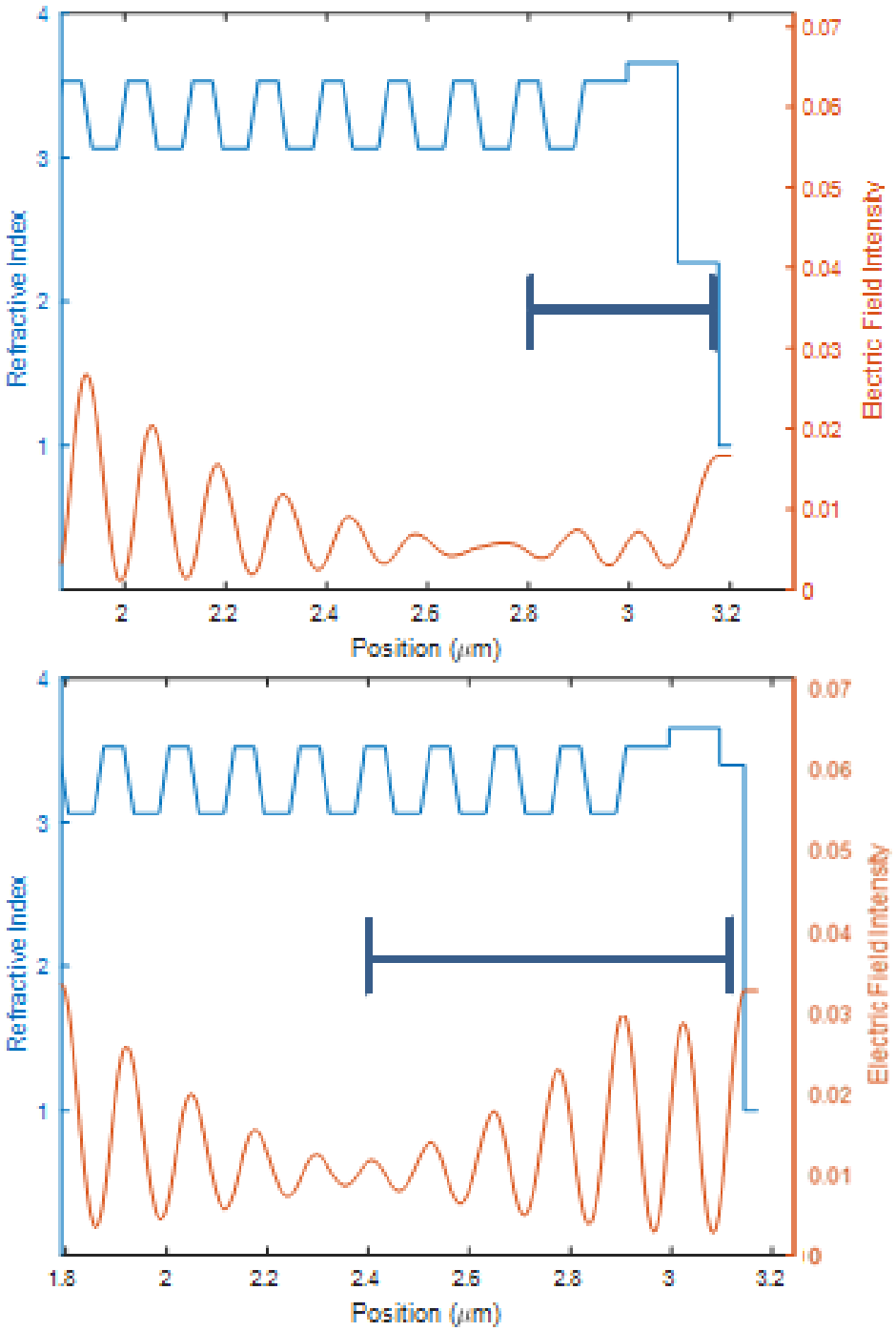

Figure 3.8: Standing wave near surface of VCSEL utilizing a low-refractive index material (TiO_2, top) and a high-refractive index material (Si, bottom) depicting destructive interference caused by anti-phase reflections.

while the overall phase of the standing wave is unaltered, the local phase

near the surface of the device is perturbed. Furthermore, it can be seen that using the higher refractive index silicon causes deeper destructive interference, where the penetration of the reflected wave spans 5 DBR pairs. This leads to even more decreasing of Γ and increasing of g_{th} compared to TiO_2.

These simulation results culminate in the final figure shown below illustrating the threshold modal gain g_{th} of two VCSELs using a TiO_2 and silicon anti-phase coating, respectively. Since the epitaxial material used is the same for both simulations, the threshold modal gain of the structure with the fully intact GaAs cap layer is minimized without the coating (100 nm mark). Therefore, the center of the device where there is no coating experiences a minimized threshold modal gain, preferentially lasing the fundamental mode present there. Meanwhile, for a TiO_2 coating, the threshold modal gain is maximized at at thickness of 80 nm. This leads to a maximized threshold modal gain for the higher-order modes, suppressing their lasing. However, as observed earlier, this effect can be strengthened using the high refractive index silicon. While the amplitude of the peak threshold modal gain for a TiO_2 coating reaches 131 cm^{-1}, 40% of the peak presented by the GaAs cap layer, the silicon coating threshold modal gain peak amplitude reaches 250 cm $^{-1}$, over 50% higher. This leads to more effective suppression of the higher-order modes, ensuring fundamental-mode operation.

As seen, the strength and feasibility of the anti-phase coating makes it an effective mode-control method in VCSELs. The ease presented by the deposition of a single-layer coating can be an attractive solution to not only VCSEL design companies but also industrial fabrication facilities. The flexibility of tailoring the material refractive indices and therefore thicknesses furthermore eases manufacturing tolerances.

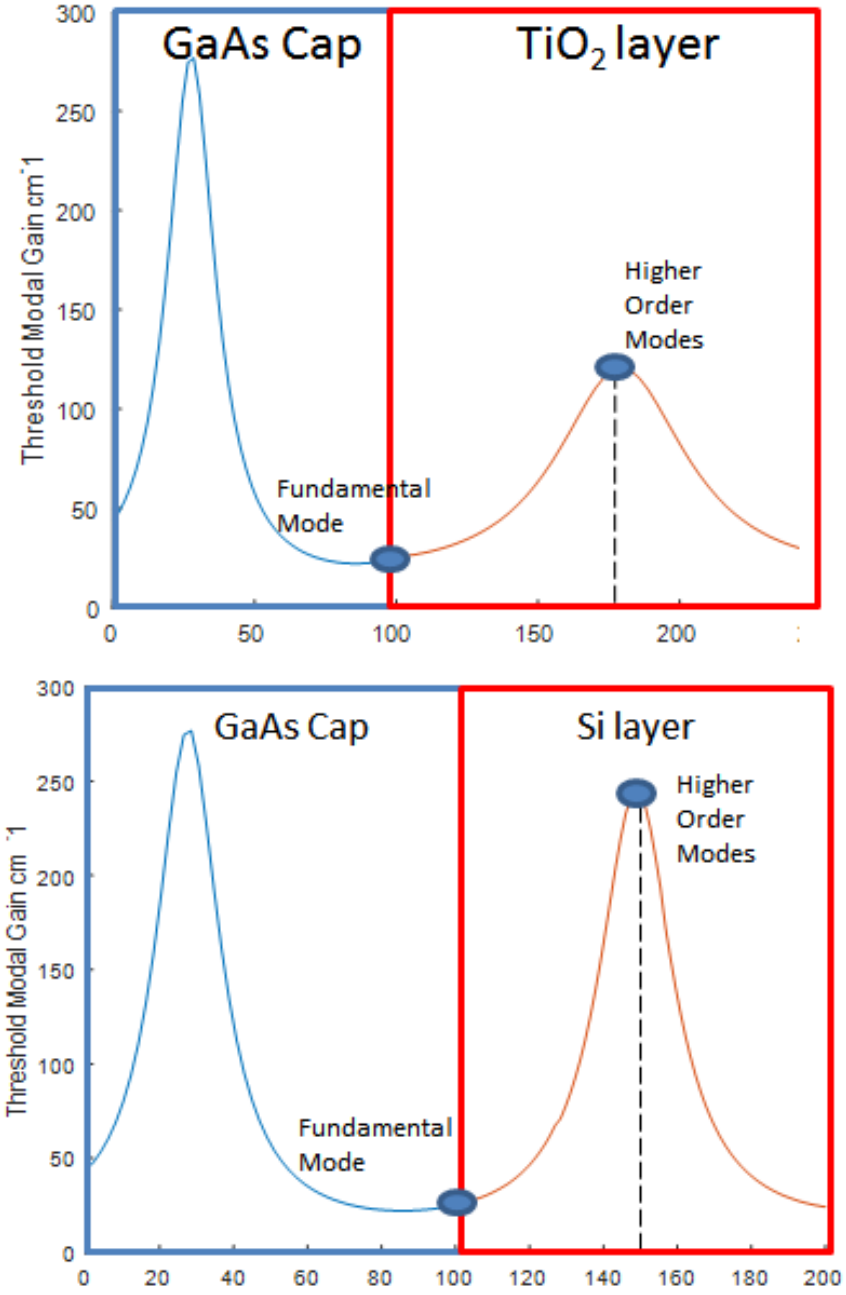

Figure 3.9: Threshold modal gain of VCSEL structure with TiO_2 (top) and Si (bottom) anti-phase coating. Modal gain for fundamental mode is minimized and maximized with a 50 nm thick Si coating and 80 nm thick TiO_2 coating.

CHAPTER 4

FABRICATION OF OXIDE-CONFINED VCSELS

4.1 Epitaxial Material Structure

The VCSEL fabrication process is conducted in the Nick Holonyak, Jr. Micro and Nanotechnology Laboratory class 100 and 1000 cleanrooms utilizing state-of-the-art equipment and a standard VCSEL process flow. The epitaxial material is grown via Metal-Organic Chemical-Vapor Deposition (MOCVD) at the II-VI EpiWorks located in Champaign, Illinois. The growth of the epitaxial material begins with an insulating GaAs substrate followed

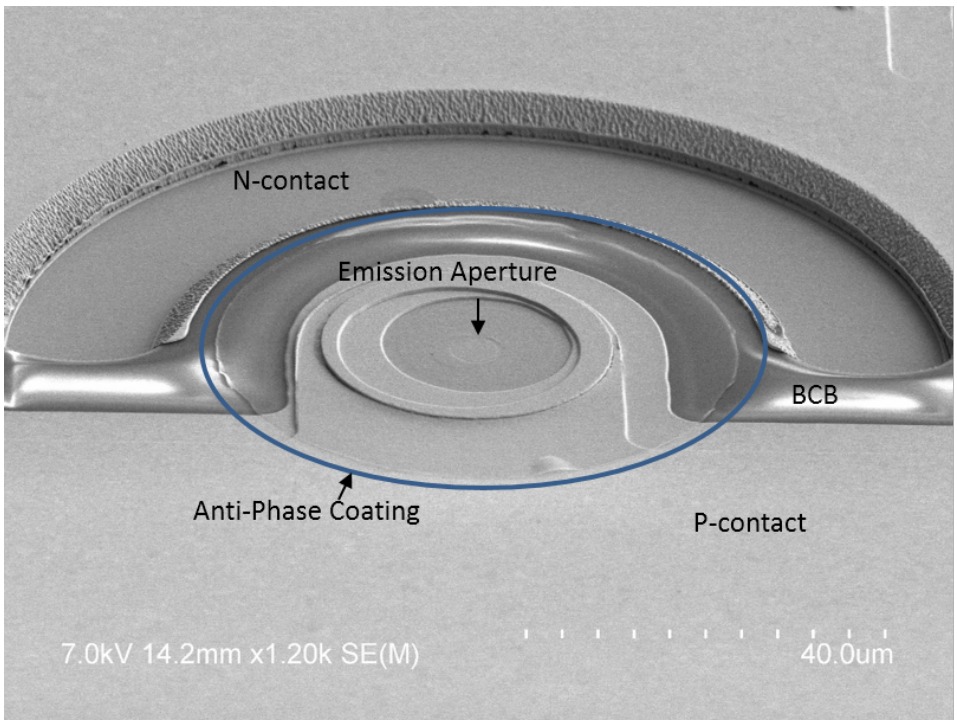

Figure 4.1: Scanning electron microscope (SEM) image of top structure of VCSEL including the two top-side contacts, the anti-phase coating (outlined with blue ring), and BCB.

by 28 AlAs/$Al_{0.12}Ga_{0.88}As$ n-type DBR pairs. This binary composition was specifically chosen to help dissipate heat from the active region of the device due to its low thermal impedance. Above this layer is grown 4 additional $Al_{0.9}Ga_{0.1}As/Al_{0.12}Ga_{0.88}As$ in order to prevent the certain oxidation of the bottom DBR pairs.

Due to their high composition of aluminum, should they be exposed to the furnace during the oxidation process, they will oxidize quicker than the $Al_{0.98}Ga_{0.02}As$ [12] inadvertently creating an oxide aperture in the lower DBR rather than the top DBR and potentially "pinching off" the emission aperture. Following the bottom DBR is the multiquantum well active region consisting of 6 $Al_{0.37}Ga_{0.63}As$ barrier layers and 5 $In_{0.10}Ga_{0.90}As$ quantum wells. The active region is immediately surrounded by 2 $Al_{0.37}Ga_{0.63}As$ cladding layers. $In_{0.10}Ga_{0.90}As$ quantum wells were chosen due to their ability to provide a higher differential gain while remaining lattice-matched, thereby increasing the power output of the device. Above the active region is the $Al_{0.98}Ga_{0.02}As$

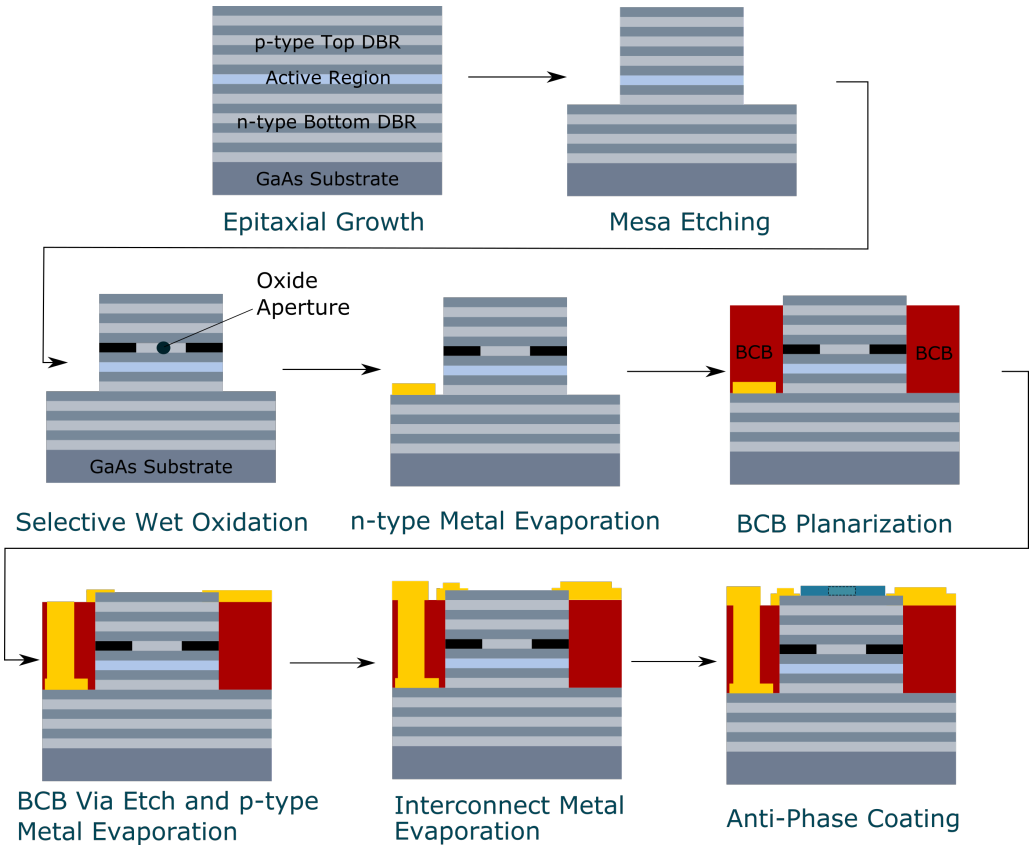

Figure 4.2: Fabrication process of oxide-confined VCSEL with anti-phase coating.

oxidation layer that will form the oxide aperture. Lastly is the top p-type DBR consisting of 20.5 $Al_{0.90}Ga_{0.10}As/Al_{0.15}Ga_{0.85}As$ pairs and a 100 nm GaAs cap layer. An important note for practical applications of DBR pairs is that they necessitate graded layers between the pairs. This is done to assist in carrier mobility and reduce electrical resistance.

4.2 VCSEL Fabrication Process Flow

The fabrication process flow is shown in Figure 4.2 and begins with the photolithographic patterning of a 550 nm Silicon Nitride hard mask deposited via an Oxford Plasma Enhanced Chemical Vapor Deposition (PECVD) system. The hard mask defines the VCSEL mesas, which range in size from 24 μm to 35 μm in diameter. All of the photolithography pattering is done by a Karl Suss MJB3 Contact Mask Aligner utilizing an ultra-violet 320 nm lamp. After this, the hard mask is patterned via an Oxford Inductively-Coupled Plasma Reactive-Ion Etching (ICP-RIE) system utilizing a silicon hexaflouride (SF_6) gas chemistry. Following this step is the definition of the mesas and etching of the n-type DBR utilizing a similar ICP-RIE system with a chlorine-based (BCl_3, Cl_2, Ar) gas chemistry. The etch is monitored in-situ via a laser interferometer that allows for careful etching of the appropriate number of DBR pairs. The etch removes 3.4 μm of epitaxial material and ends once 2 n-type DBR pairs are etched away.

Next is the oxidation step that defines the oxidation aperture and terminates any residual surface states on the mesa left after etching. After an initial dilute 9:1 hydrochloric acid (HCl):H_2O dip to remove sidewall roughness, the wet and dry furnaces are purged with nitrogen (N_2) gas to remove residual oxygen that can hinder the oxidation process and create uneven and asymmetrical oxidation apertures. The samples are first oxidized in a wet furnace at 430 °C by flowing H_2O/N_2 vapor, creating an amorphous oxide. A subsequent dry oxidation step at 400 °C crystallizes the oxide and forms the stable oxide capable of confining current and optical modes. Note that while the $Al_{0.98}Ga_{0.02}As$ oxidized the most due to the high aluminum content, the other high aluminum content pairs in the structure will oxidize to a lesser degree. This can be seen in Figure 4.3, where a focused-ion beam (composed of gallium ions) perpendicular to the surface has bombarded and

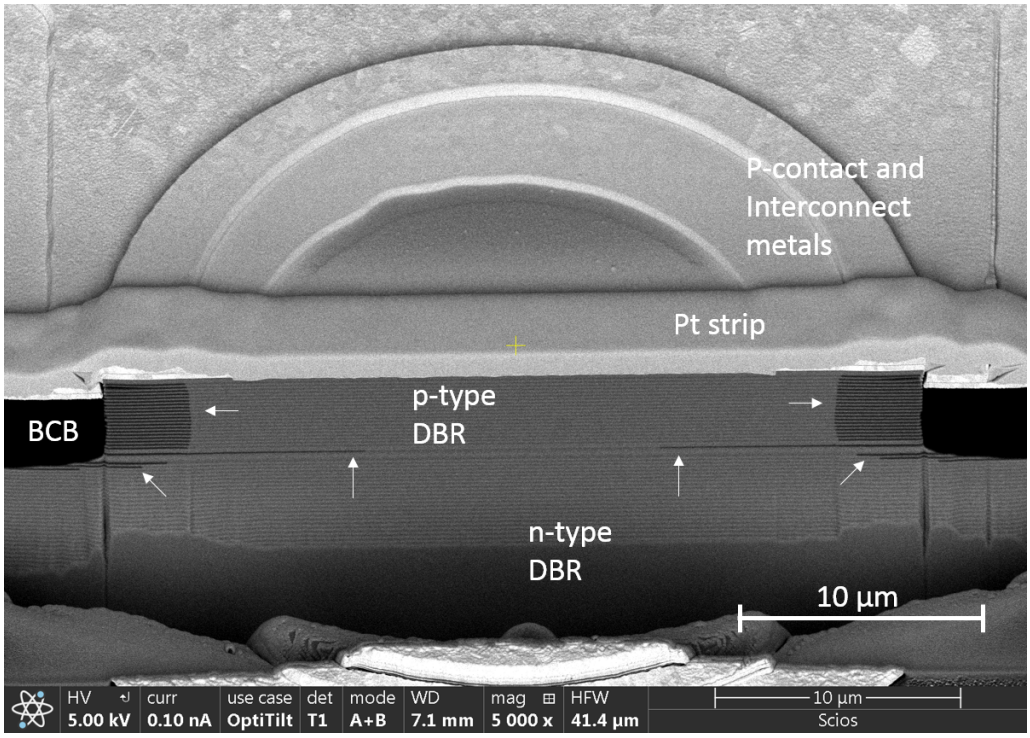

Figure 4.3: Focused-Ion Beam Scanning-Electron Microscope (FIB-SEM) image of oxide-confined VCSEL cross-section.

etched away a cross-section of a device. This process was done in a Thermo Scios 2 Dual-Beam SEM/FIB and it allows for the observation of the structure and confirmation of the oxide aperture size. The device shown in Figure 4.3 is 34 μm in diameter which corresponds to an oxide aperture of 12 μm (length between oxidized $Al_{0.98}Ga_{0.02}As$ edges). In the image, the p-contact and interconnect metal stacks can be observed in the top half of the image while both of the DBR mirrors, the active region, and the BCB (darkest feature) reside in the image below the strip of platinum (Pt). This thin Pt strip was deposited during the cross-section and cleaning etches of the VCSEL to protect the devices features and provide less "curtaining", or translation of the device features into the etch. Additionally, the vertical arrows point to the oxidized $Al_{0.98}Ga_{0.02}As$ layer, the horizontal lines point to the oxidized $Al_{0.90}Ga_{0.10}As$ p-type DBR layers, and the angled lines point to the oxidized $Al_{0.90}Ga_{0.10}As$ n-type DBR layers.

After this the gold-germanium/nickel/gold (AuGe/Ni/Au) n-contact is deposited via electron-beam evaporation and patterned by a liftoff process into the shape of a ring surrounding the mesa. It is then annealed at 400 °C

to form an Ohmic contact. This is followed by planarization with benzocyclobutene (BCB) meant to reduce extrinsic parasitic effects such as pad capacitance [39] that hinder high-speed modulation performance. The BCB is first spun-on, cured at 250 °C to form a solid layer, and etched back in an Oxford RIE system utilizing a $O_2/SF_6/N_2$ gas chemistry to expose the mesas. This is followed up with a Via etch through the BCB allowing for contact to be made with the n-contact. The Via is formed by spinning a thick layer of masking photoresist that is exposed, developed, and reflowed. Reflow of the resist permits a gradual sloping of the resist and underlying BCB after etching enabling good metal climbing up the BCB sidewall. The next step involves depositing and patterning the titanium/platinum/gold (Ti/Pt/Au) p-contact metal following a similar process flow as mentioned above. The penultimate step is the deposition and patterning of a Ti/Au interconnect

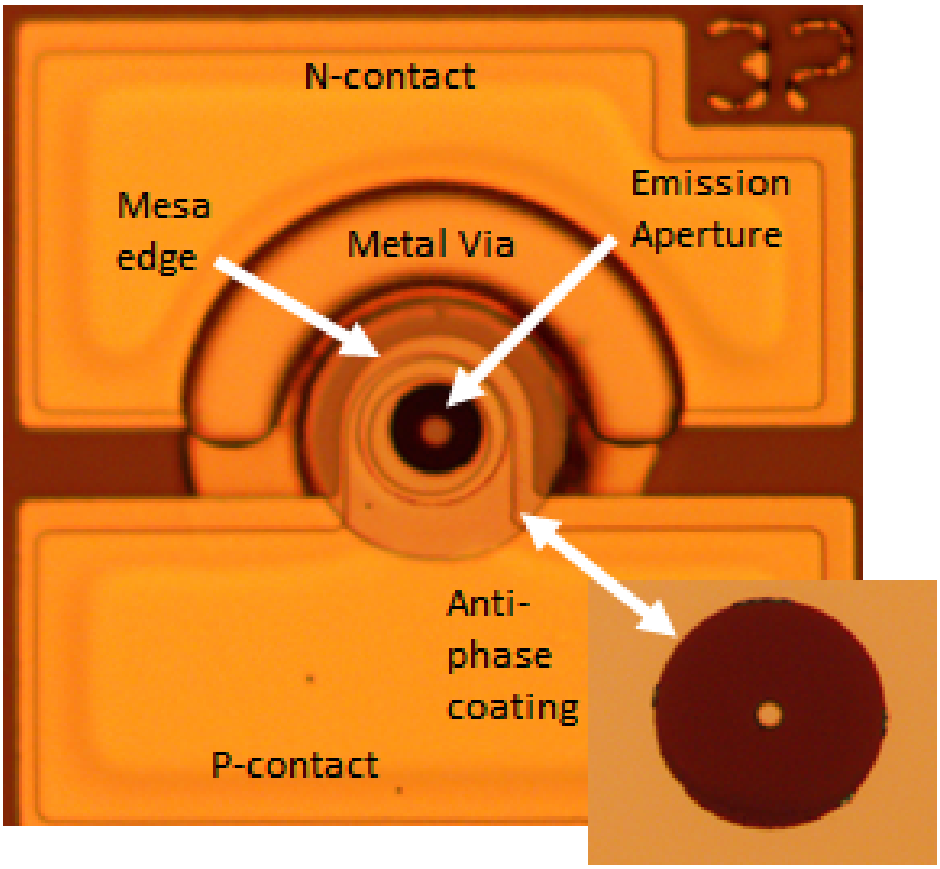

Figure 4.4: Optical micrograph of fabricated 32 μm device with silicon annulus anti-phase coating (inset: annulus on GaAs witness sample highlighting shape of coating).

metal across both contact pads meant for increasing metal conductivity, aiding in high-speed measurements.

Lastly is the patterning and deposition of the silicon anti-phase coating. The silicon is purchased in shard form and due to its high-melting point (1,410 °C), it is only compatible with FABMATE (high-strength graphite) or tantalum crucibles. Other crucibles such as tungsten are not suitable due to the growth of unfavorable oxides that will be detrimental to film quality. The evaporation is done in a Denton Dielectric Optical Coater via e-beam evaporation. Evaporation ramping conditions are vital to maintain and monitor to avoiding crucible breakage and tool damage. Slow ramping up and down leads to the best success of keeping FABMATE crucibles for more than one evaporation run. During evaporation, the chamber contains a witness sample (GaAs or glass) that can be readily patterned with kapton tape. The film is then characterized for thickness and refractive index using optical profilometry and spectroscopic ellipsometry, respectively. Additionally, the quality of the film is quantified via x-ray reflectometry.

A completely fabricated device can be seen in Figure 4.4. The gold-colored layers represent the n- and p-contacts while the darker brown color represents the BCB. Additionally, the gold ring surrounding the mesa and the anti-phase coating constitutes the metal stack contacting the n-type DBR. This occurs underneath the BCB and is contacted by the crescent-shaped via n-contact (see Figure 4.2). The outline of the coating can be seen on the device and inset, indicating total coverage of the mesa. On the device, the dark-colored annulus represents the silicon anti-phase coating defining the emission aperture.

CHAPTER 5

PERFORMANCE CHARACTERISTICS OF MODE-CONTROLLED VCSEL

5.1 VCSEL Optical Spectra

Once devices are fabricated, they are characterized for various performance characteristics including maximum-single-mode power, optical spectra, threshold current, and near-field profile. Firstly, higher-order mode suppression is standardized with a parameter called the side-mode suppression ratio (SMSR). Measured in dB, it records the difference in amplitude between the fundamental mode and the first higher-order mode where a SMSR of greater than 30 dB constitutes a single-mode VCSEL. As mentioned before, the diameter sizes of the fabricated VCSELs range in size from 24 μm to 35 μm with oxidation apertures (active areas) ranging from 2 μm to 13 μm due to the standardized 11 μm encroachment from the oxidize $Al_{0.98}Ga_{0.02}As$ layer. Meanwhile, the anti-phase coating inner diameter ranges from 1.6 μm - 7.35 μm. Both unaltered and mode-controlled devices are fabricated in order to create a baseline showing the improvements made by the anti-phase coating. For an unaltered device with no mode-control techniques, as the active area increases in size, the total amount of optical power increases due to the increase in supported modes and injected current. This allows for more carriers to enter the active region that can recombine and generate photons. However, this is detrimental to single-mode performance leading to a balance that needs to be met between the two.

It is first important to discuss how in order to achieve optimal device performance, photolithographic alignment of device features needs to be reasonable and within fabrication tolerances. Egregious misalignment of the metal contacts and especially the anti-phase coating can change the shape of the cavity enough to change the shape of the supported modes, in addition to negating the effects of any sort of mode-control technique. In the

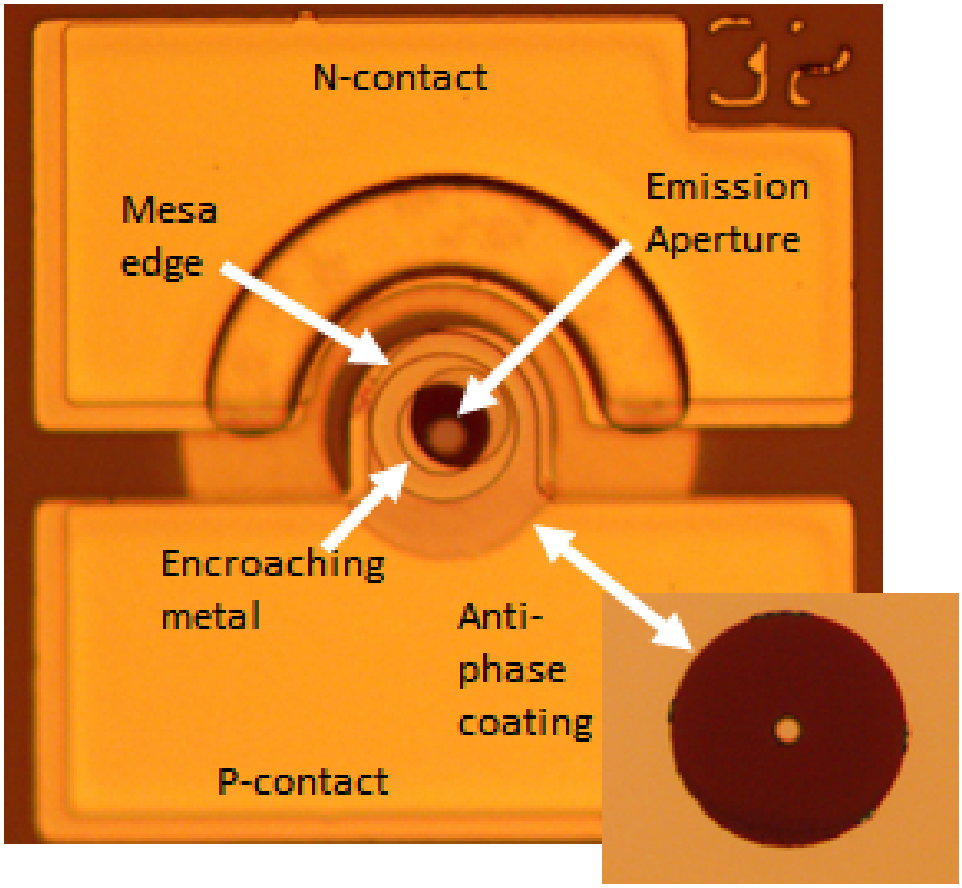

Figure 5.1: Optical micrograph of misaligned VCSEL with metal encroaching on emission aperture.

case of the latter, misalignment of the coating can cause the favorable lasing of modes other than the fundamental mode. As shown in Figure 5.1, misalignment of both the p-contact and interconnect metal layers occurred. This gross misalignment leads to metal encroaching on both the oxide and emission apertures, greatly affecting the device performance.

One important parameter for characterizing VCSEL performance includes measuring optical spectra because of the ability to measure and quantify the emitted optical modes of a VCSEL. It is measured by fiber coupling emitted light into an Optical Spectrum Analyzer (OSA). Figure 5.2 below illustrates the typical optical spectra. It also confirms how misalignment affects performance, where the device operates with a maximum SMSR of 3.07 dB at an injection current of 10 mA. Therefore as expected, in this case the anti-phase coating is not able to suppress lasing of higher-order modes.

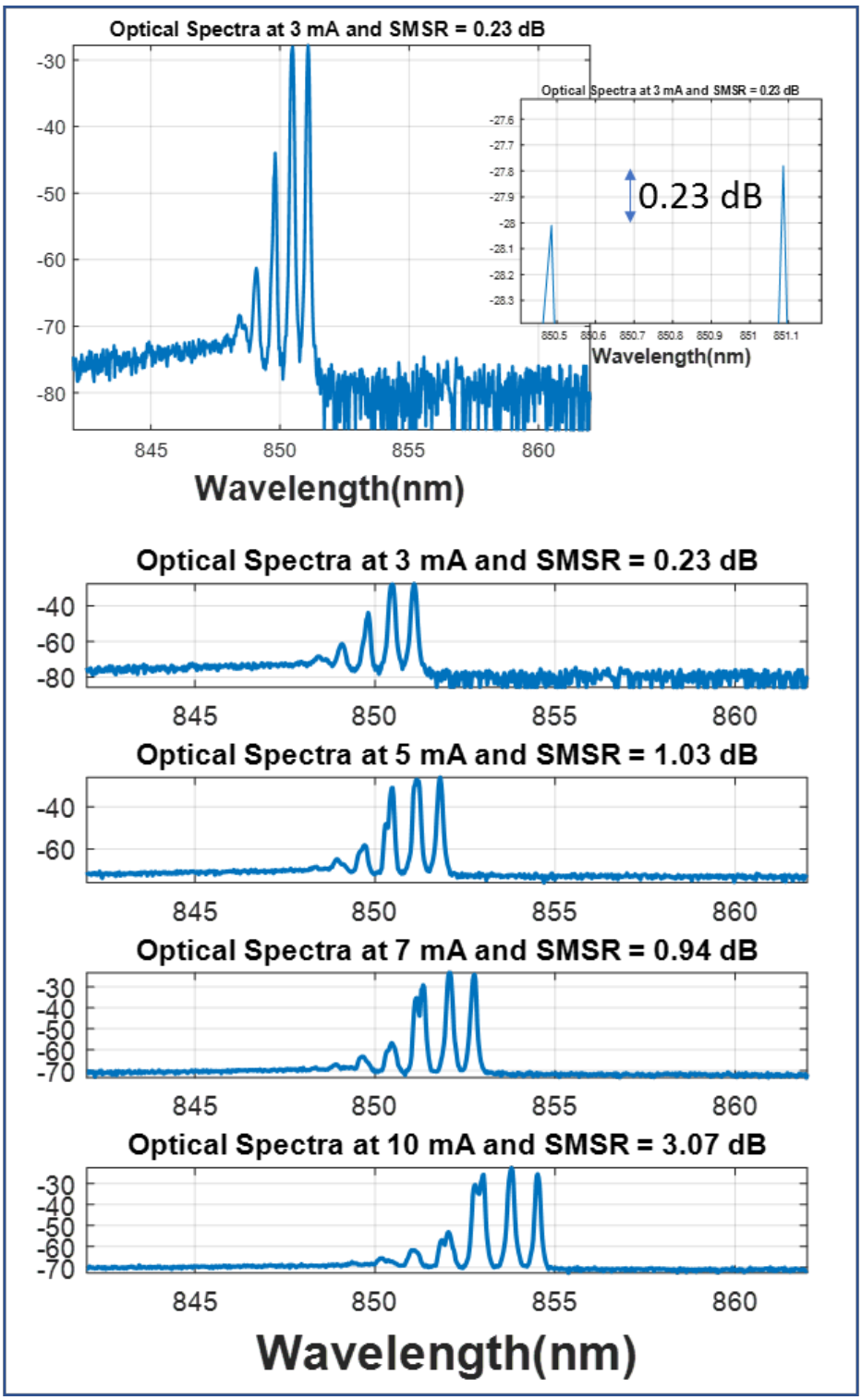

Figure 5.2: Optical spectra of misaligned VCSEL with anti-phase coating operating in the multimode regime over the entire current injection range, indicating no higher-order mode suppression. (Top right) SMSR of 0.23 dB at 3 mA injection current, where the right mode is the fundamental mode and the left mode is the next highest-order mode.

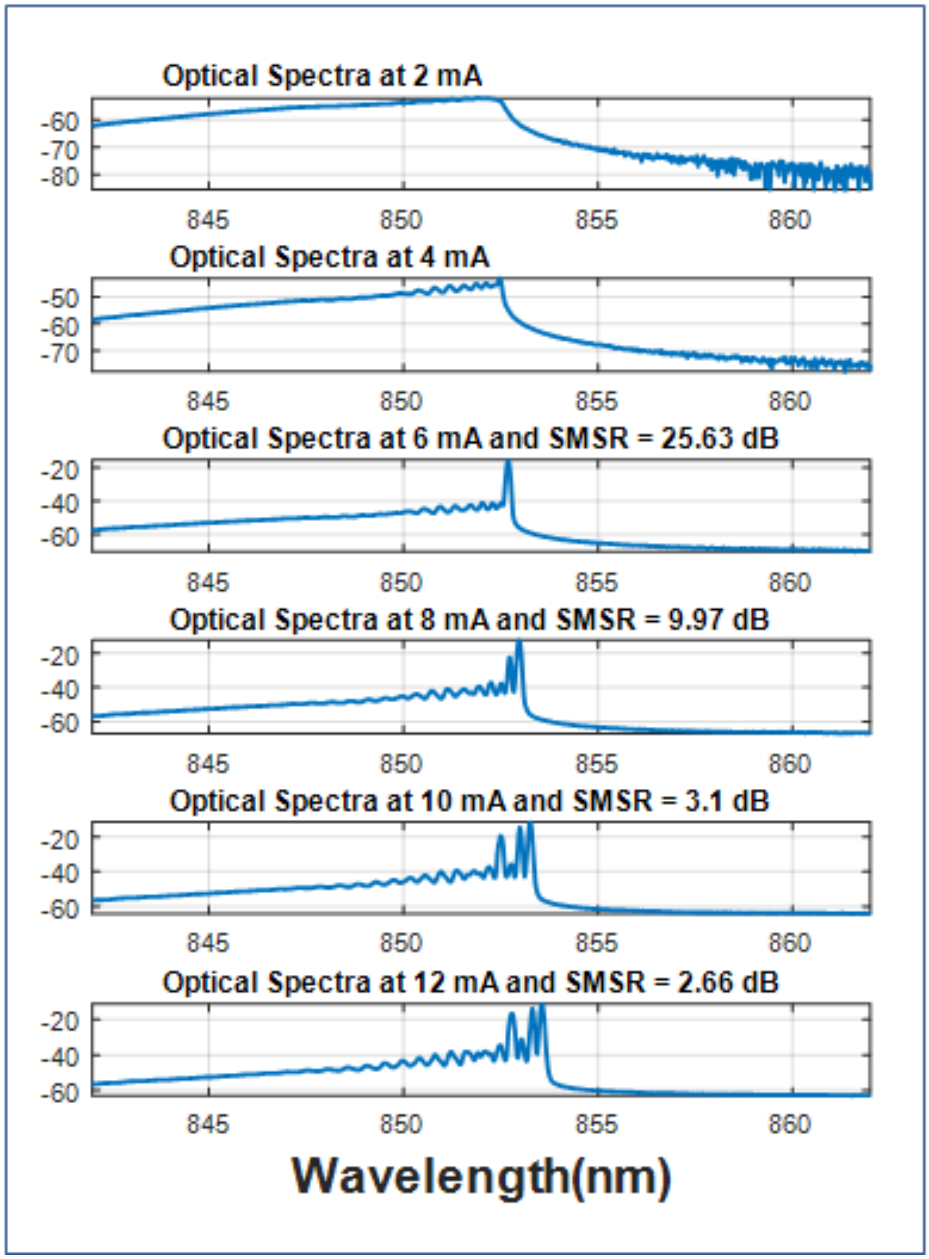

Figure 5.3: Optical spectra of multimode VCSEL with anti-phase coating operating with a maximum SMSR of 25.63 dB, indicating too large of an aperture to suppress higher-order modes.

Correct alignment of the VCSEL structures occurs in Figure 4.4, where the mesa, p-contact and interconnect layer form concentric circles not impinging on the emission aperture.

For devices meeting alignment specifications, further analysis of optical spectra and power output can be completed. As mentioned before, deter-

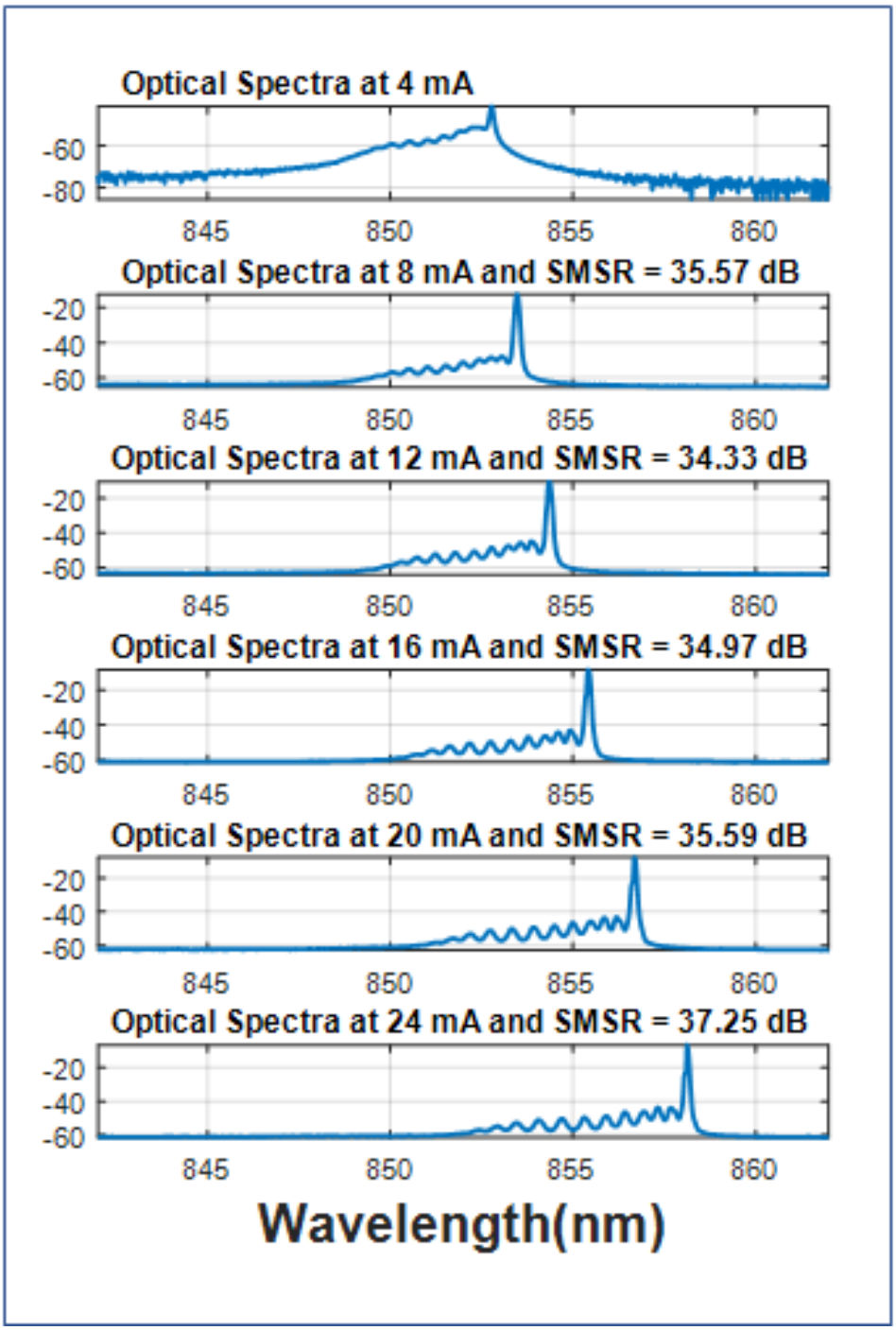

Figure 5.4: Optical spectra of single-mode VCSEL with anti-phase coating, indicating good suppression of higher-order modes with a minimum SMSR of 34.33 dB.

mining the appropriate the anti-phase coating aperture size is important to balancing optical power and single-mode operation. An example of a multi-mode VCSEL optical spectra can be seen in Figure 5.3, where the injection current ranges from 2 mA to 12 mA. At injection currents of 2 mA and 4 mA, the device is still lasing spontaneously hence the lack of a discernible mode peak. However once the device begins to lase at an injection current of 6 mA, the device operates with a SMSR maximum value of 25.63 dB and drops to 2.66 dB as more mode competition occurs and higher-order modes begin to lase. This device had an oxide aperture of 20.5 μm with a 5.7 μm anti-phase coating aperture. While this shows improvements over other purely multimode devices, the data suggests that a smaller coating aperture is still needed.

A noteworthy effect illustrated in the optical spectra curves shown is the red-shift of the fundamental mode and operating wavelength. VCSEL lasing is determined by the gain spectrum overlap with the mode spectrum of the VCSEL. Because a VCSEL is a Fabry-Pérot cavity with a certain free spectral range (FSR), the modes with the highest overlap with gain spectrum lase. However, as more current is injected into the cavity, cavity heating leads to a red shift of both the gain and the FSR. In this case of the latter, this is attributed to heating altering the refractive indices of the active region materials, therefore altering the cavity and the FSR. Furthermore, thermal effects increase the energy bandgap of semiconductor materials (Varshni Equation, [40]) altering the gain spectrum. Eventually, the gain spectrum out shifts the FSR leading to thermal rollover of the optical power curve (see high injection current regions in Figures 5.5 and 5.6). Figure 5.4 shows the optical spectra family of curves of a VCSEL with an appropriately sized coating aperture. This device has an oxide aperture of 10.5 μm with an anti-phase coating aperture of 2.4 μm. Over the whole injection current range of operation from 4 mA to 24 mA, the device maintained a minimum SMSR of 34.33 dB, well over the threshold for single-mode operation. This data indicates that decreasing the anti-phase coating aperture ensures great higher-order mode suppression. The L-I-V curve of this device is presented later in the next section.

5.2 L-I-V Family of Curves

Once devices are characterized for their higher-order mode suppression performance, optical power and voltage characteristics are measured via Light-Current-Voltage (L-I-V) curves. As the device is swept over a current range, the voltage across the device is measured via probes contacting the p- and n-contacts. Additionally, a broad-spectrum silicon photodetector with a collimating hemispherical lens attachment is placed overhead the device, capturing the emitted light. Processing of the I-V curve allows for the procurement of several parameters, including differential series resistance and wall-plug efficiency while the L-I curve provides slope efficiency, threshold current, and maximum optical power. Figure 5.5 below shows an L-I-V curve of a few-moded device, meaning that while not performing single-mode past 15 mA of injection current (white circle mark), only the first few modes of the device lase. The maximum optical power of the device while operating single-mode and few-mode is 4.4 mW and 11.6 mW, respectively. These results aid in confirming the effectiveness of the anti-phase coatingwith room for improve-

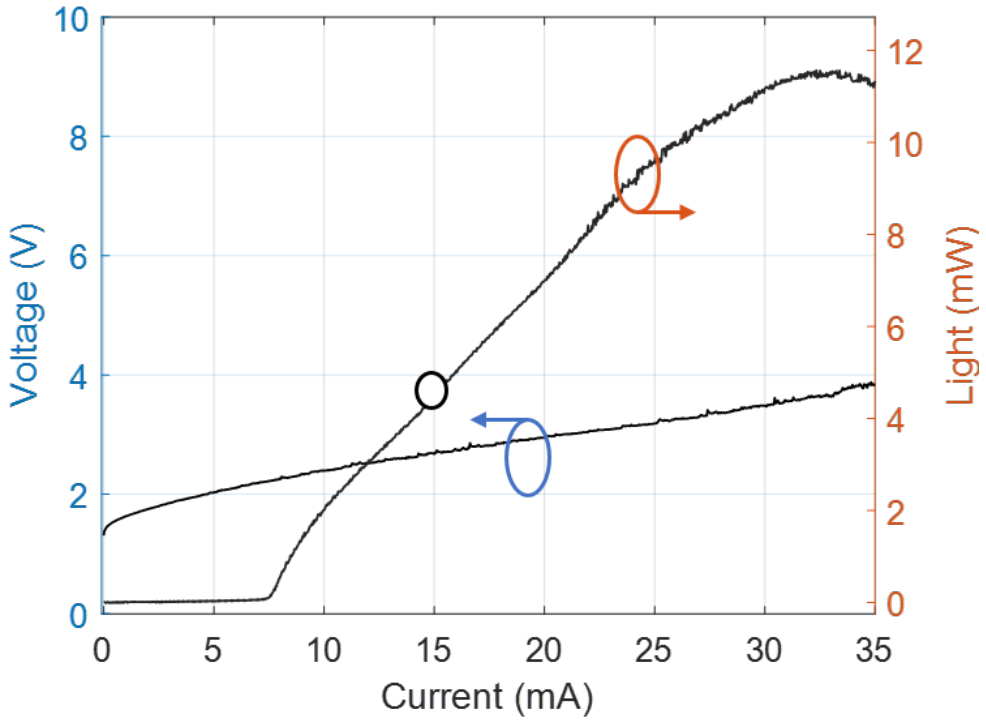

Figure 5.5: L-I-V curve of multimode VCSEL operating single-mode below 15 mA of injection current and multimode above.

ment due to the lack of single-mode operation over the whole injection current range.

This large power can be attributed to several factors. A larger-than-expected oxide aperture allows for increased current injection and supported mode (confirmed by the high threshold current, see kink in L-I curve). Additionally, in order to increase differential series resistance and enhance device performance, the devices presented in this work had Zinc shallowly diffused into the top p-type DBR. Due to the presence of only a few lasing modes and strict mode competition, the L-I curve has a visual dip at the 15 mA mark where the first higher-order mode begins to lase.

To fully illustrate the effectiveness of the anti-phase coating, the L-I-V curve of the single-mode VCSEL used in Figure 5.4 was measured and shown in Figure 5.6. First, note the effect of both the smaller oxide aperture and anti-phase coating aperture on the threshold current that decreases from 7.3 mA to 4.2 mA, indicating electrical carriers are funneled into the active region more effectively. Due to the lower threshold modal gain of the fundamental

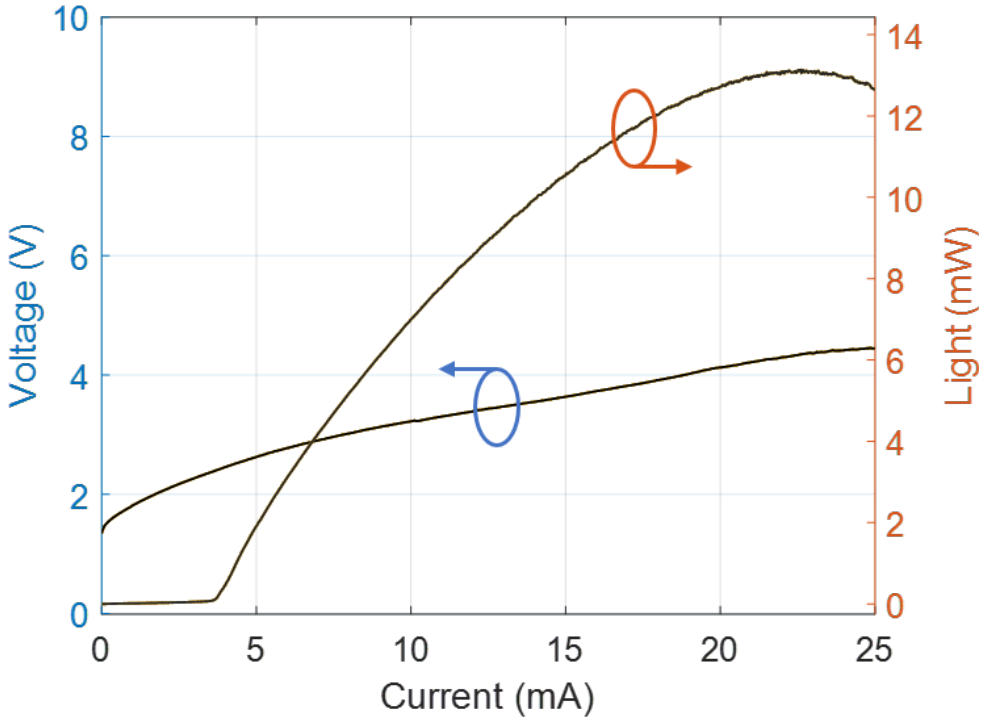

Figure 5.6: L-I-V of VCSEL operating single-mode over the whole injection current range, achieving maximum single-mode power of 13.1 mW.

mode compared to the higher-order modes, the fundamental mode is able to lase more easily. The maximum output optical power of this single-mode VCSEL reaches 13.1 mW, higher than the previously mentioned few-mode device while maintaining good single-mode operation. These results surpass the highest single-mode VCSEL reported in literature to date [41], indicating the importance and power of the anti-phase coating.

5.3 Near-Field Beam Profile

The last performance characteristic needed to fully analyze these VCSELs is the near-field beam pattern. This measurement ensures the confirmation of the lasing of the fundamental mode due to its smooth gaussian shape. This measurement is done by imaging a lasing VCSEL via a CMOS camera with two combined attenuators (OD3 and OD6). By effectively making an OD9 attenuator that reduces the amplitude of the optical power by 10^9, a clear image can be taken that avoids saturating the camera. The image is then

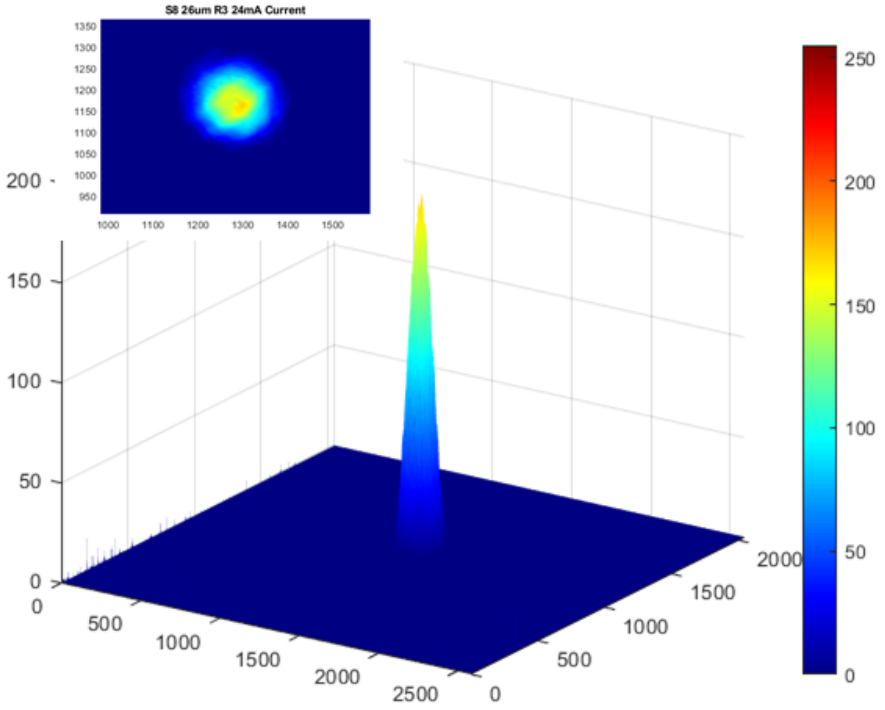

Figure 5.7: Near-field profile of single-mode VCSEL illustrating fundamental-mode lasing (inset: top-down view).

pixelated with a standard image processing package found in a commercial and academic software package. The near-field profile is shown in Figure 5.7, where the smooth beam shape of the fundamental mode is shown. Due to the in-focus beam and attenuator, the amplitude of the peak is purposely set below the maximum amplitude (red color) of the legend. The top down image shows the circular symmetry of the emission beam that peaks in the center. This is the last confirmation needed to show single-mode operation of the VCSELs.

CHAPTER 6

CONCLUSION

VCSELs have emerged as a favorite for many next-generation applications in 3D sensing and LiDAR, high-speed optical communication systems, and AR/VR applications due to their many inherent device characteristics. However, these applications demand enhanced performance from VCSELs in regards to optical power output and single-fundamental transverse-mode operation. This work presented a mode-control method called an anti-phase coating that enabled increased performance by preferentially lasing the fundamental mode while suppressing higher-order modes. Moreover, by understanding the transverse mode profile of a VCSEL cavity and simulating the base VCSEL structure via TMM, it was determined that a silicon anti-phase coating in the shape of annulus best met the requirements to ensure single-mode operation. It was found that by adding an additional $\lambda/4$n layer in the outer regions of the VCSEL device where the higher-order mode reside, an anti-phase standing wave was generated, decreasing the optical confinement factor Γ and raising the threshold modal gain g_{th} of the higher-order modes. Afterwards, VCSELs were fabricated and oxidized using a standard VCSEL process flow and characterized for optical power and SMSR. Furthermore, appropriately setting the annulus aperture size to maximize fundamental mode emission while suppressing higher-order modes achieved an optical power amplitude of 13.1 mW while remaining single-mode (SMSR $>$ 30 dB) over the entire operation range. The ease of implementation and fabrication of the anti-phase coating makes it a very attractive solution to ensure single-fundamental mode operation in the next generation of VCSELs.

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