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WHERE THE CHIP MEETS THE BOARD

Distributed-Physical-Based Transmission-Line Model of PCIe5 Connector for SI Fast Diagnosis

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Abstract

Trade-off between accurate simulation and fast signal-integrity diagnosis is one of the major challenges for high-speed connector design. FEM is commonly used to analyze high-frequency devices despite time-intensive iterations. In this work, a novel design tool is developed with distributed physical-based transmission lines (dPBTLs) for fast simulation, enabling localized failure analysis and time-efficient modifications. The dPBTL is used to predict electrical performances up to 60 GHz for PCIe 5.0 CEM (sub-)sections with/without AIC and baseboard. The dPBTL also demonstrates its potential in facilitating design modification and SI improvement for identifying resonance root causes, loss mechanisms, and reducing design cycle.

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Yulin He received the B.S degree and is currently enrolled in the direct Ph.D. program in electrical engineering at the University of Illinois at Urbana–Champaign (UIUC). She joined HSIC group led by Prof. Milton Feng in 2019. Her primary research area is the development of InP-based DHBT devices for millimeter-wave amplifications and signal integrity diagnosis for 5G electrical links. She was awarded John Bardeen Undergraduate Award in 2020, James M. Henderson Fellowship in 2021, and Ernest A. Reid Fellowship in 2022.

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I. Introduction

The technology advances in cloud computing, artificial intelligence, machine learning, 5G and other applications require a large amount of data traffic within data centers nearly tripled in the past 5 years. To support the blooming data traffic, the development of better high-speed and energy-efficient electrical links is required. Thus, PCI Express (Peripheral Component Interconnect Express) as the standard interface for connecting high-speed hardware to the motherboard has its bandwidth increasing rapidly to enable faster processing and data transferring. To analyze and address the signal integrity (SI) issues, full-wave simulators such as Ansys HFSS are commonly deployed to provide accurate scattering-parameter (S-parameter) estimations of losses and crosswalks using finite element method (FEM). However, broad bandwidth and mm-wave frequency requirements for high-speed data rate transfer cause a dramatic increase in simulation time and lead to a long cycle time for designers. Moreover, it is critical to not only generate S-parameter results but also identify the root cause of crosstalk for SI failures such as undesired resonances and loss mechanisms in high-speed connectors.

To facilitate the design optimization and achieve fast SI diagnosis, distributed equivalent circuit models are developed based on the physical structures of the connector with sectional analysis. This physical-based transmission line (PBTL) model can directly interpret the distributed and dispersive issues in equivalent circuits. Segmentation of the PBTL models will allow separate analysis and local variations on the subregions of interest in a time-efficient way. Cascading the PBTL subsystem will create a distributed PBTL (dPBTL) system for a larger structure with greater complexity.

This paper will report the development of dPBTL systems for different subsections of PCIe 5.0 Card ElectroMechanical (CEM) connector for analysis up to 64 GHz. This fast-diagnosis methodology study will shine the light on PCIe's future development above 24 GHz defined by the current specifications [1]. The segmented frequency-dependent dPBTL models are used to accelerate SI diagnosis with accurate predictions of electrical performances and physical interpretations in each subsection of PCIe 5.0 connector. Section II shows the development of the dPBTL models for PCIe 5.0 connector with discrete steps. Section II.1 exhibits qualitative and quantitative analyses along the PCIe 5.0 connector structure with the identification of location-specific and frequency-dependent phenomena. And the interactions between AIC and CEM connector (abbreviated as CEM in this paper) are demonstrated. To provide flexibility in local modifications and enable microscopic SI diagnosis of CEM, add-in-card (AIC), and baseboard (BB), the subsections of CEM mated/unmated with AIC or baseboard are evaluated and modeled in the structure-specific dPBTLs. Thus, the intrinsic CEM subsections are converted to the equivalent intrinsic dPBTL circuit systems in section II.2.a. Section II.2.b then shows dPBTL modeling for CEM under different mating conditions which involve individual and combined effects of AIC and/or BB.

By integrating sectional PBTL subcircuits into the cascaded dPBTL system models, signal integrity issues can be pinpointed via the comparisons of 3-D HFSS performances and 1-D equivalent circuit parameters. The intrinsic CEM dPBTL model, the PBTL

subcircuit segments for AIC and BB, and mating couplings are constructed and validated, thus forming the basis and fingerprints for the PCIe 5.0 connector.

In Section II.3 we integrate the segmented dPBTL subsystems to form a complete distributed equivalent circuit system and accurately predict losses and crosstalk for the PCIe 5.0 connector. A simple design modification of AIC is done under insightful guidance (pathfinder) from fast dPBTL modeling to effectively improve the SI performances of the PCIe connector.

II. Development of Distributed Physical-Based Transmission-Line Model (dPBTL) for PCIe 5.0 Connector

As shown in Figure 1, the full PCIe connector model experiences variations in pin dimensions and housing dielectric materials as well as changes in ground references from boards to CEM. Although FEM simulators can provide accurate S-parameter results with proper setups for the 3D model, the complex connector structure is treated as a "black box" with only information on input and output waves. Performing signal integrity diagnosis only based on the S-parameters is challenging. Moving from "macroscopic" analysis to "microscopic" diagnosis, running field analysis to scan over the entire frequency band is straightforward yet consumes a tremendous amount of time and disk space. Therefore, we transform the complex 3-D PCIe structure into a 1-D circuit to (1) reduce simulation time, (2) facilitate SI diagnosis with structure-specific equivalent parameters, and (3) enable fast design optimization with enhanced flexibility.

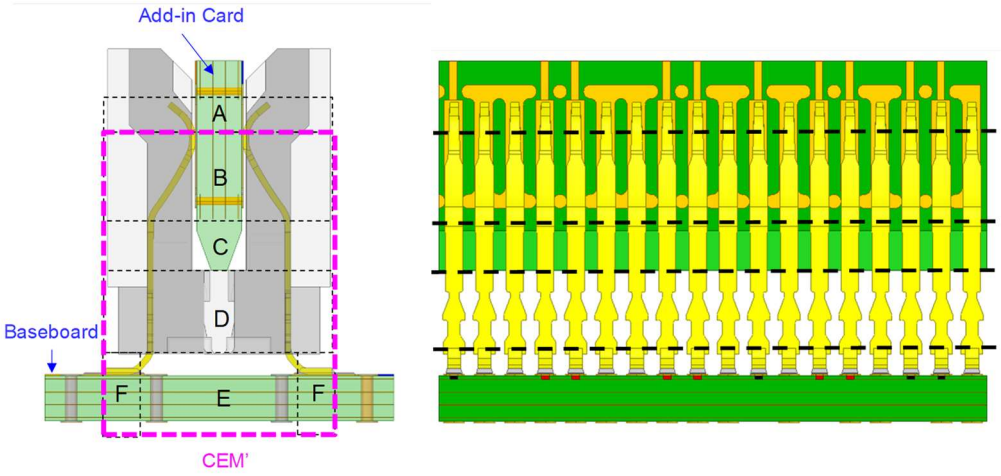

Figure 1 Side views of a multi-pair PCIe 5.0 connector: CEM' with Add-in Card and baseboard; housing are hidden to show CEM pin structures.

To reduce the 3-D structure of PCIe 5.0 to a 1-D circuit, different sections are identified and considered based on structure discontinuities and mating (or loading) conditions. The CEM connector is mated with AIC and baseboard as labeled in Figure 1. After examining the structure (shown in Figure 1), we identify the major subsections of CEM connector main body with different mating cases for subsequent systematic analysis and modeling.

Here, the whole area of subsections is defined as CEM', listed in Table 1. AIC mating effect should be considered in CEM B and CEM C subsections. We also need to discuss the performance of CEM E and CEM F with and without the baseboard separately. Therefore, the effect of CEM itself can be distinguished from the perturbations of AIC and baseboard. In each subsection marked in Figure 1, the effective parameters will be estimated and input into the corresponding segments of physical-based transmission line (PBTL) models which will be cascaded to form the distributed PBTL (dPBTL) system for the complete connector. The equivalent dPBTL subsystem of a certain subsection in PCIe 5.0 connector will directly carry the information revealing the related physics such as delay, loss, impedance, etc. As the CEM being mated and unmated with boards affects field confinement and wave propagations, different physical-based parameters will be used in the corresponding PBTL-circuit units. For simplification, the mutual couplings between adjacent subsections of the connector are neglected.

An established set of dPBTL systems will eventually consist of PBTL subsystems for intrinsic CEM (without AIC and baseboard), extrinsic segments for mated AIC and baseboard, and a complete dPBTL system with intrinsic CEM subsystems combined with and perturbed by extrinsic segments. Therefore, a set of dPBTL systems offers higher flexibility and detailed SI interpretations compared to FEM simulation on the PCIe-connector full model. Designers are able to examine and modify any internal structure and tweak the physical-based parameters for optimal performance. In the later sections of this paper, we will show how dPBTL models are developed from the simplest CEM subsections to the PCIe connector, progressing from unmated intrinsic CEM to CEM mated with external parts.

CEM' Subsection	AIC	Baseboard
B	Mated/Unmated	Unaffected
C	Mated/Unmated	Unaffected
D	Unaffected	Unaffected
E	Unaffected	Mated/Unmated
F	Unaffected	Mated/Unmated

Table 1 CEM' subsection table: BCDEF subsections with AIC and baseboard mating effect considerations. Subsections that require a separate analysis of the connector mated and unmated are labeled in the table

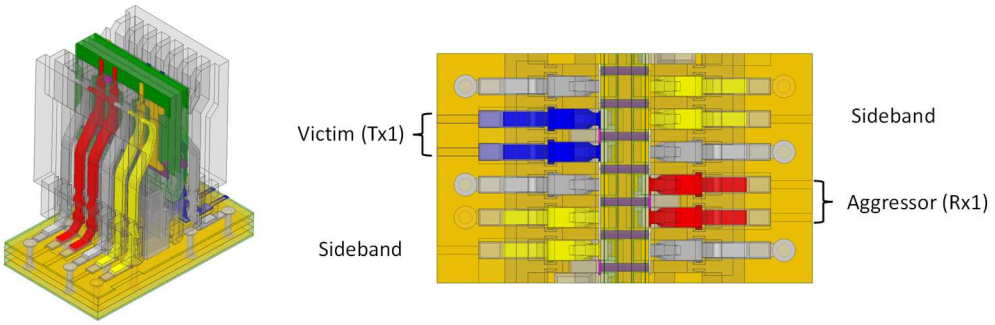

Figure 2 Reduced PCIe 5.0 model with 2 GSSG pairs (with 85 Ω reference differential impedance) and two sideband pins terminated with 42.5 Ω.

For improving simulation efficiency, the full model with 7-differential pairs PCIe 5.0

connector is simplified to a reduced model with 2-differential pairs (2xGSSG) which can still be analyzed concerning its differential-differential insertion loss (DDIL), DD return loss (DDRL), and DD near-end crosstalk (DDNEXT) at AIC side. The reduced 3D model is shown in Figure 2. This reduced 3D model can decrease the simulation time by 3X. Maintaining the basic ground-signal-signal-ground (GSSG) unit helps preserve the electrical performance with minimal errors compared to the larger PCIe model. Figure 3 shows the comparison of DDIL, DDRL, and DDNEXT for the same pairs simulated using reduced PCIe (1x Tx and 1x Rx) and larger PCIe (4x Tx and 3x Rx pairs). The DDIL and DDRL are nearly identical up to 64 GHz. The major resonance spikes are captured by the reduced 3D model up to 24 GHz. The deviation in lower-frequency DDNEXT magnitude and dislocation of small resonances above 30 GHz can be attributed to the truncated adjacent pairs. The later SI analysis and dPBTL modeling will be based on this reduced PCIe model and its subsections: CEM CD (subsections C+D), CEM BCD (subsections B+C+D), and CEM main body (CEM'-- subsections B+C+D+E+F). The effect of the CEM tip portion (CEM subsection A) will be addressed in sectional analysis and added to the dPBTL system for the PCIe connector model.

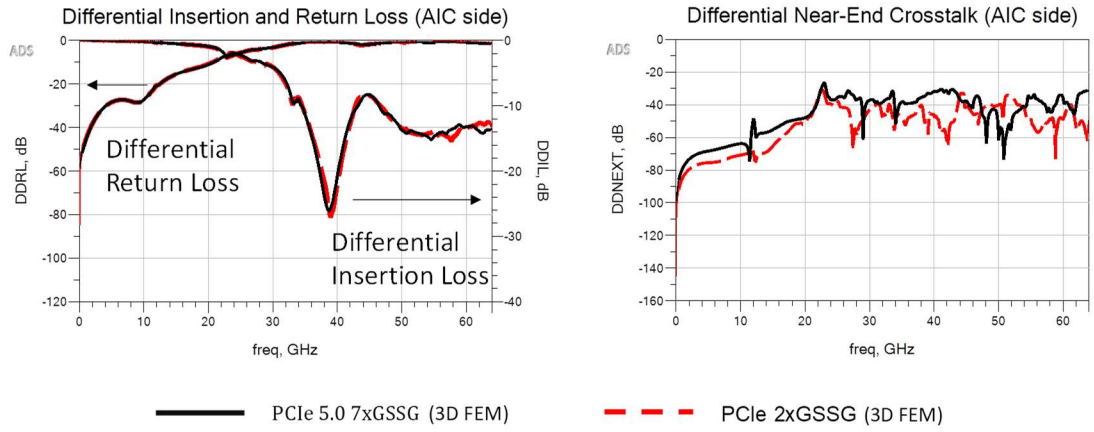

Figure 3 Comparison of simulated results on same pairs from a 7-pair PCIe (4 pair Tx GSSG and 3 pair Rx GSSG) and PCIe reduced to 2 pairs(1 pair Tx GSSG and 1pair Rx GSSG).

1. Sectional Analysis

With the multi-channel PCIe model reduced to two-channel pairs, detailed sectional analysis and segmental PBTL modeling can be done. Extraction of the effective dielectric constant (or effective relative permittivity $\varepsilon_{r,eff}$) and effective loss tangent ($tan\delta_{eff}$) as well as the characteristic differential impedance (Z_{dd}) is achieved using Ansys 2D extractor and ADS Controlled Impedance Line Designer. In this work, several representative planes along the propagation direction $+x$ are sampled to take major discontinuities into account for PBTL modeling and further SI diagnosis. Four sampled planes are labeled in Figure 4 (a) as examples.

First, an "anatomical" investigation of each section is done through field visualizations. As shown in Figure 4 (b), ground planes in AIC provide good field confinements at AIC/CEM interface (at x_a = 0 mm). The transition from AIC to CEM causes variations in

field confinements. The AIC signal pads after the interface (when x <0) still have the electric fields concentrated and thus behave as competing signals, e.g., seen on plane x_b. When CEM moves away from AIC, the transmission line structure transfers from grounded coupled coplanar waveguide to coupled coplanar waveguide, seen on plane x_c and x_d. The change of field confinements due to the conductor configurations and lossy dielectric substrate will be explained by distributed dPBTL systems in later sections.

Apart from the discontinuities, the frequency dependencies of delay and loss are also of vital importance and can possibly limit the device's performance. The location-dependent dispersion can be visualized by comparing the electric fields at 10 GHz and 30 GHz for the same selected planes as shown in Figure 4 (b) and Figure 5 respectively.

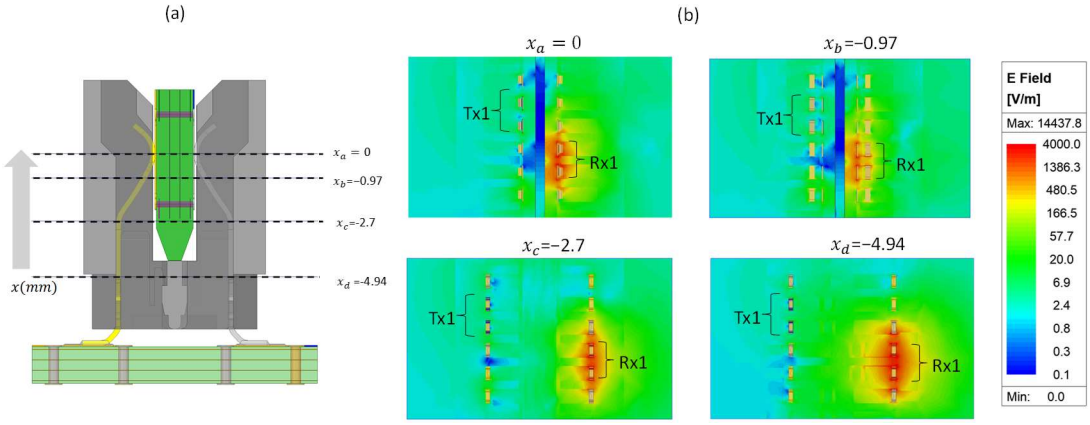

Figure 4 (a) the side view of reduced PCIe 5.0 with representative planes labeled in situ, (b) electric fields plotted (in log scale) on plane x=0, -0.97, -2.7, and -4.94 mm at 10 GHz, with differential Rx1 as aggressor pair, and Tx1 as the victim pair **[1]**.

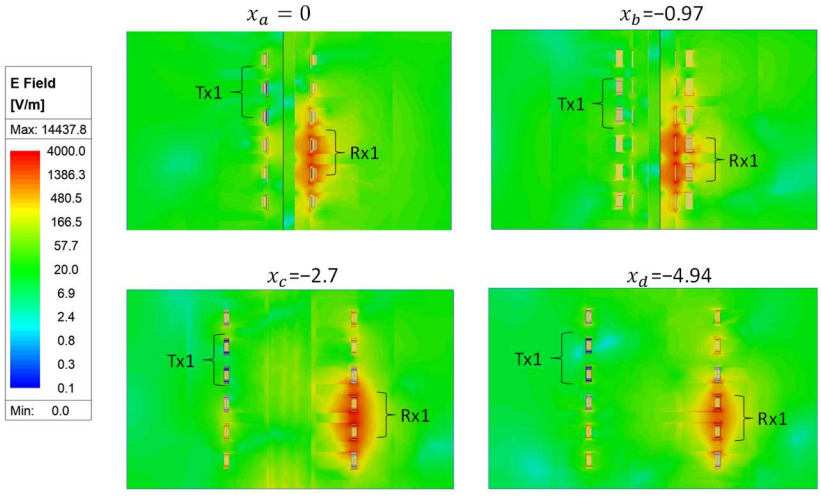

Figure 5 electric fields plotted (in log scale) on plane x=0, -0.97, -2.7, and -4.94 mm at 30 GHz, with differential Rx1 as aggressor pair, and Tx1 as the victim pair **[1]**.

The aforementioned field visualizations qualitatively demonstrate the necessity of distributed and dispersive segmentation. To further diagnose the connector, a quantitative "scanning" along x direction is constructed on not only the reduced PCIe CEM mated with AIC but also the CEM without AIC, and AIC without CEM (using Ansys 2D extractor). The ranges of analysis are labeled in Figure 6. The effect of AIC on CEM and

the effect of CEM on AIC can be then systematically examined. Note that transmission-line parameters of AIC can only exist from AIC feed lines to the end of AIC signal pads (at x_1) and AIC conductors do not exist below x_2.

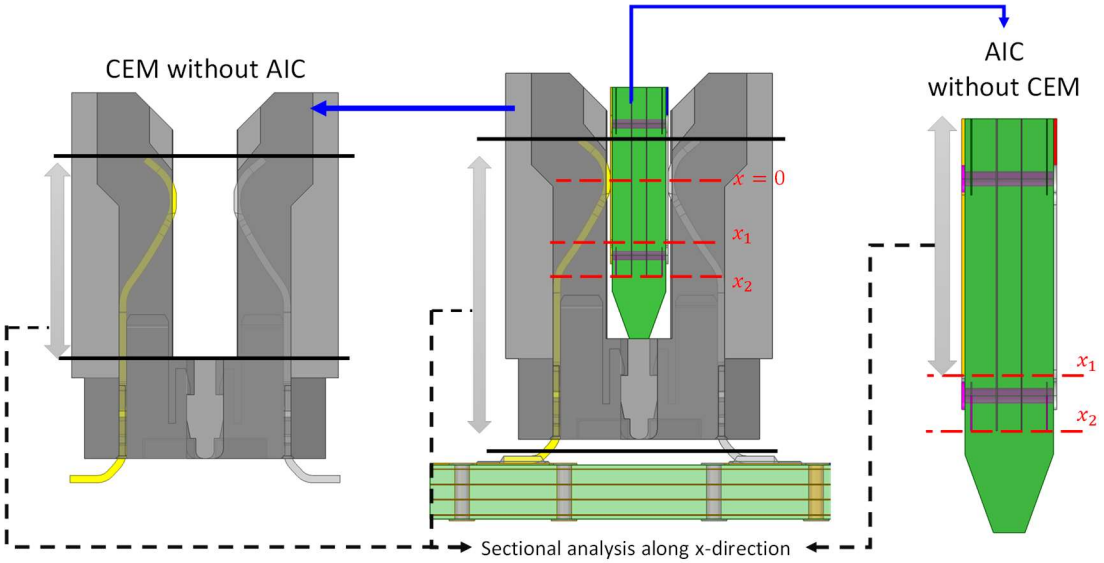

Figure 6 The ranges for sectional 2D analysis for connector alone, connector mated with AIC, and intrinsic AIC. The differential impedance $\boldsymbol{Z_{dd}}$, effective relative permittivity ($\boldsymbol{\varepsilon_{r,eff}}$) and effective loss tangent ($\boldsymbol{tan\delta_{eff}}$) of CEM connector pins (with/without AIC) and AIC pads (with/without CEM) will be extracted in the labeled ranges.

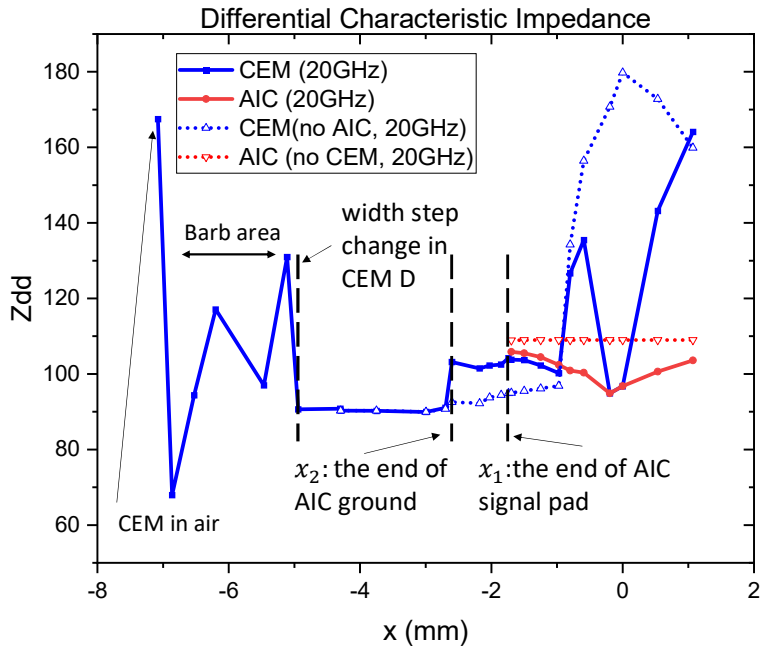

Figure 7 The differential characteristic impedance $\mathbf{Z_{dd}}$ **(20 GHz)** of CEM pins (with/without AIC) and AIC pads (with/without CEM) with labels on major discontinuities.

Figure 7 shows the location-dependent differential characteristic impedances Z_{dd} calculated at sampled planes along x direction using Ansys 2D extractor. As annotated in

the figure, the major impedance discontinuities of PCIe CEM with AIC happen at CEM/AIC interface (around x=0), the end of AIC south ground lateral bar (x =2.6 ~2.7 mm), and the non-uniform CEM barb region (from around x=-5 mm to x =-7 mm in CEM D segment). It is worth noticing that the CEM subsegment fully in the air (CEM E) also gives rise to a large impedance mismatch with the highest impedance and lowest dielectric constant.

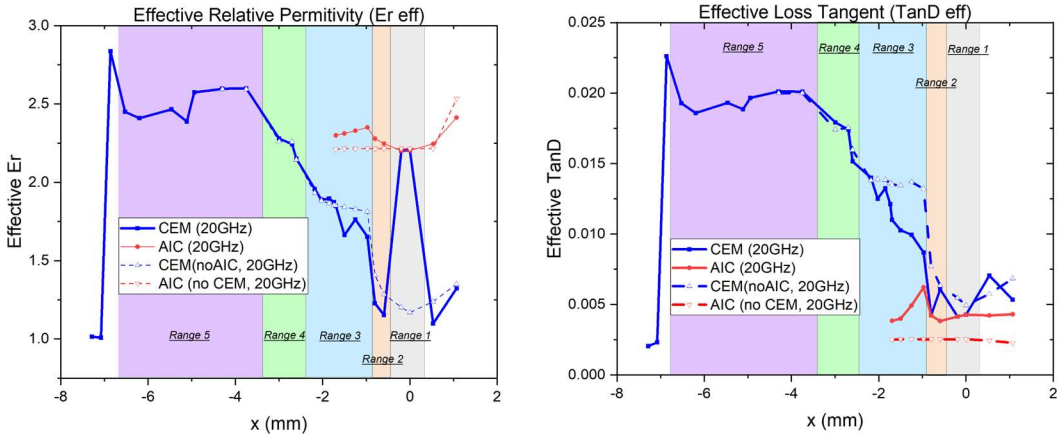

Figure 8 The effective relative permittivity ($\varepsilon_{r,eff}\ (20GHz)$) and effective loss tangent ($tan\delta_{eff}\ (20GHz)$) of CEM pins (with/without AIC) and AIC pads (with/without CEM) with respect to the distance to CEM/AIC interface (x=0), with ranges for later evaluations of averaging dispersive effects.

In addition to impedance mismatch, the dielectric discontinuity is also unneglectable. Figure 8 illustrates the length-dependent effective dielectric constant (or effective relative permittivity $\varepsilon_{r,eff}$) and effective loss tangent ($tan\delta_{eff}$), both evaluated at 20 GHz. Aside from the distributiveness, the dispersive effect should also be quantitively investigated. Ranges labeled in Figure 8 are partitioned based on the trends in the frequency domain. Thus, the average $\varepsilon_{r,eff}$ and $tan\delta_{eff}$ in the major subsections of CEM with AIC inserted are plotted with piecewise linear fitting in Figure 9 and Figure 10 for each x-direction range. Range 3, 4, and 5 (majorly in the CEM BCD subsection) have their averaged $\varepsilon_{r,eff}$ decreasing with frequency and $tan\delta_{eff}$ increasing with frequency (after f_0) due to a highly dispersive housing material.

Since $tan\delta_{eff}$ is related to both attenuation coefficient (α) and $\varepsilon_{r,eff}$ (shown in Equation 1) , the tradeoff between the two parameters determines to trend of $tan\delta_{eff}$. When the increasing trend of attenuation exceeds the decreasing trend of $\varepsilon_{r,eff}$, $tan\delta_{eff}$ will increase along frequency. The slopes $(\dot{tan\delta_{eff}}) = \partial tan\delta_{eff}/\partial f$ and intercept ($tan\delta_{eff,dc}$) of $tan\delta_{eff}\ (range_i, f)$ are listed in Table 2.

$$tan\delta_{eff} = \sqrt{\left(1 + \frac{2\alpha^2}{\omega^2 \mu \varepsilon_0 \varepsilon_{r,eff}}\right)^2 - 1} \quad (1)$$

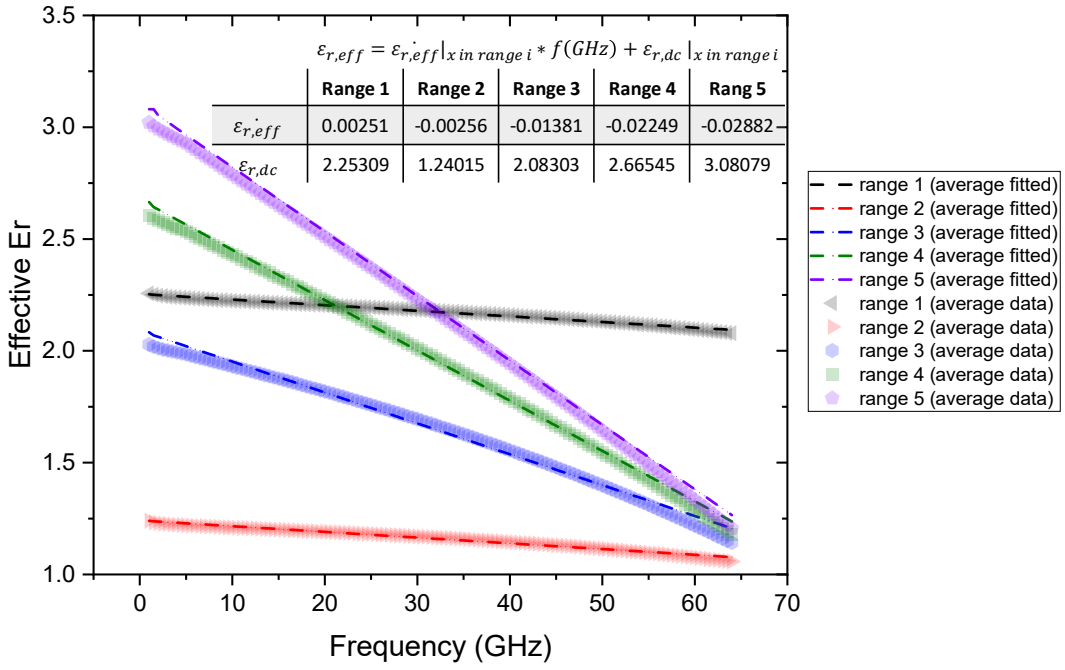

Figure 9 The frequency dependent $\boldsymbol{\varepsilon_{r,eff}}$ $(\boldsymbol{range_i, f})$ extracted in several ranges from CEM (mated with AIC) with average approximation. Tabular Linear fitted slopes ($\boldsymbol{\dot{\varepsilon_{r,eff}}}$) and intercepts ($\boldsymbol{\varepsilon_{r,dc}}$) are listed in the figure.

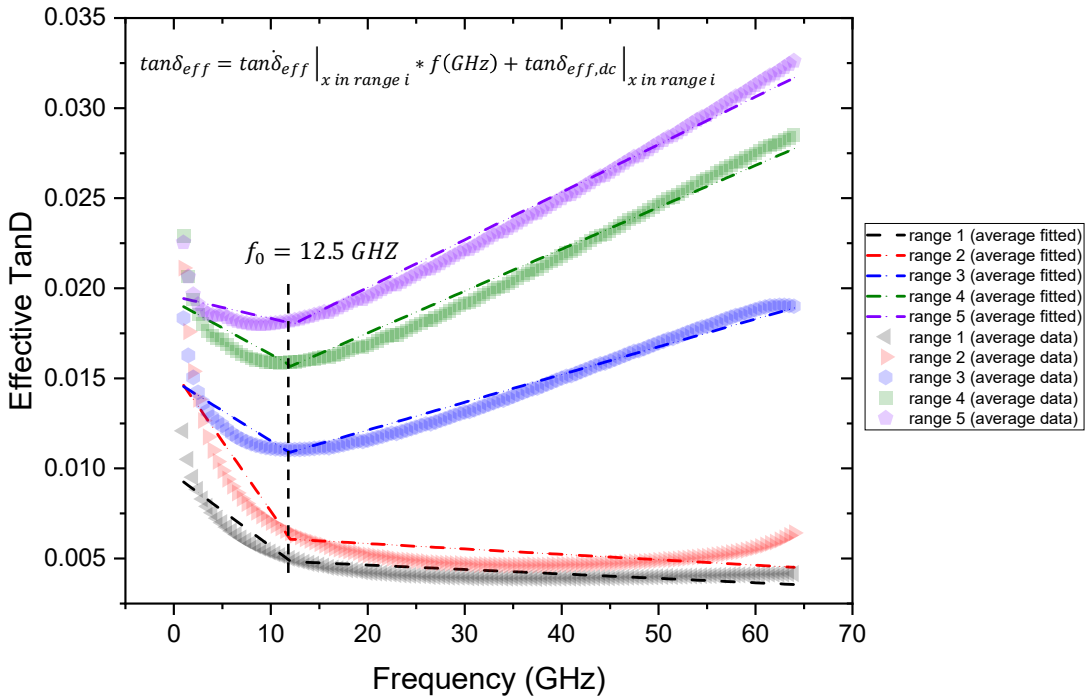

Figure 10 The frequency dependent $\boldsymbol{tan\delta_{eff}(range_i, f)}$ extracted in several ranges from CEM (mated with AIC) with average approximation. Two-segmented piecewise-linear approximation for each range will be used for later PBTL parameterization.

Tabel 2 Tabular piecewise-linear effective loss tangent

	Range 1	Range 2	Range 3	Range 4	Rang 5
$tan\dot{\delta}_{eff}$(f < f_0)	-0.00039900	-0.0007765	-0.000334966	-0.000294059	-0.000122548
$tan\delta_{eff,dc}$ (f < f_0)	0.00965000	0.0153900	0.014880000	0.019270000	0.019550000
$tan\dot{\delta}_{eff}$(f ≥ f_0)	-0.00002464	-0.00002999	0.000154067	0.000232517	0.000264639
$tan\delta_{eff,dc}$ (f ≥ f_0)	0.00513000	0.00643000	0.009050000	0.012870000	0.014750000

2. dPBTL: PCIe 5.0 CEM' and CEM' Subsections

Given the qualitative and quantitative sectional analyses on the connector of interest, a system of dPBTL models can be quickly developed concerning different subsections and (sub)sections under different mating conditions.

Figure 11 shows a 4-port m-segmented lossy dPBTL system feasible for any electrically long structure with distributed and dispersive effects. To be more specific, the preceding sectional analysis yields initial values of effective parameters for the equivalent subcircuits (as PBTL segment) in the dPBTL system. Zooming into the dPBTL system, the i-th PBTL segment with physical length Len_i and differential characteristic impedance Z_{dd} (F_1) will experience frequency-dependent delay and loss, as the equivalent propagation constant γ_i of a transmission line is defined by

$$\gamma_i = j\omega\sqrt{\mu\varepsilon_{c,eff_i}(f)} \tag{2}$$

, where the complex permittivity effective permittivity ε_{c,eff_i} is directly related to frequency-dependent $\varepsilon_{eff_i}(f)$ and $tan\delta_{eff,i}$ (f). Note that characteristic impedance itself is also inevitably dispersive for a lossy transmission line as defined in Equation (3).

$$Z_{0,i} = \frac{j(2\pi f)L+R}{\gamma_i} = \sqrt{\frac{j(2\pi f)L_i+R_i}{j(2\pi f)C_i+G_i}} \tag{3}$$

, where R_i, G_i are related to the total resistive loss and shunt dielectric loss, L_i, C_i are inductance and capacitance of the i-th transmission-line structure. The propagation constant can also be written as

$$\gamma_i = \sqrt{(R_i + j(2\pi f)L)(G + j(2\pi f)C)}\,. \tag{4}$$

Therefore, a PBTL segment contains physical-based information for a specific structure.

Furthermore, physical discontinuities along the connector can be well explained by connecting the segments of PBTLs with non-ideal transitions. Shunt parasitic admittances are used to interpret nonideal ground transitions and fringing effects at discontinuities [2]. For the unmated connector structures, the coupling is mainly due to capacitive couplings through different dielectric materials such as the CEM housing. For PCIe and its CEM subsections with mated boards, additional capacitive couplings occur through the dielectric substrate and inductive couplings occur at the ground vias of the mated boards.

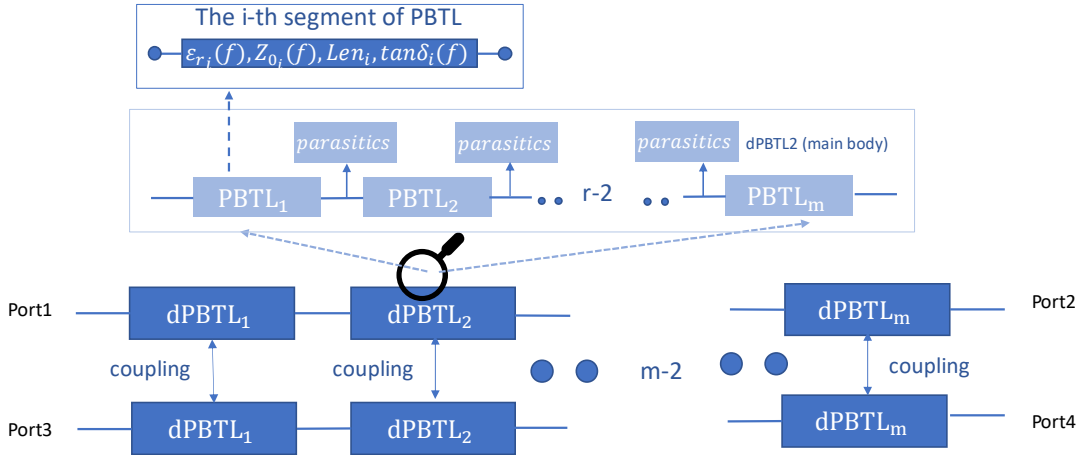

Figure 11 The m-segmented dPBTL system with zoom-in view of the **dPBTL$_2$** subsystem showing the i-th PBTL segment.

2.a dPBTL: Intrinsic PCIe 5.0 CEM'

For intrinsic dPBTL for CEM main body (CEM'), CEM subsections without the mated AIC and baseboard are modeled with the corresponding intrinsic dPBTL system. The abovementioned dPBTL framework is first applied to CEM' unmated subsections, including CEM CD, CEM BCD, and CEM'. The 3D models of the subsections under investigation are listed in Figure 12.

As shown in Figure 7 and Figure 8, the effect of the AIC substrate of the chamfer region is negligible from x=-2.7 mm to x=-4.3 mm (in the CEM C sub-section) concerning Z_{dd}, $\varepsilon_{r,eff}$, and $tan\delta_{eff}$. Therefore, CEM CD$_{unmated}$ (including pins and housing, shown in Figure 12) is converted to a circuit based on the parameters extracted from sectional analysis. Similarly, CEM BCD$_{unmated}$ (seen in Figure 12) has an extra CEM B subsection extended to $+x$ direction. Its equivalent PBTL segment has Z_{dd,CEM_B} slightly higher than Z_{dd,CEM_C} of CEM C segment. The dPBTL subsystem for CEM'$_{unmated}$ simply needs to add one more segment for the bottom CEM pins in the air ($\varepsilon_{r,eff} \approx 1, tan\delta_{eff} \approx 0$) which consequently leads to the highest impedance discontinuity at the bottom side.

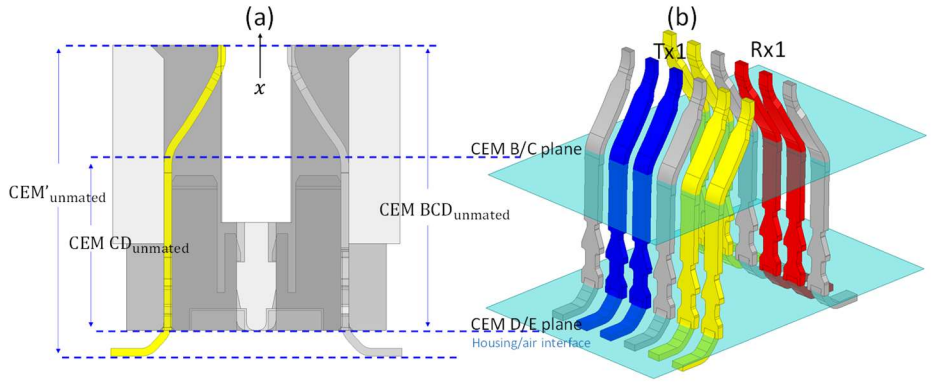

Figure 12 The reduced 3D model of PCIe 5.0 CEM subsections: (a) annotated side view of CEM'$_{unmated}$ with CEM BCD$_{unmated}$, and CEM CD$_{unmated}$ subsections; (b) tilted view of CEM'$_{unmated}$ with CEM B/C plane and CEM D/E plane as housing/air interface, housing structure is hidden for clear display.

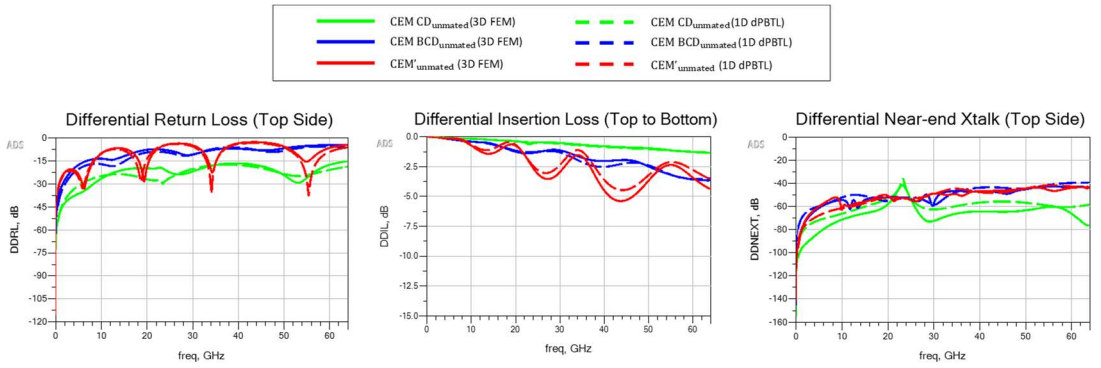

Figure 13 The DDRL, DDIL and DDNEXT of PCIe 5.0 CEM $CD_{unmated}$, CEM $BCD_{unmated}$, and CEM'$_{unmated}$ fast predicted by dPBTL systems and simulated by Ansys HFSS (FEM).

After the implementation of physical equivalent parameters into PBTL segments, differential S-parameter results are calculated from combined dPBTL systems. With reference to the corresponding S-parameters generated by 3D FEM in Ansys HFSS, the PBTL systems provide a sufficiently accurate estimation of losses and crosstalk, as shown in Figure 13. Based on the validated dPBTL circuit setups, we now can attribute the widening of periods in reflections and transmissions to the decreasing $\varepsilon_{r,eff}$ along frequency. This frequency dependency is due to heterogenous medium and dispersive materials which are defined between 1 GHz to 10 GHz and linearly extrapolated to extend the frequency range up to 64 GHz. Further material measurement should be conducted to validate the material datasets and improve simulation to measurement correlation. Nevertheless, the dPBTL method demonstrates its ability to predict electrical performances with distributed and dispersive effects, speeding up the simulation process by 50x. For future modifications on the dielectric properties, designers can simply update the equivalent transmission-line parameters of the corresponding PBTL subsystems after sectional analysis to acquire quick evaluations.

2.b dPBTL: PCIe 5.0 CEM' with Mated Boards

On top of the intrinsic dPBTL models constructed for CEM $BCD_{unmated}$ and CEM'$_{unmated}$, the mating effects of AIC and baseboard (BB) are further investigated. The reduced 3D models of CEM $BCD_{AIC,\ mated}$, and CEM' (including CEM'$_{BB,\ mated}$, CEM'$_{AIC,\ mated}$, and CEM'$_{AIC\text{-}BB,\ mated}$) are shown in Figure 14. The separation of mating cases followed by the formulations of their case-specific dPBTL systems provides a novel insight for localized SI diagnosis, such as the perturbation from mated parts to intrinsic performances.

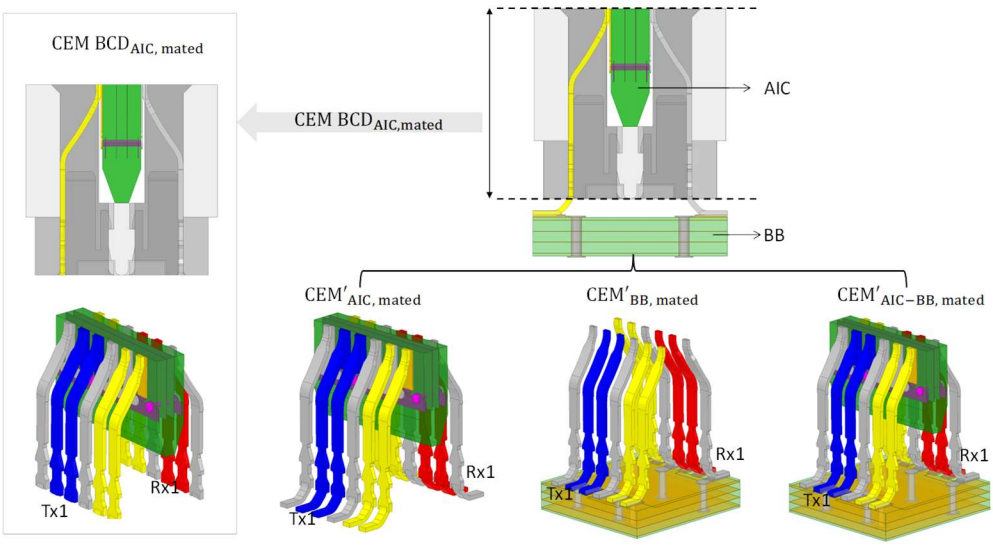

Figure 14 The reduced 3D model of CEM'$_{AIC-BB, mated}$ (CEM'), decomposed to CEM BCD$_{AIC, mated}$, CEM'$_{BB, mated}$, and CEM'$_{AIC, mated}$ with Tx1 and Rx1 labeled. The tilted views are shown with housing structure hidden for clear display.

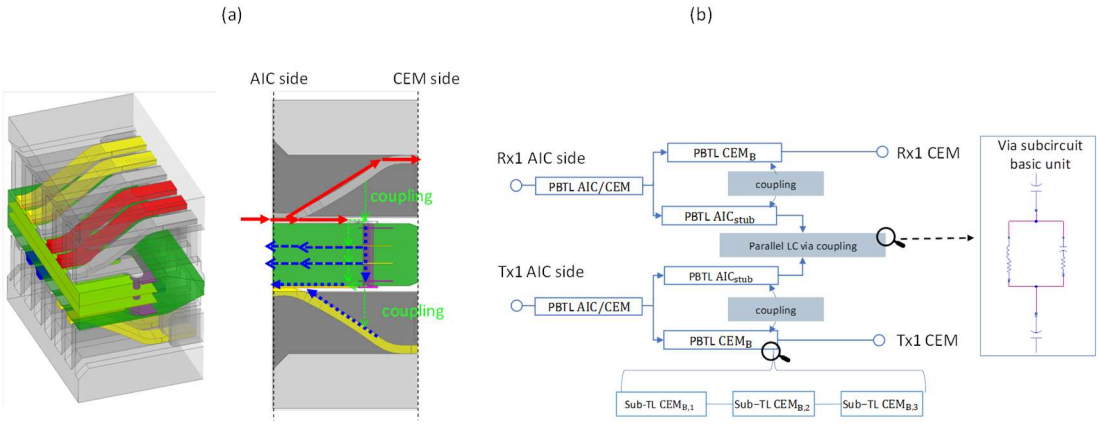

Figure 15 (a) the PCIe subsection showing the mating effect with AIC via couplings and couplings between AIC and CEM; (b) the equivalent dPBTL CEM B$_{AIC, mated}$ subsystem at AIC south side consisting of multi-segmented PBTL CEM$_B$, and shunt PBTL AIC segments along with inductive and couplings through AIC ground vias, capacitive couplings from signal to ground bar and through board substrate. Capacitive couplings also exist between CEM and AIC through housing dielectrics.

Through field visualization and 2D sectional analysis of the mated region, we observed the coexistence of differential transmissions guided in AIC and CEM as illustrated in Section II.1. Therefore, the transmission-line parameters ($Z_{dd,CEM}$, $\varepsilon_{r,ef\ ,CEM}$, and $tan\delta_{eff,CEM}$) of the formerly developed dPBTL systems for the CEM and its subsections are also updated to reflect the influence of inserted AIC on the wave propagation along CEM.

Therefore instead of one uniform PBTL segment for CEM B$_{unmated}$ subsection, a multi-segmented PBTL circuit is employed for CEM B$_{AIC, mated}$ subsections with different $Z_{dd}, \varepsilon_{r,eff}, tan\delta_{eff}$ to approximate the tapering mating effect when CEM pins move away from the interface (evaluated in Section II.1) seen in Figure 15. In addition, a shunt PBTL AIC$_{stub}$ segment is implemented in parallel with the intrinsic PBTL CEM$_B$ as

illustrated in Figure 15 (b). Similarly, CEM also experiences couplings at the baseboard side – through ground vias and ground planes despite the much weaker effect. The major crosstalk due to AIC is modeled as parallel RLC circuits to include capacitive coupling between ground planes through the dielectric substrate and inductive coupling through ground vias interconnecting the aggressor pair and victim pair [3]. The resonance cavities for high crosstalk are formed between the large discontinuities with their discrete return paths related to the resonance frequency [4] [5]. The dPBTL CEM $B_{AIC,\ mated}$ subsystem is validated by simulating circuit alone and comparing the resultant DDNEXT and DDIL with HFSS (FEM) results of CEM $BCD_{AIC,mated}$. Figure 16 demonstrates decent matches of the stub-induced valley in DDIL and major resonance spikes in DDNEXT between the dPBTL subsystem and the 3D FEM model of CEM $BCD_{AIC,mated}$. Later, the validated CEM $B_{AIC,\ mated}$ dPBTL subsystem will replace the intrinsic CEM_B PBTL segment in the full dPBTL circuit model.

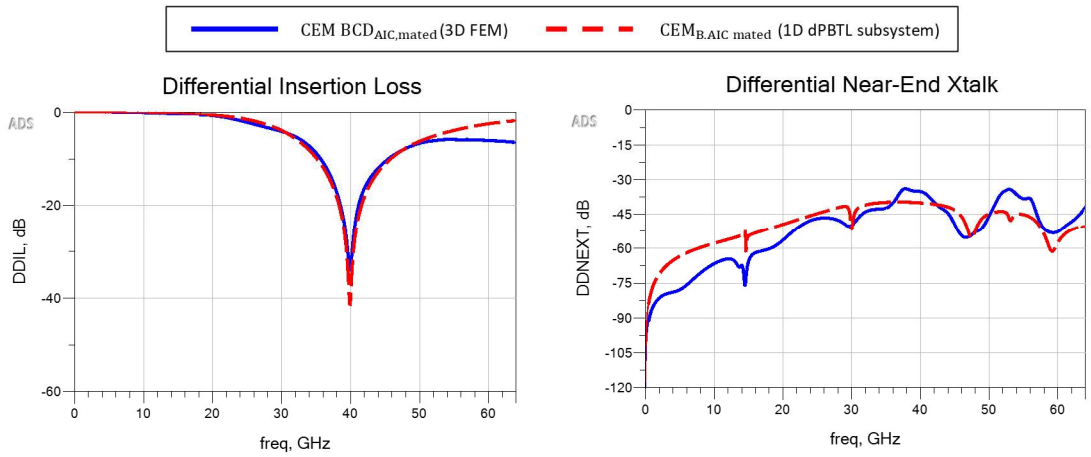

Figure 16 DDIL and DDNEXT results of CEM $BCD_{AIC,mated}$ yielded by 3D FEM and $CEM_{B,AIC\ mated}$ 1D dPBTL subsystem. DDIL of $CEM_{B,AIC\ mated}$ dPBTL is the loss from AIC side to CEM side, and DDNEXT of $CEM_{B,AIC\ mated}$ dPBTL is evaluated at AIC side.

After loading the dPBTL CEM $B_{AIC,\ mated}$ subsystem onto CEM BCD dPBTL system, CEM BCD mated with AIC (CEM $BCD_{AIC,mated}$) can be well interpreted. The mating effect of AIC can be observed by comparing the results of CEM $BCD_{unmated}$ and CEM $BCD_{AIC,\ mated}$, as seen in Figure 17. The match between dPBTL-predicted results and FEM-simulated results proves their accurate equivalence. The resonance at around 40 GHz in differential insertion loss is validated to be directly related to the electrical length of the AIC stub. Equivalently, the unterminated PBTL segment for the AIC stub below AIC/CEM interface ($x < 0$) leads to the reflection coefficient $|\Gamma|$ or the magnitude of return loss approaching one due to quarter-wavelength transformation.

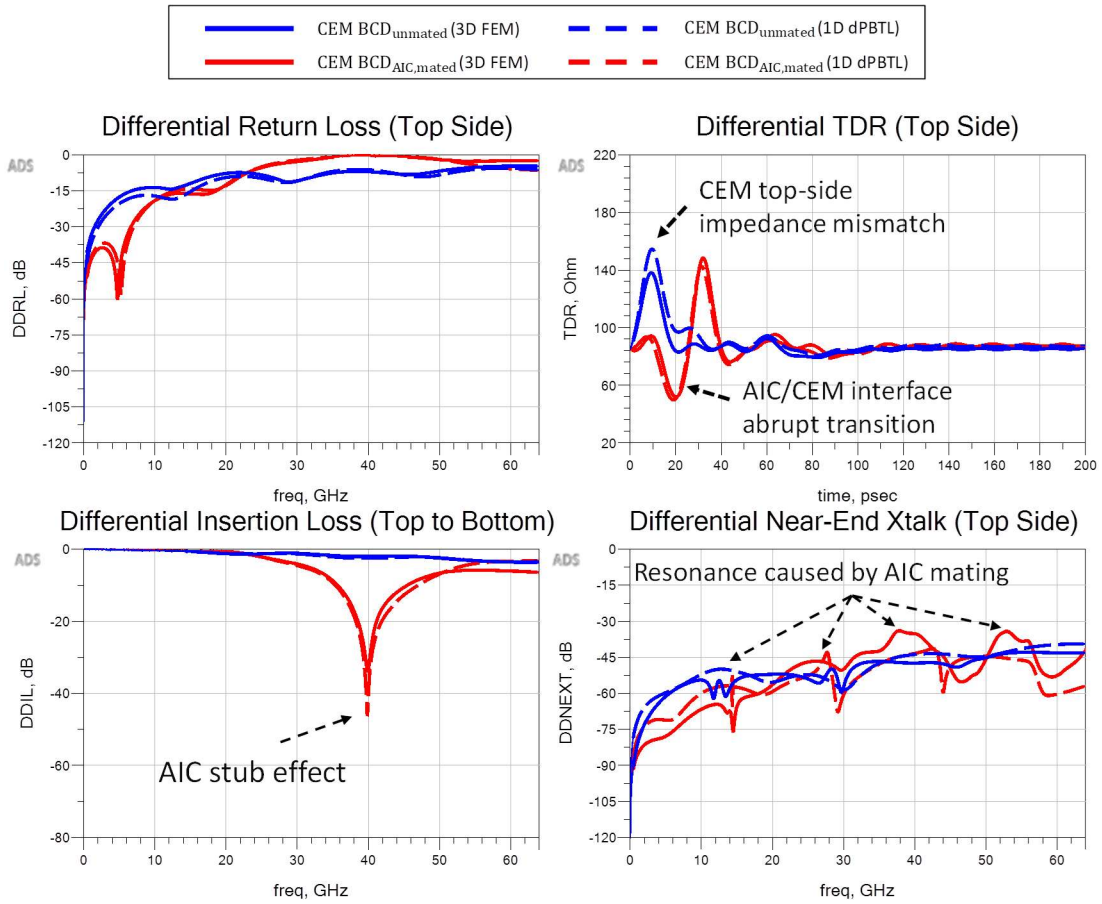

Figure 17 Annotated electrical performances generated by HFSS and fast evaluated by equivalent dPBTL models for CEM BCD$_{unmated}$ and CEM BCD$_{AIC,mated}$. Plots include DDRL, differential TDR transformed from DDRL (normalized to differential 85 ohm with no window function applied), and DDIL of the aggressor pair, DDNEXT at top side experienced by the victim pair.

The substantial change in impedance around AIC/CEM interface is also double confirmed by Time Domain Reflectometry (TDR) directly calculated from DDRL. Inserting AIC into CEM alleviates the large impedance caused by reduced CEM pin size and reduced housing-to-air ratio from around x = -1 mm to x=1 mm. However, the enhanced field confinement provided by AIC further reduces the $Z_{dd,CEM}$ at interface region (from x = -0.19 mm to x = 0.19 mm), creating a large impedance mismatch with maximum difference $\Delta Z_{dd,CEM} \approx 40\ \Omega$. Therefore, both TDR in the time domain and the quantitative Z_{dd} analysis along the x-direction shows the change of impedance transitions. This tapering mating effect is correctly modeled by PBTL CEM$_B$, given the match of TDRs from HFSS FEM and the dPBTL system, seen in the differential TDR curves of Figure 17, comparing CEM BCD$_{unmated}$ and CEM BCD$_{AIC,mated}$.

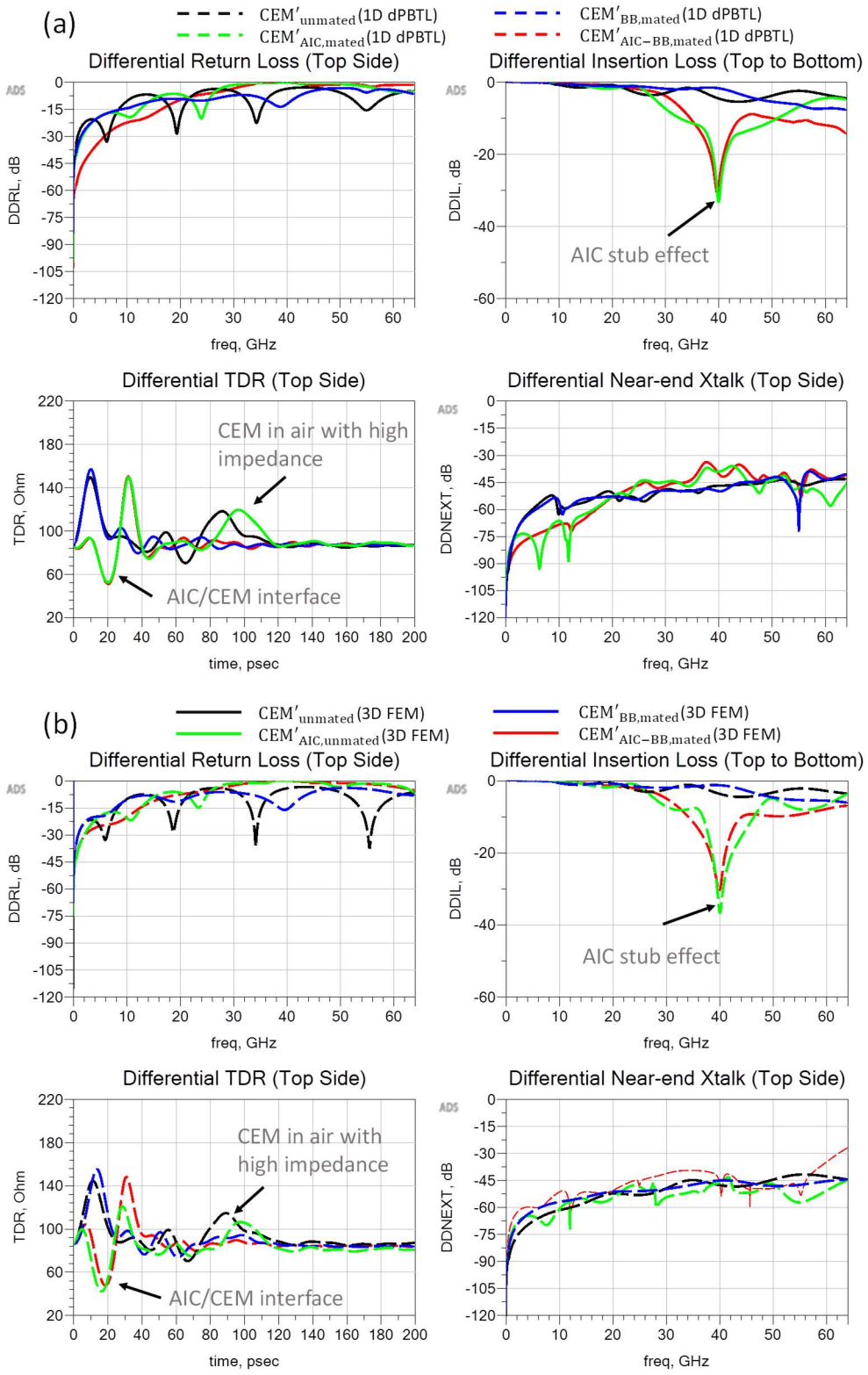

Figure 18 Annotated electrical performance of CEM' under different mating conditions compared with the intrinsic CEM'. Performances include DDRL, DDIL, and differential TDR, of the aggressor pair, and DDNEXT at top side experienced by the victim pair. (a) FEM simulation and (b) dPBTL model simulation on CEM'$_{unmated}$, and CEM'$_{BB,\ mated}$ CEM'$_{AIC,\ mated}$ and CEM'$_{AIC\text{-}BB,\ mated}$.

With the insights gained by preceding analysis and modeling on CEM $BCD_{unmated}$ and CEM $BCD_{AIC,\ mated}$, we then proceed to the main body – CEM'. Referring to Table 1, CEM' has two mated parts to consider: AIC and baseboard. The mating effects of the two boards are first considered and modeled separately. This step will verify previous SI diagnoses and enable localized changes on one board for future designs. Then a combined circuit model is constructed to reflect the performance of CEM' mated with both AIC and baseboard.

Figure 18 shows the S-parameter results and TDRs evaluated by FEM and dPBTL for CEM' under different mating conditions. By comparing CEM'$_{AIC,\ mated}$ and CEM'$_{AIC\text{-}BB,\ mated}$ with CEM'$_{BB,\ mated}$ and CEM'$_{unmated}$, we can easily observe the AIC stub-induced valley in DDIL at around 40 GHz as shown in both Figure 18 (a) and Figure 18 (b). This is consistent with CEM $BCD_{AIC,\ mated}$ (from dPBTL and FEM) and CEM $B_{AIC,\ mated}$ dPBTL subsystem alone given the AIC-stub structure and the equivalent PBTL AIC_{stub} unchanged.

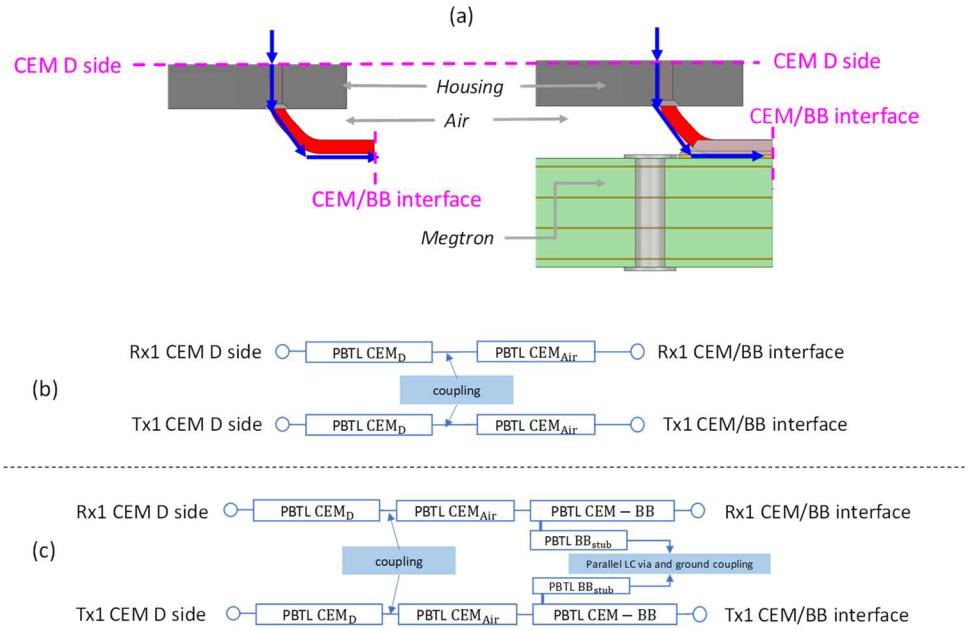

Figure 19 (a) the annotated subsection at the bottom side of CEM without and with baseboard (BB). (b) equivalent dPBTL subsystem for CEM bottom side (CEM D to CEM F subsection) without BB, and (c) equivalent dPBTL subsystem for CEM bottom side with BB as PBTL CEM-BB in parallel with PBTL BB_{stub} + ground via coupling subcircuits.

Comparing the TDRs transformed from DDRLs, the root causes of impedance mismatches can be distinguished, as labeled in the differential TDR plots of Figure 17. With step wave sending from top side to bottom side, the first impedance discontinuity is caused by AIC/CEM interface when AIC is mated, i.e., for $CEM_{AIC,\ mated}$ and $CEM_{AIC\text{-}BB,\ mated}$; the second large mismatch is due to the bottom subsection – unmated CEM E and CEM F in the air (with lowest $\varepsilon_{r,eff}$ and highest Z_{dd}). Mating CEM' with the bottom baseboard can effectively alleviate the strong mismatch, as shown in the TDRs for CEM'$_{BB,\ mated}$ and CEM'$_{AIC\text{-}BB,\ mated}$. A circuit-level interpretation is (1) the length of PBTL CEM_{Air} is reduced, and (2) the rest of the structure is changed to PBTL CEM-BB which equivalently represents the differential CEM pins mounted on the baseboard with

increased $\varepsilon_{r,eff}, tan\delta_{eff}$ and reduced Z_{dd} (~ 88 Ω). The 3D subsection and 1D dPBTL subsystem of the CEM bottom side along with the equivalent PBTLs is shown in Figure 19 for CEM' without and with baseboard.

3. dPBTL: Reduced PCIe 5.0 and PCIe Pathfinding Connectors

The preceding systematic work on the diagnosis and modeling of CEM' subsections lays a solid foundation for analyzing the complete PCIe 5.0 connector structure. Compared to CEM'$_{\text{AIC-BB, mated}}$, the PCIe connector simply has the GSSG pad connected to 1.27-mm differential microstrip feed lines with ground vias at the transition. Simply, RLC circuits are added to model the AIC north vias which also give rise to resonances in DDNEXT. Coupling between the pin stub (at x > 0) of the CEM connector and the active AIC pins is modeled with shunt capacitive through housing dielectrics. Similar to the AIC stub converted to PBTL AIC_{stub} explained in Section II.2.b, the CEM pin stub (CEM A) is modeled as an unterminated PBTL segment based on sectional analysis in Section II.1. Without further parametric tweaking, an accurate prediction on the PCIe 5.0 reduced model (2xGSSG) is achieved using the dPBTL 1D circuit system as shown in Figure 20. The decent match in DDRL and differential TDRs at both AIC side and the baseboard side demonstrate accurate physical-based modeling in terms of impedance transitions in the PCIe 5.0 connector. The DDIL is inherited from CEM'$_{\text{AIC-BB, mated}}$ with additional losses and delays from pads and feed lines. The major resonance spikes in DDNEXT at the AIC side are also well captured by the dPBTL system.

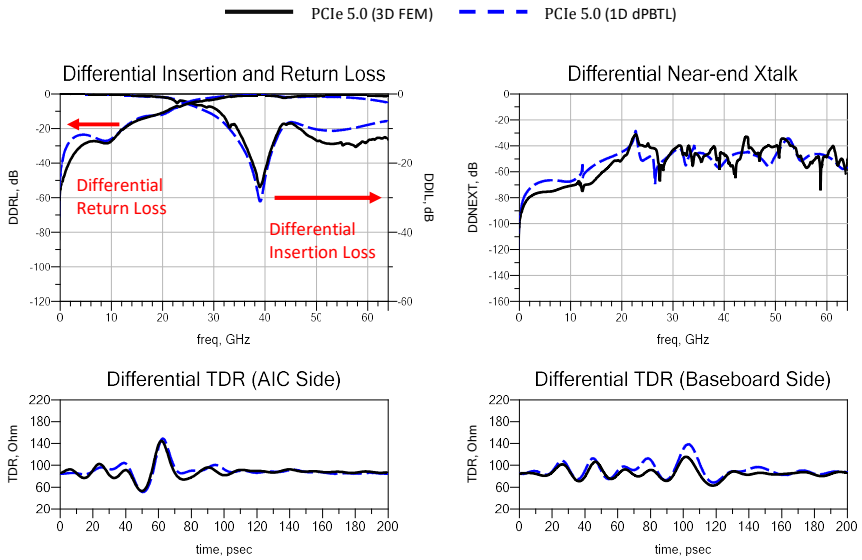

Figure 20 Electrical performances of PCIe 5.0 reduced model including DDRL, differential TDR transformed from DDRL at AIC side and Baseboard side, and DDIL of the aggressor pair, DDNEXT at top side experienced by the victim pair.

Now the dPBTL system is established for the PCIe connector with fast SI diagnosis and low occupancy in disk space, enabling fast design modifications and efficient integration with other circuit components. Table 3 compares the simulation time, estimated tool setup time, and disk space for HFSS FEM and dPBTL circuit. Setting up an HFSS FEM simulation is faster than a dPBTL system since the dPBTL system requires scrutinization of each subsection. However, dPBTL requires substantially less simulation time and disk

storage. Therefore, dPBTL can serve as a fast SI tool with sufficient physical-based parameters for designers to do detailed examinations on each dPBTL subsystem.

Table 3 SI design tool time and space management

Tools for Reduced PCIe 5.0 Analysis	Simulation time	Estimated setup time	Disk Space
HFSS FEM	4 hr 35 min	5 – 10 min	225 GB
dPBTL Circuit	<1 min	5 min/ subsection	500 KB

Aside from fast SI diagnosis, this established PCIe-specific dPBTL system provides a complementary approach for design pathfinding. A preliminary thought on design modification is to (1) reduce the AIC stub length to eliminate the DDIL valley at around 40 GHz and (2) move AIC south ground lateral bar to AIC south end for a better return path and eliminate the second DDNEXT resonance (which corresponds to the cavity between north vias and south vias). To avoid rerunning FEM simulation on an unvalidated idea, the dPBTL model is first updated accordingly --- (1) reduce the length of the PBTL AIC_{stub} segment, (2) attach via coupling subcircuit at the end of the reduced PBTL AIC_{stub} segment, and (3) update dPBTL CEM subsystem around interface based on previous sectional analysis (with AIC vs. without AIC). The dPBTL pathfinding system is modified without further performing the detailed sectional analysis on the 3D model. Nevertheless, the results of the PBTL pathfinding system provide desired performances, showing no DDIL valley and no high DDNEXT resonance spike at around 23 GHz, as shown in Figure 21. The pathfinding solution offers a smoother impedance transition at the AIC side than the original PCIe 5.0 design, seen in the differential TDR.

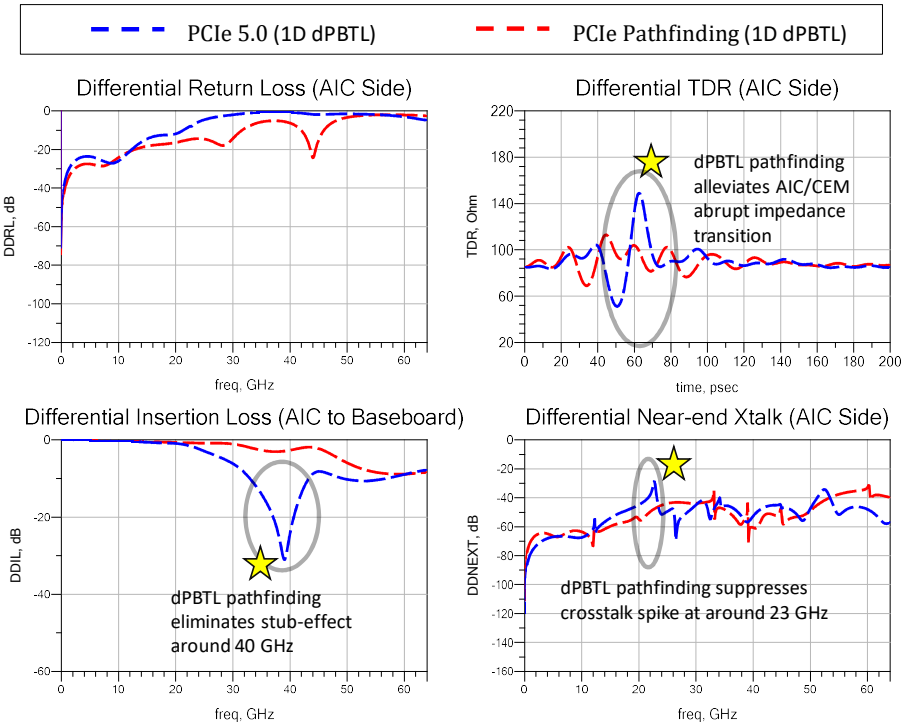

Figure 21 Showcase of PBTL system as a design tool: PBTL pathfinding model improves electrical performances-- reduces impedance mismatch at AIC/CEM interface, eliminates stub effect in differential insertion loss and high resonance spike in differential near-end crosstalk.

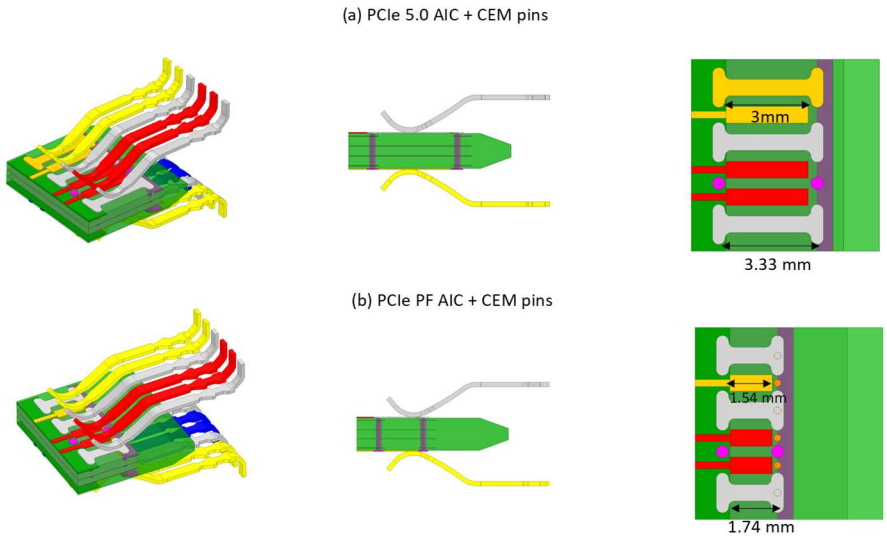

Figure 22 The illustrated original design of PCIe 5.0 AIC and the pathfinding (PF) design

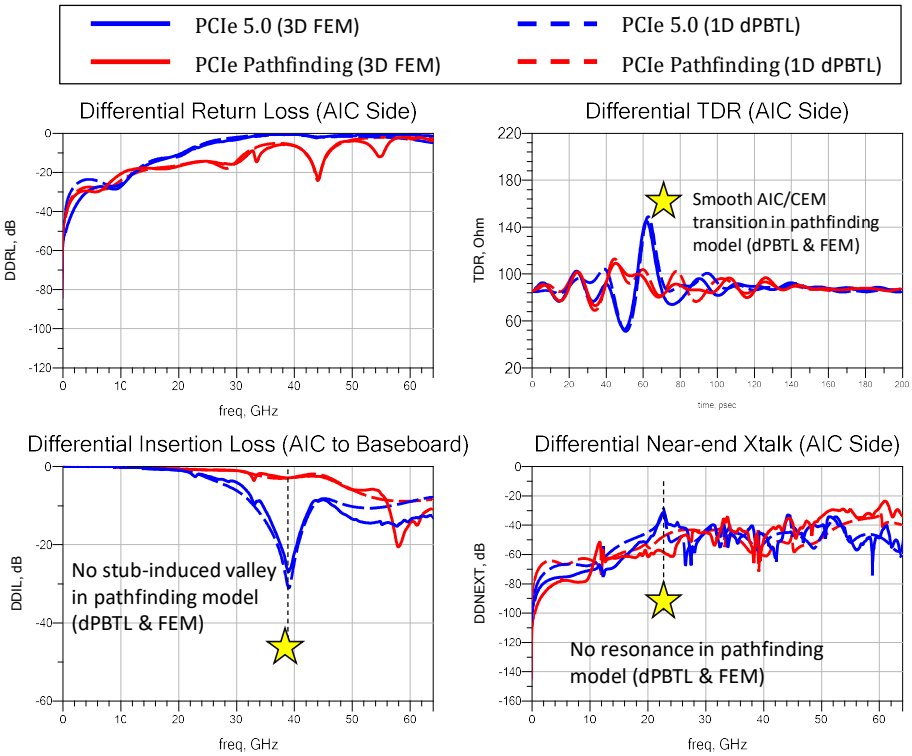

Figure 23 The differential S-parameter results and differential TDR of PCIe 5.0 and PCIe pathfinding, generated in HFSS 3D simulation and estimated by 1D PBTL circuit.

With insights offered by dPBTL as a pathfinder, the HFSS 3D model is updated as shown in Figure 22. Finally, we compare the pathfinding model and the original model which are evaluated by both the dPBTL system and HFSS FEM, as illustrated in Figure 23. The updated 3D model based on dPBTL pathfinding also shows improvements in impedance transitions, reduction in crosstalk resonance, and elimination in stub effect at around 40 GHz. Therefore, the dPBTL system shows its potential in not only assisting signal

integrity diagnosis and fast simulation but also efficiently guiding the design-optimization process as a design tool with sufficient accuracy. As shown in Table 4, the root-mean-square errors (RMSE) of dPBTL prediction on DDIL for original PCIe 5.0 and the updated pathfinding PCIe are calculated up to 16 GHz as the Nyquist frequency for 32 GT/s data rate. Underestimation of radiation in higher frequencies could lead to a larger RMSE over DC-64 GHz compared to RMSE over DC-16 GHz.

Table 4 RMSE of DDIL between PBTL and HFSS for PCIe 5.0 and PCIe pathfinding (PF)

	PCIe 5.0 PBTL vs HFSS	**PCIe PF PBTL vs HFSS**
RMSE (0-16 GHz)	0.00542	0.00200
RMSE (0-64GHz)	0.07551	0.06954

Finally, channel simulation in ADS is deployed to visualize the high-speed data quality of the designed connector with reference to the specified testing conditions of the eye diagram in PCIe 5.0 Specification [6]. The simplest channel simulation is set with the transmitter and receiver connected to the testing ports without equalizations and jitters, shown in Figure 24. The transmitter is connected to the AIC side of PCIe 5.0 or PCIe pathfinding, set with 32 Gb/s, 128B/130B encoding [6] [7]. Pseudorandom binary sequence (PRBS) 13 and 11-ps rise/fall time are used at the transmitter in simulation to approximate the real eye-diagram testing with our ready-to-use M8194A Arbitrary Waveform Generator for future reference [8]. Eye diagrams are measured after the receiver at the baseboard side. This channel analysis is conducted on both PCIe 5.0 original design and the PCIe pathfinding design based on HFSS FEM and dPBTL circuit system. Figure 25 displays the four received eye diagrams, measured after the AIC-side receiver for both PCIe 5.0 and PCIe pathfinding connectors modeled in HFSS and dPBTL respectively. All intrinsic channels show sufficiently wide eye openings [6].

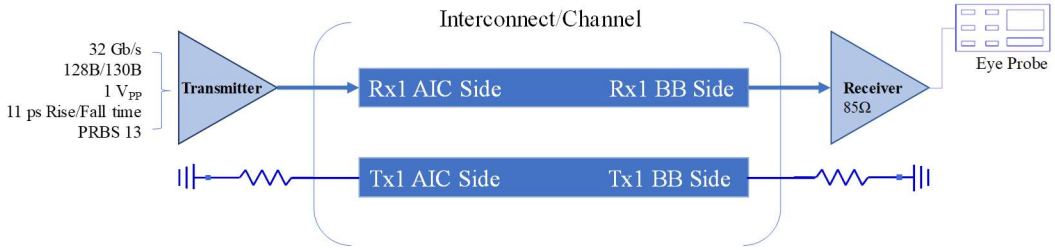

Figure 24 Channel simulation setup for PCIe 5.0 and PCIe pathfinding

SI improvement from the dBTL-driven pathfinding connector can be observed by comparing the eye diagrams in Figure 25. The original PCIe 5.0 3D and 1D connector models all experience the stub-induced valley which leads to strong dispersive effects for high-frequency components and impairs the eye patterns. The PCIe pathfinding conector has this deep valley eliminated as well as reduced impedance mismatches. Therefore, both dPBTL-based and HFSS-based PCIe pathfinding connector models demonstrate enlarged eye width (EW) and reduced jitters compared to the original PCIe 5.0 models. Since the dPBTL-based PCIe pathfinding model has not been calibrated with the updated 2D sectional analysis, the location-dependent dispersion, shunt couplings, or parasitics at the AIC side could be overestimated. Thus, the dPBTL pathfinding channel experiences relatively slower rising/falling with higher jitter. Nevertheless, the dPBTL method can

provide a quick preview of the channel performances showing correct trends, in addition to the S-parameter results.

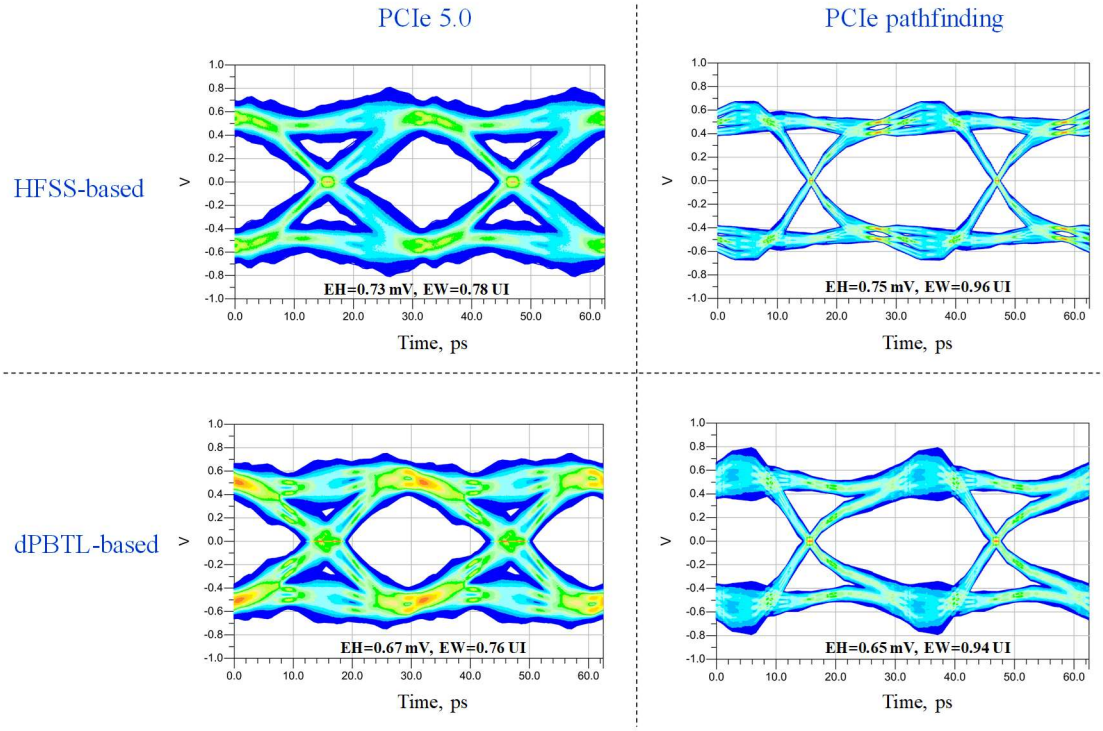

Figure 25 Results of eye-diagram channel simulation for HFSS-based and dPBTL-based PCIe 5.0 and PCIe pathfinding connector models, at at 32 Gb/s with one-million total number of bits.

Conclusion

To promote fast SI diagnosis and assist design-optimization for high-frequency devices, such as the PCIe connector, we developed a novel tool to reduce the 3-D structure complexity to the 1-D simplified circuit level, i.e., the distributed physical-based transmission line (dPBTL) model. We established a complete systematic workflow of distributed PBTL based on physical sectional analysis.

The dPBTL (sub-)systems are constructed for different subsections of CEM with/without BB and AIC, to not only perform fast simulation on the device but also provide equivalent parameterized PBTL-circuit segments regarding the structure-specific sectional losses, delay, impedance, etc. The mm-wave frequency-dependent distributed and dispersive effects in the connector are well interpreted in multisegment circuits. Thus, the dPBTL models for CEM and its mated parts are established with unique fingerprints of the device under analysis, unlocking microscopic diagnosis, and localized modifications. Time-efficient design optimization is accomplished based on the device-specific distributed dPBTL system as a pathfinder. As a result, we demonstrate the dPBTL model for assisting SI diagnosis and accelerating design optimization to reduce cycle time in designing new products.

Acknowledgments

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References

[1] "PCI Express Card Electromechanical Specification Revision 5.0, Version 0.9," PCIe Express, 2021.

[2] M. Steer, "Chapter 4: Extraordinary Transmission Line Effects," in *Microwave and RF design : a systems approach*, NC State University, 2019, pp. 165-191.

[3] S. H. Hall, "Topics In High-Speed Channel Modeling," in *Advanced Signal Integrity For High-Speed Digital Designs*, New Jersey, A JOHN WILEY & SONS, INC., PUBLICATION, 2009, pp. 434 - 437.

[4] S. B. Smith and M. Rengarajan, "Overcoming the SI Challenges in Designing 25-40 Gb/s Backplane Channels," in *DesignCon*, 2014.

[5] Y. Li, Y. Huang, A. S. Wander, A. Key, L. He, S. B. Smith and Y. Zhou, "PCIe Gen. 5 CEM Connector and Add-In Card PCB Design Optimizations," in *DesignCon*, 2019.

[6] C. Abhayagunawardhana, R. Abraham and S. Aditham, in *PCI Express® Base Specification Revision 5.0 Version 1.0*, PCI-SIG, 2019, pp. 1033-1065.

[7] Samtec, in *Interconnect Signal Integrity Handbook*, Samtec, Inc, 2007, p. 10.

[8] Keysight Technologies, "M8194A 120 GSa/s Arbitrary Waveform Version 1.0 Data Sheet," 2019.