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STABLE ON-CHIP CLOCK GENERATION

BY

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ABSTRACT

Generation of temperature invariant reference clocks on-chip may eliminate the need for bulky off-chip temperature compensated crystal oscillators. RC time-constant-based reference oscillators are well-suited for this role since they occupy a small area, consume little power, and can be easily integrated in any standard CMOS process. However, their performance is sensitive to the operating temperature. Using novel architectures discussed in the literature, we present a complete design of an RC-time constant-based reference oscillator with active temperature calibration achieved via two-point trimming of the circuit post-fabrication. The oscillator is designed to achieve a 100 MHz output frequency with less than 1000 ppm frequency variation from -30°C to 90°C .

ACKNOWLEDGMENTS

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CHAPTER 1

INTRODUCTION

Modern synchronous digital circuits use clock signals in order to synchronize different parts of the circuit. A clock signal oscillates between logic zero and logic one at a precise frequency. Quartz based off-chip temperature compensated crystal oscillators (TCXO) have been the standard way to generate reliable clock signals. But these crystals are bulky, hard to integrate, and not cost efficient. With the rise in popularity of Internet of Things (IoT), there has been a strong push to reduce circuit area and power consumption, resulting in increased popularity of on-chip clock generation techniques. RC time-constant-based reference oscillators provide a viable means to replace TCXO with an equally good on-chip solution. These oscillators occupy much smaller area compared to TCXOs, can be designed to consume a lot less power and they are well suited for integration in any standard CMOS process.

A typical RC time-constant-based reference works by locking the time-period of a voltage controlled oscillator to some RC-time constant formed by the circuit components. Such a feedback circuit is called frequency-locked loop (FLL). This circuit compares the frequency of a controllable oscillator to the reference, automatically raising or lowering the frequency of the oscillator until its frequency is matched to that of the reference. In contrast to phase-locked-loop (PLL), which locks the phase of the output signal with the phase of the reference input, the phase of the output signal in FLL is not determined and remains largely irrelevant.

CHAPTER 2

LITERATURE REVIEW

Several on-chip oscillator architectures have been studied in the literature. Options for on-chip oscillators range from tunable low-jitter LC-oscillators[1] to RC-referenced oscillators [2] [3] that involve the use of a voltage controlled ring-oscillator. Ring oscillators are a popular choice in integrated circuits, as they have small area, can produce a large range of frequencies, and can be made in any process technology. The project builds from the ideas used in the paper by A. Khashaba [4]. Our project uses the frequency locked loop and the temperature compensation techniques presented in the paper. Our aim is use those techniques to produce a clock signal at higher frequency.

An important aspect of designing integrated circuits is the system level modelling of the components. Behavioral modeling of voltage controlled oscillators, as well as design techniques for analog integrated circuits, are discussed extensively in the book, ‘Desing of Analog CMOS Integrated Circuits’ by Professor Behzad Razavi [5]. This textbook is used in the design of some of the crucial sub-circuits such as the integrator and the ring-oscillator. ‘Feedback Control of Dynamic Systems’ by Franklin [6] is used to study core concepts of control theory, which is important to understand the dynamics of the frequeuncy locked loop.

CHAPTER 3

RC-REFERENCED RING OSCILLATOR

3.1 Working principle

The RC-referenced ring oscillator architecture is shown in Fig. 3.1. The FLL locks the period of a voltage-controlled ring oscillator to a scaled reference RC time-constant, $R_{REF}C_R$. The FLL output is generated by the voltage-controlled ring oscillator. It is driven by the control voltage produced by integrating the difference between reference voltage, V_{REF} , and frequency-dependent voltage, V_F . V_{REF} is generated by scaling the supply voltage, V_{DD} , using resistors (R_D and xR_D) of the same type.

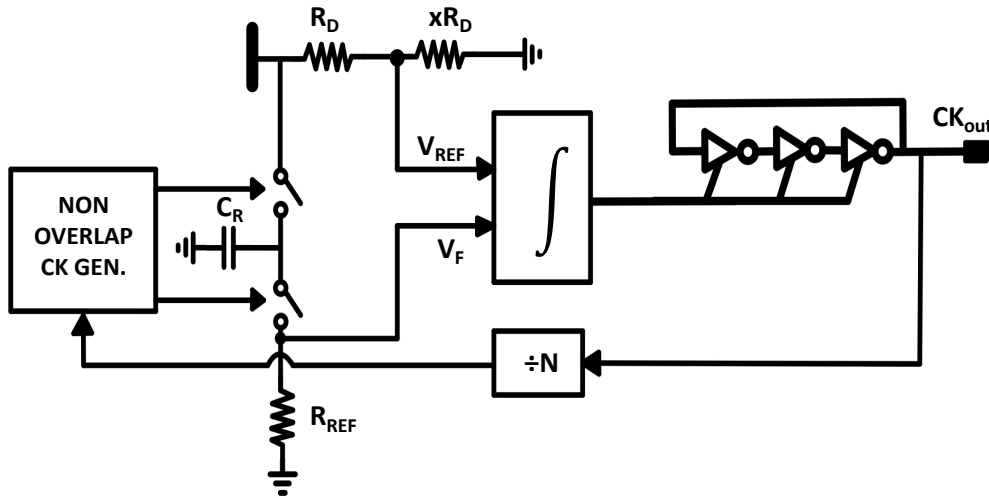


Figure 3.1: RC-referenced Ring Oscillator

Thus V_{REF} is given by

$$V_{REF} = \frac{V_{DD}}{1 + 1/x} \quad (3.1)$$

and is independent of temperature since (R_D and xR_D) will have same temperature variation.

The output of the voltage-controlled ring-oscillator is divided and sent to a non-overlap clock generator. The non-overlap clock generator produces two output clock signals ϕ_1 and ϕ_2 . When ϕ_1 is high (and ϕ_2 is low), the capacitor gets charged to V_{DD} . When ϕ_2 is high, the capacitor discharges through R_{REF} . In the ideal case, the switched capacitor acts as a resistor of value

$$R_C = \frac{N}{F_{out}C_R} \quad (3.2)$$

where F_{out} is the frequency of the voltage controlled ring oscillator and N is the division factor. Therefore, the frequency dependant voltage V_f will be given by voltage division of R_C and R_{REF} as follows

$$V_F = \frac{V_{DD}}{1 + R_C/R_{REF}} \quad (3.3)$$

Assuming a stable loop, in the steady state, the inputs of the integrator will be equal. Thus, $V_F = V_{REF}$. Solving for F_{out} , gives us

$$F_{out} = \frac{Nx}{R_{REF}C_R} \quad (3.4)$$

For our desing, we will use $R_{REF} = 100k\Omega$, $C_R = 1pF$, $N = 32$ and $x = 0.25$. With these values we predict $F_{OUT} = 106.66$ MHz. The exact value of F_{OUT} is not relevant since our architecture allows us to change R_{REF} even after the circuit is fabricated [7].

3.2 Temperature compensation

From equation (3.4), we see that F_{out} depends of N, x, C_R , and R_{REF} . Out of these quantities, N, x, C_R are nearly independent of temperature. As we discussed previously, R_D and xR_D are made from the same type of resistors, hence both will show similar temperature variation and thus x will not be affected by temperature. The temperature coefficient of C_R is negligible. N is a division factor typically implemented using digital logic and hence doesn't change with temperature. Therefore, we can safely assume that in the ideal case, all of the temperature dependence of F_{OUT} arises from the temperature variation of R_{REF} . Therefore, to reduce the temperature variation of F_{OUT} , we only need to reduce the temperature variation of R_{REF} . We can achieve this by constructing R_{REF} using two controllable resistors with opposite temperature coefficients connected in parallel to each other such. that

$$R_{REF} = R_1 || R_2 \tag{3.5}$$

where R_1 increases its resistance with increase in temperature and R_2 reduces its resistance with increase in temperature. After the circuit is fabricated, we can measure the the output frequency at two different temperatures and use that information to trim the resistor values R_1 and R_2 such that $R_1 || R_2$ has zero temperature variation. The details of such trimming mechanisms are beyond the scope of this thesis. Temperature compensation techniques for resistors have been extensively discussed in the senior thesis of Mingyuan Han, UIUC '22 [7].

CHAPTER 4

CIRCUIT DESIGN

We will be fabricating the temperature compensated RC-referenced ring oscillator using TSMC's 65nm CMOS process. However, we will first describe the system-level-design and show the simulation results. Using the insights gained from the system level simulations, we present the transistor-level integrator design and discuss the techniques used to overcome some of the non-idealities of the integrator. Finally, we discuss the layout techniques used to build the integrator.

4.1 System-level design

We model the architecture presented in Fig 3.1 using Verilog AMS in Cadence design suite.

4.1.1 Integrator modelling

For this simulation we will model the integrator in time domain. We can describe the integrator block as having two differential inputs (V_{in+} and V_{in-}) and an output (V_{out}) with one parameter, namely the integrator gain K_{int} . A simple equation captures this behaviour.

$$V_{out} = K_{int} \cdot (V_{in+} - V_{in-}) \cdot \Delta T \quad (4.1)$$

where ΔT is simulation time step.

4.1.2 Voltage-controlled oscillator modelling

We will model the voltage-controlled oscillator (VCO), with one input port (V_{in}) and one output port (V_{out}). An ideal voltage-controlled oscillator is a circuit whose output frequency is a linear function of its input voltage.

$$\omega_{out} = \omega_0 + K_{VCO}V_{in} \quad (4.2)$$

Here, ω_0 represents the free running frequency of the VCO corresponding to $V_{in} = 0$ and K_{VCO} denotes the gain of the VCO. The instantaneous frequency of the oscillator is defined as the derivative of the phase (ϕ) of the oscillator output.

$$\omega_{out} = \frac{d\phi}{dt} \quad (4.3)$$

We can thus compute the phase at the time t as.

$$\phi(t) = \int_0^t \omega dt + \phi_0 \quad (4.4)$$

Using equation (4.2) for the frequency, we get that

$$\phi(t) = \omega_0 t + K_{VCO} \int_0^t V_{in} dt + \phi_0 \quad (4.5)$$

Therefore, the output of the oscillator can be represented by

$$V_{out}(t) = V_0 \cos(\phi(t)) = V_0 \cos\left(\omega_0 t + K_{VCO} \int_0^t V_{in} dt + \phi_0\right) \quad (4.6)$$

Since we are working with clock signals, we would like the output of the VCO to oscillate between 0V and 1V rather than being a sinusoidal wave. Thus to obtain a square wave, we can just add an ideal comparator with threshold of 0 at the output of the VCO described above.

4.1.3 Feedback network modelling

The first component of the feedback network is the frequency divider. The divider output signal controls the switched capacitor resistor. The voltage division between the switched capacitor resistor and the reference resistor R_{REF} produces the voltage at the negative input of the integrator. We calculate that by combining equation (3.2) and (3.3).

$$V_F = \frac{V_{DD}}{1 + \frac{N}{F_{out}C_R R_{REF}}} \quad (4.7)$$

If we assume that the frequency of the oscillator is given by equation (4.2), then we can describe the entire feedback network using one input (V_{in}) and one output V_F .

$$V_F(V_{in}) = \frac{V_{DD}}{1 + \frac{N}{(F_0 + K_{VCO}V_{in})C_R R_{REF}}} \quad (4.8)$$

4.1.4 Simulation results

Using the high-level behaviour of the components described in the previous section, we run the simulation to verify the settling of output frequency and check that steady state value matches the prediction. The plot in Fig 4.1 shows that the output frequency settles to 106.66 MHz, which is exactly what was expected given that our models have not accounted for any non-ideality.

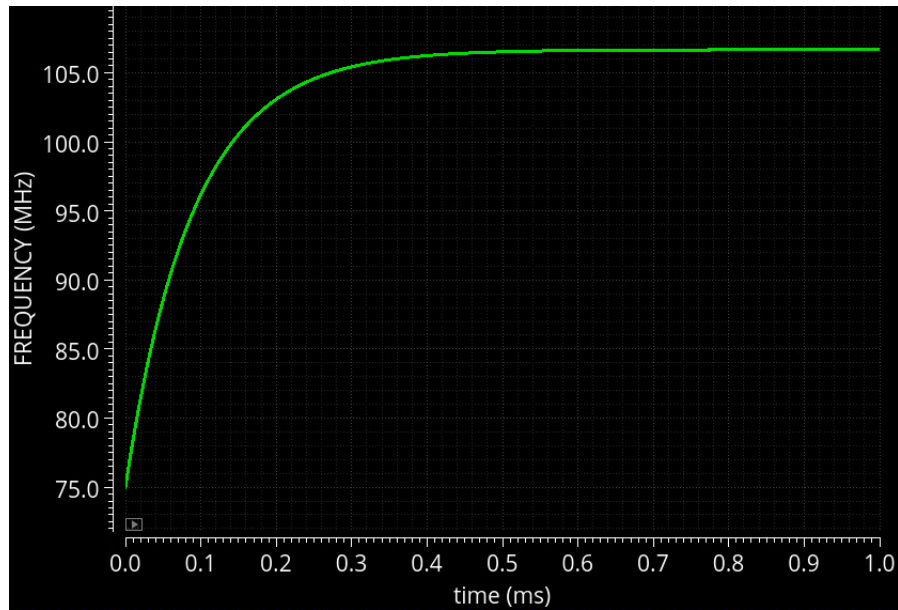


Figure 4.1: Settling of output frequency of the RC-referenced ring oscillator

4.2 Transistor level design of the integrator

4.2.1 Integrator topology

To achieve the functionality of an ideal integrator described by equation (4.1), we will use two trans-conductor stages and a capacitor wired up as shown in Fig 4.2. Such a configuration is known as Gm-C integrator.

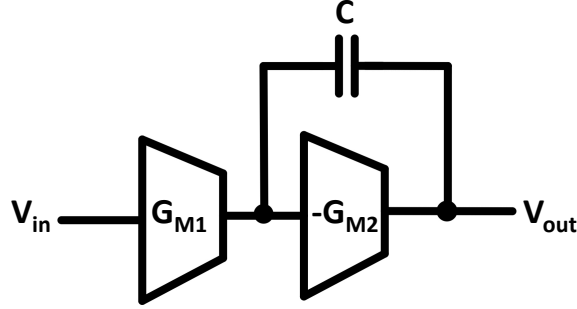


Figure 4.2: Gm-C integrator

The first stage has trans-conductance G_{m1} and an output impedance R_1 . The second stage has trans-conductance G_{m2} and an output impedance R_2 . Defining the input $V_{in} = V_{in+} - V_{in-}$, the transfer function of the Gm-C integrator can be approximately written as

$$\frac{V_{out}(s)}{V_{in}(s)} = A_{DC} \frac{(1 - s/\omega_z)}{(1 - s/\omega_{p1})(1 - s/\omega_{p2})} \quad (4.9)$$

where A_{DC} is the low frequency gain of the integrator and

$$\omega_{p1} = \frac{-1}{R_1(G_{m2}R_2)C} \quad (4.10)$$

$$\omega_{p2} = \frac{-G_{m2}}{C} \quad (4.11)$$

$$\omega_z = \frac{G_{m2}}{C} \quad (4.12)$$

are the poles and zeros of the transfer function. If the gain of the second stage is high enough ($(G_{m2}R_2) \gg 1$) then the poles are widely separated. However, the right half plane zero ω_z degrades the phase margin. Hence to eliminate that term, we add a resistor (R) in series with the capacitor. After

adding the resistor, the new value of ω_z is given by

$$\omega_z = \frac{G_{m2}}{C(G_{m2}R - 1)} \quad (4.13)$$

If we set the value of the resistor to be precisely equal to $R = 1/G_{m2}$, then we can push ω_z to infinity, thereby eliminating its effects. Even though fabricating precise resistor is not possible, we can still have R be close enough to $1/G_{m2}$ so that ω_z is pushed beyond to very high frequency, preferably beyond the unity gain frequency.

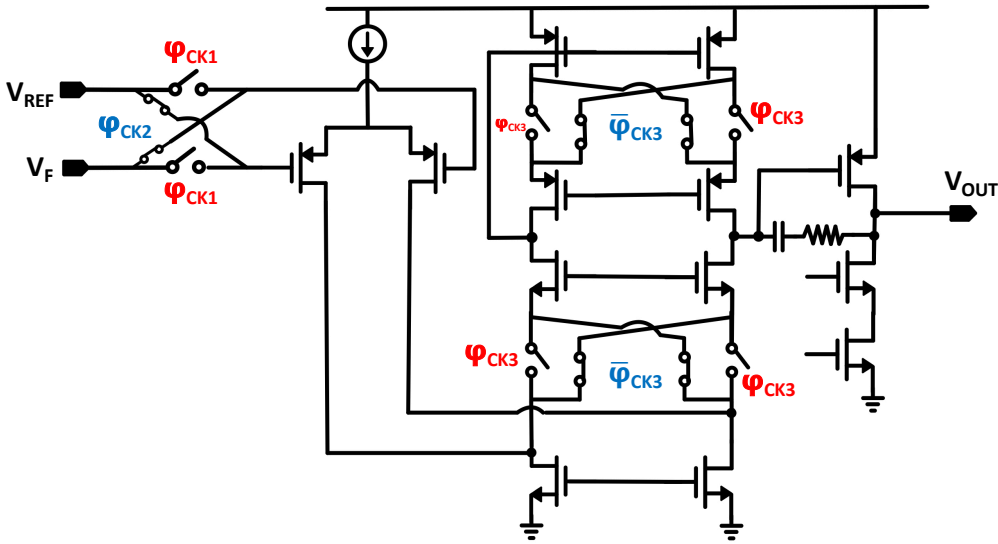


Figure 4.3: Transistor level implementation of the integrator

To suppress the temperature variation of the voltage controlled oscillator, we require A_{DC} to be very large. For our design, the desired value of A_{DC} is greater than 100dB. The first stage of the integrator is implemented with a folded-cascode topology with PMOS input pairs. Having first stage as folded cascode allows input common mode to go all the way down to 0V. The second stage of the integrator is implemented with a common-source stage. The integrating capacitor, C_{int} , is a 30pF capacitor.

4.2.2 Integrator non-idealities

One of the core assumptions in designing the integrator at transistor level is that the transistors are matched. For example, we expect that the lengths, widths, and the threshold voltages of the input differential pair transistors are exactly equal. However, such a precision is impossible to achieve and manufacturing errors result in transistor mismatch. The mismatch between transistors can result in complicated behavior that is difficult to quantize exactly. However, we can model such mismatches by adding input referred offset in our ideal models. Input referred offset is the differential voltage which must be applied to the input of an integrator to produce zero output. Assuming an integrator offset ΔV , in the steady state we will have

$$V_F - V_{REF} = \Delta V \quad (4.14)$$

Plugging equations. 3.3 and 3.1 into Eq. 4.14 and solving for the new output frequency we get

$$F_{OUT} = \frac{N}{R_{REF}C_R} \cdot \frac{x \cdot V_{DD} + (1+x)\Delta V}{V_{DD} - (1+x)\Delta V} \quad (4.15)$$

The output frequency is different from the expected steady state value. Moreover, the offset ΔV can vary with temperature and hence degrades the temperature stability of the output clock signal. We also observe that the frequency has supply dependence. Thus, any noise in V_{DD} will further degrade the performance of the oscillator. To reduce the effects of offset voltage, we can chop the first stage of the integrator. The switches that flip the inputs and the outputs of the first stage are shown in Fig 4.3. The input chopping is controlled by the signals ϕ_{ck1} and ϕ_{ck2} and the de-chopping is controlled by ϕ_{ck3} and $\bar{\phi}_{ck3}$. ϕ_{ck1} and ϕ_{ck2} are non-overlapping so that inputs don't get shorted and ϕ_{ck3} and $\bar{\phi}_{ck3}$ have some overlap to keep the bias current flowing.

Another assumption in integrator modelling is that no current flows through its inputs. However, if the oxide thickness is too low, a temperature dependant leakage current flows through the gate of the MOSFETs. To prevent this leakage, we use thick oxide transistors for constructing the integrator.

4.2.3 Simulation results

We run the complete simulation with the transistor level design for the integrator with the feedback factor defined by equation (4.8). Fig. 4.4 shows the settling of output frequency, which is similar the expected behaviour from the ideal simulations.

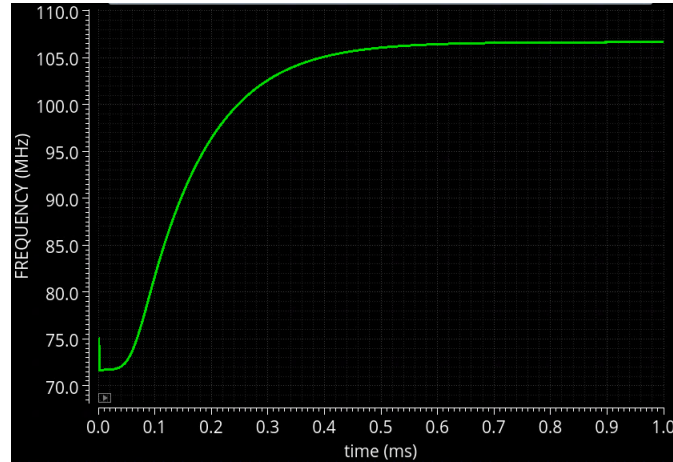


Figure 4.4: Settling of output frequency of the RC-referenced ring oscillator

Fig. 4.5 shows the loop gain of the loop transfer function with the feedback factor defined by equation (4.8). The integrator has a DC gain close to 110 dB and the feedback factor adds -20dB, resulting in low frequency loop gain of ≈ 90 dB.

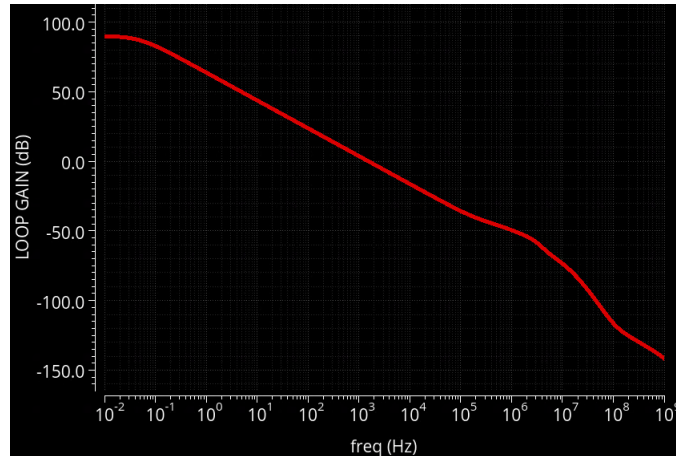


Figure 4.5: Loop gain

Fig 4.6 shows the phase of the loop transfer function.

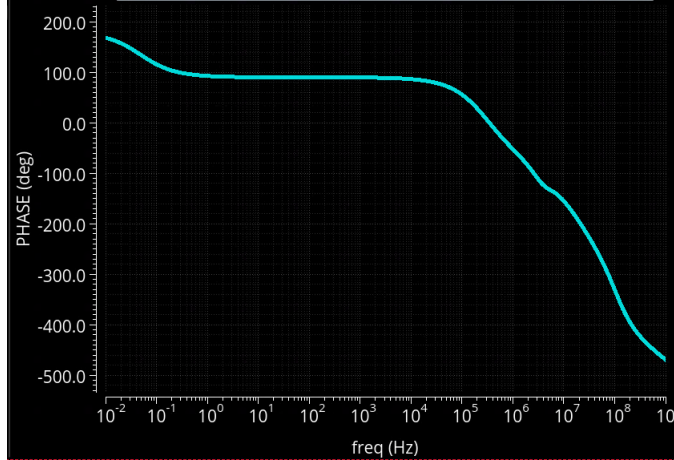


Figure 4.6: Phase

Compared to the ideal system level simulation, we observe that loop has additional poles and zeros. However, these do not affect the loop dynamics a since these extra poles and zeros occur at frequencies greater than the loop-gain unity gain frequency. Table 4.1 shows the stability margins of our circuit.

Phase margin	89.45° at 1.546 kHz
Gain margin	43.6 dB at 346.6 kHz

Table 4.1: Measured component values

To check the robustness of our integrator design, we run Monte-Carlo simulations where the transistor parameters are randomly varied. Under mismatch we calculate the offset voltage by calculating the difference between inputs of the integrator. Shown in Fig 4.7 is the distribution of offset voltage values when the first stage of the integrator is not chopped. Notice that the worst case values for the offsets approximately reach ± 25 mV. Shown in Fig 4.8 is the distribution of offset voltage values when the first stage of the integrator is chopped. Clearly chopping the first stage has an advantage because the worst case values for the offsets are now less than ± 1 mV.

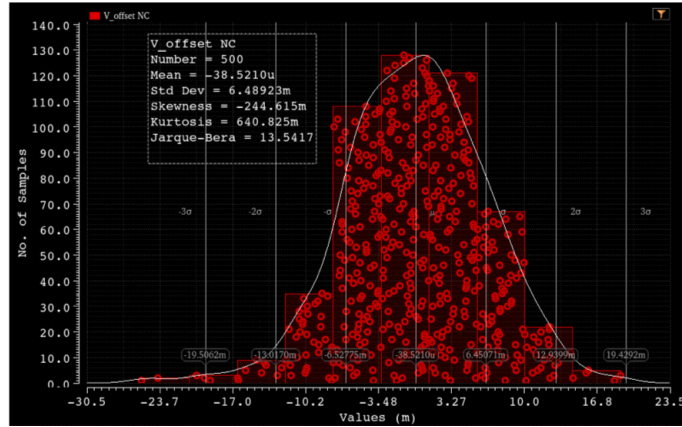


Figure 4.7: Distribution of offset voltage values without chopping

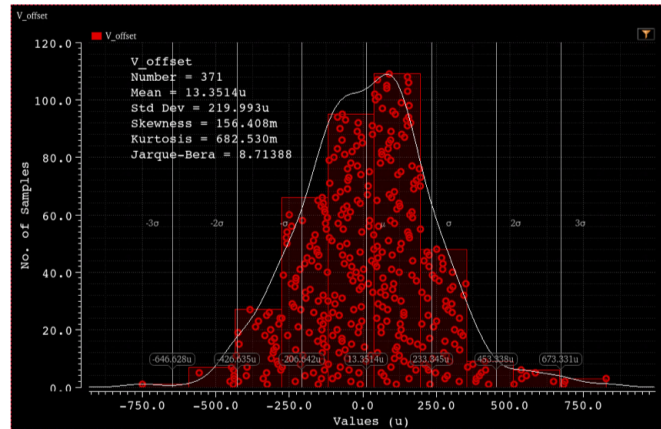


Figure 4.8: Distribution of offset voltage values with chopping

4.3 Layout of the integrator

The final stage of the integrator design involves the physical layout of the transistors and routing the connections between its various components. Fig 4.9 shows the completed layout of the integrator including the chopping switches, and the integrating capacitor. The integrator measures $290 \mu m$ by $300 \mu m$ in dimension.

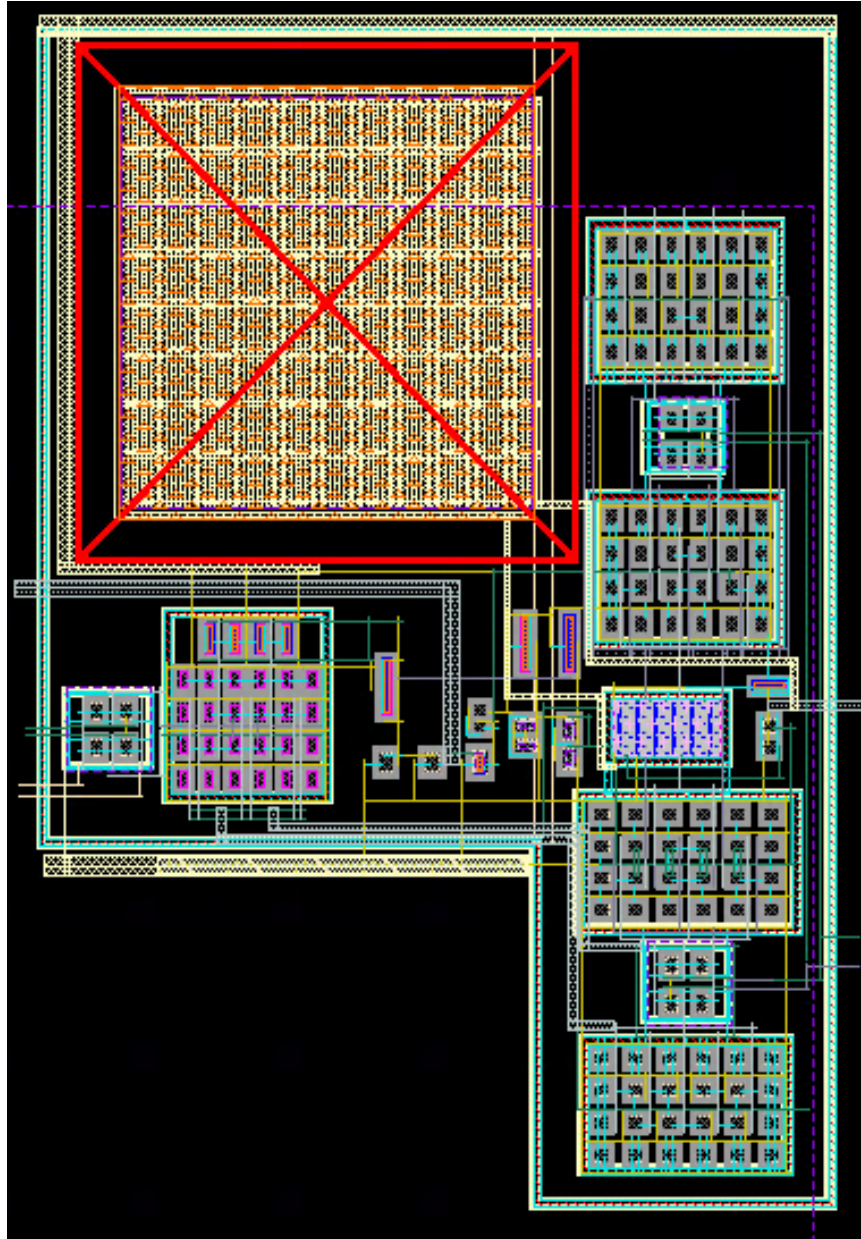


Figure 4.9: Layout of the integrator

As discussed previously, mismatch between transistors can result in input referred offset for the integrator. Chopping the first stage reduces the effects of offset. However, we can further reduce the magnitude of offset voltage by systematically ensuring that the transistors that need to be matched are identical. A powerful layout technique known as common centroid layout is very effective at matching transistors with each other. This technique involves splitting the two devices to be matched into several fingers and placed in a interleaved pattern surrounded by dummy transistors. It is important to ensure that the centroids of each device coincide; the devices orientations should be the same. Moreover, the array of devices should be as compact as possible. Fig 4.10 shows the input differential pair of the integrator placed using common centroid. Transistors marked 'A' and 'B' are the fingers of the input differential pairs. Transistors marked 'X' are dummy transistors. These dummy transistors ensure that immediate environment of any active transistor is identical to any other active transistor within the same common centroid layout.

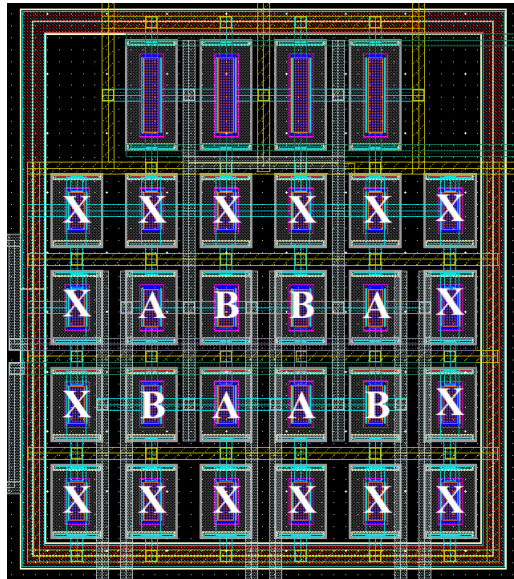


Figure 4.10: Common centroid layout of the input differential pair

Additionally, to ensure noise isolation we fabricate the integrator using deep n-well process. On top of that, we surround each of the matched differential pairs with guard rings.

CHAPTER 5

CONCLUSIONS

In this thesis, we focused on the techniques of reliable on-chip clock generation. Using existing architectures from the literature, we designed a RC time-constant-based reference oscillator. In chapter 3, we discussed the working principle of the frequency locked loop and derived the steady state output frequency. We briefly mentioned the techniques used to compensate for temperature variation. Chapter 4, focused on the system level architecture and dived deeper into the integrator design. We presented key issues that must be corrected when fabricating integrators using transistors. Chopping is used to remove the the temperature-dependent offset of the integrator and a high-gain 2-stage integrator guarantees good stability by rejecting the sensitivity of the voltage controlled oscillator. At the end of chapter 4 we presented the complete layout of the integrator in TSMC's 65nm CMOS process. The complete chip will be submitted for tape-out in early May of 2022. [4]

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